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Cross-Sectional Carrier Lifetime Profiling and Deep Level Monitoring in Silicon Carbide Films Exhibiting Variable Carbon Vacancy Concentrations

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The carrier lifetime control over 150 μm thick 4H-SiC epitaxial layers via thermal generation and annihilation of carbon vacancy (V_C) related $Z_{1/2}$ lifetime killer sites is reported. The defect developments upon typical SiC processing steps, such as high- and moderate-temperature anneals in the presence of a carbon cap, are monitored by combining electrical characterization techniques capable of V_C depth-profiling, capacitance–voltage (CV) and deep-level transient spectroscopy (DLTS), with a novel all-optical approach of cross-sectional carrier lifetime profiling across 4H-SiC epilayer/substrate based on imaging time-resolved photoluminescence (TRPL) spectroscopy in orthogonal pump-probe geometry, which readily exposes in-depth efficacy of defect reduction and surface recombination effects. The lifetime control is realized by initial high-temperature treatment (1800 °C) to increase V_C concentration to $\approx 10^{13}$ cm^{-3} level followed by a moderate-temperature (1500 °C) post-annealing of variable duration under C-rich thermodynamic equilibrium conditions. The post-annealing carried out for 5 h in effect eliminates V_C throughout the entire ultra-thick epilayer. The reduction of V_C-related $Z_{1/2}$ sites is proven by a significant lifetime increase from 0.8 to 2.5 μs. The upper limit of lifetimes in terms of carrier surface leakage and the presence of other non-radiative recombination centers besides $Z_{1/2}$, possibly related to residual impurities such as boron are discussed.

1. Introduction

Silicon carbide (SiC) is a wide bandgap semiconductor with material properties allowing for electronic applications operating under harsh conditions, such as high temperature and radiation. Among the key challenges yet to be resolved is mastering and control of the electrically active point defects, particularly in the technologically most relevant 4H-SiC polytype. The point defects spontaneously generated in a radiation-hard environment usually shorten the carrier lifetime degrading the performance of power electronics and radiation sensors. In contrast, the irradiation by swift ions, e.g., by MeV protons, can be used as a tool for the controlled introduction of radiation-defect-related recombination centers for optimizing lifetime and dynamic characteristics.[1] Still, the longest possible minority carrier lifetime in 4H-SiC epitaxial layers is the key prerequisite for the realization of high-voltage bipolar power devices; e.g., to modulate carrier conductivity in the voltage-blocking layer of a 10 kV class device comprised of 100 μm thick epilayer with doping concentration $\approx 10^{15}$ cm^{-3}, the required carrier lifetime is in the range of 10 μs. In recent years, carrier lifetimes in excess of several microseconds are being demonstrated after the origin of inherently short (sub-microsecond) lifetimes has been associated with intrinsic point defect, carbon vacancy (V_C), acting as a lifetime killer.[2] In response, several remedies to diminish such defects have been developed, such as carbon implantation, high-temperature oxidation, and thermal equilibration in carbon-rich conditions.[3–6] In 4H-SiC, V_C exhibits electrical

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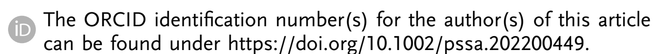
The ORCID identification number(s) for the author(s) of this article can be found under https://doi.org/10.1002/pssa.202200449.

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DOI: 10.1002/pssa.202200449

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activity as a double acceptor ($V_C(2-/0)$) positioned 0.7 eV below the conduction band edge (E_C) and referred to in the literature as $Z_{1/2}$ level, and also as a single and double donor ($V_C(0/+/2+)$) at E_C-(1.5–1.6) eV known as $EH_{6,7}$ level.[2] The typical concentration [V_C] in the present-day 4H-SiC epilayers remains in the range of 5×10^{12} cm^{-3} thus limiting carrier lifetimes in excess of ≈5 µs. Extensive efforts are made to reduce the [V_C] by post-growth processing, in particular by injecting highly-mobile carbon interstitials (C_i) from the surface into the bulk of the epilayer to recombine with V_C[3–6] and reach the targeted levels of [V_C] $< 10^{11}$ cm^{-3}. Despite the convincing demonstrations of the [V_C] control, there remain several important aspects that need clarification. First, the literature reports validating [V_C] contents typically employ capacitance spectroscopy on Schottky barrier diodes (SBD) formed on the tested material disregarding the important consequences of the high-temperature processing step inevitable in the *p*-n diode manufacturing; e.g., ≈1800 °C anneals are necessary to activate p-type dopants introduced by ion-implantation. For the bipolar applications, mastering the initial [V_C] $<10^{11}$ cm^{-3} levels seems impractical since the imminent 1800 °C anneals might be sufficient to re-generate V_C defects in view of their relatively low formation energy of ≈4.8 eV.[7,8] Apparently, the V_C defect elimination should rather follow after p-n junction formation as a final processing step, and testing of such C_i-injection strategy constitutes one of the key objectives in the present work. Yet another aspect calling for clarification relates to the fact that until now the reports on V_C contents with relation to carrier lifetimes involve relatively thin epilayers without clear discrimination of the surface effects. Indeed, besides recombination via $Z_{1/2}$ centers that delimit so-called bulk lifetime, there is also an inherent constraint to carrier lifetimes due to the finite thickness of epilayers, implying that sufficiently thick layers with respect to carrier diffusion length ($d_{EPI} > L_D$) are vital for minimizing the detrimental effects of carrier recombination at the surface and interface with the substrate.[9] It should be mentioned in this regard that carrier lifetime control in such optically thick epilayers has already gained considerable attention worldwide.[10–18]

Accordingly, the material of choice for the thermal generation and C-injection experiments should preferably involve ultra-thick and low-doped epilayers to ensure a broader profiling range and depth discrimination.

In the present work, the aforementioned issues are tackled by demonstrating a viable lifetime control through 150 µm-thick 4H-SiC epitaxial layers validated by combining electrical V_C-profiling methods with a novel all-optical approach for profiling carrier lifetimes across the epitaxial layer, which allows for depth-resolved monitoring of defect reduction efficiency as well as surface recombination effects.

2. Results and Discussion

The present work focuses on the lifetime control over ultra-thick (150 µm) 4H-SiC epitaxial layers via thermal generation and annealing of V_C -related $Z_{1/2}$ recombination sites limiting bulk carrier lifetime. The article is arranged as follows: first, we introduce an all-optical approach of depth-resolved lifetime measurements across 4H-SiC epilayers/substrate based on imaging time-resolved photoluminescence (TRPL) spectroscopy in orthogonal pump-probe geometry (ortho-TRPL). Next, the defect developments are discussed by combining optical results on cross-sectional carrier lifetime profiling with an electrical characterization of V_C depth profiles by capacitance–voltage (CV) and deep-level transient spectroscopy (DLTS).

2.1. Cross-Sectional Carrier Lifetime Profiling by Ortho-TRPL Spectroscopy

TRPL is a common technique for studying recombination processes in 4H-SiC,[19] which is typically operated in back-scattering optical configuration with PL emission being collected from the same side and surface spot as laser excitation. It is important to note that such TRPL measurements provide an integrated carrier lifetime across the probed epilayer thickness and possibly also involve substrate. The latter contribution can be minimized by adjusting the excitation wavelength to match penetration with epilayer thickness, however, the steep gradient of the photogenerated carriers and their initial localization close to the surface in turn actuate the processes of diffusion and surface recombination. As a result, TRPL decay generally represents carrier transport dynamics rather than minority carrier lifetime, which is a fundamental material property. All this clearly emphasizes the importance of a method capable of discriminating carrier transport constituents, diffusion and recombination, by providing depth-resolved lifetime distribution across the epilayer. To date, such insights can be attained by the transient free-carrier absorption (FCA) technique in a perpendicular pump-probe beam configuration, a challenging method requiring precision alignment of the two focused laser beams and specially prepared stripe-shaped specimens.[20] In the present work, a novel approach in depth-resolved carrier lifetime profiling across the epilayer/substrate is realized by employing imaging TRPL spectroscopy in orthogonal pump-probe geometry (ortho-TRPL), which outperforms the FCA technique in terms of spatial resolution and simplicity of operation owing to a single-beam concept and no need for specially prepared samples. An important prerequisite for depth-resolved lifetime profiling is initially flat carrier distribution across the epilayer to suppress the carrier diffusion process at the outset. To this end, a uniform photogeneration of the electron–hole pairs throughout the epilayer is ensured by 372 nm excitation (penetration depth $\alpha^{-1} \geq 400$ µm) impinging normally onto the epilayer surface. The PL emission is collected from the cross-sectional plane orthogonal to excitation by means of a microscope coupled to an imaging spectrograph equipped with EMCCD for micro-imaging and spectral analysis along with a fast PMT detector for recording spectrally filtered PL transients.

The effective lifetime parameters were deduced from the decay transients of the band-edge emission (spectrally filtered PL region around 390 nm) from the selected regions of interest (ROI) on the cross-sectional plane. The width of ROI is set by adjusting the entrance slit of the spectrograph. **Figure 1** presents the conceptual sketch of the novel approach in depth-resolved carrier lifetime measurements across 4H-SiC epilayer/substrate

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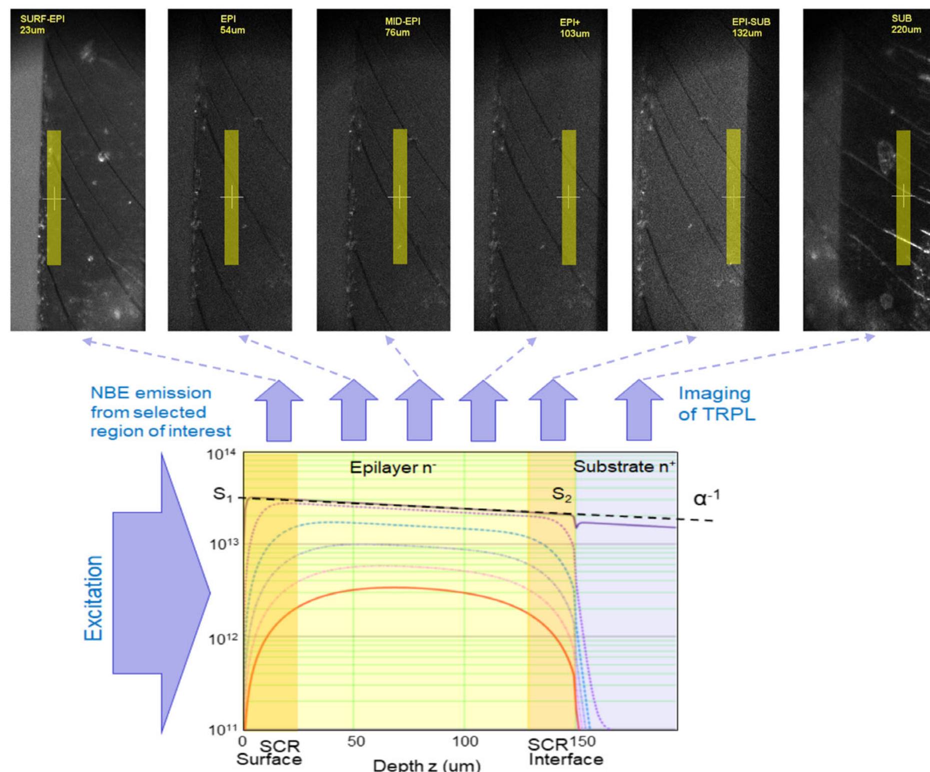

Figure 1. Conceptual sketch of the depth-resolved carrier lifetime measurements across 4 H-SiC epilayer/substrate by employing imaging time-resolved photoluminescence (TRPL) spectroscopy in orthogonal pump-probe geometry. The curves shown on the bottom panel are simulated in-depth carrier distributions for different elapsed times after excitation (10, 100, 500, 1500, and 2000 ns, respectively). The actual TRPL probing positions are indicated on the cross-sectional micrographs shown in the top panel.

structures. The TRPL signal was collected from ≈10 μm wide ROI while probing several representative positions across the exposed epilayer/substrate cross-sectional plane, i.e., 1) subsurface, 2,3,4) epilayer, and 5) interface regions as well as 6) substrate, as indicated by vertical bars on the cross-section micrographs in Figure 1.

The typical depth-resolved TRPL transients obtained in as-grown material are presented in **Figure 2**. It should be pointed out that in our experiments the estimated peak photogenerated carrier density of $<10^{14}$ cm^{-3} is below the background doping implying low-level injection conditions; thus TRPL measurements presented herein yield the minority carrier lifetimes.[21]

There is a clear correlation between the estimated carrier lifetimes with the probe position, exhibiting the maximal lifetimes of ≈2.5 μs in the middle of the epilayer and the lowest value of ≈1 μs in the vicinity of the surface, which is symptomatic of a significant surface recombination effect. This is not surprising considering the visually noticeable surface roughening of the samples subjected to high-temperature treatment. Interestingly, in stark contrast to strong surface recombination, there is virtually no carrier leakage at the interface. Indeed, the estimated lifetime (≈2.3 μs) in the proximity of the interface (ROI positions 4,5 in Figure 1) is comparable to that in the mid-epilayer (≈2.5 μs) in spite of the very fast recombination processes in the adjacent heavily-doped substrate (≈100 ns). Such a subdued leakage is attributable to the confinement

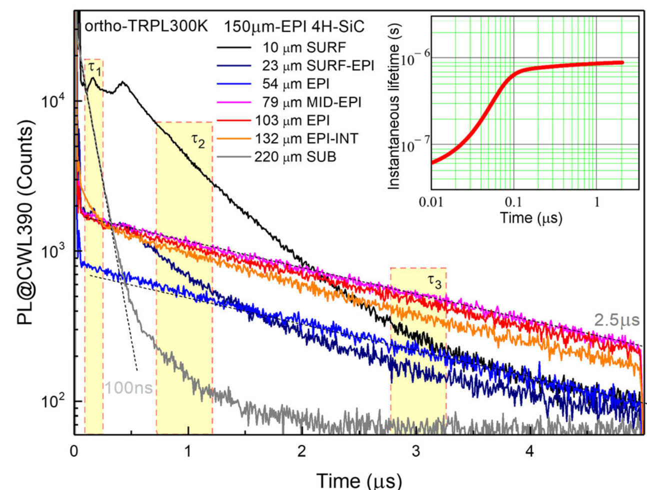

Figure 2. TRPL transients obtained at different depth locations across the epilayer/substrate starting at 10 μm from the front surface and ending deep in the substrate (220 μm). The nonlinearity of certain PL decays is caused by carrier diffusion and surface recombination as illustrated by numerically simulated temporal evolution of the instantaneous lifetime in the Inset.

of minority carriers (holes) in the epilayer by the low-high (n−/n+) doping-related potential barrier at the epilayer/substrate boundary.

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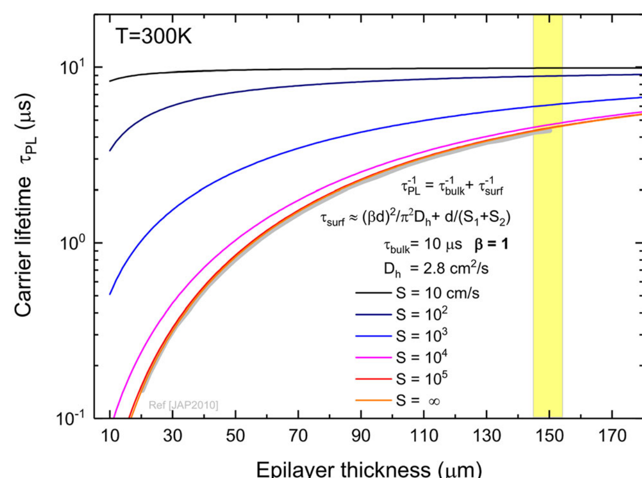

Figure 3. Effective carrier lifetime as a function of epilayer thickness for different surface recombination velocities simulated assuming bulk minority carrier lifetime of 10 μs. Note that effective lifetime is significantly affected by carrier diffusion and surface recombination even for thick 150 μm epilayers (shaded marker).

Figure 3 presents numerically simulated dependencies of the effective carrier lifetime versus epilayer thickness assuming the bulk minority carrier lifetime value of 10 μs. The general relationship[22] for surface recombination time (τ_{surf}) presented in the legend in Figure 3 considers two surfaces of d-thick epilayer with the parameters S_1 and S_2 describing surface and interface recombination velocities, S stands for an average value of both; whereas β parameter ($1 \leq \beta \leq 2$) differentiates the specific cases of large S with equal versus non-equal S_1 and S_2.

It is important to point out that even for an ultra-thick 150 μm epilayer the upper limit for the measured effective lifetime is apparently set by carrier diffusion and surface recombination, i.e., it still remains epilayer-thickness dependent. This fact underscores the extreme importance of surface passivation for applications requiring long lifetimes past 10 μs.

The extracted carrier lifetimes as a function of in-depth probe position are summarized in **Figure 4** representing cross-sectional carrier lifetime profiles for different thermal treatment and processing conditions. More specifically, the verification of the lifetime control by high-temperature C-cap annealings is presented in Figure 4a, which reveals the extent of lifetime variation achievable by C-cap annealings. One can observe considerable quenching of the lifetime after 1800 °C anneal as compared to that of the as-grown material. The lifetime gradually recovers with the increasing time of 1500 °C post-annealings, reaching 60% of that in as-grown epilayer after 300 min anneal.

Such a partial recovery could be associated with insufficient annealing time and also with the fact that other defects are being generated due to the presence of excess carbon that acts as recombination centers.

Importantly, for both the lifetime reduction after Vc generation at 1800C and for the subsequent lifetime increase after the 300 min anneals at 1500C, the change is approximately uniform throughout the entire probed region. In other words, the treatment seems to affect the entire epilayer. That this is the case for the Vc generation at 1800C is obvious, but the consistent increase in lifetime after the 1500C anneal for 300 min is interesting, and evidences that the C atoms injected from the C-cap are able to penetrate the entire epilayer to annihilate with V_C. It is noteworthy in this regard that interstitial-related defects are being extensively studied,[23] and there are also indications[24] that $Z_{1/2}$ deep traps observed in DLTS are actually related to complex defects involving carbon interstitials. Such defect complexes are considered potential sources of internal stress and, if grown sufficiently large to nucleate dislocation loops, could adversely affect the carrier lifetime. This model, however, is challenged by the reported comparative study on the carbon vacancy density (EPR) and the $Z_{1/2}$ center density (DLTS) measured on the same sample sets.[25] Furthermore, besides the formation of defect levels that are likely related to carbon interstitials, the C_i injection process reportedly has a drastic impact on the B impurity-related levels,[26] which have been linked to the carrier lifetime in SiC.[27]

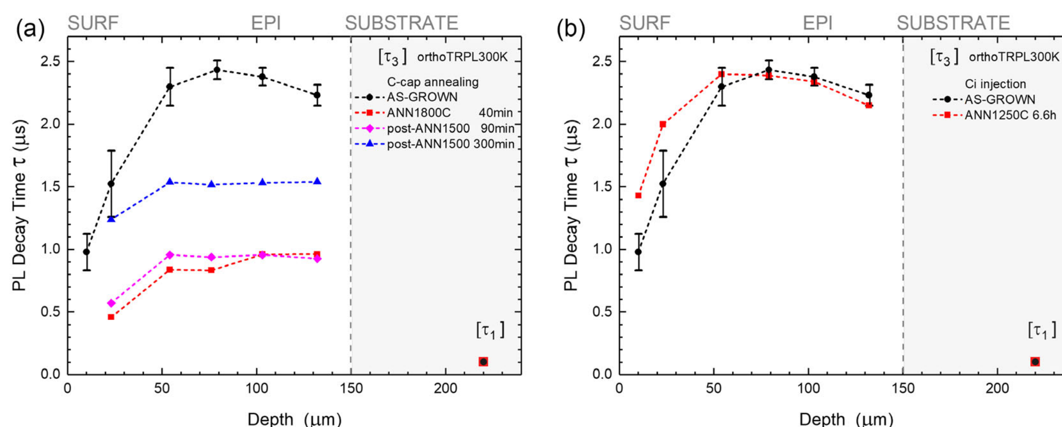

Figure 4. Cross-sectional carrier lifetime profiles obtained by ortho-TRPL for different thermal treatment and processing conditions of the 150 μm-thick 4H-SiC epilayers. a) Verification of the lifetime control by high-temperature C-cap annealings. With reference to as-grown material, note dramatic quenching of the lifetime after 1800 °C anneal and gradual recovery with the increasing time of 1500 °C post-annealings. b) Effects of the excess carbon injection by C-cap annealing at 1250 °C for 6.6 h. Note the apparent increase of the carrier lifetime for the top 80 μm as compared to as-grown material.

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Figure 4b summarizes the effects of the dedicated excess carbon injection test by C-cap annealing at 1250 °C for 6.6 h. The outcome of carbon injection is a noticeable increase in the carrier lifetime for the top 80 μm as compared to as-grown material, which is most likely caused by carbon interstitial annihilation with the preexisting V_C defects in as-grown material. Here, it is interesting to note that the effect is only observed in the top ≈80 μm of the epilayer, indicating that the injected C interstitials are only penetrating the upper region of the material.

2.2. Deep-Level Monitoring and Depth-Profiling by Capacitance Spectroscopy

Figure 5 summarizes deep-level monitoring and depth-profiling by CV and DLTS before and after annealing at 1800C to generate carbon vacancies. The free carrier profiles measured by CV at room temperature in as-grown and C-cap annealed at 1800 °C epilayers are shown in Figure 5a. DLTS depth profile of the $EH_{6,7}$ level representing the V_C-related single- and double donor state ($V_C(0/+/2+)$) at E_C-1.5 eV along with the free carrier profile measured at 650 K in C-cap annealed at 1800C epilayer are plotted alongside for comparison in Figure 5b.

The CV and DLTS depth-profiling provided thought-provoking results. Indeed, one can see in Figure 5b an increase in free carrier density after the 1800C anneal, slightly higher than that of the as-grown sample shown in Figure 5a, with the carrier density [n] increasing toward the bulk of the epilayer. One can observe a corresponding increase in carbon vacancy concentration [V_C] following the same trend as the carrier density toward the bulk of the epilayer. The as-grown material showed a low and constant [V_C] density of $\approx 2 \times 10^{11}$ cm^{-3}. Bearing in mind that $EH_{6/7}$ is a donor defect, it can contribute free carriers at high temperatures ($T > 600$ K), which explains why in Figure 5b a higher charge carrier density is observed at 650 K for 1800 °C annealed epilayer than that in Figure 5a measured for the same epilayer at room temperature.

Interestingly, both the [n] and [V_C] increase toward the sample bulk. This is because two mechanisms are competing during the 1800C anneal. Figure 5b presents data for the 1800C annealed sample that reflect the two concurrent processes: generation of V_C due to temperature, and simultaneously, annihilation of V_C due to recombination with C interstitials.

Considering these arguments we can conclude that neither Frenkel nor Schottky mechanisms acted as the source of carbon interstitials, but rather the carbon cap on the surface served as a source of carbon interstitials (C_i) diffusing into the bulk and leading to the annihilation of V_C ($V_C + C_i$). In contrast to an unvarying free carrier concentration of 2×10^{14} cm^{-3} across the as-grown epilayer, a significant degree of compensation after C-cap annealing at 1800C is exposed by CV measurements at room temperature. The free carrier density appears fully compensated starting from the surface all the way to the depth of ≈60 μm (Figure 5a) suggesting that some sort of electron traps with a density over 2×10^{14} cm^{-3} are generated near the surface region by annealing at 1800 °C with a carbon cap. The V_C density is increased towards the bulk of the epi-layer after annealing at 1800 °C, as compared to the [V_C] of 2×10^{11} cm^{-3} in the as-grown epi-layer, due to the thermal generation of carbon vacancies at high temperatures. The impact of a second annealing step at a moderate temperature of 1500 °C for different durations is shown in **Table 1**, which summarizes the different processing steps and resulting maximum [V_C] as measured by DLTS for the $Z_{1/2}$ or $EH_{6/7}$ levels depending on the degree of sample compensation necessitating high-temperature measurement. While the [V_C] concentration is enhanced by ≈2 orders of magnitude after the 1800 °C anneal, a substantial reduction is observed after the 1500 °C heat treatments. The 90 min 1500 °C anneal yields a lowered [V_C] of 4×10^{12}, and the 300 min 1500 °C anneal results in [V_C] below the detection limit of the DLTS which is around 10^{10}–10^{11} cm^{-3}. The same effect is observed upon the 1250 °C anneal with C-cap on as-grown material. In conclusion, the moderate temperature anneals are capable of reducing the [V_C] below the upper limit for high-lifetime material by the annihilation of the carbon vacancies via reactions with interstitial C injected from the carbon cap on the epi-layer surface. It is important to note that the DLTS measurements discussed earlier are only probing the upper sub-surface regions of the epilayer, e.g., down to ≈6 μm-depth as

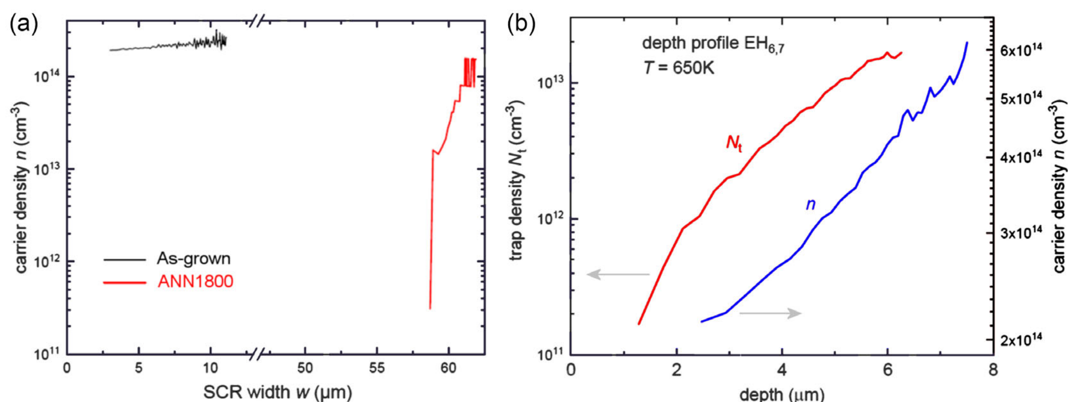

Figure 5. Deep-level monitoring and depth-profiling by capacitance–voltage (CV) and deep-level transient spectroscopy (DLTS). a) Free carrier profiles measured by CV at room temperature in as-grown and C-cap annealed at 1800 °C epilayers. b) DLTS depth profile of the $EH_{6,7}$ level representing the V_C-related single- and double donor state ($V_C(0/+/2+)$) at E_C-1.5 eV along with the free carrier profile measured at 650 K in C-cap annealed at 1800 °C epilayer.

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Table 1. Overview of the thermal processing steps and resulting carbon vacancy concentrations [V_C] extracted from DLTS measurements of either $Z_{1/2}$ or $EH_{6/7}$ levels depending on the degree of compensation in the sample.

Sample notation	1st annealing step	2nd annealing step	Purpose	V_C [cm^{-3}]
AS-GROWN	None, as-grown	None, as-grown	Reference	2×10^{11}
ANN1800C 40 min	1800C, 40 min	None	V_C generation	2×10^{13}
Post-ANN1500 90 min	1800C, 40 min	1500C, 90 min	V_C annihilation	4×10^{12}
Post-ANN1500C 300 min	1800C, 40 min	1500C, 300 min	V_C annihilation	$<<2 \times 10^{11}$ below DLTS detection limit
ANN1250C 6.6 h	1250C, 396 min	None	C injection for V_C annihilation	$<<2 \times 10^{11}$ below DLTS detection limit

shown in Figure 5b. Therefore, it is challenging from the DLTS data alone to assess whether the lifetime enhancing treatment impacts the entire epi thickness. However, this is in fact evident from the lifetime data shown in Figure 4a. After the 300 min anneal at 1500 °C, the carrier lifetime enhancement is uniform across the entire probed region. Evidently, the injected C interstitials from the C-cap penetrate and interact with V_C throughout the probed depth. In contrast, a 1250 °C anneal would not provide the interstitial C with sufficient energy to permeate the epilayer, as evidenced by the lifetime enhancement in Figure 5b only in the upper ≈80 μm of the epilayer.

In the case of carbon implantation or thermal oxidation, electron traps originating from defect complex including carbon interstitial are generated near the surface (e.g., ON1, ON2, M centers[3,28,29]), and a similar type of defect complex cannot be excluded in the present experiment. An insight into the origin of such compensation was attained by DLTS depth-profiling, which validated that the $Z_{1/2}$ (0/2−) acceptor charge transition level of the carbon vacancy defect is responsible for compensating the charge carriers. Such association is further supported by the observed DLTS and conductance measurements (not shown) of full recovery of the free charge carriers upon increasing the temperature above 370 K at which carbon vacancy becomes neutral, thus confirming its role in the compensation process. Generally, the DLTS depth-profile developments infer that carbon injection in the case of the near absence of V_C leads to the formation of new defect levels related to excess of carbon supporting similar assumptions discussed in the optical section. To sum up, the electrical measurements highlight the complexity of the V_C annihilation process by the supply of excess carbon, the incorporation of which apparently occurs via multiple pathways that lead both to the annihilation of V_C and the formation of new defects.

3. Conclusion

By forming a carbon-rich cap on the surface of 4H-SiC epilayers, we have injected excess carbon by thermal annealing. The cross-sectional profiling of lifetimes suggests that post-annealing under C-rich thermodynamic equilibrium conditions reduces V_C throughout the entire 150 μm thick epilayer, thus attesting as a potent lifetime control method suitable for 4H-SiC epilayers of all practicable thicknesses to date. The upper limit of carrier lifetimes is determined by carrier diffusion and surface recombination as well as the presence of other nonradiative recombination centers besides $Z_{1/2}$, conceivably involving residual impurities, such as boron. The cross-sectional lifetime profiling also underscores the importance of surface passivation for applications requiring the longest possible lifetimes. Generally, the combined optical and electrical profiling results point out the complexity of the V_C annihilation process via the supply of excess carbon, which involves a variety of channels leading both to the annihilation of V_C and the formation of new defects.

4. Experimental Section

The starting material was low-doped (2×10^{14} cm^{-3}) 150 μm thick epitaxial layer (Ascatron AB, Sweden) grown on heavily-doped (8×10^{18} cm^{-3}) n-type 4H-SiC substrate. Next, a high-temperature treatment (1800 °C) was employed to increase V_C concentration to ≈10^{13} cm^{-3} level, and then a moderate-temperature (1500 °C) post-annealing of variable duration was performed under C-rich thermodynamic equilibrium conditions to study defect evolutions. Throughout the high-temperature treatments, the surface of the epilayers was protected by a pyrolyzed photoresist film, a so-called carbon cap (C-cap),[6] which also acted as a source for carbon in-diffusion ensuring C-rich conditions. For studies of carbon interstitial injection, the annealing was performed at 1250 °C for 6.6 h. The C-cap was removed after high-temperature anneals by dry thermal oxidation performed at 900 °C. The thermal processing steps and sample notation used in the manuscript are outlined in Table 1.

The electrical characterization by CV profiling was carried out using a high-precision capacitance meter (Boonton, Model 7200) operating at 1 MHz frequency. The same capacitance meter coupled with a pulse generator (Agilent, 81110 A) provided means for DLTS measurements of V_C concentration via the related $Z_{1/2}$ peak ascribed to the double negative acceptor state, V_C(2−/0), located in DLTS spectra at 285 K for a rate window of (640 ms)$^{-1}$, and the EH6/7 peak assigned to V_C(2+/+/0) located at ≈600 K. For electrical measurements, Schottky barrier diodes were formed by depositing Ni contacts of 1 mm diameter on the epilayer surface using an electron beam evaporator and creating Ohmic contact on the backside (substrate) by silver paste.

TRPL measurements were performed at room temperature using 372 nm wavelength excitation of a 50-ps pulsed laser (PicoQuant, average power 2 mW @40 MHz). The emission was collected from the orthogonal to the excitation plane and analyzed by an imaging spectroscopy system comprised of a microscope (50X objective, Mitutoyo) coupled to an imaging spectrograph (HORIBA Jobin Yvon, iHR320) equipped with EMCCD camera (Andor, iXon888) and fast PMT detector (Becker&Hickl, PMC100) linked to photon counters (PicoQuant, TCSPC TimeHarp200, and MCS NanoHarp250). The spatial resolution was determined by the microscope magnification and the width of the ROI set by adjusting the entrance slits of the imaging spectrograph. In this work, the TRPL signal was collected

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from ≈10 μm wide ROI. The time resolution of the TRPL system was around 50 ps, which is achievable in time-correlated single photon counting (TCSPC) mode upon deconvolution of the system response function. This high resolution is relevant for measuring fast PL decay transients typical to SiC substrate material (nanosecond time domain). For the high-crystallinity epilayers demonstrating minority carrier lifetimes in the microsecond range, the TRPL system is operated in multichannel scaling (MCS) photon counting mode offering ≈4 ns resolution.

Acknowledgements

Financial support was kindly provided by the Research Council of Norway and the University of Oslo through the frontier research project FUNDAMeNT (Nr. 251131, FriPro ToppForsk-program) and FRIPRO project QuTe (Nr. 325573). The Research Council of Norway is acknowledged for the support to research project NoSiCaR (project Nr. 274742) and the Norwegian Micro- and Nano-Fabrication Facility, NorFab (project Nr. 245963). The work of MEB was supported by an ETH Zurich Postdoctoral Fellowship.

Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

carbon vacancy, carrier lifetime, photoluminescence, proton irradiation

Received: June 30, 2022
Revised: October 27, 2022
Published online:

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