Ultra-Low-Voltage and Energy-Efficient Circuit Techniques for iOTs

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Acronyms:

ADC	**Analog to Digital Converter**
ASIC	**Application Specific Integrated Circuits**
BGR	**Bandgap Reference**
CMRR	**Common Mode Rejection Ratio**
CMOS	**Complementary Metal Oxide Silicon**
CRTMOM	**RTMOM capacitor**
DAC	**Digital to Analog Converter**
DRC	**Design Rule Check**
FC	**Folded Cascode**
FG	**Floating Gate**
HVT	**High Threshold Voltage**
IC	**Integrated Circuits**
iOT	**Internet of Things**
JLCC	**J-Leaded Chip Carrier (ceramic)**
LCD	**Liquid Crystal Display**
LDO	**Low Dropout Regulator**
LED	**Light Emitting Diode**
LP	**Low Power**
LVT	**Low Threshold Voltage**
LVS	**Layout Versus Schematic**
MOMCAP	**Metal-Oxide-Metal Capacitor**
MOSFET	**Metal Oxide Semiconductor Field-Effect Transistor**
MSB	**Most Significant Bit**
NMOS	**N-type MOSFET**
Op-Amp	**Operational Amplifier**

OTA	**Operational Transconductance Amplifier**
PCB	**Printed Circuit Board**
PMOS	**P-type MOSFET**
PSRR	**Power Supply Rejection Ratio**
RGC	**Regulated Cascode**
RTMOM	**Rotative Metal-Oxide-Metal**
SAR	**Successive Approximation Register**
SC	**Simple Cascode**
SFG	**Semi Floating Gate**
SOC	**System on Chip**
TFC	**Triple Folded Cascode**
TSMC	**Taiwan Semiconductor Manufacturing Company**
ULP	**Ultra Low Power**
ULV	**Ultra Low Voltage**
ULVT	**Ultra Low Threshold Voltage**
ULVSFG	**Ultra Low Voltage Semi Floating Gate**

Abstract:

The main aim of this research is to study and develop new Ultra-Low Voltage (ULV) and energy-efficient circuit techniques for low power iOT applications. In the digital domain, ULV NP-domino logic technique is studied for relatively high-speed applications while using a power supply as low as 300 mV and below. Semi-Floating Gate (SFG) technique is used to increase the speed of the conventional domino logic circuits for both single-rail and dual-rail NP-domino configurations. In the early stage of this research, a chip prototype that includes SFG ULV inverter logic gates was also fabricated and successfully measured. The intent was to study the practical challenges of the SFG ULV logic. In the analog domain, energy-efficient circuit techniques are studied for the iOT applications. For the high-performance LCD displays in iOT devices, a high-speed and energy-efficient buffer amplifier is proposed. Finally, an energy-efficient, successive approximation register (SAR), Analog to digital converter (ADC) is designed, fabricated and measured during this research work, which is suitable for ultra-low-power iOT applications. Several techniques have been used to reduce the power consumption of the ADC, which operates with power-supply as low as 0.6 V. The proposed SAR ADC is powered up by a simple energy harvester in the lab. Utilizing lower power supply voltages, minimizing the static currents, designing circuits with different threshold voltages, sleep-mode designing, and minimizing leakage currents were the techniques that employed in this thesis to reduce the power consumption of the circuits.

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Several people have made my pursuit of a PhD a rewarding experience. I would like to take this chance to thank them all for making it possible and enjoyable. First, my deepest gratitude goes to my thesis advisors Prof. Yngvar Berg and Associate Prof. Omid Mirmotahari for their supervision, patience, shared scientific knowledge, friendship and support in hard times. I would also like to thank the Nanoelectronics group, my colleagues, and my friends. Thanks to our head engineer Olav Stanley Kyrvestad for his support and engagement in achieving measurement results. Thanks to Dr. Ali Zaher, Prof. Joar Martin Østby, Dr. Alessio Paolo Buccino, Dr. Hans Kristian Berge, Dr. Kristian Gjertsen Kjelgård, Girish Aramanekoppa Subbarao, Mathias Tømmer, Dr. Behnam Samadpour Rikan, Candice Quinn and Dr. Thanh Trung Nguyen. I would also like to thank my office mates and Dr. Amir Hasanbegovic for the great times we spent together and the many different topics we discussed. I should not forget to thank all the colleagues there for the discussions we had, and the hospitality they show. I would like to thank Nano-Network for making it possible with their generous funding for me to travel and participate in different workshops and conferences. Finally, I would like to thank my mother and my sisters for their unconditional love.

Chapter 1

Introduction

1.1 Motivation

Internet of Things (iOT) is revolutionizing human life by developing modern devices which are able to sense, process and transmit information, captured from any simple object in our environment [1-2]. The number of iOT devices is growing continuously and hundreds billion devices are connected in the modern cities, buildings, and homes [1-2]. These devices are becoming widely used for smart applications in various industries including farming, transportation, and health care [2]. Fig. 1, shows a typical information infrastructure of iOT system in the healthcare field (reproduced from [1]). Most iOT devices have been developed by integrating two main technologies: Micro/Nano-Electro-Mechanical technology (MEMS/NEMS), and application-specific integrated circuits (ASIC) [1-2], [8]. Traditionally, the main challenges for industry engineers and academic researchers in the iOT field are reduction of production cost, device size, and power consumption all the while still improving performance. Historically the power consumption was not very crucial issue for the wire-connected systems, since a stable source of energy was often available. However, for modern iOT devices minimizing the power consumption is one of the main challenges for the design engineers, since these devices often utilize replaceable/rechargeable batteries. In addition, if we continue to use only batteries as power sources for these devices the cost of battery change, and recharge will become unreasonably high. Furthermore, batteries are often not a viable solution for many health-related applications, such as implantable devices like a battery-powered pacemaker, due to the short lifespans and size. Battery changes pose a risk to patient because they require surgery. The body anatomy is also a limiting factor to use larger batteries for these biomedical devices, and smaller commercial batteries are not

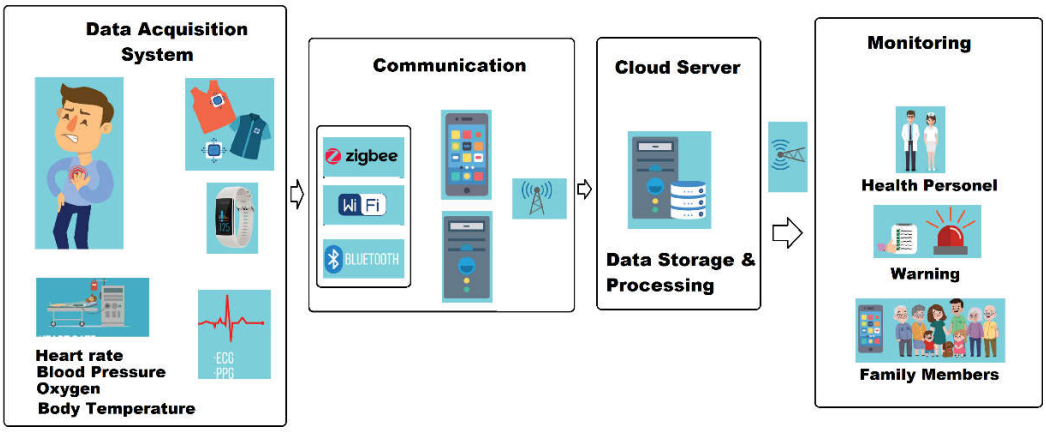


Fig. 1. iOT in healthcare (reproduced from [1])

able to provide enough power for applications which need longer lifetime. For example, a 1 mm^3 solid-state thin-film battery provides only 40 nW for a period of 1 year [3-4]. Energy harvesting from the environment is a promising solution for powering these systems [3-7]. However, the amount of harvested energy is not large enough for many applications. Improving their efficiency is a difficult challenge faced by researchers who mainly utilize NEMS/MEMS technology. For instance, the power harvested from a 1 mm^3 vibration-type energy harvester that is attached to a running person is only 7.4 nW [4-5]. As another example, the amount of harvested power from an endo-cochlear potential that is in the inner ear of a guinea pig is in the range of 1.1-6.3 nW with approximately 35-55 mV output voltage [6, P. 1241]. While the harvesting efficiency of these energy harvesters needs to be improved, at the same time the energy-efficiency of the sensors and integrated circuits, which consume the harvested energy, should be also maximized. This can be handled by developing innovative solutions both in the MEMS/NEMS based sensor technologies [8] and in the CMOS ASIC technology [4]. ASIC technology is key for implementing signal processing and data transceiver units and plays an important role in iOT devices [4]. They often used to realize the efficient analog and digital signal processing blocks for iOT devices, and normally utilized microcontrollers, radio transceivers, data-converters (analog to digital and digital to analog converters), as well as programable amplifiers and filters [4]. Further development of high-performance ASIC systems is required, since most of the modern iOT applications urgently require low-power circuit solutions to extend the lifetime of the device [4]. Therefore, improving the energy efficiency of these circuits and whole systems is one of the most important tasks for researchers.

*1.2 **ASIC Design Challenges for iOT Devices***

Fig. 2 demonstrates a typical ASIC system for iOT devices, which consists of several analog, digital and mixed-signal sub-blocks such as amplifiers, filters, memories, and data converters. The design strategy for these iOT ASICs, often is determined by the available power-budget, signal bandwidth and accuracy, silicon area, required signal to noise ratio (SNR), required dynamic-range, and available supply voltage. While CMOS technology nodes continue to scale down, the operational speed of the circuits and systems increases. All the while the power supply of these systems shrinks, which minimizes the power consumption and relaxes the power density issue [9-12]. While the power-supply voltage (VDD) scaling is a very useful technique to reduce the overall power consumption of the digital/analog circuits, it is worth noting that the threshold-voltage (Vth) cannot be aggressively scaled down, since the leakage-currents of the whole systems may become significant parts of the overall power consumption [9-11]. This issue is one of the main speed limiting factors for the high-speed CMOS digital circuits which require enough over-drive voltage for the transistors to have large enough ON-currents [9-11][21][82]. The issue is even worse in the deep subthreshold region

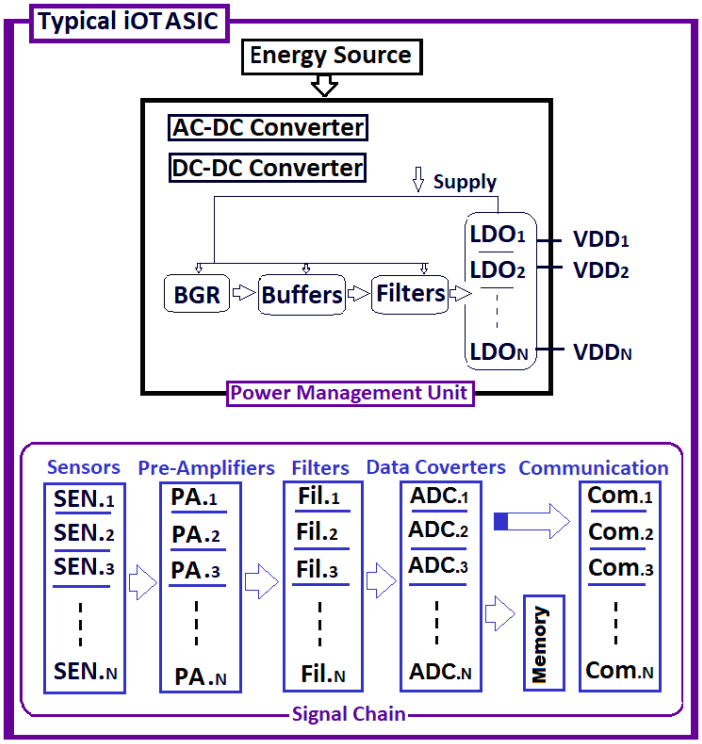


Fig. 2. A typical ASIC system for iOT devices.

where the ratio of the "ON" current to the "OFF" current is not often large enough to have stable and robust operation with enough noise-margin [9-10], [21]. The design challenges in the digital domain will be discussed in Chapter 2 with more details.

In the analog/mixed circuits and systems design, normally the required signal to noise ratio (SNR) and dynamic-range of the whole system is determined by the minimum acceptable power supply voltage for the whole system [9-13]. In this field, ULV circuits often suffer from the lower supply-voltages that reduces the available swing and dynamic-range for the current-sources, active-loads, differential pairs, and amplifiers. Each of those systems are widely used sub-blocks in many iOT devices for a large range of applications. This issue will be discussed more in detail in Chapter. 3.

1.3 ***Circuit Solutions for iOT Devices***

Portable iOT devices for wide range of application such as personal health monitoring, environment monitoring and item detectors, requires an event base signal processing. In these applications, the iOT devices often handle relatively low-frequency input signals from the environment, or human body. Therefore, ASIC for these devices often operate in low frequency mode and often utilizes an event-base structure. In this case the device operates in sleep-mode a significant part of its clock cycle. This technique significantly reduces the power consumption of the iOT devices. The concept of duty-cycling/power-gating (or sometimes called sleep-mode operation) is also employed in the always-ON sub-blocks such as reference-generators (see [4], [13]). This technique is a very effective method to minimize the power consumption and is becoming more and more popular. As an example, Bluetooth-low-energy (BLE) standard spends most of its operational time in the sleep mode. This standard is developed for low power iOT devices. However, those devices usually suffer from higher leakage currents while in sleep mode which results in a lower battery lifetime for the devices [14]. Modern SAR ADCs also use the duty-cycling technique extensively to minimize power [4][13].

As mentioned before, lowering the supply voltage is the most attractive solution to reduce power consumption. However, lowering the supply voltage introduces several difficulties to the designers, both in the digital and analog domain. As shown in Fig. 2, iOT devices utilize different type of sensors, a wide range of amplifiers, various types of filters, data converters, and wireless transceivers to communicate with other devices or a server. Depending on the required specification of the iOT device, different strategies are used to design in sub-blocks. Most of these sub-blocks utilize amplifiers that are challenging blocks to design in ULV domain, since there is not enough headroom for transistors to keep performance. For example, sub-volt bandgap-references (BGRs) and low-dropout regulators (LDOs), with a very tight power budget, can no longer utilize the classical techniques in the amplifiers in which they require often higher VDD and

demand higher power budget [13][15]. Realizing ULV and ULP reference circuits and LDOs require innovative circuit techniques (see e.g. [15]).

Generally, reducing the number of transistors, lowering the power supply voltages for both digital and analog circuits, and minimizing static and leakage currents in the analog circuits such as amplifiers, buffer amplifiers, LDOs, filters, and BGRs, may reduce the power consumption of the iOT devices.

1.4 Thesis Organization and Summary of the Research Work

In this research work, several circuit techniques are studied for iOT devices both in the digital and mixed/analog domain. In general, reducing the power supply voltage, minimizing the static currents, minimizing the leakage currents and designing the circuits and systems that can operate in sleep mode, were the main purposes.

In the digital domain, domino logic style is mainly investigated as alternative technique to increase the speed of the logic gates in the deep sub-threshold ULV operation, where the available power supply voltage is limited to 300 mV and lower, and standard static CMOS is not fast enough. Domino logic generally utilizes lower number of the transistors for the given logic function in comparison to the standard CMOS static logic. Lowering the number of transistors in the domino logic style may lead to smaller leakage currents for the iOT devices, which mostly operate in sleep mode. Domino logic is commonly known for having higher speeds when compared to the static CMOS logic. To further increase the speed in the domino logic style, the semi-floating gate (SFG) technique is used to speed up the evaluation process of the logic style. This technique is widely used in the bootstrap sample and hold circuits to increase the speed and linearity of the circuits (e.g. [12], [54]). The main aim of this technique is to increase the gate voltage of transistors to a value larger than power supply voltage (VDD), to reduce the ON resistance of the device, and increase the logic speed (see [43]). The SFG methodology is also used in implementing various analog and digital circuits such as memories, amplifiers, and filters. In the ULV operation mode below 300 mV there are no latch-up issues, so the feasibility of utilizing the bulk terminals is studied in this work for further speed enhancement [85]. Furthermore, SFG technique is used in the dual-rail domino logic style [86-89]. The design issues for utilizing SFG in dual-rail domino logic is studied and a new keeper structure is developed to eliminate the sensitivity of the logic style to the delayed input signal in large chain of logic [86-89]. While the feasibility of utilizing the SFG technique in the ULV domino logic is investigated in many references (e.g. [43]), applying the technique to the dual-rail domino logic and utilizing a new and robust keeper structure have been done during this research work. A chip prototype including n-type and p-type ULV7 [43], is also fabricated during this research work to study the practical challenges of the ULV7 gate, using 90nm CMOS.

Amplifiers, as one of the most widely used blocks in iOT devices, studied in this thesis. Amplifiers are the key elements in many power-hungry analog blocks such as LCD column drivers, LDOs, BGRs, power amplifiers, and filters. All of which are key blocks in any iOT devices. The main issues for the modern amplifiers in the submicron CMOS technologies are limited intrinsic gain of transistors, speed-gain tradeoff, and static current consumption. In the iOT devices which utilize LCDs, the buffer amplifiers used to drive the column pixels which normally have a heavy capacitive load around 1-10 nF. For these buffer amplifiers, a new energy efficient structure is proposed that reduces the static current and power consumption, and in the same time, improves the speed [141]. Energy efficiency is very important for these LCDs, since they are one of the most power-hungry part of these iOT devices. Furthermore, the proposed amplifier may be used in any iOT applications with heavy capacitive loads, such as LDOs and ADC reference generators.

In order to study the feasibility of powering a battery-free miniature iOT system with an energy harvester, an ultra-low-energy ASIC is designed, fabricated, and tested during last part of this research work. The ASIC includes a SAR ADC with an internal clock generator. Data converters (ADCs/DACs) are commonly used sub-blocks in almost any iOT devices. These converters have been used to digitize the analog signals which are directly produced by the sensors. Several circuit techniques, including multi-Vth design, sleep-mode operation, lowering supply voltage (VDD), leakage current reduction techniques, are used to minimize the power consumption. The energy harvester is formed by small commercial 0.69 mm^2 photodiode array, composed of three TEMD7000X01 photodiodes in series configuration. By connecting three devices in series, a supply voltage of 0.6 V is generated to power up the ASIC chip. In this case the harvested voltage is directly connected to the VDD pin of the ADC core, without any extra regulator. Several techniques are used to minimize the power consumption of the designed ADC. SAR ADC is chosen, since the topology provide an energy-efficient performance. SAR ADCs are very attractive for these applications since they do not utilize any analog block with static current consumption. In other words, all blocks in the SAR ADC are dynamic circuits which utilize the clock signal to operate and avoid static currents. When used for low speed iOT applications, the SAR ADC can operate with a sub-volt supply voltage which minimizes power consumption. ADCs in these low speed applications are often designed to operate in sleep mode for the majority of their clock period to minimize power. In addition, such low power SAR ADCs usually utilize at least one high-threshold-voltage transistors for any path from VDD to ground, in order to minimize the leakage currents in the sleep mode. A new custom-made capacitor array is designed to minimize the effects of routing parasitic capacitances on the accuracy of the capacitor array and SAR ADC.

The thesis is mainly based on a collection of published papers related to the ULV and ULP digital/analog CMOS circuit design techniques for iOT applications. In addition, a brief background information and simulation results related to the topic are discussed throughout the chapters. During this research work two chip prototypes were also designed and produced via EUROPRACRICE, and the details are discussed in Chapters 2 and 3. The thesis is based on the following published papers:

Paper I: "High-Speed, Modified, Bulk stimulated, Ultra-Low-Voltage, Domino Inverter" *Ali Dadashi, Yngvar Berg and Omid Mirmotahari. IEEE proceedings, ISVLSI 2015, Montpelier, France.*
Paper II: *"An Ultra-Low-Voltage, Semi-Floating-Gate, Domino, Dual-Rail, NOR Gate" Ali Dadashi, Omid Mirmotahari,and Yngvar Berg. IEEE Proceedings, ICECS 2015, Cairo, Egypt.*
Paper III: "Domino Dual-Rail, High-Speed, NOR Logic, with 300 mV supply in 90 nm CMOS Technology" *Ali Dadashi, Omid Mirmotahari, and Yngvar Berg. IEEE Proceedings, ISCE 2016, Sao Paolo, Brazil.*
Paper IV: "NP-Domino, Ultra-Low-Voltage, High-Speed, Dual-Rail, CMOS NOR Gates" *Ali Dadashi, Omid Mirmotahari, and Yngvar Berg. Circuit and Systems, 2016.*
Paper V: *"A High-Performance CMOS Modified Amplifier" Ali Dadashi, Yngvar Berg, and Omid Mirmotahari, IEEE Proceedings, ISCE 2016, Sao Paolo, Brazil.*
Paper VI: *"Fast-Settling, Energy-Efficient, Amplifier for High-Resolution LCD Displays" Ali Dadashi, Yngvar Berg, and Omid Mirmotahari. IEEE Proceedings, AM-FPD 2017, Kyoto, Japan.*
Paper VII: "Energy-Efficient, Fast-Settling, Modified Nested-Current-Mirror, Single-Stage-Amplifier for High-Resolution LCDs in 90-nm CMOS" *Ali Dadashi, Yngvar Berg, and Omid Mirmotahari, Journal of Analog Integrated Circuits and Signal Processing, 2018.*

In the papers I-IV, the ULV domino logic gates with SFG are studied [85-88]. Paper I present the design and simulation results of the bulk stimulated ULV7 (see [43]) inverters in 90 nm standard CMOS process [85]. The purpose of the research was decreasing of the evaluation and pre-charge time of the ULV7 domino inverter. Paper II III, and IV [86-88] present the design and simulation results of an ULV, SFG, Dual-Rail, NOR Gate in 90 nm standard CMOS process. The purpose of the research was to implement a new NOR gate in dual-rail domino logic to speed up the evaluation time of the ULV domino NOR gate. Increasing the speed of the gate in lower supply voltages and improving robustness against delay variations of the input signal were the main advantages of the proposed gate in comparison to the previously reported domino dual-

rail NOR gates. Paper IV [87] investigates the design and simulations of a new NOR gate based on the ULVSFG dual-rail domino logic structure. A new keeper structure is introduced which makes the SFG technique more robust against the delay of the input signal. Thanks to the new keeper structure in the SFG technique, high-depth logic gates are feasible to implement. This paper is a more complete version of paper II [86] and III [88]. Paper V introduces a new cascode amplifier that is suitable for applications which require high-gain amplifiers. Increasing the linearity of the structure was the main purpose of the research. Papers VI and VII investigate the details of a buffer for column-driver of high-resolution, liquid crystal display (LCD) panels, which are very widely used structures in iOT applications. Both speed and dc-gain are improved while the power consumption, gain-bandwidth product (GBW), noise, output voltage swing range, and the phase margin of the structure are not affected to a great extent [141]. The technique may be utilized in other blocks that drive large and wide range capacitive loads.

The rest of this thesis is organized as follows: Chapter 2 presents a general overview of the background information related to the ULV digital CMOS logic design in the sub-threshold region and covers the basic principles and challenges in the low-power and ULV CMOS SFG domino logic design. Additionally, design, fabrication details and measurement results of the ULV7 SFG inverter logic, which were fabricated in chip prototype I, are also discussed. Summary of the published papers in the domino ULV logic field is provided in this chapter.

Chapter 3 presents a general overview of the background information related to the ULV and ULP analog/mixed mode CMOS design and covers the basic principles and challenges in the low-power CMOS design and ULV and ULP operation for energy efficient iOT systems. Summary of the published paper are also provided in this chapter. Chapter 3 also presents the design, fabrication, and functionality measurements of the ULP miniature ASIC, including details about the SAR ADC, with internal clock generator. The ASIC was fabricated in chip prototype II.

Finally, in Chapter 4 the conclusions of this work, as well as suggestions for the future research, are given.

Chapter 2

ULV Digital Design

In this chapter the circuit design challenges in the ULV digital domain for the iOT applications discussed. Section 2.1 briefly introduces the design challenges of digital modules in the iOT devices. Section 2.2 addresses the sub-threshold operation of the transistor, which is an attractive operation region for the ULV digital design. Section 2.3 discusses the challenges of the designing high performance ULV domino logic. Section 2.4 discusses the SFG ULV logic technique. Section 2.5 provides summary of the published paper related to this chapter. Finally, section 2.6 provides a brief summary of the silicon fabrication of the ULV7 inverter logic gates.

2.1 Digital Design for iOTs

CMOS technology downscaling has been the main driving factor in the modern semiconductor industry for at least few decades [20-22]. Smaller transistor size normally reduces the parasitic capacitance of the devices, resulting in faster charging/discharging of the internal nodes in the complex digital ICs. At the same time the power consumption related to the parasitic capacitances reduces significantly. Technology scaling has enabled a tremendous signal-processing density over specific amount of silicon die, and this often imposes a higher power-density [20-22]. Higher transistor density also helps to reduce the price for the consumer electronic. In addition, pressures from consumers demanding low power, low cost, long-lasting, and portable iOT devices increases the importance of the low-power logic styles in integrated circuit design [16-24]. This is why there is an increasing demand for the novel ULV design techniques, and power consumption becomes the most important design challenge for this energy restricted systems. Traditionally reducing the supply-voltage is the most widely used technique for reducing the overall power consumption (and power density) for these iOT applications. For these ULV systems with reduced supply and threshold voltages, the leakage power becomes a significant part of the overall power consumption. Overcoming this challenging task requires innovative design techniques for digital integrated circuits and systems. It is considerable that, for the ULV systems, it is not often practical to scale the threshold voltage down since it results in a significant increase in the leakage current and reduction of the noise margins of digital gates [20-22]. This is especially important for the duty-cycled iOT systems, where the device is mainly operating in the sleep mode. Duty-cycled

iOT systems are very attractive and widely used structures for the applications that uses batteries and energy-harvesters. These duty-cycled systems are often event-based systems that normally utilize a low-frequency clock with low duty-cycle. In the other hand, utilizing devices with higher threshold voltages, in theses ULV systems, often lead to lower speed for the logic gates since the gate-source voltage of the devices reduces.

While the conventional static CMOS logic is a widely used solution for the digital systems, it does not normally provide fast enough solution for the high-speed ULV systems. For high-speed applications, traditionally domino logic is utilized extensively, and high-speed processors often utilize the domino logic to boost their operational performance. Domino logic is a fast logic family that normally uses a low number of transistors to implement some digital function, making it a very attractive architecture for portable iOT devices as they are energy restricted systems. Lower number of transistors can lead to lower leakage currents and consequently lower power consumption in the systems which are often implemented in the duty-cycled mode. In this thesis NP-domino logic is investigated and SFG technique is used to further increase the speed of the NP-domino logic in the ULV applications with a supply voltage as low as 300mV and below.

The rest of this chapter is organized as follow: section 2.2 provides basic information about the subthreshold operation of the MOS transistor and related challenges, section 2.3 provides background information about domino logic, section 2.4 discusses SFG ULV NP-domino logic and related challenges, and finally the section 2.5 summarizes the published articles in this research work. Section 2.6 provides details of the silicon fabrication of the ULV7 inverter logic gates.

2.2 Subthreshold Operation

Nowadays, designing circuits in the sub-threshold region is becoming more and more attractive solution for the IC designers. In the CMOS technology, subthreshold region of a transistor occurs when the gate-source voltage (V_{gs}) of transistor is smaller than threshold voltage (V_{th}) of that transistor. The V_{th} of a transistor is not a constant value and depends on different parameters such as temperature, oxide thickness, bulk-voltage, device dimension, substrate doping and so on, in the given process (see [25] and [11, P.14]). As an example, the dependency of V_{th} on the source-bulk voltage (V_{SB}) is given in (2.1) [11 P.24]. Where the V_{th0} is the threshold voltage at V_{SB}=0, α is body bias coefficient, and $\emptyset_S$ is surface potential [11 P.24].

$$Vth = V_{th0} + \alpha.\left(\sqrt{|V_{SB} + \emptyset_S|} - \sqrt{|\emptyset_S|}\right) \quad (2.1)$$

In addition, in the given process some fabrication companies normally offer different types of transistors with different threshold voltages, bringing extra freedom for designers to use in different part of their design. As an example, standard V_{th}, Low-threshold (lvt), ultra-low-threshold (ulvt), zero-threshold (native device), and high-threshold (hvt) are 5 different NMOS transistor types which are available in the 90nm TSMC process.

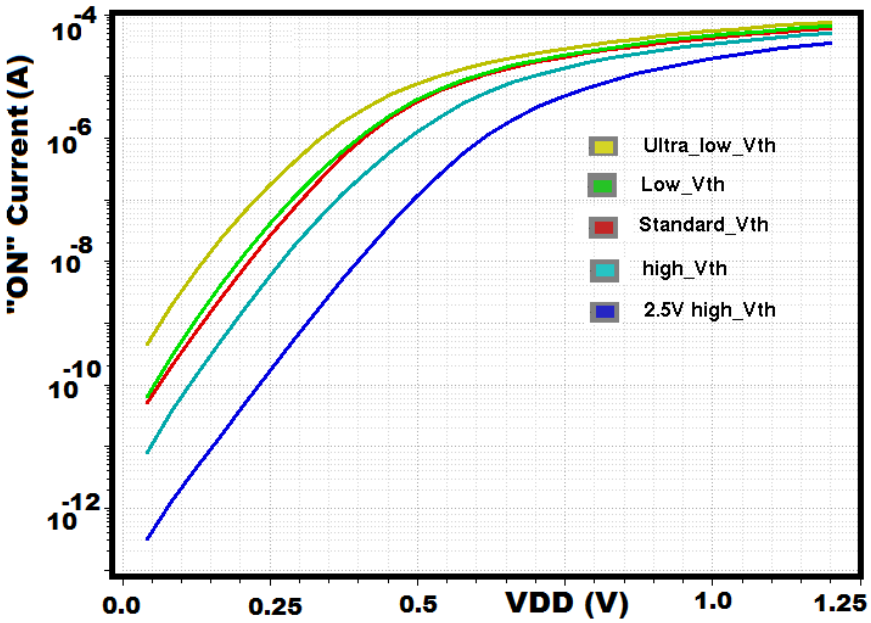
In the early days of the semiconductor industry, where the higher supply-voltage of 5 V and V_{th} above 1V were in practice, the subthreshold region was often considered as "cut-off" or "OFF" region, and device current was considered as "OFF" current (I_{off}) or leakage current. The ratio of "ON" to "OFF" currents in those high supply-voltage and high-Vth processes were normally high. However, with shrinking feature size, supply-voltage and V_{th} in the modern IC industry, the ratio of "ON" to "OFF" currents are not often as large as before. Subthreshold current ($I_{sub\text{-}threshold}$) of an NMOS device can be simplified by [20]:

$$I_{Sub-threshold} \simeq I_o.\left(\frac{W}{L}\right).e^{(Vgs-Vth)/n.vt}.(1-e^{-(Vds)/vt}) \quad (2.\ 2)$$

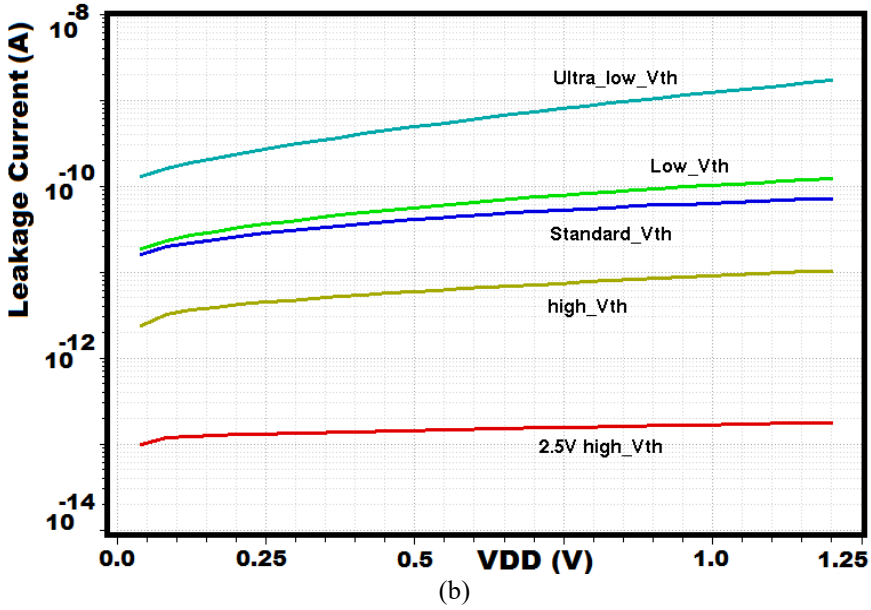
Where V_{gs} is the gate-source voltage of the device, vt is the thermal-voltage (about 25 mV in the room temperature), W/L is the device dimension, V_{ds} is the drain-source of the device, V_{th} is the threshold-voltage, I_o is the technology-dependent subthreshold current extrapolated for $V_{gs}=V_{th}$ [20], and n is the subthreshold factor (see [11][19][20]). The over-threshold (or above-threshold) current of the MOS can be simplified as [11]:

$$I \simeq \frac{1}{2}.C_{ox}.\left(\frac{W}{L}\right).\ (Vgs-Vth)^2 \quad (2.\ 3)$$

Where W/L is the device size, C_{ox} is the gate oxide capacitance per area, and V_{gs}, V_{th} are the gate source and threshold voltages respectively. As it is shown in Equation 2. 3 the device current in the above-threshold region, has quadric relation to the V_{gs} and V_{th}. However, as it is shown in Equation 2. 2, in the subthreshold region, the device current has an exponential relation to the V_{gs} and V_{th}, and has therefore sharper dependency on those voltages, comparing to the above-threshold region. This makes the subthreshold region very attractive for the Analog designers, since higher transconductance and gain, is achievable for the given value of device current. That is the reason the subthreshold region becomes more and more popular for wide range of the applications in the modern analog design, specifically for the ULV and LP applications. However, in the subthreshold region, as it shown in equation 2.1, the process, supply-voltage and temperature variations (PVT) can have significantly larger effect on the overall performance of the systems, comparing to the above threshold region, for both analog and digital design. This is the reason that often the design engineers spend substantial amount of design time and energy to satisfy the required specifications in the different PVT corners. Fig. 2.1 demonstrate the simulated current variations for different type of minimum size NMOS devices, in different supply voltages (VDD), in a 90nm TSMC process. In Fig. 2.1 (a) SPECTRE simulation results for "ON" current variation as function of different VDDs, when $V_{gs}=V_{ds}=VDD$, are shown. The results have good agreement with the theory presented in Equation 2.1 and Equation 2.2. The current variation has larger slope for smaller VDD, where the devices operating in subthreshold, for all type of the NMOS devices. In Fig. 2.1 (b) simulation results for leakage current variations across different VDDs, when $V_{gs}=0$ and $V_{ds}=VDD$ are plotted. The leakage current is smaller for the device with higher Vth, and also has relatively lower variation across different VDDs for these high-threshold devices.



(a)



(b)

Fig. 2. 1. Current variation versus different supply voltages (VDD), for minimum size NMOS in 90nm TSMC process, for different type of transistors. (a) “ON” Current, Vgs=Vds=VDD (b) Leakage Current (“OFF” Current), Vgs=0, Vds=VDD.

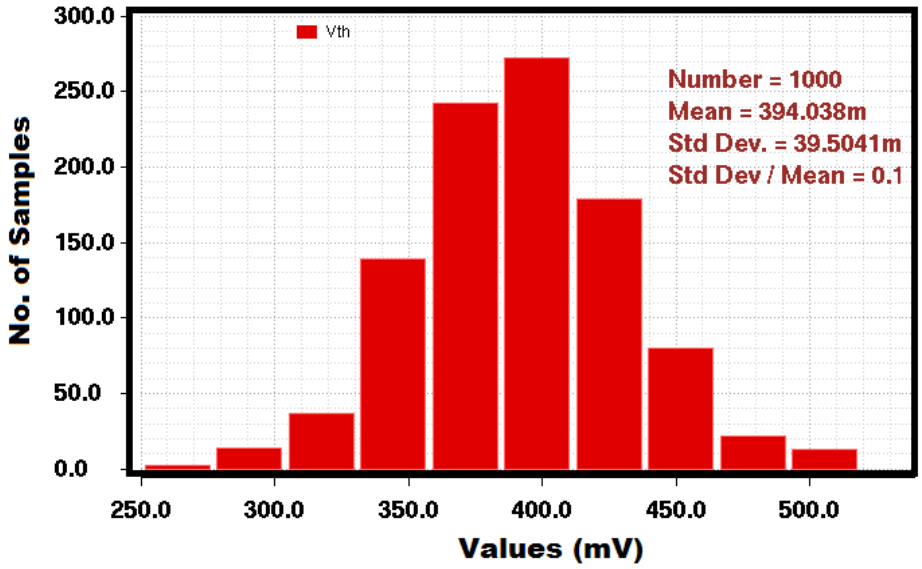


Fig. 2. 2. Threshold voltage variation for a standard-Vth, minimum size, NMOS in a 90nm TSMC process. 1000-run Monte-Carlo SPECTRE simulation utilized to extract and plot the data.

Fig. 2. 2 demonstrates Monte-Carlo simulation results, for threshold voltage variation of a standard-Vth, and minimum size, NMOS device, in a 90nm TSMC process. 1000 run Monte-Carlo SPECTRE simulation utilized to extract and plot the data.

To study the process variations effect on the performance of a simple static CMOS inverter gate in sub-threshold and above-threshold, an inverter with minimum size NMOS device, and 2x minimum size PMOS device, in a 90nm TSMC process, implemented and simulated with SPECTRE. For both devices, standard-Vth transistors utilized for simulations. Fig. 2. 3 demonstrates the 200-run, Monte-Carlo simulation results for the rise-time (10%-90%) of the inverter, when driving the similar-size inverter as load, at VDD= 0.2 V. In this low supply voltage, the devices are in deep sub-threshold operation region, and the gate is relatively slow. In addition, statistic data from Monte-Carlo simulation results, demonstrate that the gate is very sensitive to the process variations. The standard-variation value is relatively high, and is close to the mean value, and this prove substantial variation in the performance of the gate.

The same inverter has been simulated with higher power supply, VDD = 0.7 V, and statistic results from Monte-Carlo simulations are given in the Fig. 2. 3 (b). This Figure demonstrates the 200-run, Monte-Carlo simulation results for the rise-time (10%-90%) of the inverter, when driving the similar-size inverter as load, at VDD= 0.7 V. In this supply voltage, the devices are operating in the above-threshold operation region, and the gate is relatively fast. In addition, statistic data from Monte-Carlo simulation results, demonstrate that the inverter gate operating in above-threshold is significantly robust against the process variations, comparing to the sub-threshold region. The ratio of the standard-variation value to the mean value is relatively low comparing to the previous case, where the gate was operating in deep sub-threshold region. The results have a good agreement with the theory presented in the Equations 2.1 and 2.2.

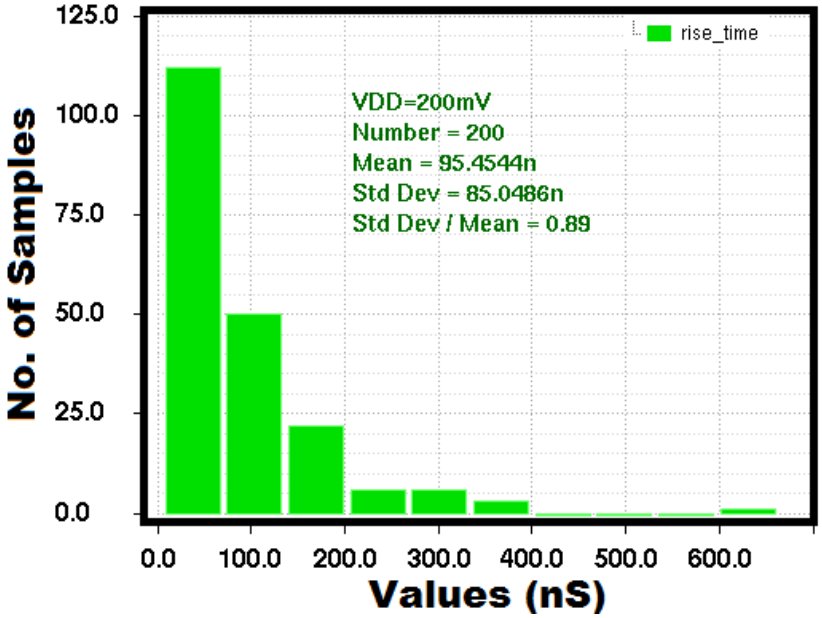
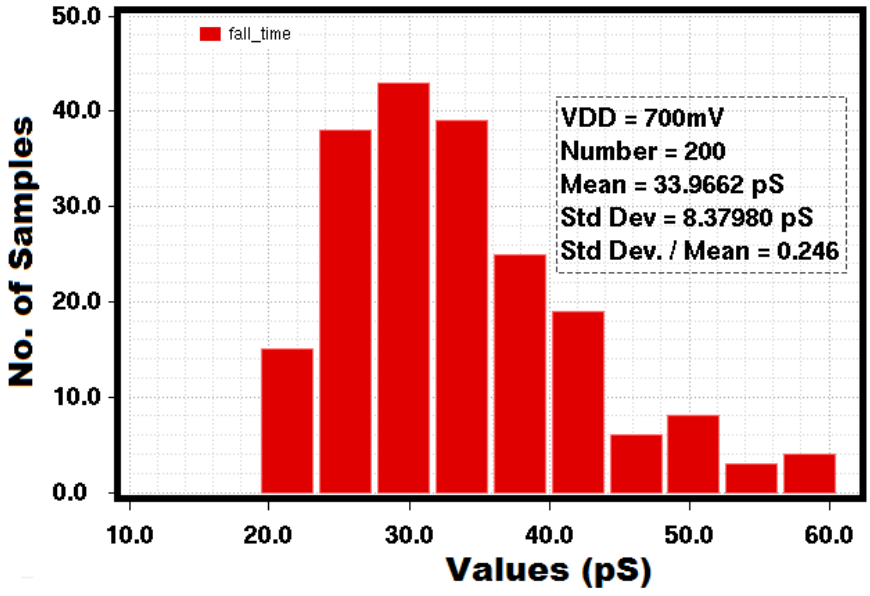
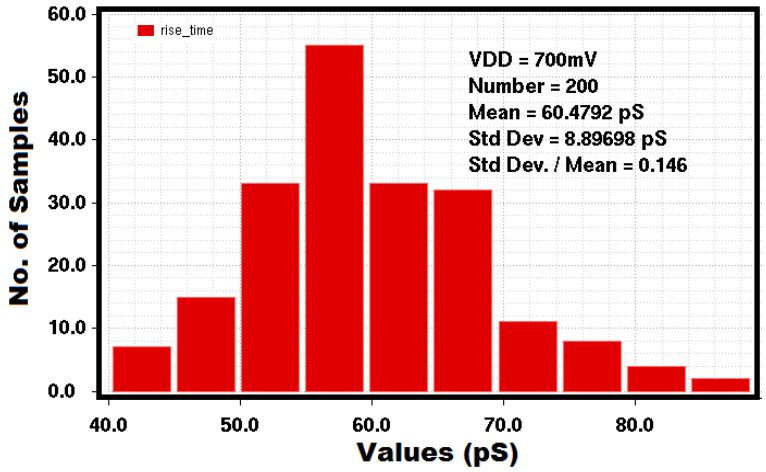


Fig. 2. 3. Rise-time (10%-90%) variation statistic (VDD=0.2 V), for an INVERTER gate with minimum-size NMOS (W/L=120nm/100nm), and 2X minimum-size PMOS (W/L=240nm/100nm) in a 90nm TSMC process, with standard-Vth transistors.



(a)



(b)

Fig. 2. 4. Rise-time (10%-90%) variation statistic (VDD=0.7 V), for an static CMOS INVERTER gate with minimum-size NMOS (W/L=120nm/100nm), and 2x minimum-size PMOS (W/L=240nm/100nm) in a 90nm TSMC process, with standard-Vth transistors.

2.3 Domino Logic

Domino logic is known as a high-performance circuit configuration which normally utilizes clocking scheme and is embedded in the static-logic environment [21]. Domino CMOS has become a popular logic family for high-performance and high-speed applications, and it is extensively used to implement high-speed processors [16-24], since they provide advantages over static-CMOS logic, including fast operation, and lower number of transistors (lower silicon area) [21-22]. Fast operation of domino logic style is basically because of the lower noise margins of domino circuits as compared to static CMOS gates. This property makes domino logic circuits highly sensitive to noise as compared to the static CMOS gates [33-36]. As on-chip noise becomes more severe with technology scaling and increasing operating frequencies, error free operation of domino logic circuits has become a major challenge [31-36], [52-53].

Domino circuits are in function very similar to the clocked CMOS circuit. In Domino logic a single clock is used to pre-charge and evaluate a cascaded set of dynamic logic blocks. The drawback of domino CMOS is that it provides only non-inverting functions because of its monotonic nature [21]. Dual-Rail Domino logic where both polarities of the output are generated, provides a robust solution to this problem [21]. The penalty associated with dual-rail domino logic is the increased power-dissipation compared to static-CMOS as well as dynamic-logic techniques [21]. This type of domino logic is widely used in the high-speed applications like high-speed

processors (e.g. 1-GHz 0.75W ARM Cortex A8 designed by INTRINSITY) and studied in detail in many papers and books [16-38]. This type of logic operates in two different phase of "pre-charge" and "evaluate". Fig. 2.5 shows the conventional domino pre-charge to 1, single-rail and dual-rail NOR gates which are studied and analyzed in detail in many references e.g. [21]. Domino logic has two phases of operation, "pre-charge" and "evaluation" phases. In the pre-charge phase, all the logic gates, become pre-charged (either 1 or 0, depend on the N-type or P-type) at the same time and in a parallel manner. In the next phase (evaluation phase) which happen in the next clock phase, the output logic is produced in a domino manner, based on the type of implemented digital function and input signals. Since the evaluating of the data happens in a domino manner, the speed of the overall implemented gate, limits by the speed of the gate in the "evaluation" phase, which is normally slower than the pre-charge phase, which happens in a parallel manner [21]. Hence the speed of the NP domino logic is determined often by the speed of the evaluation phase [21].

In this thesis domino logic style is investigated as alternative technique to increase the speed of the logic gates in the ultra-low-voltage (ULV) operation, while the available power supply voltage is limited to 300mV, and standard static CMOS is not fast enough. As mentioned before, domino logic generally utilizes smaller number of the transistors for the given logic function comparing to the standard CMOS static logic. Lower number of transistors in the domino logic style, may lead to smaller leakage currents for the iOT devices, which often utilize duty-cycling technique and operating in the sleep-mode most of their life-time.

2.4 Semi-Floating-Gate (SFG) ULV Logic

For further increasing the speed in the ULV domino logic style, the SFG technique is used to speed up the evaluation process of the logic style [40-51], [68-76]. This technique is widely used in the

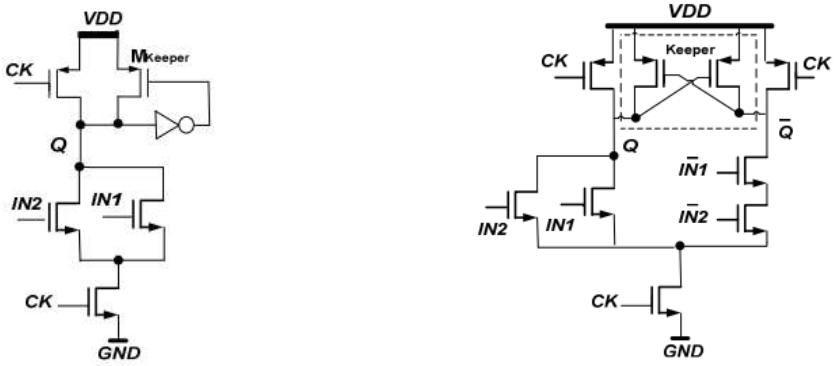


Fig. 2. 5. Conventional pre-charge to 1, dynamic NOR gates. (a) single-rail (b) dual-rail.

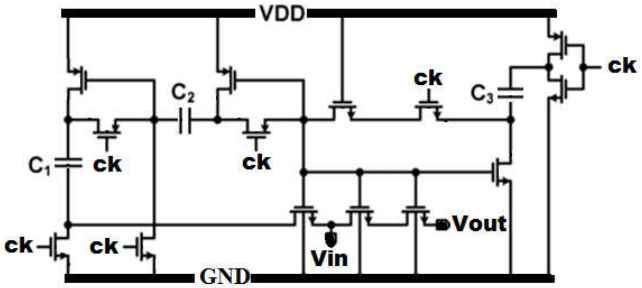


Fig. 2. 6. A double-bootstrapped sample and hold in an ULV ADC [54]

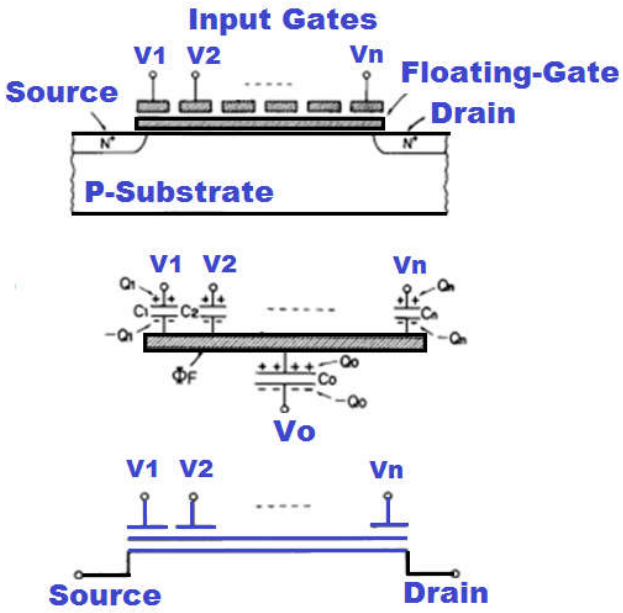


Fig. 2. 7. A neuron-MOS transistor utilizing FG technique proposed in [39].

bootstrap sample and holds, as shown in Fig. 2.6, to increase the speed and linearity of the sample and holds [54-55]. The SFG technique is used in different structures including current to voltage converters, digital to analog converters [57-58], filters, neuron MOS circuits [59-60] (shown in Fig. 2.7), amplifiers [56], and so on, to improve the performance of the structures [54-64]. As mentioned before, the SFG technique is used to increase the speed of the evaluation phase of the domino logic, as shown in different iteration of the ULV logic in Fig. 2.8 [43]. ULV7 was developed to minimize the static current in the ULV gate, and minimize power

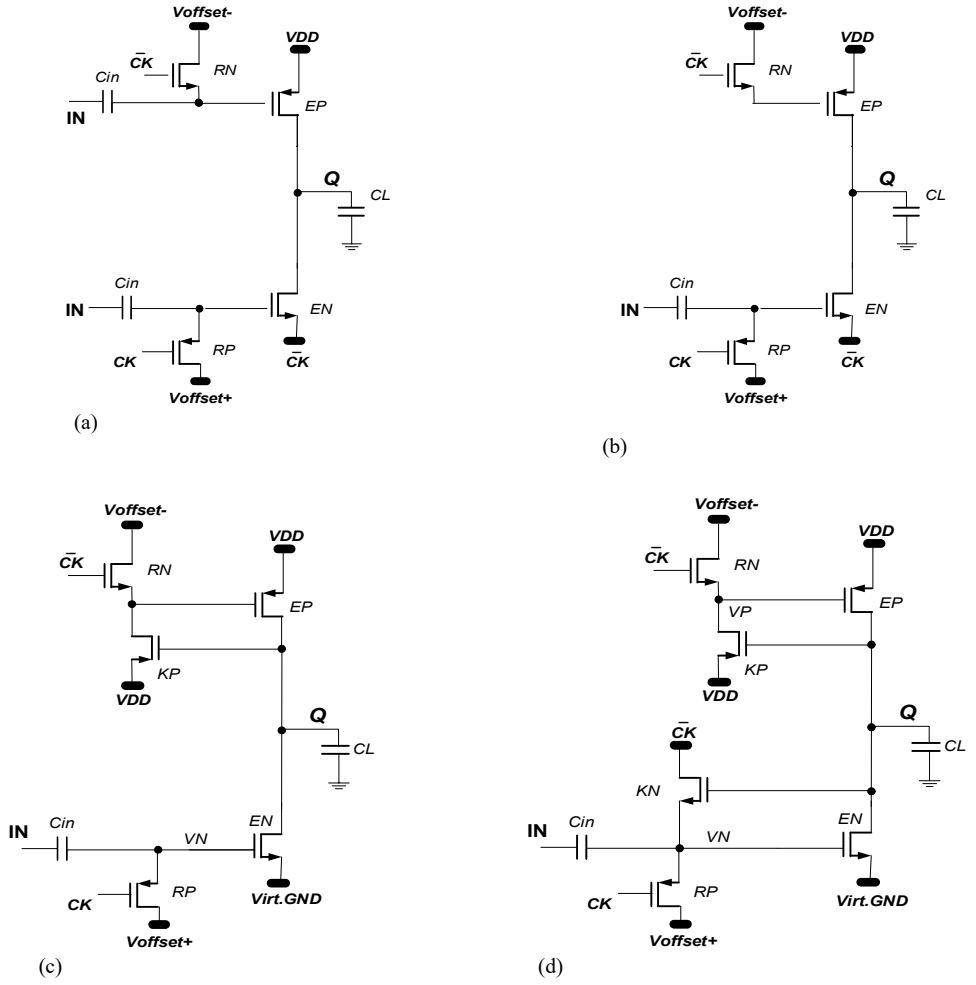
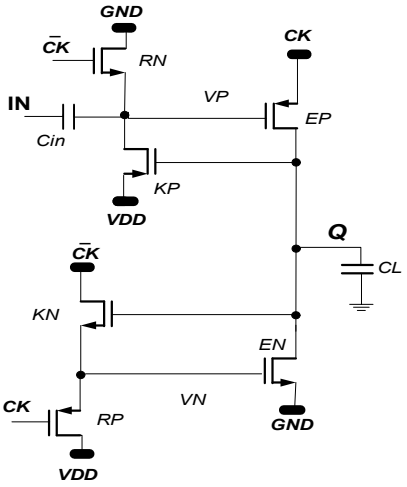
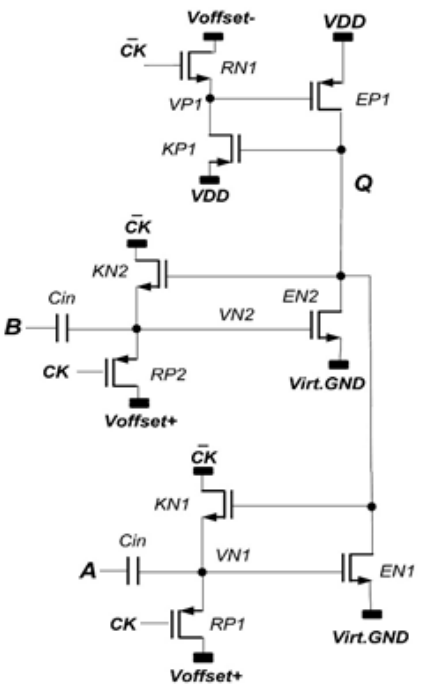


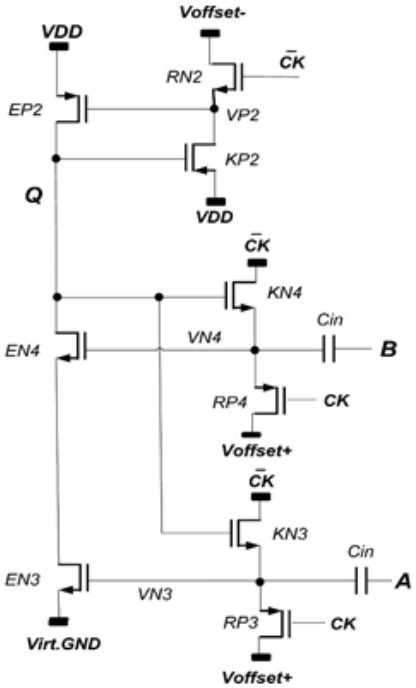
Fig. 2. 8. different iterations of SFG ULV logic ([43]) (a) ULV2 INVERTER gates [43] (b) ULV3 INVERTER gates [43] (c) ULV5 INVERTER gates [43]. (d) pre-charge to 1, ULV7 INVERTER gates [43]



(a)



(b)



(c)

Fig. 2. 9. SFG ULV logics (a) pre-charge to 0, ULV7 INVERTER gates [43] (b) pre-charge to 1 ULV NOR gate. (c) pre-charge to 1 ULV NAND gate.

consumption [43]. In the SFG technique, the main aim is to increase the gate voltage of transistors to a value larger than available power supply voltage (VDD), to increase the speed in very low voltage power supplies. The pre-charge to 1, NP domino Semi-Floating-Gate ULV (ULVSFG) inverter, and NOR gates are shown in Fig. 2.9 respectively. Voltage increases at the SFG node, due to a rising input signal can be calculated as:

$$\Delta V_{SFG} \approx \left(\frac{C_{in}}{C_{par}+C_{in}}\right).\Delta V_{in} \tag{2.4}$$

Where C_{par} is the parasitic capacitance of the SF node, and the C_{in} is the input capacitance of the gate.

As discussed in [43], the ULVSFG logic, operates significantly faster than conventional static CMOS logic [43-47]. The ULVSFG logic gates can be operated at a clock frequency more than 10 times than the maximum clock frequency of a similar complementary static CMOS gate operating at the same supply voltage [43]. However, in the modern CMOS technology nodes, there are significant leakage currents which undermine non-volatile SFG circuits [43]. SFG gates implemented in a modern CMOS process require frequent pre-charging to avoid significant leakage currents effect [43].

Fig. 2.9 (a) shows the pre-charge to 0 (p-type), ULV7 Inverter gate using SFG technique [43]. The N-type ULVSFG domino NOR and NAND 2 input gates (pre-charge to 1), are shown in Fig. 2.9 (b) and (c). The clock signals are used both as control signals for the recharge transistors RP and RN, and as reference signals for NMOS evaluation transistors EN. These kind of ULV logic gates, operate in two different phase called "pre-charge" and "evaluate" and follow the sequences in the normal NP-domino logic style [21&38]. When CK is low (0), the logic gates become in the pre-charge phase. During this phase, RP transistors turn on and recharge the gate of the EN transistors to VDD [43]. Meanwhile RN transistors turn on and recharge the gate of EP transistors to 0. Thus, EP transistors turn on and pre-charge the output nodes to VDD [43]. The keeper transistors, KN and KP, are inactive during this phase as the output node is pre-charge to VDD, and input signals are in the low (0) level since the gates follow the NP-domino logic [43]. In the evaluation phase, in both inverter and NOR/NAND gates shown in Fig. 2.9, when clock signal CK switch from 0 to 1, both recharge transistors RP and RN switch off which makes the charge on the gate terminals (Vp and Vn) become semi-float [43]. The output nodes remain at high level until an input transition occurs [43]. The input signals (IN) must be monotonically rising to ensure the correct operation for the N-type domino logic [43]. This can only be satisfied if the input signal (IN) is low at the beginning of the evaluation phase, and if IN only makes a single transition from 0 to 1 in the evaluation phase [43]. When this transition happens (IN goes from 0 to 1), the voltage of the SFG (VN) increase above VDD, based on a capacitive coupling from input node to SFG node, and this increases the current of EN devices in the evaluating phase and speed up the evaluation process [43]. In this case the keeper transistors KN will be turn off and the elevated SFG voltage will be stable. Also, the keeper transistors (KP) will be turned on and will increase the gate voltage of the Ep transistor and eventually turn the Ep transistors off. This helps to reduce the static current which directly impacts on the noise margin and the power consumption of the logic [43].

In the second scenario (when no change at the input), the output voltage should remain high. In this case, keeper transistors (KN) will continue to reduce and discharge the voltage of VN nodes and thereby turning the EN transistors off. The main necessity to have the keeper transistors KN in the ULV7, is to turn off the EN transistors, and minimize the current dissipation during the evaluation phase, when there is no raising input signals edge (input signals remain 0) [43]. This reduces the static power consumption significantly [43]. As demonstrated in [43] there is a 10.000 times lower static power consumption due to the keeper transistors [43]. Fig. 2. 10. Shows a pre-charge to 1, 3 input SFG ULV NOR gate. Fig. 2.11. (a) and (b) show 200 run Monte-Carlo, rise-time (10%-90%) simulation results, for a P-type ULV7 (pre-charge to 0), ULV SFG inverter logic and for a standard CMOS Inverter (with minimum size devices). Fig. 2. 12. Shows 200-run Monte-Carlo, Fall-time (10%-90%) simulation results, with minimum size devices for a standard CMOS Inverter and for an N-type ULV7 (pre-charge to 1), ULVSFG inverter logic at VDD=0.2 V.

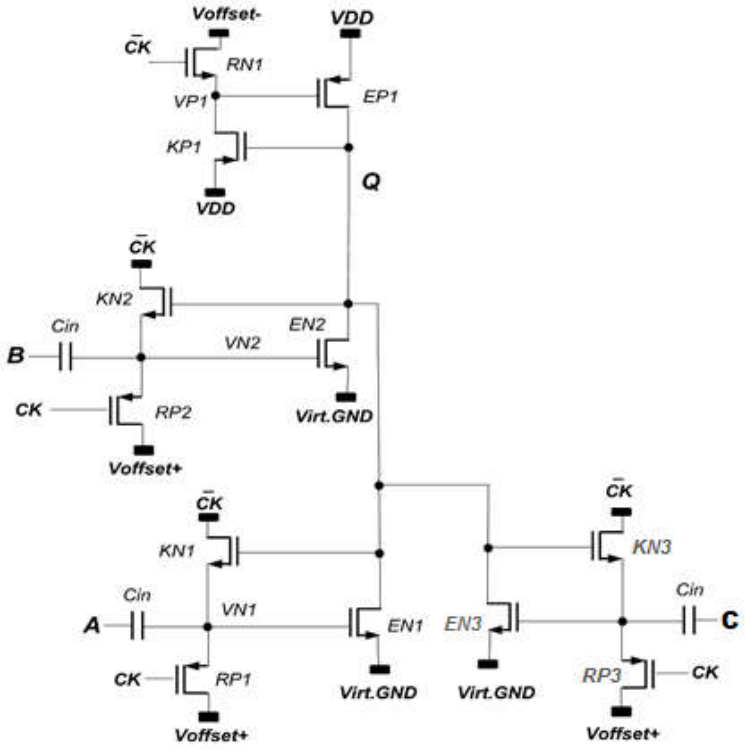
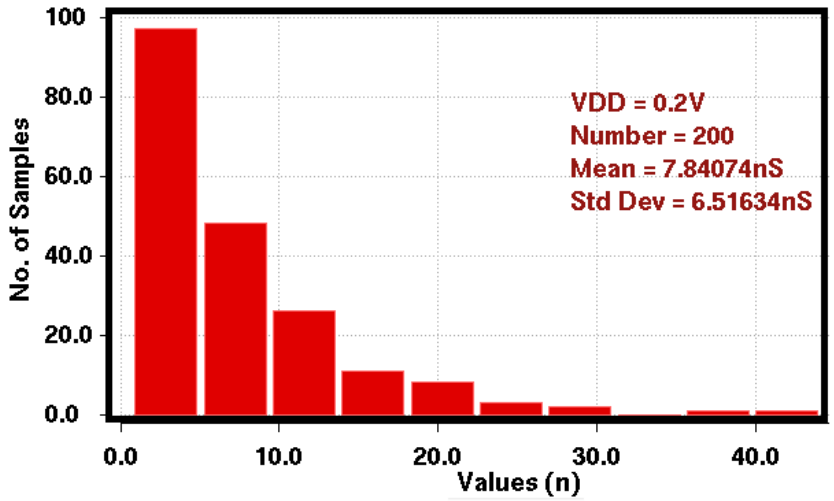
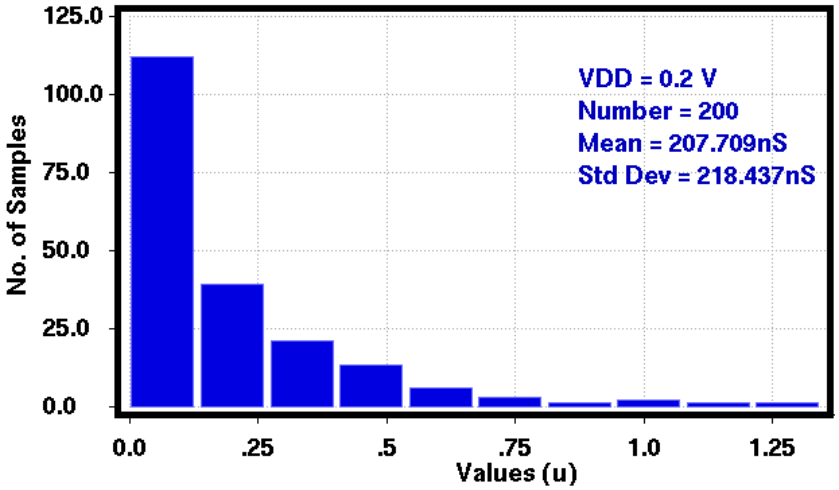


Fig. 2. 10. A pre-charge to 1, 3 input ULV7 NOR gate.

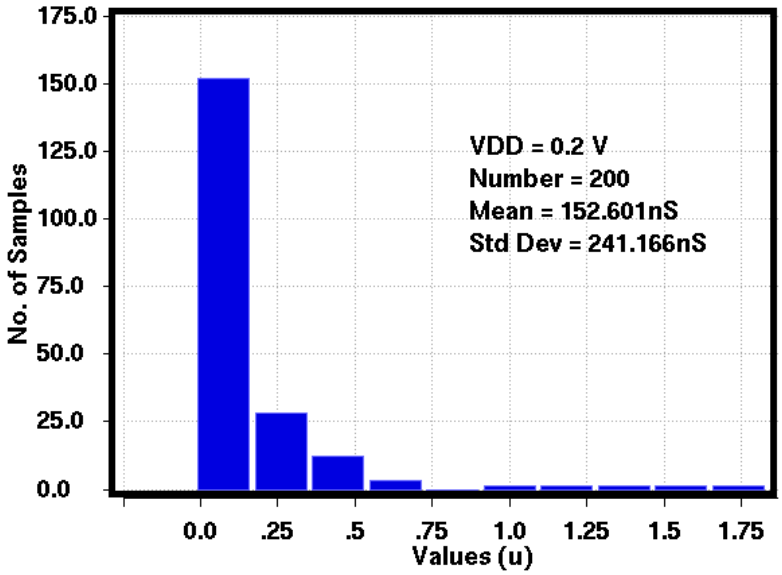


(a)

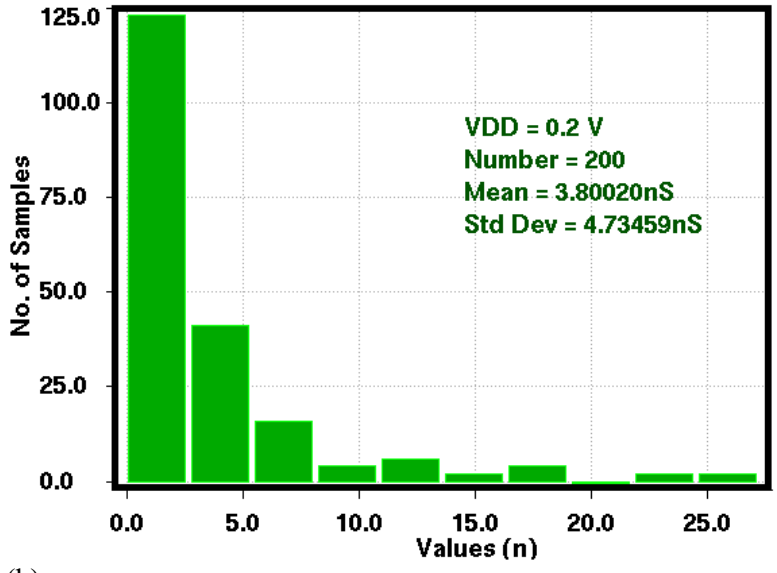


(b)

Fig. 2.11. 200 run Monte-Carlo, rise-time (10%-90%) simulation results, with minimum size devices (a) P-type ULV7 (pre-charge to 0), NP domino ULVSFG inverter logic at VDD=0.2 V. (b) Standard CMOS Inverter.



(a)



(b)

Fig. 2. 12. 200-run Monte-Carlo, Fall-time (10%-90%) simulation results, with minimum size devices (a) Standard CMOS Inverter. (b) N-type ULV7 (pre-charge to 1), NP domino ULVSFG inverter logic at VDD=0.2 V.

2.5 Summary of Papers

In this section, the summaries of the papers included in this thesis and related to this chapter are presented. Published papers related to this chapter are paper I, "High-Speed, Modified, Bulk stimulated, Ultra-Low-Voltage, Domino Inverter" [85], paper II, "An Ultra-Low-Voltage, Semi-Floating-Gate, Domino, Dual-Rail, NOR Gate" [86], paper III, " Domino Dual-Rail, High-Speed, NOR Logic, with 300mV supply in 90 nm CMOS Technology" [88], and paper VI, "NP-Domino, Ultra-Low-Voltage, High-Speed, Dual-Rail, CMOS NOR Gates" [87].

2.5.1 Paper I: "High-Speed, Modified, Bulk Stimulated, Ultra-Low-Voltage, Domino Inverter" [85]:

In the paper I, "High-Speed, Modified, Bulk stimulated, Ultra-Low-Voltage, Domino Inverter", feasibility of utilizing the bulk pins, are studied. The main purpose was to increase the speed of the logic by reducing the threshold voltages of the devices. Forward bias bulk technique is used in many applications in both analog and digital domain.

New inverters logic circuits based on the ULV7 domino logic [43] structure, were presented in which the bulk pins of the different devices in the original ULV7 domino logic inverter structure, used to speed up the circuit's operation. The bulk voltages of the transistors, in the different topologies, manipulated and the threshold voltages of these devices are reduced to speed up the circuits. The delay of the bulk manipulated ULV7 domino logic inverter is reduced more than 40% in both pre-charge and evaluating phases [85]. Different FGULV domino logic inverter topologies were considered, and advantages and disadvantages are studied. Higher speed in the lower supply voltages and robustness against process variations are the main advantages of the proposed approach in comparison to the conventional FGULV and other ULV methods.

In the ULV operation of below 300mV supply voltage, the possibility of the latch-up reduces significantly. However, for the fare evaluating of the performance, in the bulk manipulated ULV7, the silicon fabrications and measurement results should be considered for the further studying of the technique.

2.5.2 Paper II "An Ultra-Low-Voltage, Semi-Floating-Gate, Domino, Dual-Rail, NOR Gate" [86]:

In this research paper, a new SFGULV dual-rail NOR logic gate based on the SFG structure is presented. Higher operational speed in the lower supply voltages was the main advantages of the proposed approach in comparison to the previous domino dual-rail NOR gate. The simulation results in a typical TSMC *90nm* CMOS technology, using CADENCE software, show that the proposed NOR gate is more than 20 times faster than conventional dual-rail NOR gate at the same supply voltage of 300mV. This paper is discussed more in details in the journal version of the paper [87].

2.5.3 Paper III "Domino Dual-Rail, High-Speed, NOR Logic, with 300mV Supply in 90 nm CMOS Technology" [88], and Paper IV "NP-Domino, Ultra-Low-Voltage, High-Speed, Dual-Rail, CMOS NOR Gates" [87]:

Paper IV “NP-Domino, Ultra-Low-Voltage, High-Speed, Dual-Rail, CMOS NOR Gates” [87] and paper III, “Domino Dual-Rail, High-Speed, NOR Logic, with 300mV supply in 90 nm CMOS Technology” [88], presents a new NOR gate based on the ULV SFG dual- rail domino logic. Paper IV is a complete version of the paper II and paper III. The speed of the NP domino gate increased significantly by applying the SFG technique to the conventional dual-rail NOR gate logic, at the cost of increasing the complexity of the structure. The simulation results in a typical TSMC 90nm CMOS technology show that the proposed NOR gate is more than 20 times faster than conventional dual-rail domino NOR gate. Higher speed in the lower supply voltages and robustness against process variations, are the main advantages of the proposed approach in comparison to the conventional domino dual-rail NOR gate. In the paper III, “Domino Dual-Rail, High-Speed, NOR Logic, with 300mV supply in 90 nm CMOS Technology” [87], a new ULVSFG dual-rail domino logic NOR gate, designed with new keeper structure. The new keeper structure makes the SFG technique more robust against the delay of the input signal in the large chain of NP domino logic structures. Using the new keeper structure, high-depth logics are feasible to implement with the SFG technique. The new keeper structure can be applied to any dual rail NP domino logic gates, including multi input NOR/OR, NAND/AND gates, and flip-flops utilizing SFG technique. For further evaluating of the performance of the proposed technique, the silicon fabrication of a relatively large chain of logic gate (including clock drivers) should be implemented, and measurement results should be considered for the further studying and improving the proposed technique.

2.6 Fabricated ULVSFG Domino (ULV7) Logic Inverters

To study the effectiveness of the ULV SFG domino inverter logic on silicon, and study the practical challenges of the ULV7 logic, a test chip including different type of ULV7 with different feature sizes were designed and fabricated using TSMC 90nm CMOS process. In order to compare and evaluate their speed, their equivalent standard CMOS inverters also fabricated in the same chip. The N-type and P-type versions of the ULV7 SFG domino inverters, shown in Fig. 2. 8 (d) and Fig. 2.9 (a), were designed and scaled to drive the capacitive load of a test setup which was estimated to be around 20pF. This capacitive load is due to a combination of parasitic capacitive of oscilloscope probe, PAD and PCB trace. The fabricated N-type and P-type domino inverter are shown in Fig. 2.8 (d), and Fig. 2.9 (a) with utilized feature sizes shown in Table. 2.1 and Table. 2.2. Low-threshold devices chosen for the PMOSs, and NMOSs are standard devices. The theoretical functionality and details of ULV7 is discussed in section 2.4 and [43]. Input capacitor (Cin) of 890 fF was chosen for both inverters.

The measured 1 to 0 transient (evaluation phase) of the fabricated N-type inverters are shown in Fig. 2.13. The measurements show that the designed N-type ULV7 with given feature size is more than 7 times faster than similar size conventional CMOS inverter in a 300mV supply voltage. The P-type version was 2.5 time faster than similar size standard CMOS inverter. The micrograph of the fabricated chip is shown in Fig. 2. 16. Cin capacitor (Cin= 890 fF) implemented by using standard CRTMOM capacitor type. To implement smaller capacitors (in the range of the Femto Farad) in the SFGULV logic, fringing parasitic capacitances similar to those of MDAC capacitors in the SAR ADCs [154-157], can be used (see section 3.4 and [154-157]). Micrograph of the packed chip including designed ULV7, with bonding diagram and with JLCC84 package is shown in Fig. 2.15. CADENCE software is used to design and simulate the chip. After Schematic and layout (shown in Fig. 2. 14) implementing of the circuits, DRC, LVS are done by CALIBRE

tool. Chip production has been done via EUROPRACRICE program of IMEC in a TSMC 90nm CMOS process. Bonding diagram and JLCC84 Packaging are also done by IMEC. PCB board shown in Fig. 2. 17, designed with EAGLE software for chip measurements.

Table 2.1: Size of transistors used in the fabricated N-type ULV7 inverter gate

Device	W μm/ L μm	Device	W μm/ L μm
EN	20 / 0.1	RN	3 / 0.1
KP	6 / 0.1	KN	0.4 / 0.1
EP	18 / 0.1	RP	6 / 0.1

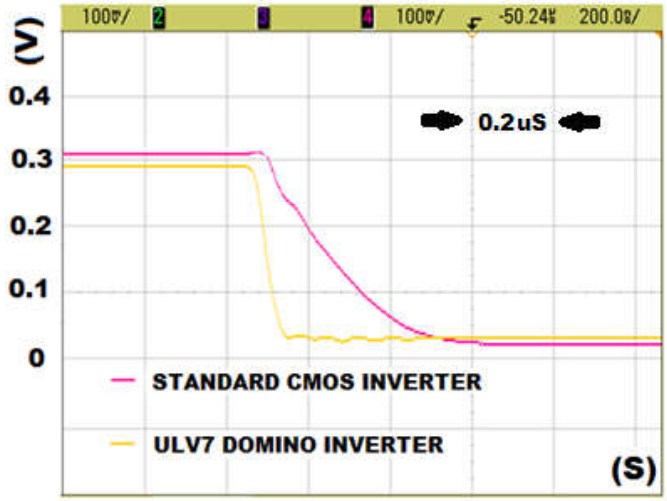


Fig. 2. 13. 1 to 0 transient of inverters (Evaluation phase), VDD=0.3V.

Table 2.2: Size of transistors used in the fabricated P-type ULV7 inverter gate

Device	W μm/ L μm	Device	W μm/ L μm
EN	20 / 0.1	RN	3 / 0.1
KP	6 / 0.1	KN	0.4 / 0.1
EP	5.6 / 0.1	RP	6 / 0.1

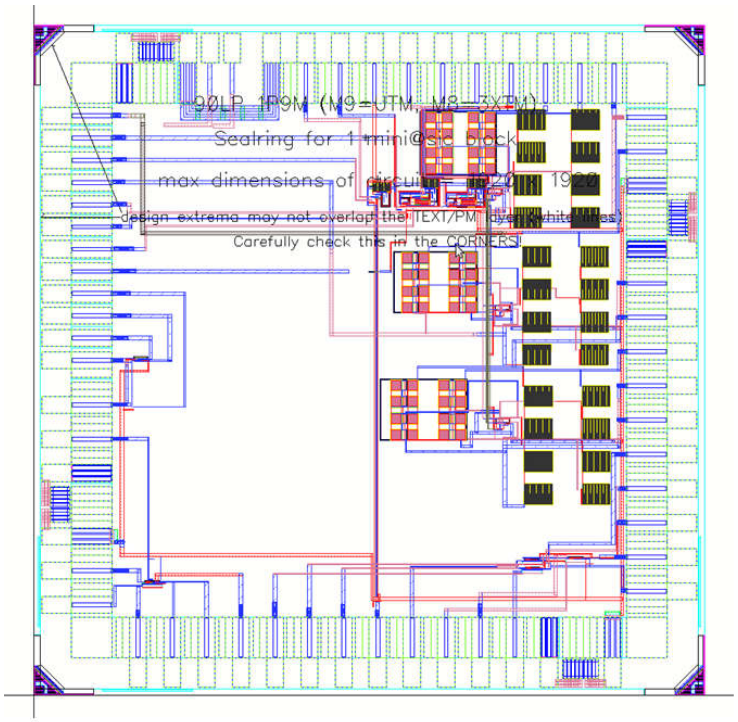


Fig.2. 14. Layout of the chip with Pads.

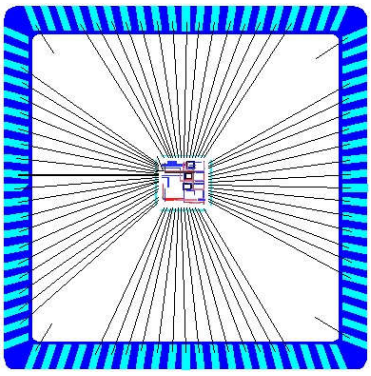


Fig. 2.15. Chip including designed ULV7, with bonding diagram and with JLCC84 package.

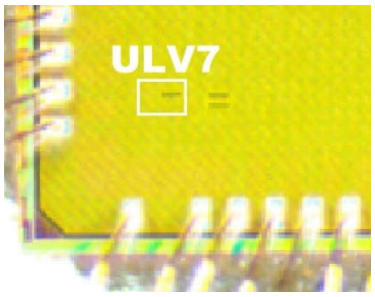


Fig. 2. 16. Micrograph of the chip including designed ULV7.

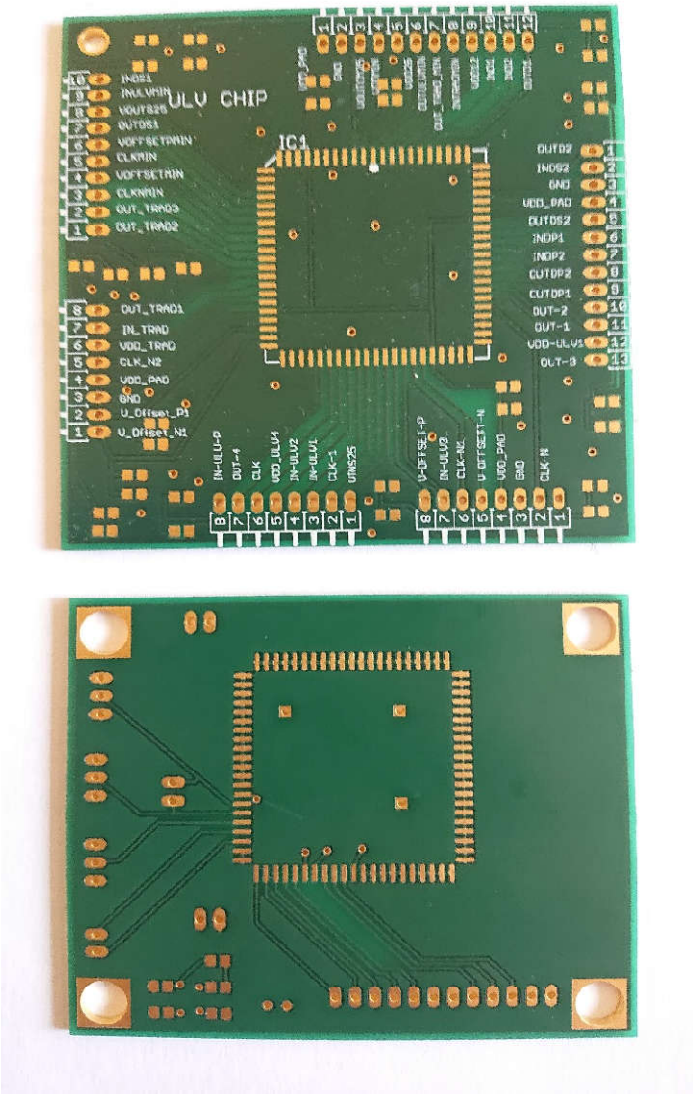


Fig. 2. 17. Two-layer PCB board prepared by EAGLE software for measuring the chip.

Chapter 3

ULP and ULV Analog Circuit Techniques for iOTs

In this Chapter the circuit design challenges in the ULP and ULV analog domain for the iOT applications discussed by reviewing the literature. Section 3.1 briefly discusses different widely used sub-modules in the iOT devices and design challenges for these modules. Section 3.2 addresses some design challenges for the ULP and ULV reference circuits in iOT devices. Section 3.3 discusses the challenges of the designing high performance amplifiers in the ULP and ULV domain. Section 3.4 briefly discusses the details of a fabricated ULV and ULP energy-efficient SAR ADC, which was powered-up successfully with utilizing a simple energy-harvester in the lab and functionality verified successfully. Finally, section 3.5 provides summary of the published paper related to this Chapter.

3.1 Circuit Design Challenges for ULV and ULP iOTs

CMOS technology down-scaling is posing difficulties for analog circuit designers [92-93]. Leakage currents, and complexity of the device modeling are increasing while intrinsic-gain and supply voltages are decreasing [91-96]. For the high-precision sub-blocks such as high-resolution data-converters (ADCs and DACs) which intensively utilize switched-capacitor circuits, decreasing dc-gain and supply-voltages, are increasing the difficulties of implementing a high-precision charge-transfer operation in a negative-feedback loop [92-96]. For these types of applications, one of the most important sub-blocks is amplifier. Amplifiers should have high open-loop gain, low noise, and low power consumption, and at the same time should have higher speed and stability in the negative-feedback configuration [92-96]. Satisfying these requirements often poses difficult challenges for the designers and requires innovative techniques in the modern technologies [91-96].

Fig. 3.1 shows different sub-blocks in a typical ASIC for wide range of the applications. These ASICs normally utilize power managements blocks to provide required supply voltages to different sub-blocks. The power management blocks in these systems normally consists of bandgap references (BGRs), low-dropout-regulators (LDOs), dc-dc converters, ac-dc converters, and so on. Energy sources for these systems are often batteries or energy harvesters. There is an increasing demand to utilize energy harvesters in modern iOT systems. In the signal chain normally iOT devices utilize pre-amplifiers to increase the signal swing range that can be detectable for the data converters, and filters that normally used to suppress unwanted signals. Also, ADCs are important part of this signal acquisition systems. ADCs are mainly needed since the information in nature, and output signal of sensors are mainly analog, while our processors are mainly digital. Therefore, ADCs are needed almost in any signal chain, and they are often one of the power-hungry blocks in the chain. SAR ADCs becoming more and more popular for these applications since they are generally a power efficient topology as do not use blocks with static currents and are compatible with new CMOS processes. In addition, different type of filters such as passive, or active intensively used in any signal acquainting systems. Discrete time and continuous time filters such as gm-C filters are developed for these types of applications [93].

Amplifiers are one of the widely used sub-blocks in these iOT systems. For instance, in the power managements block, most of the BGRs, and LDOs require high-performance amplifiers to meet their requirements. However, the requirements for these amplifiers are varies and often depend on the application, available energy, and type of signal (speed and accuracy) that should be

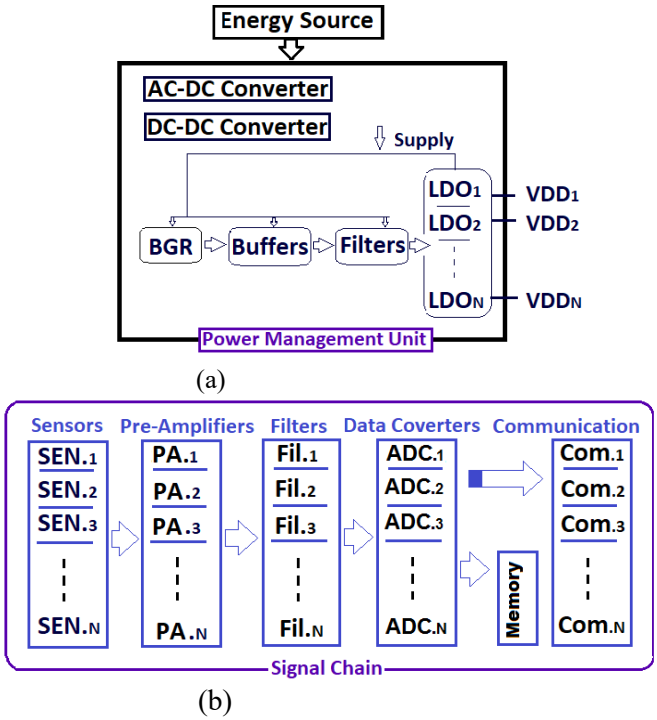


Fig. 3. 1. (a) Typical power management block (b) Typical signal acquisition/processing chain.

processed by the iOT device. The main issues for the modern amplifiers in the submicron CMOS technologies are limited intrinsic-gain of transistors, speed-gain tradeoff, leakage current, and static current consumption [92-93].

For data transceivers in the commercial iOT devices, different standards and topologies are proposed and utilized. Low-energy-Bluetooth, Zigbee, Low Power Wide Area Networks (LPWANs), Wi-Fi, Radio Frequency Identification (RFID) are some of these technologies that used based on the available power budget, required data and so on. However, these standards are still power hungry and not suitable for applications with extremely tight power budget. Reducing the leakage current in the sleep mode is a challenging task for these modules. All over the globe, promising wireless communication solutions published in literature for next generations of the iOT devices. For example, for the ultra-low data rate sensor applications, P.P Mercier, et. al, proposed a sub-nano watt transmitter and antenna system, which achieves an average power consumption as low as 78 pW [97]. The system operates at a duty-cycled data rate of 1 bit per second (bps) and is fabricated in a 0.18 µm CMOS process [97]. The low complexity architecture, in combination with aggressive power-gating techniques and device sizing optimizations, reduced the standby-power of the transmitter to 39.7 pW at 0.8 V supply voltage [97]. The topology is suitable for low speed applications such as body implants systems, processing very slow signals.

3.2 ULP and ULV Reference Circuit Design Challenges

The BGR circuit is one of the most popular reference generators that successfully utilized in almost any high-precision systems. For example, BGRs are extensively utilized to generate a regulated supply voltage for the different blocks in the iOT systems as shown in Fig.3.1 (a). As another example, utilizing a BGR for an ADC reference generator circuit, is a must (see [102]). The conventional BGR circuit is still popular in both industry and academic research [98]. The output voltage of the conventional BGR is 1.25 V, which is nearly the same voltage as the bandgap of silicon [98-99]. This fixed output voltage of 1.25 V limits the application range of the circuit. The BGR proposed in [99] generates lower output voltage and successfully operated with sub-1-V supply [99]. Stability, power consumption, area, functionality in lower supply voltages, power supply rejection, noise and more specifically low frequency noise (Flicker noise), are challenging factors that generally should be handled in designing any BGR circuit for given application. [98-103].

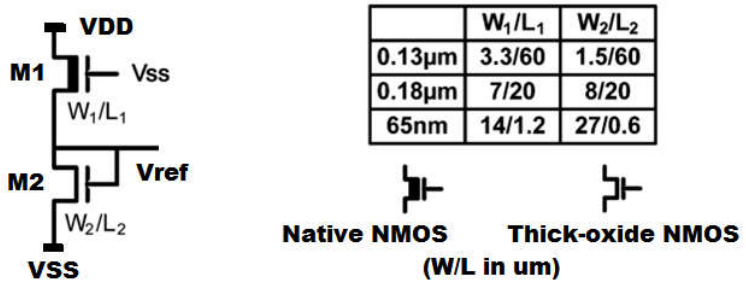


Fig. 3. 2. (a) A 2T ULP, and ULV picowatt BGR proposed in [100]. (reproduced from [100])

Fig. 3.2 shows a 2T BGR topology proposed in [100] for the ULV applications. This topology is very attractive for the sensing systems such as biomedical implants, and infrastructure monitoring systems, where the overall system consume only picowatts to nanowatts in standby and active mode, respectively [100]. The fabricated prototype chips in 0.13 μm, consumes only 2.22 pW and the lowest functional supply voltage is 0.5 V [100]. A comprehensive study about ULV and ULP reference circuits are done in [100] and some energy efficient and ULV and ULP reference circuits are also proposed in [100], which are suitable solution for iOT applications. However, the value of output voltage in [100] is relatively low and boosting this small voltage to a higher voltage require additional circuits which normally consumes significant power. BGR circuits are normally located at the beginning of the reference generation chain. This means that the noise of these circuits amplifies by the other blocks further in the chain. To suppress noise in the chain, very large capacitors that are normally off-chip, are used (see [102]). Another technique is the chopping method, which is very useful technique to suppress the low-frequency noise which is often the dominant source of the noise at the output of the chain [102].

Fig. 3. 3 (a) shows a typical conventional LDO structure which is extensively used in both industry and academic research [93-94]. Similar topology also often used to generate reference voltages for the ADCs and DACs in both single ended and differential modes [93,94,102]. Size of the power-PMOS (shown as MP in Fig. 3.3 (a)) and other devices change depending on the application and availability of the power, and load requirements. Native transistors are also used instead of the MP device to supply the required current of the load [93-94]. A comprehensive study of the LDOs and their performance merits such as PSRR, noise, stability, is done in [94].

For the ULV and ULP BGRs and LDOs, that receive sub-volt supply from an energy-harvester, designing error-amplifier is a challenging task [103]. As it discussed in [103] and shown in Fig. 3. 3 (b), for the ULV error-amplifier (EA) with supply voltage of about 0.65 V, the reference voltage from BGR, should be as low as 50 mV in order to keep the P-type differential pair of the EA in the saturation mode. Producing such low value reference voltage is not normally easy and is somewhat impractical to implement [103]. However, utilizing N-type differential pair in the error-amplifier (at the cost of higher flicker noise), or utilizing bulk driven p-type differential pair (at the cost of increased latch-up risk) in the error-amplifier may relieve this limitation. As a solution for this limitation, Wei-Chung Chen et. al, proposed a current-mode and compact structure that eliminate utilizing voltage-mode error-amplifier with an input differential pair, as shown in Fig. 3. 4. The topology merges the reference-generator with a simple LDO, resulting a compact structure that operates with supply voltage as low as 0.65 V and produces a 0.6 V output voltage that supplies a biomedical ASIC chip. A relatively short chain in this work may provide a low noise solution, which is very attractive for both supply and reference generator for the high-precision data converters.

While the reference circuits are known traditionally as always-ON blocks, recently duty-cycling is used to further minimize the power consumption of these circuits [104,102]. For instance, the duty-cycled reference generator circuit shown in Fig. 3.5 is proposed in [104] for the energy-efficient SAR ADCs. At 0.8 V VDD, the measured power consumption is 38 nW and at the

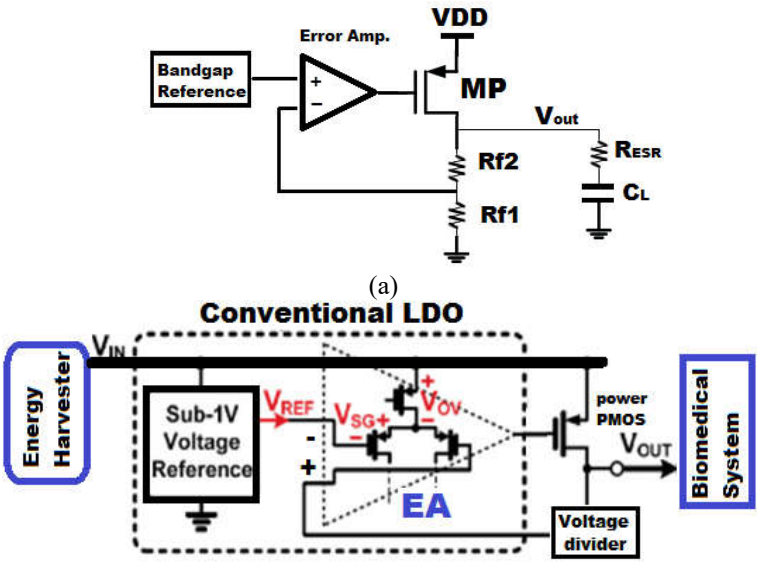


Fig. 3. 3. (a) A conventional LDO with error-amplifier (EA) [93-94] (b) An LDO in a ULV biomedical application. (reproduced from [103])

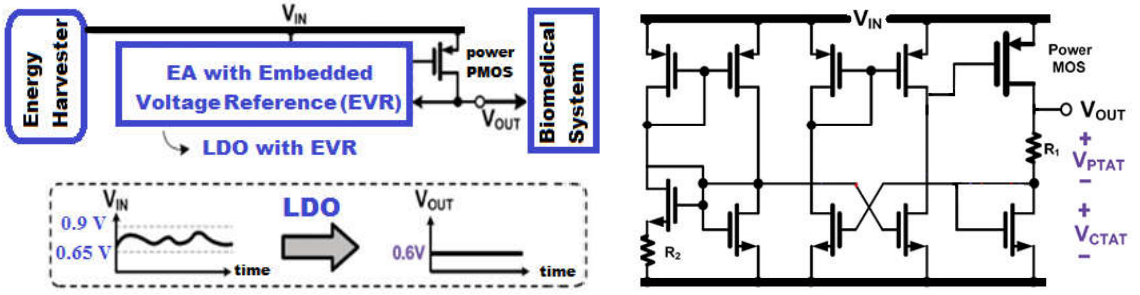


Fig. 3. 4. (a) A ULV LDO and reference generator proposed in [103] (b) Transistor level implementation of the LDO and reference circuit in the [103] to supply regulated 0.6 V to biomedical system. (reproduced from [103])

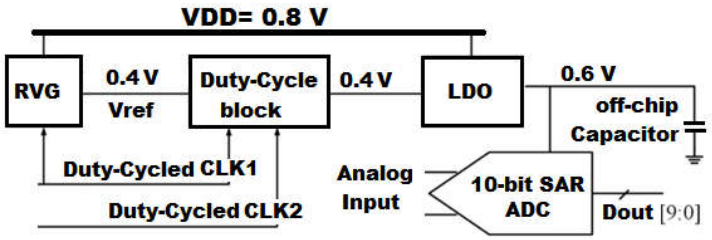


Fig. 3. 5. A duty-cycled, reference generator topology for ULP SAR ADCs proposed in [104]). (reproduced from [104])

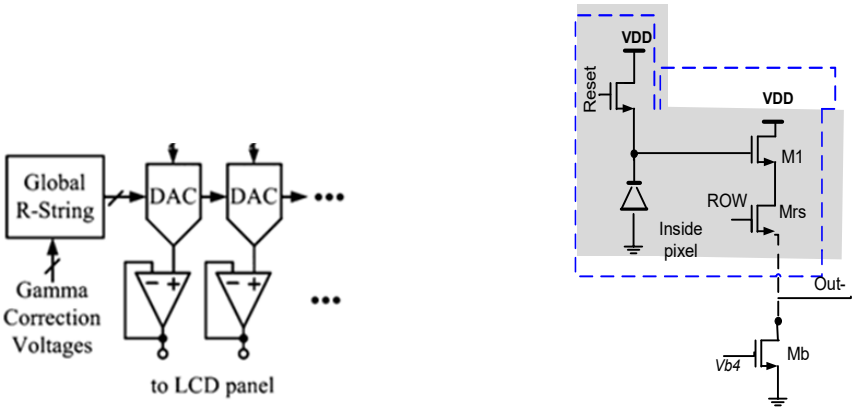
minimum functional supply of 0.62 V, the measured power consumption is 25 nW. At 10% duty-cycle of the reference generator, the power consumption reduced to only 3.7 nW from 0.8 V VDD, which is far less than that of the ADC core [104]. Comprehensive information about sub-nanowatt power management units and reference circuits provided in [106].

3.3 Design Challenges of ULV and ULP Amplifiers

In this section, design challenges of ULP and ULV amplifiers discussed since they are one of the widely used sub-blocks in any iOT devices. For example, BGRs, LDOs, filters, LCD column buffers, pixel readout circuits, ADCs, and transceivers require high-performance amplifiers to meet their requirements. However, requirements for these amplifiers varies and often depend on the application, available energy, and type of signal that should be processed by the iOT device. The main issues for these ULV amplifiers in the submicron CMOS technologies are limited intrinsic-gain of transistors, speed-gain tradeoff, leakage current, lower swing, and static current consumption [91-96].

Fig. 3.6 shows some examples of the amplifiers in the closed loop and open loop configurations. In the iOT devices which utilize LCDs, the buffer amplifiers extensively used in the column driver of the LCD panels, in order to drive a heavy capacitive load, as it depicted in Fig. 3.6 (a). These buffers normally employ closed loop amplifiers to drive a heavy capacitive load around 1-10 nF depending on the size and resolution of the display. Energy efficiency is very important for this LCDs, since they are one of the most power-hungry parts of these iOT devices [136-145]. As another example, Fig. 3.6 (b) shows an open loop amplifier (source follower) used extensively in commercial image sensors to readout the pixel data and deliver the data to other signal processing units, outside pixel arrays. In this case the gain of the source follower amplifier is normally less than 1 (typically around 0.8) and at the same time the buffer imposes a dc-shift to the input signal [109] and consequently it demands a relatively high supply. This limits the minimum value for the supply voltage in the imager that also affects the dynamic range of the image sensor. Nonlinearity of these buffers also limits the performance of the imagers [133-134].

Modern transceivers are also example of systems that require high performance amplifiers. The industry need for high-speed transceivers has resulted in an increasing demand for high-resolution and high-speed data converters such as delta-sigma and pipeline ADCs. Designing high-performance switched-capacitor filters and OTAs for such applications is a challenging task in modern CMOS technologies with limited intrinsic gain [91-96]. Traditionally, the speed-accuracy trade-off is one of the most important challenges for the analog circuits. Fast settling needs both a high unity-gain bandwidth (UGBW) and a high slew rate (SR), whereas accurate settling requires a high dc-gain [91-96]. Compensated multistage OTAs and cascode structures, such as telescopic, Folded cascode (FC), and triple FC, have been widely used to provide the required specifications. High dc-gain amplifiers usually utilize cascoding and cascading techniques



(a) (b)

Fig. 3. 6. (a) A closed-loop buffer amplifier used in column driver of a LCD (reproduced from [108] (b) A source follower buffer amplifier (formed by M1 and Mb devices) in commercial image sensors [109].

with long channel-length devices biased at relatively low bias current levels. On the other hand, high-speed amplifiers often utilize single-stage (SS) designs with short channel-length transistors, biased at high current levels to speed-up the circuit [93]. In cascading of gain-stages, each stage normally produces a low-frequency pole and results in lower UGBW and instability (lower phase margin) for the structure [93]. The triple-cascode amplifiers often provide higher dc-gain at the cost of lower signal swing range, lower UGBW, and complexity of the bias generator circuit [92-93]. The gain boosting techniques presented in [110-112] are variations of the regulated cascode (RGC) structure presented in [113] and [114] to enhance the Output Impedance (OI) of the cascode structure. Extra gain-boosting amplifiers are used to boost the OI and dc-gain of the OTAs. While the technique increases the OI and gain, it comes at the cost of increased power, area, settling time (du to pole-zero doublet), complexity and noise. These challenges become more difficult to handle in the modern CMOS technologies, in which a smaller intrinsic-gain imposes the utilization of complex high-gain topologies for the auxiliary amplifiers.

To increase the dc-gain of the amplifiers, positive feedback technique is used in some research works [116-121]. B. Nauta used the positive feedback (negative impedance) to increase the gain of the simple inverter-based amplifiers and implement high-speed transconductance-C filters [116]. The technique attracted many researchers to improve the performance of the structure, since the structure provide fast operation. Laber and Mayer utilized the positive feedback concept to increase the gain of the FC OTA [117] for the high-frequency, high-Q CMOS switched-capacitor filters. Recycling FC [115] improves the performance of the FC at the cost of reducing the phase margin and adding extra nodes to the FC topology, and the gain enhancement value is not sufficient for high-precision applications.

Inverter-based amplifiers are used extensively in recent ULV systems, where the lower supply voltage and consequently lower swing range of the structure prevents utilizing the conventional differential pairs at the input stage of the amplifiers [122-125]. Inverter and cascode inverter amplifiers, are used in ULV audio delta-sigma modulators, and often designed in subthreshold region where the transistors has higher transconductance for given bias current [123].

In order to overcome the limitation of the input swing range of the differential pairs in amplifiers, native transistors are also utilized to increase the input common mode range at lower supply voltages of 0.5 V (see [126]).

Recently, bulk amplification attracted many researchers to investigate the possibility of utilizing bulk terminals of the transistor to increase the gain of the amplifiers. It is considerable that the possibility of latch-up is reduced significantly for the supply voltages lower than 0.5 V [128-129].

As mentioned before, the ULV systems, suffer from lower maximal input/output signal swings in the analog circuits that lead to lower dynamic-range. The minimal detectable signal value is normally determined by the integrated noise that normally do not improve with technology downscaling. For these ULV systems, fully differential circuit topologies are very widely used structures due to their larger signal swing and also better supply and substrate noise rejection performance [9-10].

Switch-capacitor techniques, such as correlated double-sampling (CDS) and correlated level shifting (CLS) are used to decrease errors from finite OTA gain [130-132]. As mentioned before, in the modern technologies with lower supply voltages, lower amplifier dc-gain and lower output swing range, are two limitations for the ULV analog circuits. These limitations are more challenging at lower supply voltages where limited headroom prevents the utilizing of cascode structures to improve the dc-gain [131-132]. Gain variation across output voltage swing is another challenge for this ULV amplifiers. These limitations are discussed in detail in [131]. The problem is illustrated in Fig. 3. 7 for a two-stage amplifier in a 0.18um process. The circuit has a closed-loop gain of two, but it falls short because of the finite dc-gain of the amplifier. The open-loop gain of this amplifier is approximately 36 dB. When configured for a closed-loop gain of 2, the overall loop gain is about 30 dB. This loop gain decreases dramatically when the output is near the rails as the driven second stage device enters the linear region, as it is shown in Fig. 3.7 (a). Fig. 3.7 shows that with a loop gain of 30 dB the closed loop gain is only 1.95 and this poor gain is maintained only over a small output range [131]. This structure is expected to have a 5 bit performance with a useful swing of 0.6 V [131]. However, with CLS technique the performance can be better than 10 bits over most of the supply range as discussed in [131] in details.

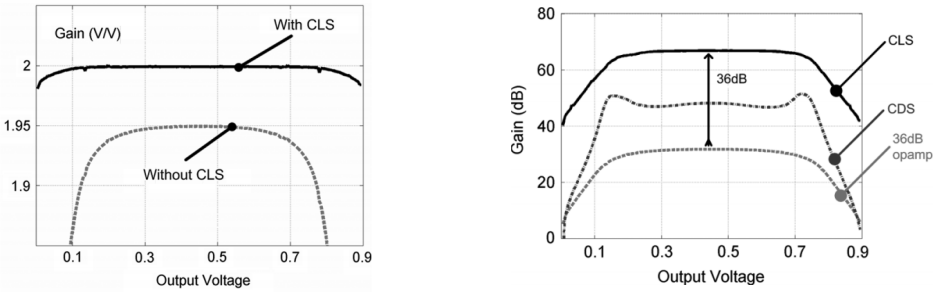


Fig. 3. 7. (a) Output voltage with and without CLS technique [131] (b) Dc-gain comparison. (reproduced from [131])

3.4 Fabricated Energy-Efficient ASIC for iOT and Energy Harvesters

This section briefly explains a fabricated nano-watt ASIC that designed during this research work. To study the feasibility of powering a battery-free miniature iOT system with an energy harvester an Ultra-low-energy ASIC including a charge redistribution SAR ADC with internal clock generator is designed, fabricated and measured during this research work. ADCs are vital sub-blocks in almost any iOT devices. These blocks used to digitize the analog signals which usually produces by sensors. Several circuit techniques are used to minimize the power consumption. The utilized energy harvester formed by small-size commercial 0.69 mm2 photodiode array, composed of TEMD7000X01 photodiodes in series (see [157]). By connecting three devices in series connections, a supply voltage of 0.6 V is generated to power-up the ADC chip. Several techniques are used to minimize the power consumption of the designed ADC. A capacitive charge redistribution SAR ADC is usually used for the energy limited applications in iOT devices [157]. SAR ADCs are very attractive for these applications since they do not utilize any analog block with static current consumption. All blocks in the SAR ADC are dynamic circuits which utilize the clock signal to operate and avoided any static current. These ADCs for low speed iOT applications usually utilize sub-volt supply voltages to minimize power consumption. SAR ADCs for these applications use heavily clocked cycled structure with a sleep mode lasting over 90% of the clock cycle in order to minimize power consumption.

3. 4. 1 Summary of the Fabricated SAR ADC

In this section the summary of an energy-efficient asynchronous 10-bit resolution SAR ADC with a 0.6-V supply and with an internal clock generator, is presented which was designed, and fabricated during this research work. The prototype is designed and fabricated in a 65-nm TSMC CMOS process. All timing signals are generated internally. Also, the designed SAR ADCs utilized at least one high-threshold-voltage transistors for any path from VDD to ground in order to minimize the leakage currents in the sleep mode [154-157]. A custom-made capacitor array, shown in Fig. 3. 9, that is similar to those presented in [54] and [154-157], is also designed which minimizes the effects of routing parasitic capacitances on the accuracy of the capacitor array and SAR ADC. The ADC applies a self-oscillating comparator (similar to that of [154-157]), a custom-made capacitive DAC with 250 aF unit elements (shown in Fig. 3. 9) and utilize static CMOS logic for SAR logic, as shown in Fig. 3. 8. Long channel, and high-Vth transistors are used in the logic design to minimize the leakage currents. Furthermore, to demonstrate the ultra-low-power consumption property of the designed system, and to study the feasibility of powering a miniature size system by energy harvesters, the supply of the ADC core is directly provided by a 0.69 mm2 photodiode array (as energy harvester), composed of three tiny TEMD7000X01 photodiodes in series, as shown in Fig. 3. 12 ([157]). In indoor office lighting conditions, a single TEMD7000X01 photodiode has an open circuit voltage around 0.2 V. By connecting three devices in series, a supply voltage of 0.6 V is generated for the chip core (excluding the supply for the pad drivers). Decoupling capacitors, and SMA (Sub-Miniature version A) cables are used to furthermore suppress the supply, and external noise. While simulation results show a 1 kHz clock frequency for the ADC sampling clock, the measurements results show the frequency of the sampling clock is around 2.4 kHz. Higher sampling clock frequency indirectly shows that the utilized devices in the current-generators-block for the internal oscillator have relatively larger leakage currents than what

simulation shows. Fig. 3. 10 and Fig. 3. 11 show the ADC layout and silicon die. Further measurements reveal that the ENABLE signal for the internal comparator does not function properly and comparator internal clock (self-oscillation), oscillates for longer time than what it designed to be. This is caused mainly because of the higher leakage currents in the fabrication process, and consequentially wrong signal transition in the last flop-flop in the SAR logic which is responsible to generate the ENABLE signal for the comparator. This does not affect the functionality of the SAR ADC. Higher leakage currents for the MOS devices, higher frequency for the clock generator (ADC's sampling clock), and longer oscillation for the comparator internal clock (self-oscillation loop around comparator [153]), resulted in relatively higher power consumption for the chip, comparing to the simulation results. At 2.4 KS/s the measured current for the ASIC, including ADC core and internal signal generators, was approximately 105 nA at 0.6 V supply. Higher leakage current of the utilized process was the main reason of the higher measured current consumption. At 1KS/s simulated current was smaller than 10 nA in the typical process corner. All 10 ADC samples were measured for functionality, and all the sample were functional.

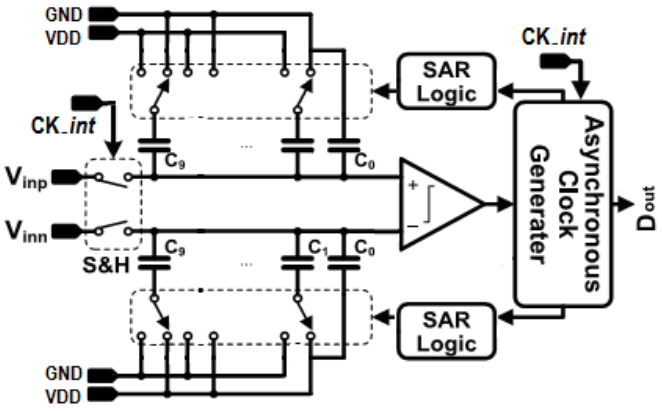


Fig. 3. 8. Implemented 10 bit asynchronous SAR ADC.

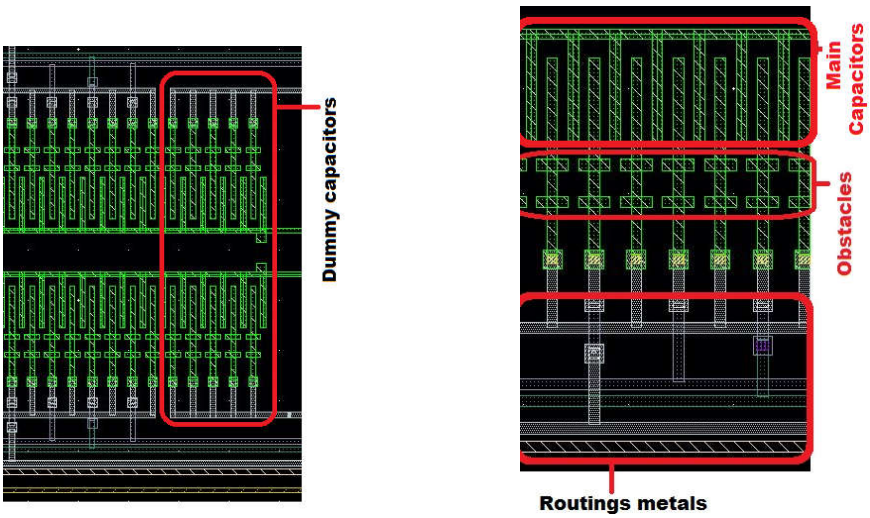


Fig. 3. 9. Layout of capacitor array.

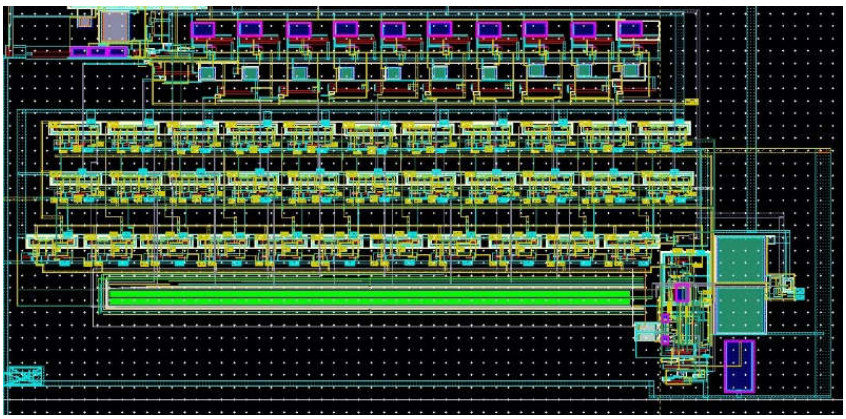


Fig. 3. 10. ADC Layout

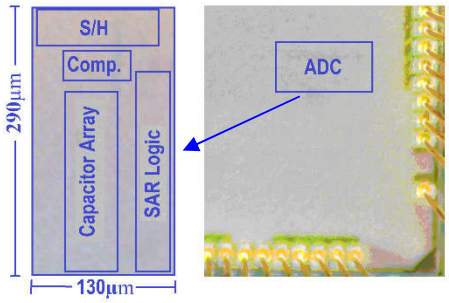


Fig. 3. 11. Die photo of the ADC in 65 nm TSMC.

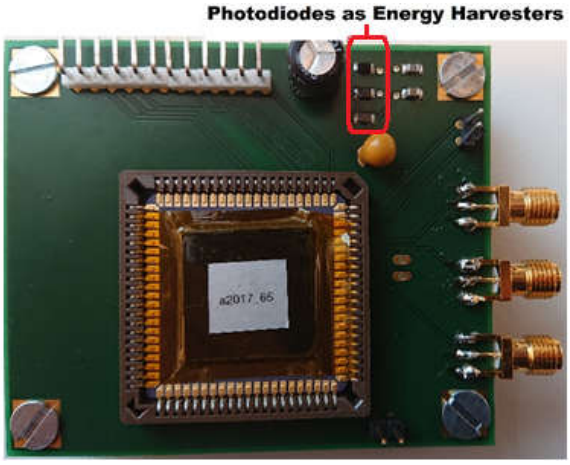
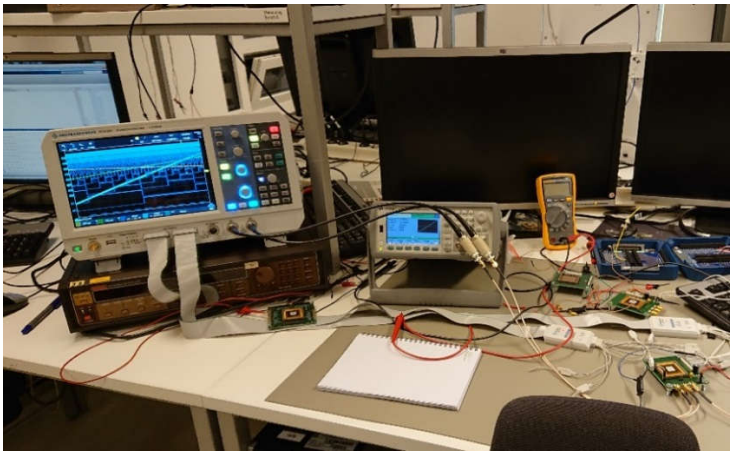
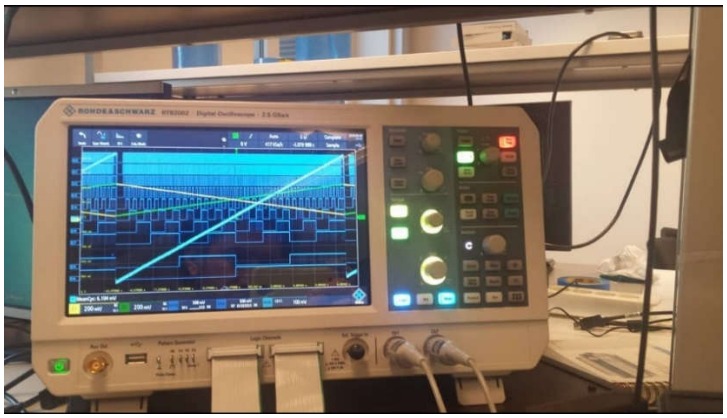


Fig. 3. 12. PCB with designed chip and three tiny TEMD7000X01 photodiodes in series, as energy harvesters.



(a)



(b)

Fig. 3. 13 (a) Measurement set-up (b) Input differential ramp signals (blue ramp) and digitized 10 bit output data (bottom MSB).

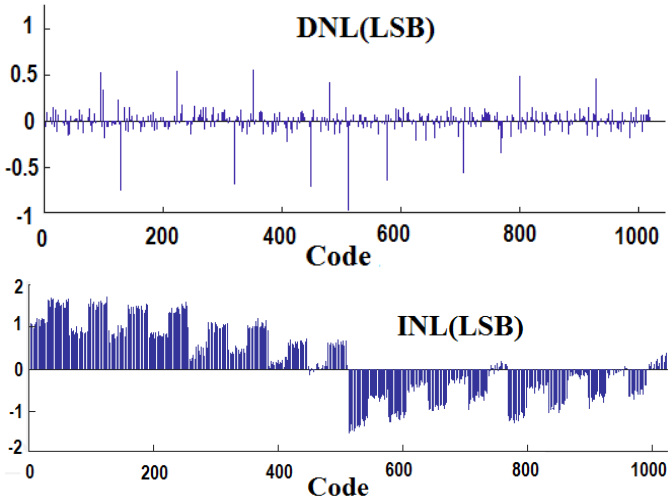


Fig. 3. 14 Static performance of the ADC.

Fig. 3.14 shows the measured static linearity using the code density test with full-swing, using very slow differential ramp signal (sub-Hz), while the internal clock generator had a 2.4 kS/s sample rate. The peak DNL and INL are 0.95 LSB and 1.5 LSB respectively. Using thermometer-encoded for 3 MSBs in CDAC can minimize the INL error, significantly [154-157]. For CDACs with fringing capacitors array, the large errors in the INL often cause by the systematic layout mismatch. These systematic errors, often causes by the parasitic capacitances of the asymmetric capacitors wiring (routing metals), the non-uniform metal density around the capacitors (even though Dummy-Exclude layer was used heavily over the custom-made capacitors), or an insufficient amount of dummy elements around capacitors array in CDAC structure [154-157]. 10 sample were measured and only one sample showed a missing code in the 511 code. 2 samples were functional with supply voltage as low as 450 mV. Fig. 3.13 shows the measurement set-up and 10 bit ADC output data, for a slow fully differential ramp input signal. According to the simulations with CADENCE, the ADC core was functional with supply voltages as low as 300 mV at some process corners. The sampling frequency of the ADC reduces significantly with reducing supply voltage. The main restriction for utilizing ADC in lower power supply is the leakage currents of the flip flops in the SAR logic.

3.5 Summary of Papers

In this section, the summaries of the paper included in this thesis and related to this Chapter are presented. The paper contributions related to this Chapter are the Paper V: "A High-Performance CMOS Modified Amplifier", Paper VI : "Fast-Settling, Energy-Efficient, Amplifier for high-Resolution LCD Displays" [160], and Paper VII "Energy-efficient, fast-settling, modified nested-current-mirror, single stage-amplifier for high-resolution LCDs in 90-nm CMOS" [141].

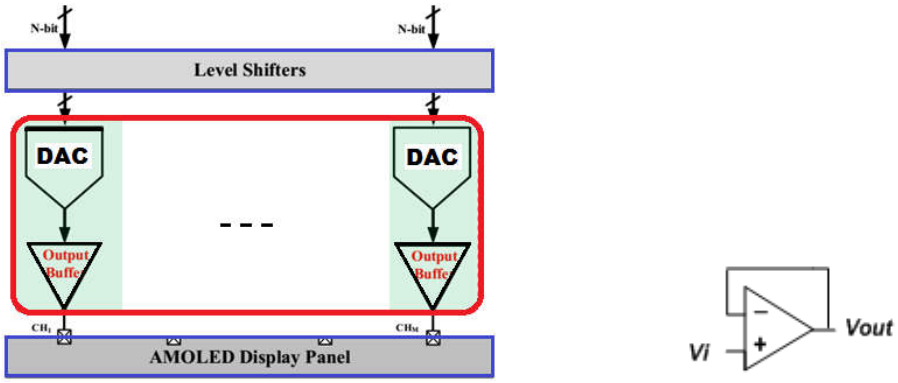
3.5.1 Paper V [161]: "A High-Performance CMOS Modified Amplifier"

A new operational transconductance amplifier (OTA) based on the conventional triple folded cascode (TFC) topology is proposed in this research work. Applying the proposed positive feedback method, the dc-gain of the amplifier enhanced significantly, similar to other positive feedback structures reported in [116-121]. The simulation results for the designed OTA in a typical 0.35µm CMOS technology show more than 20dB dc-gain enhancement while bandwidth, output voltage swing range, and the phase margin characteristics are not affected to a great extent. The main aim in this research work was to increase the functionality range of the positive feedback technique across wider output signal swing range, which is a well-known issue for the topologies utilizing the positive feedback technique in the amplifiers [116-121]. The technique can be utilized in other cascode structure such as folded cascode and telescopic amplifiers. A silicon implementation, fabrication, and measurements of the OTAs can give more reliable results to study the effectiveness of the technique.

3.5.2 Papers VI, VII [160], [141]: "Fast-Settling, Energy-Efficient, Amplifier for high-Resolution LCD Displays", and "Energy-efficient, Fast-Settling, Modified Nested-Current-Mirror, Single Stage-Amplifier for High-Resolution LCDs in 90-nm CMOS"

3.6.2.1 Introduction

LCD panels are widely used modules in iOT applications. Modern mobile devices, smart phones, modern medical/health-care systems, and modern TVs utilize high performance LCDs, which have a wide range of capacitive loads [135-150]. As these displays increase their resolution, quality and size, the design of column output buffers becomes more and more challenging [140].



(a) (b)

Fig. 3. 15 (a) Output buffer in a column drive of an active matrix organic light-emitting diode (AMOLED) [148]. (b) Buffer in single ended form.

Fig 3.15 (a) shows buffer amplifiers in a column driver module of an AMOLED display. These buffers are normally amplifiers in a unity-gain configuration as shown in Fig. 3.15 (b). These buffer amplifiers need to be fast to deal with larger load capacitance and thereby achieve smaller settling time [135][141]. Furthermore, thousands of these output buffer amplifiers are often integrated into one column driver chip. Therefore, the buffers should occupy a small silicon area and consume small static power to meet the market pressure on cost, image quality and display size [135-141]. It also should provide a rail-to-rail voltage driving capability so that higher grey levels can be accommodated [135-141].

The LCD column drivers includes data-latches, shift-registers, input-registers, level-shifters, DACs and output-buffers as shown in Fig. 3.6 (a) [135-141]. DACs and output buffers often determine the speed, resolution, voltage swing, and power dissipation of a column driver [135-141]. Multi-stage amplifiers utilized intensively to implement these buffers because of their high dc-gain and output swing [140]. However, the frequency compensation of these amplifiers increases their design complexity, which also restricts their drivability range and maximum feasible load-size, silicon area and power efficiencies [140-150]. Because of the stability issue, the multiple-stage amplifiers should be designed as different types to drive different values of CL and also should be optimized differently for different CL [140]. To reduce the design complexity and time, a single type of amplifier that can drive various values of CL is desirable [140]. This can be accomplished by utilizing single-stage amplifiers which were not used in those buffers because of their limited performance merit in most metrics despite being almost un-conditionally stable at any CL value [140].

3.5.2.2 Original Nested-Current-Mirror (NCM) Single-Stage Amplifier

For LCD column drivers, simple current-mirror amplifiers (CMA) shown in Fig. 3.16 (a) are favored for their rail to rail output swing, and extra design flexibility by adjusting the mirror ratio, K [140]. However, their performance metrics such as the gain is relatively low, only comparable to that of the differential-pair (DP) amplifier shown in Fig. 3.16 (b) [140]. This is the reason that most classical single-stage amplifiers were underused in large CL applications when compared with their multi-stage counterparts [140]. In the same power budget, regardless of how large the power budget is, the CMA is lagging behind the DP amplifiers for most of performance metrics (see [140]). For this reason, the DP amplifier is chosen in [140] as the “golden reference”

for comparing and justifying the performance of the different amplifier topologies.

The original NCM technique is shown in Fig. 3.16 (c) [139][140]. The technique significantly improves the overall performance of the single-stage CMA. DC-gain, GBW and SR of the simple CMA is improved, and the reported measurement results for the fabricated prototype, confirm comparable figure of merit (FOM), comparing to the other state-of-the-art, single-stage and multi-stage amplifiers. Both $FOM_1=[(GBW.C_L)/(Power.Area)]$ and $FOM_2=[(SR.C_L)/(Power.Area)]$ are comparable with other state-of-the-art works (see Table V in [140]). The C_L drivability (C_{Lmax}/C_{Lmin}) is wider than those of [145-150], while it avoids the stability limit at the heavy C_Ls.

In the original 4-step NCM, 33 times improvement in GBW, 1.9 times improvement in SR, and 2.27 times improvement in settling-time are reported comparing to the standard DP amplifier [139-140]. For the 3-step NCM in [140], 7.5 times improvement in GBW, 1.33 times improvement in SR, and 1.5 times improvement in the average settling-time are reported, comparing to the standard DP amplifier. The technique presented in [140] improves the small-signal settling-time significantly by increasing the transconductance of the amplifier by collection of the nested current mirrors. However, the large-signal speed, and the overall settling-time of the amplifier, is limited by the limitation of the SR. This limitation originated mainly by the SR limitation of the structure. As calculated in [140], the SR of the original 4-step NCM in [140], is:

$$SR= 2K_7.(1+K_6).I_u/C_L \quad 3.5$$

And the SR of the original 3-step NCM amplifier is:

$$SR= 2K_5.(1+K_4).I_u/C_L \quad 3.6$$

Where the I_u for the 3-step, and 4-step NCMs are 100nA and 50nA respectively. As shown in Eq. 3.5, 3.6 and Fig. 3. 16, during SR phase, when a large transition in the input signal happens, in the 3-step NCM, the bias current of M_1, and M_2 does not have any role in the SR of the NCM. In fact, there is no current path for the bias currents of those devices to contribute in the charging or discharging process of the C_L, as shown in Fig. 3.16 (c). Similarly, for the 4-step NCM, the bias current of M_1, M_2 and M_3 does not contribute to the SR of the NCM. Therefore, bias currents of M_1, M_2 and M_3, dissipate without any contribution to the speed of the buffer amplifier. This reduces the energy efficiency of the structure and topology becomes less attractive for the energy restricted portable devices in which the batteries or energy harvesters provide the required supply voltage.

It is considerable that the buffer amplifier in a typical LCD column driver normally receives a sampled signal at its input terminal [135]. Therefore, in order to have a fair merit of speed evaluation, the worst-case settle time should be used. Both the rising and falling edge should be considered, and the settling time should be evaluated during the largest signal transition. The clock period should also be adjusted for the longest transition. Main shortcomings of the NCM structure are higher noise of the topology, and sensitivity of the gain and UGBW to the process variations in the 4-step NCM [140].

3.5.2.3 Modified NCM Single-Stage Amplifier [141]

This section summarizes the proposed NCM single-stage amplifier [141], which is a modified version of the original NCM topology presented in [139-140]. The modified version furthermore

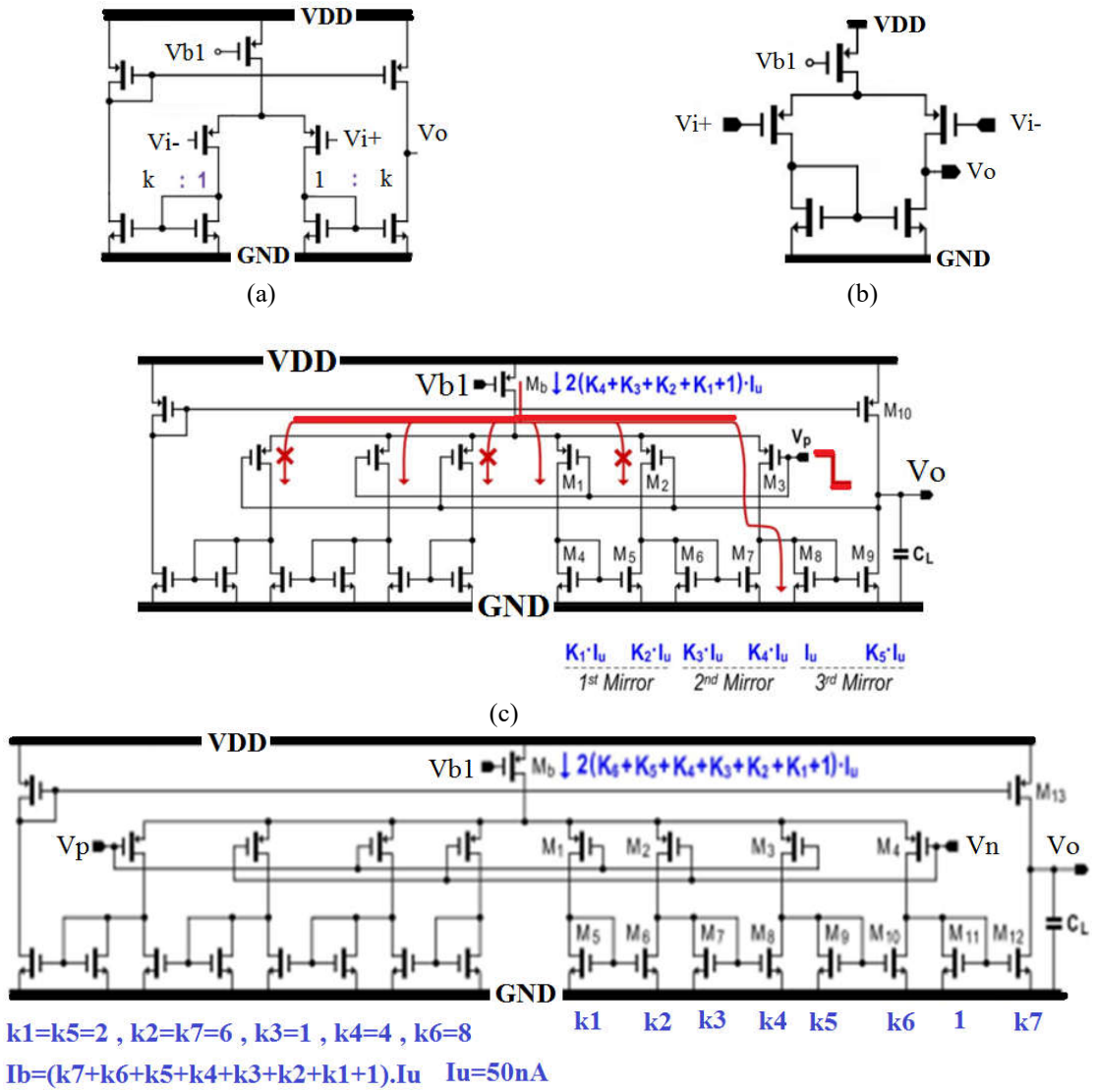


Fig. 3. 16. (a) conventional CMA [140]. (b) conventional DP amplifier [140] (c) Slew-rate condition in Original 3-Step NCM [140]. (d) Original 4-Step NCM [140]. (reproduced from [140])

speed-up the topology and improve the gain and noise performance of the NCM amplifier without any significant power, output swing range, noise, or stability penalties.

As mentioned before, in a typical LCD column driver, the input signal for the buffer amplifiers are normally sampled signal. Therefore, the clock period of the column driver should be adjusted to the slowest signal transitions that imposes by the largest

possible signal. In addition, to have a fair merit evaluation of the amplifiers, the worst-case settling-time which is normally largest signal transition, should be used to calculate FOM, and not only UGBW or SR of the amplifiers. Therefore, in this paper [141] a new SR enhancer circuit is designed to reduce the settling-time of the NCM amplifier. In addition, the gain of the amplifier is increased by 6 dB, using cascode structure for the PMOS devices in the output stage. Noise performance of the modified NCM is also improved by assigning higher bias currents for inner differential pairs that have larger noise contribution in the structure.

Fig. 3.17 shows the proposed 4-step NCM amplifier in this work with SR enhancer circuit. For simplicity, the bias current generator device (Mb) in [140], is split into two different devices in this design called M_{b0} and M_{b1}. As depicted in Fig. 3. 17 and discussed in previous section, when a large transition in the input signal happens, despite the I_{b0}, the bias current of M_{b1} (I_{b1}), cannot have a role in the SR of the NCM. In fact, there is no path for I_{b1} to contribute in the charging or discharging process of the C_L. To speed up the NCM structure and improve the energy efficiency of the structure, a SR detector and SR enhancer is designed in [141] as shown in Fig. 3. 17. (b) and (c)). The SR booster circuit activates during the slew phase and feeds the bias current of I_{b1} to either the V_{cm1} or V_{cm2} nodes, depending on the rising or falling transition.

The total current of $I_{b0}+I_{b1}$, multiplies by the current-mirror ratio (K_7) of the last current mirrors and feeds to C_L. This technique significantly increases the SR and speed of the NCM, with only negligible extra current consumption of about 50 nA which dissipates in the designed SR detector circuit. In this case the SR increases to $[2K_7.(1+K_1+K_2+K_3+K_4+K_5+K_6).I_w/C_L)]$. Using the same current-mirror ratios (K), used in [140] for 4-step NCM (K_1=2, K_2=6, K_3=1, K_4=4, K_5=2, K_6=8, K_7=6), proposed technique increases the SR of the original 4-step NCM, about 2.65 times. Also, applying the proposed technique in the 3-step NCM version, and with the same mirror ratio used in [140] (K_1=2, K_2=3, K_3=1, K_4=3, K_5=5), the SR increases 2.5 times. Fig. 3.17 (c) shows the circuit designed for extra SR and speed boosting. It is activated by the SR detector circuit shown in Fig. 3.17 (b), and feeds the current from I_{bs1} to the $V_{cm1,2}$ node. That increases the total charging and discharging current of the C_L by at least five times using the $M_{s16,\ 17}$ devices. These devices are normally OFF, during the small-signal operation of the NCMs [141].

The proposed low-power slew detector is shown in Fig. 3. 17 (b) and formed by the M_{s0}-M_{s10} transistors. This circuit is partially non-active during the small-signal operation of the amplifier and activates only when a large-signal transition happens. Transistors M_{s0} to M_{s4} have static current in the normal small-signal conditions. Hence the circuit does not affect the noise, UGBW, gain, and small-signal settling-time specification of the original NCM amplifier, to a great extent. When a large-signal falling transition happens, M_{s11} and M_{s16} devices activate by the slew detector circuit, and feed the bias current of $I_{b1}+I_{bs1}$ to V_{cm2} node. In the same manner, when a large-signal raising transition happens, M_{s12} and M_{s17} devices activate by the slew detector circuit and feed the bias current of $I_{b1}+I_{bs1}$ to the V_{cm1} node [141].

During the small-signal operation of the amplifier the M_{s5}-M_{s8} devices as well as M_{s11}-M_{s14} devices are inactive and the bias current of I_{bs0}, is carried by M_{s3} and M_{s4} devices. Therefore, for the small-signal operation mode, sr1 and sr2 nodes are pulled up to the supply voltage (~VDD), by the bias current generator devices (M_{s9} and M_{s10}).

In the large-signal operation, depend on the rising or falling phase, I_{bs0} directs to the either M_{s1} or M_{s2} devices. In this case, I_{bs0}-$I_{bs3,4}$, flows throw M_{s5} (or M_{s6}) and amplifies by the current-mirrors formed by M_{s5}-M_{s8}. The current gain of these current mirrors is set to 5. In this case, the current of M_{s7} (or M_{s8}) device becomes larger than the bias current of M_{s9} (or M_{s10}),

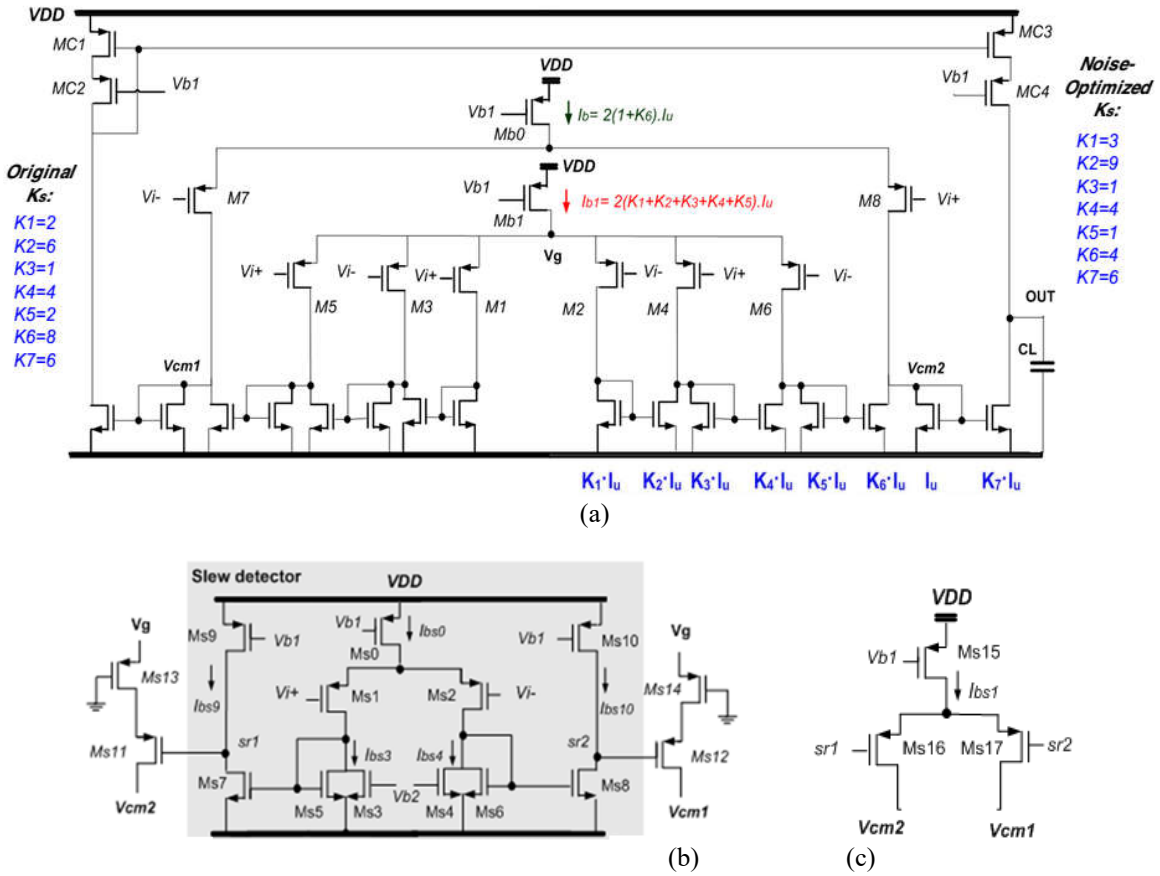


Fig. 3. 17. Proposed 4-Step NCM [141]. (reproduced from [141])

and the voltage of $sr_{1,2}$ node, drops to approximately lower supply voltage. Therefore, M_{s11} and M_{s16} devices (or M_{s12} and M_{s17}), become ON and direct the bias current of $I_{b1}+I_{bs1}$, to V_{cm2} (or V_{cm1}) node. This technique increases the total currents that charges or discharges C_L, in the SR phase. Since the source of M_{s13} and M_{s14} devices are connected to the virtual ground node (V_g), their parasitic capacitances do not influence the frequency response of the amplifier, and the small-signal settling-time of the amplifier remain unaffected by these devices. M_{s11} and M_{s12} devices are used to separate the parasitic capacitance at the drain node of $M_{s13,14}$, from $V_{cm1,2}$ nodes.

It is worth nothing that despite the core NCM amplifier, the SR detector circuit can utilize smaller device size, for better area efficiency. On the other hand, as discussed in [140], to minimize the noise (both flicker and thermal noise), offset, and process variation and improve the matching, the NCM amplifier should have relatively large device dimensions for the most of the utilized transistors in the core, and more specifically for the devices located at the beginning of the signal chain.

In the NCM structure, the noise of the transistor is also amplified by the mirror ratios as discussed in [139, 140]. The 4-step NCM structure [141], tradeoffs noise performance for a higher

SR. This is realized by utilizing larger bias currents and mirror ratios in the last current-mirrors (K_6 and K_7) and at the same time, using smaller bias currents (I_{b1}) for the M_1-M_6 devices and their corresponding current mirrors. Since the noise generated by M_1-M_4 devices, are amplified with higher gain, noise of these devices dominates the overall noise performance of the amplifier. This issue relaxed in the 4-step NCM proposed in [141], by increasing K_1, K_2, and the bias currents and feature sizes of the M_1-M_4 devices, and at the same time by decreasing K_5, K_6, and the bias currents and feature sizes for the M_5-M_8 devices, as shown in Fig. 3. 17. (a) (K_1=3, K_2=9, K_3=1, K_4=4, K_5=1, K_6=4, K_7=6). Since the proposed 4-step NCM already benefits from the SR enhancer circuit, it is not necessary to have large value for K_6. At the same time, other performance metrics of 4-step NCM such as dc-gain, GBW, and SR remain largely unchanged.

In the 4-step NCM proposed in [141], using cascode PMOS current-mirror, formed by the Mc1-Mc4 devices, the output impedance of the amplifier is increased 2 times, and dc-gain of the amplifier is improved 6 dB compared to [139]. Since the amplifier is used in the unity-gain configuration of Fig. 3. 15 (b), the Vi- node is connected directly to the output node. Therefore, the output voltage swing range, is limited by the threshold voltages and the overdrive voltages of the input differential pair devices ($M_{b0,1}$, M_1-M_8) rather than the PMOS cascode devices. In addition, using the cascode structure for the PMOS current mirror, improves the linearity of the current mirror and the NCM amplifiers. In this case the large voltage swing at the output node, cannot cause large variations in the drain-source voltage of the M_{c1} and M_{c3} and in the current-mirror ratio formed by M_{c1}-M_{c4}.

In addition, [141] proposed a new FOM to evaluate and justify the performance of the amplifiers. The FOM is:

$$FOM_3 = C_L / T_{st.max}.Power.Area \qquad 3.7$$

According to this FOM, the worst-case settling-time considering both rising and falling edges, used to evaluate the performance of the amplifiers. This normally happens in the largest signal transition.

3.5.2.4 Further Discussion about NCM Amplifiers

In summary, as mentioned in the previous section, in the proposed energy-efficient NCM [141], thanks to the designed SR enhancer circuit, the worst-case settling-time of the NCM amplifier, is improved more than 8 times, while preserving the power consumption, output swing, UGBW, Phase margin, and wide CL drivability without entailing any compensation capacitor or resistor. The performance boost realized at the cost of increased complexity and negligible area. DC-gain is also improved 6 dB, and a noise optimized NCM with modified mirror ratios (Ks) is proposed. Simulations for implemented 3-step and 4-step NCM amplifiers confirmed the theoretical study and performance claims. In addition, a new FOM is defined to evaluate and justify the performance of the amplifiers.

The proposed technique is suitable for the LCD drivers in the portable battery-powered iOT devices which utilize power efficient user-interface screens. The applications of the NCM amplifier is not limited to the LCD column drivers and the topology is suitable for any applications that require large capacitive load and with large variations. Such applications include ADC reference generators and error amplifiers in the LDOs.

Chapter 4

Discussion, Conclusion and Suggestions for Future Research

In this Chapter the conclusions of this research work in the different analog, digital and mixed-mode domains are provided, as well as some suggestions for future research.

In this research work, different circuit techniques studied for the next generation of battery-free and energy-restricted iOT devices. Reducing the power supply voltage, as a powerful technique used in both digital and analog, as well as mixed-mode circuits to minimize power. Minimizing the number of transistors for the digital gates may result in significant reduction of the leakage currents for the whole iOT devices which operates most of their life cycle in the sleep-mode. This is the reason that logic styles with lower number of transistors, such as domino logic, are good candidates for the energy-efficient portable iOT devices. For the analog blocks that require static bias currents, reducing the static and leakage currents, is a powerful technique to improve the energy-efficiency of the sub-systems and iOT devices. Duty-cycling is also a powerful and widely used technique that improves the energy efficiency of the analog blocks.

In the digital domain, SFG ULV technique is investigated in this research work for high speed and low voltage applications. As mentioned before logic styles that require lower number of transistors, are attractive for duty-cycled iOT applications. This is mainly due to lower leakage current in the sleep mode for this logic families. This is the reason that domino logic style is an attractive option for such energy efficient iOT devices. Feasibility of utilizing domino logic in ULV domain combined with SFG technique are investigated in this research work. Power supply voltages as low as 300 mV and below are used for these logic gates. Feasibility of utilizing bulk terminals in the ULV7 was also investigated. A prototype of N-type and P-type ULV7 was also fabricated on silicon and measured successfully. For further research work in this topic, a silicon prototype of a logic chain may be implemented for further studying, including the clock drivers. The SFG technique is applied to dual-rail NP domino logic to increase the speed of evaluation phase. A new keeper structure is investigated for dual-rail domino logic to increase the noise immunity of the logic to leakage current and also to the delay of the input signal in the chain. For future research work in this topic, silicon fabrication of a complex logic using ULV SFG dual-rail domino technique is highly suggested to further study the characteristics such as leakage current, noise immunity and power consumption of the logic. Studying the practical challenges of the clock driver for the SFG ULV logic is an interesting research topic in this field.

In the analog domain, some important circuit techniques have been discussed in Chapter 3. Some state-of-art and widely used sub-blocks such as reference generator, including BGR and LDOs for the iOT systems, are also discussed. Furthermore, the ULV and ULP amplifier design was investigated in this thesis, and design challenges were discussed in Chapter 3. High-performance amplifiers are a necessary part of any iOT devices. Improving the performance of the amplifiers may improve the performance of the iOT devices to a great extent. In addition, an energy efficient technique is proposed to improve the performance of the NCM amplifier. NCM is a suitable topology for applications which require large capacitive loads, such as LCD column drivers. For further research work in this topic, a silicon prototype should be laid-out for further studies.

In the mixed-mode domain, a 0.6 V energy-efficient 10-bit asynchronous SAR ADC with internal clock generator has been designed and fabricated. The prototype is designed and fabricated in a 65 nm CMOS process. The ADC has an INL and DNL of 1.57 LSB and 0.95 LSB respectively at 0.6 V supply. The ADC employs a self-oscillating comparator, a custom-made capacitive DAC with 250 aF unit elements and static CMOS logic for the SAR logic. Utilizing thermometer coding for the 3 MSBs in the CDAC, may reduce the probability of large INL and DNL errors. The target application for this ULV ADC are ULP biomedical and iOT devices that utilize energy harvesters. For the future research, developing leakage tolerant ULV sub-modules is highly recommended.

In the ULV and ULP energy restricted miniature size sensor applications, the design of voltage reference including BGRs and LDOs is a challenging task. While numerous numbers of power-efficient, sub-volt SAR ADCs are reported in the literature, the LDOs and reference generators for these nano-watt ADCs are still power-hungry. These reference generators consume significant part of the available power for the whole signal acquisition systems, which is often provided by a tiny energy-harvester. Developing energy-aware reference-generators, designing supply-adaptive systems, and also noise-adaptive SAR ADCs are promising solutions for these iOT devices, which requires innovative circuit techniques.

Publications

Paper IV

"NP-Domino, Ultra-Low-Voltage, High-Speed, Dual-Rail, CMOS NOR Gates"

Ali Dadashi, Omid Mirmotahari , and Yngvar Berg.
Circuit and Systems, 2016.

Bibliography Reference [87]

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NP-Domino, Ultra-Low-Voltage, High-Speed, Dual-Rail, CMOS NOR Gates

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Abstract

In this paper, novel ultra low voltage (ULV) dual-rail NOR gates are presented which use the semi-floating-gate (SFG) structure to speed up the logic circuit. Higher speed in the lower supply voltages and robustness against the input signal delay variations are the main advantages of the proposed gates in comparison to the previously reported domino dual-rail NOR gates. The simulation results in a typical TSMC 90 nm CMOS technology show that the proposed NOR gate is more than 20 times faster than conventional dual-rail NOR gate.

Keywords

Ultra Low Voltage (ULV), Semi-Floating-Gate (SFG), Speed, NOR Gate, Monte Carlo, Dual-Rail NP Domino, TSMC 90 nm, CMOS

1. Introduction

Modern electronic technology faces trade-offs between power budget, and performance. Traditionally for the high-performance systems, design considerations assume a sufficient and stable supply of energy source to maintain constant performance throughout overall system operation [1]. For decades, the supply voltage of this system, has been set above the transistor's threshold voltage (Vth), and called above-threshold (or super-threshold) operation. However, in the modern low-power (LP) and ultra-low-voltage (ULV) portable applications, the energy supply is strictly limited, and the overall system benefits from the innovative techniques for active energy minimization and standby power reduction [1]-[5]. Examples of such power saving techniques include supply-voltage scaling, multi-threshold logic, transistor-stacking, and power-gating [1]-[5]. These ULV systems are extensively used in the modern applications such as low-cost iOT devices, wearable-electronics, intelligent remote sensors, implantable/wearable medical-devices, and energy-harvesting systems. For these ULV applications, often innovative techniques utilized to reduce the overall energy consumption. Sub-threshold design often consi-

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dered as a very suitable, and energy-efficient solution for these emerging energy-constrained applications [1]-[5].

The downscaling of CMOS technology (for higher transistor-density and computing-capacity) and reducing supply-voltage results in degradation in the speed of the logic circuits due to reduced gate-source voltage of the transistors [1]-[5]. Furthermore, existence of substantial leakage current in the modern CMOS nodes prevents the scaling of Vth aggressively [1]. In one side, increasing the market of low-cost portable-devices demands the design of the low-power blocks that enable the implementation of long-lasting battery-powered systems. On the other side, the general trend for increasing the operating frequencies and circuit complexity, in the modern high-performance processing applications, requires the design of very innovative high-speed circuits [2]-[19]. Current digital design techniques do not offer reliable and high-speed logic circuit that can operate at deep sub-threshold voltages. Hence, operability is the main goal in implementing ULV systems in these high-speed applications [13]-[19]. Domino logic is known as a high-performance circuit configuration which normally utilizes clocking scheme and is embedded in the static-logic environment [1]. Domino CMOS has become a popular logic family for high-performance and high-speed applications and it is extensively used to implement high-speed processors [6]-[10], since they provide advantages over static-CMOS logic, including fast operation, and lower number of transistors (lower silicon area) [11].

SFG technique has been proposed for ULV NP-domino logic structures [13]-[19]. ULVSFG logic implemented in a modern CMOS process requires frequent initialization (pre-charge) to minimize leakage. By applying the input signals, using input capacitors (Cin), to the gate of evaluation transistors (EN), these nodes (SFG nodes) can have a larger voltage level than power supply-voltage (VDD) [13]-[19]. The main aim is to increase the current of the evaluation transistor (EN) to achieve higher speed in the evaluation phase. In this paper, we used the SFG concept to speed up the performance of the conventional dual-rail logic. We compared the performance of the designed SFG dual-rail NOR gate with the conventional dual-rail NOR gate. Simulation result shows significant speed improvements. Furthermore, we discussed the inclusion of a new keeper transistor which improves the stability of the gate, to hold the voltage of the floating gate node and the output node, for a delayed input signal, especially when these gates are utilizing in a chain of gates in a large system.

This paper is organized as follows: in Section 2, a short introduction to the simple conventional dynamic single-rail and dual-rail domino logic is provided and also the ULVSFG inverter and ULVSFG NOR gates are discussed. In Section 3, the proposed ULVSFG dual-rail domino NOR gates are discussed, and we study the delay and stability of the new logic gate. In Section 4, the simulation results, for the different NOR gates are given, and compared; finally, Section 5 concludes the paper.

2. Domino Dynamic ULV Logic

2.1. Conventional Dynamic and Dual-Rail Domino NOR

Figure 1 shows the conventional dynamic pre-charge to 1, single-rail and dual-rail NOR gates [1]. This type of domino logic is widely used in the high-speed applications like high- speed processors (e.g. 1-GHz 0.75 W ARM Cortex A8 designed by INTRINSITY) and studied in details in many papers and books (e.g. [1]). Domino logic gates, operate in two different phases of "pre-charge" and "evaluate". Compared to the simple static CMOS NOR, dynamic domino logic achieves higher speed at the cost of higher power consumption [1]. However A major limitation in the single-rail Domino logic is that only non-inverting logic can be implemented [1] [2]. This requirement has limited the widespread use of the pure domino logic style. This limitation is overcome with utilizing the "true" and "complemented" logic outputs of the dual-rail domino logic, at the cost of approximately doubling the power/energy consumption and utilized silicon-area [1] [2].

2.2. Semi-Floating-Gate Domino Logic

Figure 2(a) shows the dynamic, pre-charge to 1, single-rail Inverter gate using SFG technique [14]. This kind of ULVSFG NP-domino logic is introduced and discussed in details in many papers [13]-[19]. The main purpose of the ULVSFG domino style is to increase the current of the transistors at the low supply voltages without increasing the transistor widths. We may increase the current and speed compared to conventional domino and static CMOS, using different pre-charge voltages to the gates, and applying capacitive coupled inputs [14], similar to neuron MOS in [12]. In these topologies Voffset+ pins are connected to VDD and Voffset- pins are connected to GND. The High-speed N-type ULVSFG domino NOR (pre-charge to 1), is shown in **Figure 2(b)**. The

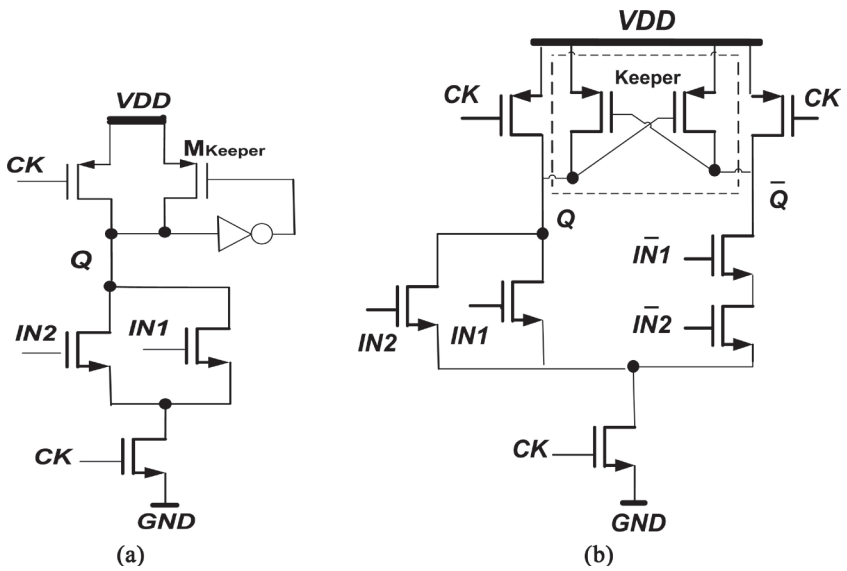


Figure 1. Conventional precharg to 1, dynamic NOR gates. (a) single-rail (b) dual-rail.

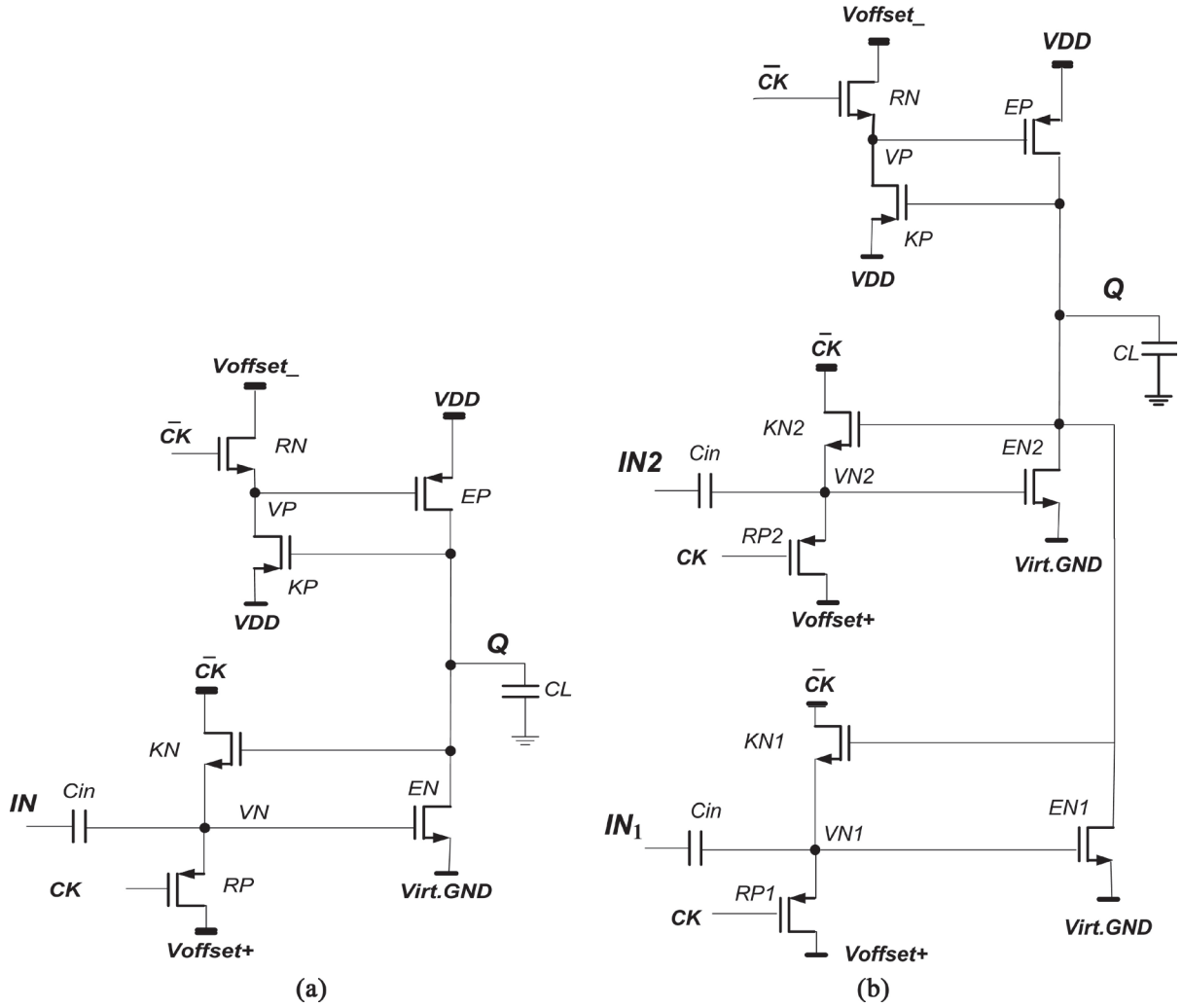


Figure 2. Simple precharge to 1, ULVSFG (a) Inverter (b) NOR gate.

clock signals are used both as control signals for the recharge transistors RP and RN, and as reference signals for NMOS evaluation transistors EN. Both inverter and NOR gates shown in **Figure 2**, operate in two different phase called "pre-charge" and "evaluate" and follow the sequences in the normal NP-domino logic style. The virtual ground signal (Virt.GND) is synchronized with the clock signal, with transistor dimensions sufficient enough to drive the needed current through the EN transistors during the evaluation phase.

When CK is low (0), and Virt.GND is high (1), both inverter and NOR gates becomes in the precharge phase. During this phase, RP transistors turn on and recharge the gate of the EN transistors to VDD. Meanwhile RN transistors turn on and recharge the gate of EP transistors to 0. Thus EP transistors turn on and precharge the output nodes to VDD. The keeper transistors, KN and KP, are inactive during this phase as the output node is precharge to VDD, and input signals are in the low (0) level since the gates follow the NP-domino logic.

In the evaluation phase, in the both inverter and NOR gates shown in **Figure 2**, when the clock signal CK switch from 0 to 1, and Virt. GND = 0, both recharge transistors RP and RN switch off which make the charge on the SFG nodes (Vp and Vn) become semi-float. The output nodes remain at high level until an input transition occurs. The input signals (IN) must be monotonically rising to ensure the correct operation for the N-type domino logic. This can only be satisfied if the input signal is low at the beginning of the evaluation phase, and if IN only makes a single transition from 0 to 1 in the evaluation phase. When this transition happens (IN rises from 0 to 1), the voltage of the semi-floating gates (VN) increase well above VDD, based on a capacitive coupling from the input node to the SFG node, and this increases the current of the EN devices in the evaluating phase and speed up the evaluation process. In this case the keeper transistors (KN) will be turn off and the voltage of the VN will be stable. Also, in this case, the keeper transistors (KP) will be turned on and will increase the gate voltage of the Ep transistor (VP), and eventually turn the Ep transistors off. This helps to reduce the static current which directly impacts on the noise margin and the power consumption of the proposed logic. In the second scenario (when no change/rise) the output voltage will be remained high. In this case, the keeper transistors (KN) will continue to reduce and discharge the voltage of VN nodes and therefore turning the EN transistors off, also the keeper transistors (KP) remain off and voltage of VP nodes will be float. The main necessity to have the keeper transistors KN is turn the evaluation transistors (EN) off to minimize the current dissipation during the evaluation phase when there is no raising input signals edge (input signals remain 0). This reduces the static power consumption significantly as discussed in [14]. The ULVSFG logic demonstrates significant speed improvements in comparison to conventional static CMOS logic [14]-[19]. However, as mentioned before, a major limitation in the single-rail domino logic is that only non-inverting logic can be implemented [1] [2]. As a solution, we propose a dual-rail version of the ULVSFG NOR gate in the next section.

3. Proposed Dual-Rail NOR Gates

As mentioned before, the NOR gate shown in **Figure 2(b)**, is a single-rail logic, and although it is quite high speed logic when compared to static CMOS logic, it is not enough to implement inverting logics.

3.1. Dual-Rail SFG NOR Gate

Figure 3 shows the proposed ULVSFG, precharge to 1, dual-rail, NP-domino, NOR gate. Operation of the proposed NOR gate (shown in **Figure 3**) is similar to the operation of the single-rail version shown in **Figure 2(b)**. The circuit has both true (A, B) and complementary version of the input signals ($\overline{A}$, $\overline{B}$) and produce both true (Q) and complementary output signals, and follows the sequences of the normal NP-domino logic (precharge and evaluate phases). SFG technique is used to boost the current of EN transistors in the evaluate phase as it is done in the single-rail version. In the precharge phase, as discussed before, output nodes charge to VDD by turning the RN and EP devices on. In this phase the gate of EN devices charge to VDD by turning the RP devices on. As in the single-rail version, in the precharge phase, since the logic gate is an NP-domino type logic, all input signals (including complementary versions) come from the previous stage dual-rail domino gates (which are precharge to 0), and are low during the precharge phase, while making a conditional 0 to 1 transition during evaluation. In the evaluate phase, each input signal, either remains at 0 or goes to high logic level (VDD). When a true input signal (A, B) remains at low (0) logic, the complementary version of that signal goes high, and when the true signal goes from 0 to 1 logic level, the complementary version remains at the low (0) level. As it mentioned before during precharge phase both Q and $\overline{Q}$ precharge to 1 and output signal either remain in 1 or goes low (0), depend on the input signals in the evaluation phase. The functionality of the gate is quite similar to

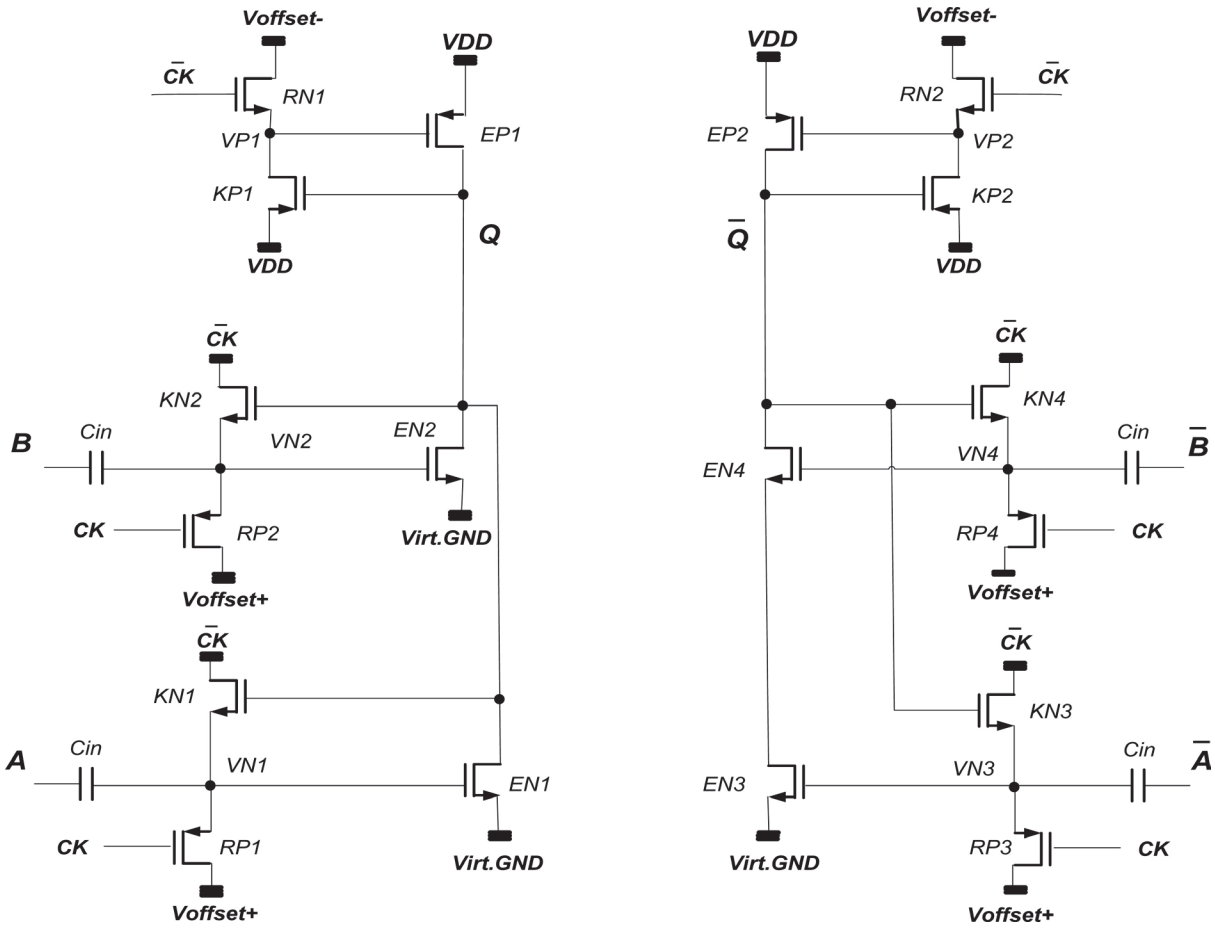


Figure 3. Dual-rail ULVSFG NOR gate.

that of the conventional dual-rail ones. In this topology the role of the keeper transistors (KN and KP) are the same as the keeper transistors in the single-rail version, as discussed in Section II. These transistors (KN) remain off, when there is a raising input signals edge. The KN devices turn on when there is no raising input signals edge (input signals remain 0) and discharge the floating nodes (VN) and this causes the evaluation transistors (EN) become off and the current dissipation to be reduced significantly, during the evaluation phase. This reduces the static power consumption significantly [14]. In the evaluation phase, simulation results show that a falling transition (1 to 0) in the output (Q) takes less than 50 pS, while the same transition in the conventional dual-rail NOR gate, shown in **Figure 1(b)**, takes 1.7 nS. However, in both circuits, the falling transition (1 to 0) in the $\overline{Q}$ side is slower than Q side. This happens since both circuits are using stacked (cascode) transistors in the $\overline{Q}$ path. For the proposed NOR gate falling transition in $\overline{Q}$ takes 140 pS and for the conventional NOR gate shown in **Figure 1(b)** it takes 2.4 nS to switch from high to low level. However it is considerable that the structures utilizing the SFG technique (both single and dual-rail versions) are sensitive to the delay of the input signals. If the input voltage signals rise late enough, the voltages on the SFG nodes will be discharged by the ON currents of the keeper transistors (KN) and also by the leakage currents of the devices connected to the SFG nodes. In this case the structures will lose the benefits of having the higher voltage (over than VDD) on the SFG nodes and this causes significant speed reduction in the evaluation phase and even failure in the functionality of the gate for a delayed input signal. This condition happens when these structures are utilizing in the high-depth logic circuits. Therefore, the timing of the input rising signals is important for the proper operation of the structures which are utilizing the floating gate technique. If the voltages of the SFG nodes are lower than VDD, the EN transistors will not be able to pull down the voltages of output nodes to GND. The timing issue gives constraints in term of a valid timeframe for a delayed input. The evaluation speed of the SFG gates is affects by the delay of the input edge. This will affect the next gate and all gates in a chain, thus limiting the number of cas-

caded gates. Simulation results show that the evaluation delay of the proposed SFG dual-rail NOR gate is approximately 50 ps at 300 mV power supply and the input edge delay less than 1 ns. For a 1.7 ns delay at the input signal, the evaluation delay becomes more than 80 ps. Furthermore, the simulated data show that the swing will not be sufficient enough for high-speed operation.

3.2. Modified Dual-Rail SFG Domino NOR Gate

In order to make the proposed ULVSFG NOR gate more robust and less dependent on the delay of the input edge, a new keeper structure should be applied. In the new keeper structure, the keeper devices should be off before raising the input signals, and conditionally turn on, depend on the transitions on the output nodes. One way to make it is applying a signal to the drain terminals of the keeper devices (KN), instead of $\overline{CK}$ signal, which are similarly linked to the timing of the input signals. These signals should be precharged to 1, when the output of the ULV gate is precharged to 1, and switche to 0 if the both input signals (A and B) remain 0 for the entire evaluation phase. **Figure 4** shows the modified version of the dual-rail SFG, NOR gate which is tolerant to the delay of the input signal. In this topology the drain terminals of the keeper devices (KN) are connected to the output nodes of the complementary side, instead of the $\overline{CK}$ signal in the NOR gate shown in **Figure 3**. In this modified version of the ULVSFG dual-rail NOR gate, KN1 and KN2 keeper devices will be ON, if both A and B input signals remain low and both $\overline{A}$ and $\overline{B}$ signals become high (1) and consequently a high to low transition happens in $\overline{Q}$. In this condition, both KN3 and KN4 will be OFF, and Q remains in the high level. On the other hand, if there is at least one raising transition on the input signals (A, B), a high to low transition will happen in the output voltage of the NOR gate (Q), and both KN1 and KN2 transistors become OFF. In this case both KN3 and KN4 devices will be ON and will discharge the SFG nodes (VN3 and VN4). Thanks to improvement in the robustness of the modified NOR gate (shown in **Figure 4**), in terms of holding the voltage of the SFG nodes (until a input signal edge arrives), larger logical depths is feasible to implement with SFG technique.

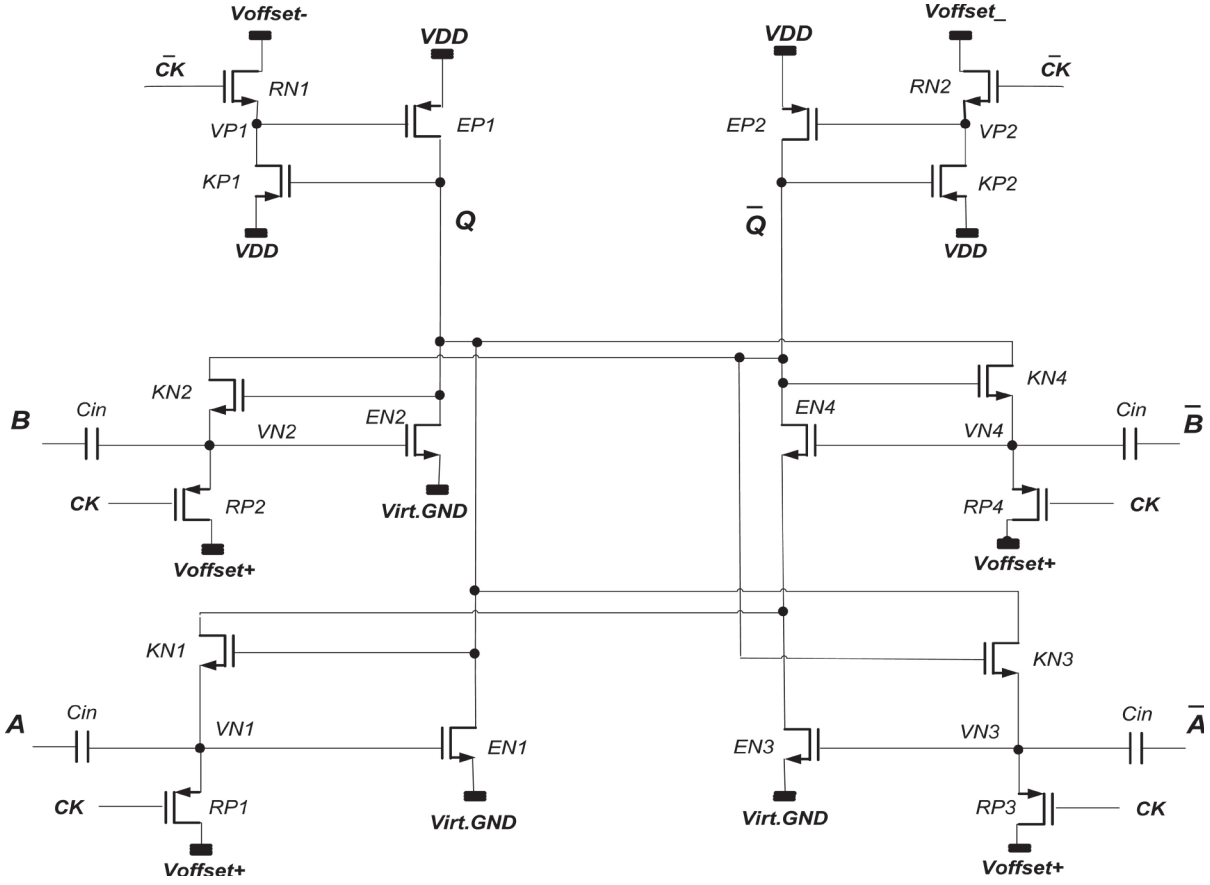
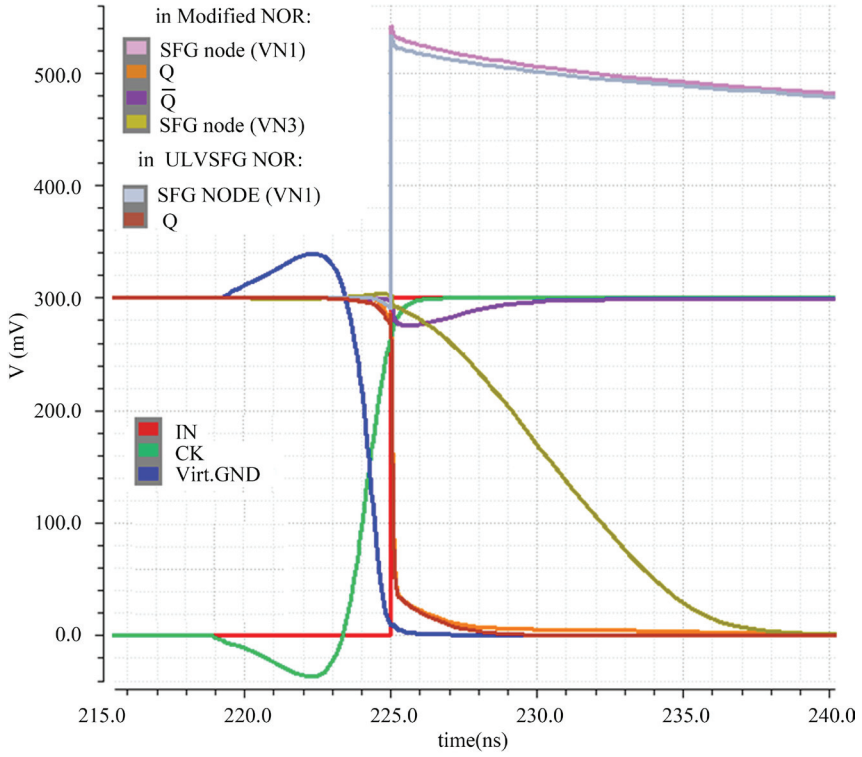


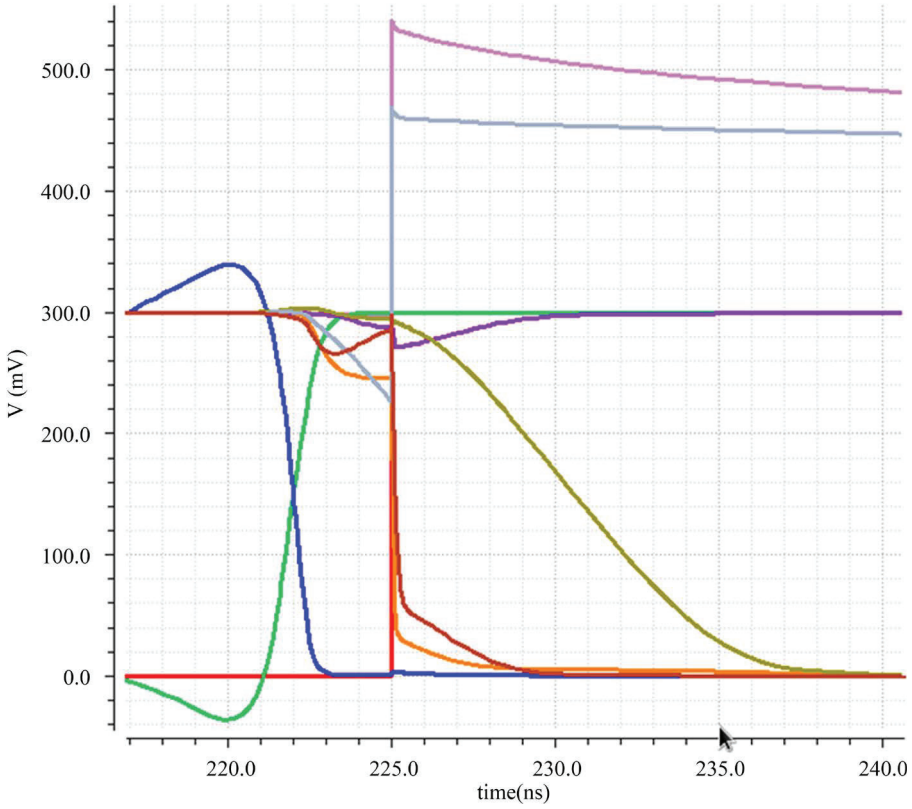
Figure 4. Modified dual-rail ULVSFG NOR gate.

4. Simulation Results

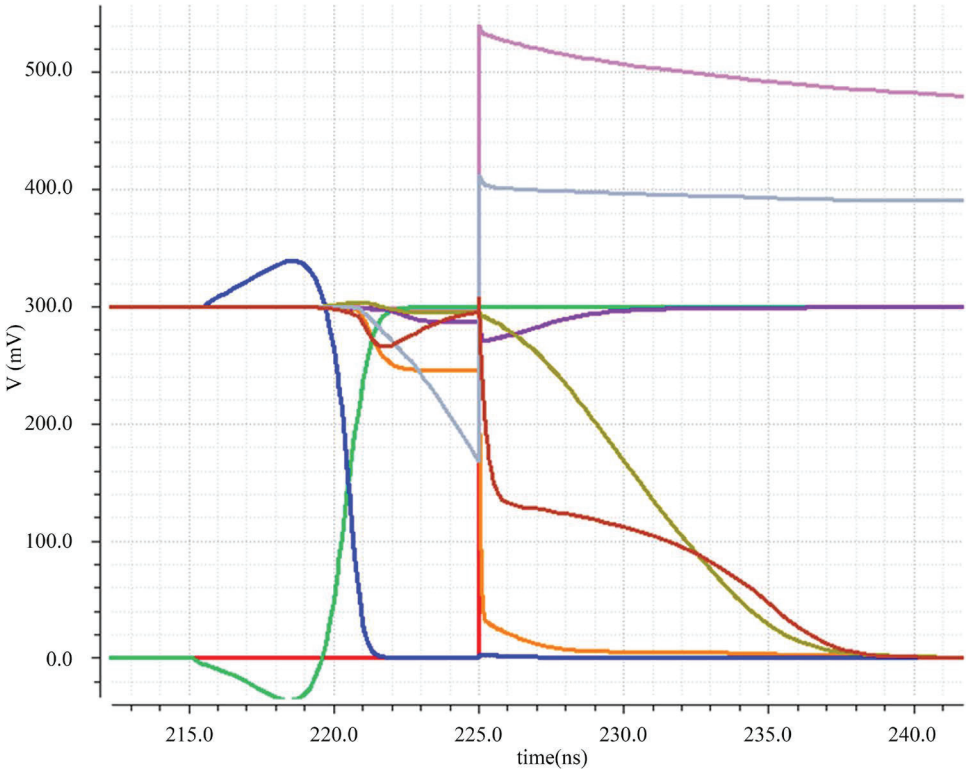
The simulations for the designed logic circuits are done using Cadence software (version 6.1.6) in a typical 90 nm TSMC CMOS technology. Low threshold voltage devices are chosen to speed up the circuit. To verify the effect of the SFG technique on the performance of the ULV dual-rail NOR gate, ULVSFG NOR gates, shown in **Figure 1(b)**, **Figure 3** and **Figure 4** are designed in the same device size, power supply voltage (300 mV) and load capacitors (CL = 2 fF), and finally the characteristics are studied. In the all designed circuits, a 2 fF capacitor is chosen for the input (Cin) capacitors. Simulation result shows that this size is the optimum capacitor size for the maximum speed, when the minimum size devices are used for the precharge devices. In the evaluation phase, simulation results for ULVSFG NOR gates shown in **Figure 3** and **Figure 4**, show that a falling transition (1 to 0) in the output (Q) takes less than 50 pS, while the same transition in the conventional dual-rail NOR gate, shown in **Figure 1(b)**, takes 1.7 nS. However, in both circuits, the falling transition (1 to 0) in the $\overline{Q}$ side is slower than Q side. This happens since both circuits are using stacked (cascode) transistors in the $\overline{Q}$ path. For the proposed NOR gate falling transition in $\overline{Q}$ takes 140 pS and for the conventional NOR gate shown in **Figure 1(b)** it takes 2.4 nS to switch from high to low level. **Figure 5** shows the transient simulations results for the both simple ULVSFG NOR gate shown in **Figure 3**, and for modified version shown in **Figure 4** when the input signal arrive with different delays compared to the CK signal, and in this case, there is at least one rising edge in the input signals (True sides) of the NOR gates which pulls down the output voltage signal to the Virt.GND. In **Figure 5(a)**, there is not significant delay in input signal compared to CK signal and both NOR circuits shown in **Figure 3** and **Figure 4** manage to pull down the output voltage to Virt.GND in the almost same evaluation time. In this case, for both circuits, the voltage of the SFG node (VN1) is larger than 500 mV which is well above VDD = 300 mV. It is considerable that the Virt.GND signal is settled down to 0 before arriving the input signal. In **Figure 5(b)**, there is a 3nS delay in the input signal compared to CK signal and both NOR circuits shown in **Figure 3** and **Figure 4** manage to pull down the output voltage to Virt.GND. However the modified version is faster than ULVSFG NOR gate shown in **Figure 3**, since it holds the voltage of the SFG node, longer and has larger voltage at that node. In this case the voltage of the SFG node (VN1) in modified version is larger than 500 mV while it is reduced to 460 mV in the simple ULVSFG NOR gate. In **Figure 5(c)**, there is a 4.5 nS delay in the input signal compared to CK signal and both NOR circuits shown in **Figure 3** and



(a)



(b)



(c)

Figure 5. Transient simulation results when a 1 to 0 transition occurs in Q.

Figure 4 manage to pull down the output voltage to Virt.GND. However the modified version is much faster than ULVSFG NOR gate shown in **Figure 3**, since it hold the voltage of the SFG node, longer and has larger voltage at that node when input signal arises. In this case the voltage of the SFG node (VN1) in modified version is larger than 500 mV while it is reduced to less than 400 mV in the simple ULVSFG NOR gate. The evaluation delay of the simple ULVSFG NOR gate is significantly increased by the delay of the input signal as shown in **Figures 5-7**. The simulated response for the ULVSFG NOR gates, when a delayed input-signal edge of 7 ns relative to the clock signal (CK), are shown in **Figure 6**. As expected the voltage of the SFG node in the ULVSFG NOR gate shown in **Figure 3**, is reduced well below VDD by the leakage currents and the ON currents of the KN transistors. The EN transistors are not be able to pull down the output to 0 (Virt. GND) given the voltage swing at the capacitive coupled input signal. Clearly, the responses of the ULVSFG gates are significantly affected by the input delay as depicted in **Figure 7**. For the modified version shown in **Figure 4**, the case is different, the functionality of the structure will not be affected by the delayed input edge and the voltages of the SFG nodes of the gate remain stable at VDD. With given feature sizes of **Table 1** for the ULVSFG NOR gates, the longest delay for an input signal edge is approximately 4.7 nS to manage to respond correct logically. The timing of the input signals significantly degrade the performance of the simple ULVSFG NOR gates as shown in **Figures 5-7**. This is because the initial charge of the SFG node in the ULVSFG NOR gate is reduced to smaller than VDD/2 and the current provided by the EN transistor is reduced significantly. The input swing gives the same capacitive transfer to the SFG node, but due to the fact that the voltage of the SFG node is VDD/2, the maximum peak would be approximately 300 mV on this node. One other crucial aspect is the outputs voltage swing. Considering a chained structure, the succeeding gate would receive an input signal with a lower swing than expected and hence would give a slower response. Hence the simple ULVSFG NOR gate has less noise margin comparing to modified version. In summary, the ULVSFG NOR gate suffers both from the increased output delay as well as the degenerated voltage swing (less noise margin). For smaller delays in the input signal, e.g. less than 3 ns, the response of the simple ULVSFG NOR is only affected by the reducing speed in the evaluation phase compared to the modified version shown in **Figure 4** which is not sensitive to delay of the input signals and has better output signal swing and noise margin. By increasing the delay at the input signal,

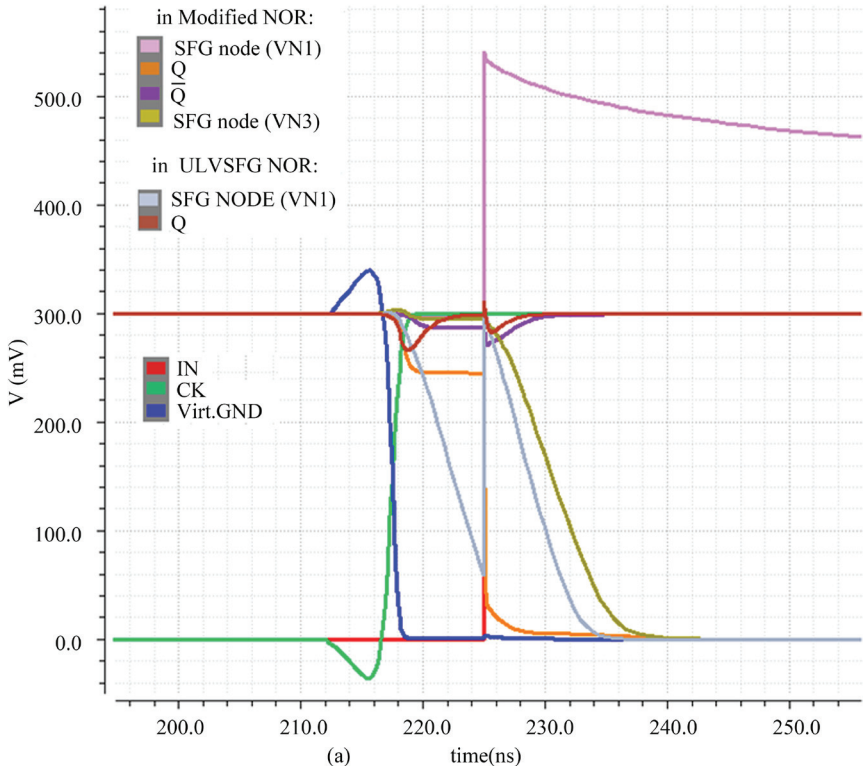


Figure 6. Transient simulation results when a 1 to 0 transition occurs in Q, and when the input signals has significant delay compared to the CK signal.

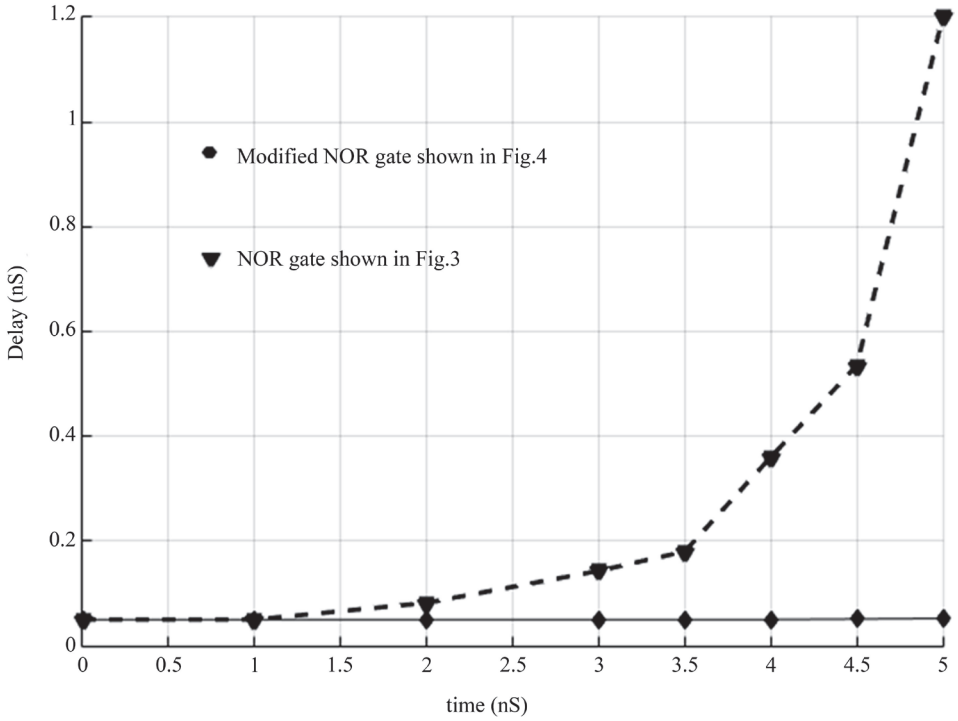


Figure 7. The evaluation delay of the simple ULVSFG NOR and modified version of ULVSFG NOR, gates for delayed input signals, relative to the clock signal CK.

Table 1. Size of transistors used in the ULVSFG NOR gates.

Device	W*nm*/L*nm*	Device	W*nm*/L*nm*
EN1-EN2	120/100	RN1-RN2	120/100
EN3-EN4	315/180	KN1-KN4	120/100
EP1-EP2	480/120	RP1-RP4	120/100

noise margin degrades significantly. Moreover, that is not the case for the Modified ULVSFG NOR gate. The delay of the ULVSFG NOR and ULVSFG modified NOR gate as functions of the input delay (relative to the CK) are shown in **Figure 7**. For input delays above 1.5 ns the delay of the ULVSFG NOR gate increases almost exponentially, whereas the delay of the modified ULVSFG NOR gate is stable at approximately 50 ps. The details of the evaluation delay of the ULVSFG NOR gate compared to modified version, is shown in **Figure 7**. The improvements as the data shows are 25 times at 4.8 nS. The delay for the proposed NOR gates are less than 5% of the delay of the conventional dual-rail NOR gate in same device size and power supply voltage. Simulation results show that the proposed circuit is operating properly with power supplies down to 100 mV. At those low power supplies, the speed reduces significantly, structures become more sensitive to process variations and overall performance of the structure reduces. However, ULVSFG structures are faster and more robust than conventional static CMOS and dual-rail domino logic in those ultra low voltage power supplies, as mentioned in [13]-[19].

5. Conclusion

In this paper, new NOR gate based on the ULVSFG dual-rail domino logic structure is presented. By applying the floating gate technique to the conventional dual-rail NOR gate, speed of the circuit increased significantly at the cost of increasing the complexity of the structure. Using the proposed method, delay of the ULVSFG Domino dual-rail NOR gate, is reduced more than 20 times in the evaluating phases and structure becomes robust significantly. The delay for the proposed NOR gates is less than 5% of the delay of the conventional dual-rail NOR gate in same device size and power supply voltage. Also a new keeper structure is introduced which makes

the SFG technique more robust against the delay of the input signal. Using the new keeper structure, high-depth logics are feasible to implement with the SFG technique. Simulation results using 90 nm TSMC CMOS process parameters and Cadence software, confirm the predicted improvements.

References

[1] Rabaey, J.M., Chandrakasan, A. and Nikolic, B. (2003) Digital Integrated Circuits: A Design Perspective.

[2] Harris, D. (2004) Introduction to CMOS VLSI Design—Lecture 9: Circuit Families (Lecture Notes on the Subject). Harvey Mudd College, Claremont.

[3] Arthurs, A., *et al.* (2012) Ultra-Low Voltage Digital Circuit Design: A Comparative Study. *IEEE Faible Tension Faible Consommation* (*FTFC*), June 2012, 1-4.

[4] Ijjada, S.R., Ayyanna, G., Reddy, G.S. and Rao, D.V.M. (2011) Performance of Different CMOS Logic Styles for Low Power and High Speed. *International Journal of VLSI Design & Communication Systems* (*VLSICS*), **2**, No. 2.

[5] Aguirre-Hernandez, M. and Linares-Aranda, M. (2011) CMOS Full-Adders for Energy-Efficient Arithmetic Applications. *IEEE Transactions on Very Large Scale Integration* (*VLSI*) *Systems*, **19**, 718-721.

[6] Heald, R. (2000) A Third-Generation SPARC V9 64-b Microprocessor. *IEEE Journal of Solid-State Circuits*, **35**, 1526-1538. http://dx.doi.org/10.1109/4.881196

[7] Bearden, D.R. (2000) A 780 MHz PowerPC/Sup TM/Microprocessor with Integrated L2 Cache. *International Solid-State Circuits Conference*, August 2000, 90-91.

[8] Silberman, J., *et al.* (1998) A 1.0-GHz Single-Issue 64-Bit Power PC Integer Processor. *IEEE Journal of Solid-State Circuits*, **33**, 1600-1607. http://dx.doi.org/10.1109/4.726542

[9] Sung, R.J.-H. and Elliott, D.G. (2007) Clock-Logic Domino Circuits for High-Speed and Energy-Efficient Microprocessor Pipelines. *IEEE Transactions on Circuits and Systems II*: *Express Briefs*, **54**, 460-464. http://dx.doi.org/10.1109/TCSII.2007.892212

[10] Kumar, R. (2001) Interconnect and Noise Immunity Design for Pentium 4 Processor. *Intel Technology Journal*, **Q1**, 1-12.

[11] Kundu, R. and Blanton, R.D. (2003) ATPG for Noise-Induced Switch Failures in Domino Logic. ICCAD-2003. *International Conference on Computer Aided Design* (IEEE Cat. No.03CH37486), San Jose, CA, 765-768.

[12] Shibata, T. and Ohmi, T. (1992) A Functional MOS Transistor Featuring Gate-Level Weighted Sum and Threshold Operations. *IEEE Transactions on Electron Devices*, **39**, 1444-1455.

[13] Mahmood, S.M. and Berg, Y. (2013) Ultra-Low Voltage and High Speed NP Domino Carry Propagation Chain. 2013 *IEEE Faible Tension Faible Consommation*, Paris, 1-4.

[14] Mirmotahari, O. and Berg, Y. (2013) Robust Low-Power CMOS Precharge Logic. *Proceedings of the* 11*th Edition of IEEE Faible Tension Faible Consommation*, Paris, June.

[15] Berg, Y. and Mirmotahari, O. (2012) Ultra Low-Voltage and High Speed Dynamic and Static Cmos Precharge Logic. *FTFC* 2012: *The* 11*th International Conference of Faible Tension Faible Consommation* (*FTFC*), IARIA, Paris, 6-8 June 2012, 1-4. http://dx.doi.org/10.1109/ftfc.2012.6231718

[16] Berg, Y., Lande, T.S. and Næss, Ø. (2001) Programming Floating-Gate Circuits with UV-Activated Conductances. *IEEE Transactions on Circuits and Systems*, **48**, 12-19.

[17] Berg, Y. (2011) Novel High Speed Differential CMOS Flip-Flop for Ultra Low-Voltage Applications. *Proceedings of the* 9*th Edition of IEEE New Circuits and Systems Conference* (*NEWCAS*), Bordeaux, 26-29 June 2011, 241-244. http://dx.doi.org/10.1109/newcas.2011.5981300

[18] Berg, Y. and Mirmotahari, O. (2012) Ultra Low-Voltage and High Speed Dynamic and Static Precharge Logic. *Proceedings of the* 11*th Edition of IEEE Faible Tension Faible Consommation*, June 2012, Paris.

[19] Berg, Y. and Mirmotahari, O. (2012) Novel High-Speed and Ultra-Low-Voltage CMOS NAND and NOR Domino Gates. *Proceedings of the* 5*th international Conference on Advances in Circuits*, *Electronics and Micro-Electron- ics*, Rome, 19-24 August 2012.

Paper VII

"Energy-Efficient, Fast-Settling, Modified Nested-Current-Mirror, Single-Stage-Amplifier for High-Resolution LCDs in 90-nm CMOS"

Ali Dadashi, Yngvar Berg, and. Omid Mirmotahari
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Energy-efficient, fast-settling, modified nested-current-mirror, single-stage-amplifier for high-resolution LCDs in 90-nm CMOS

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Abstract
A modified nested-current-mirror (NCM) Single-Stage amplifier, for high-performance, liquid crystal display panels, is presented in this paper. The proposed NCM is more than 8 times faster than the original NCM structure, without any extra static power consumption. Slew rate of the NCM is improved 10 times and DC-gain is also improved 6 dB, while the power consumption, gain-bandwidth product, output voltage swing range, and the phase margin of the NCM are not affected to great extent and the input-referred-noise is reduced 12%. Proposed NCMs achieve relatively higher figure of merit in comparison to previously reported NCM amplifiers and other state-of-the-art works. The significant performance improvement is obtained due to a novel slew-rate enhancer circuit. The simulation results for the designed NCM in a typical 90 nm CMOS technology confirm the predicted performance improvements.

Keywords Nested-current-mirror (NCM) Single-Stage amplifier · Settling-time · Slew-rate · Figure of merit (FOM) · Noise

1 Introduction

Modern mobile devices, smart phones, medical systems, and modern TVs, utilize high performance active-matrix LCD, which have a wide range of capacitive loads (CL). The columns of flat display panels using organic light emitting diodes (OLEDs), are also heavily capacitive. Therefore, the active-matrix (AM) and passive-matrix (PM) LCDs, as well as voltage-driven AMOLEDs and PMOLEDs, require voltage buffer amplifiers in their column drivers. As LCD displays approach high resolution, higher color depth, high quality, and physically large panel size, the design of the output buffer amplifiers becomes increasingly challenging. More specifically, the buffer amplifier needs to be faster to deal with larger load capacitance and thereby achieve smaller settling -time. In addition, hundreds, or thousands of buffer amplifiers are integrated into one driver IC, and the buffer should occupy a small die area and consume small static power. Consequently, for active-matrix LCDs, ultra-low power and area circuit solutions are continuously urged to meet the market pressure on cost, image quality and display size. Within the LCD column driver, it contains shift registers, input registers, data latches, level shifters, DACs and output buffers. Among these components, DACs and output buffers determine the speed, resolution, voltage swing, and power dissipation of a column driver. Currently, multi-stage amplifiers dominate those applications owing to their key advantages of high DC-gain and rail-to-rail output swing. However, the frequency compensation of these amplifiers increases their design complexity, which also restricts their drivability range and maximum load size, area and power efficiencies. Because of the stability issue, the multiple-stage amplifiers should be designed as different types to drive different values of CL. However, for numerous designs, each of them is required to be individually optimized, which increases the design complexity. To reduce the design complexity, a single type of amplifier that can drive various values of CL is desirable. This can be accomplished using classical single-stage amplifiers which were not used in those buffers because of their limited capability in most metrics despite being almost unconditionally stable at any CL size. Most single-stage amplifiers

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suffer from a tradeoff between power consumption and performance. Folded cascode and telescopic amplifiers are not good candidate for low power LCD buffer amplifiers, since they suffer from limited output voltage swing, even though they have a promising GBW to power efficiency. For LCD column drivers, simple current-mirror amplifiers (CMA) are favored for their rail to rail output swing, and extra design flexibility via adjusting the mirror ratio, K [1]. The original NCM technique, presented in [1, 2], improves the overall performance of the single stage CMA, significantly. DC-gain, GBW and SR of the simple CMA is improved, and the reported measurement results for the fabricated prototype, confirm comparable figure of merit, comparing to the other state-of-the-art, single stage and multi stage amplifiers. Both FOM1 = [(GBW.CL)/(Power.Area)] and FOM2 = [(SR.CL)/(Power.Area)] are comparable with other state-of -the-art works. The CL drivability (CLmax/CLmin) is wider than [3–8], while avoiding the stability limit at the heavy-CL side. This paper introduces a modified NCM single-stage amplifier, which furthermore speed-up the settling performance of the NCM amplifier without any power, output swing range, noise, or stability penalties. In this research work, we suggested that, to have a fair merit evaluation, despite [1], the worst-case settling-time (normally for large-signal transition), should be used to calculate FOM. The speed limitation of [1], originated mainly by the SR limitation of the NCM amplifiers.

Therefore, in this paper, a new SR enhancer circuit is designed to reduce the settling-time of the amplifiers. Significant performance improvement is obtained due to a novel slew-rate enhancer circuit. The rest of this paper is organized as follows, in Section II, the Original NCM structure and the proposed NCM with SR booster is described. In Section III, the measurement results for the different NCM amplifiers are given, and compared; finally, Section IV concludes the paper.

2 Proposed NCM amplifier

The NCM single-stage amplifier is introduced in [1] as a circuit technique to optimize the performance metrics (GBW, DC-gain and SR) of the simple CMA. The NCM technique is analyzed in detail in [1, 2], and the DC-gain, SR, noise, GBW, Phase margin, and robustness specifications of the amplifier are analytically explained and discussed. However, for the 4-step NCM reported in [1], despite 33 times improvement in GBW, and 1.9 times improvement in SR, only 2.27 times improvement in the average settling-time is reported. Also for the 3-step NCM reported in [2], despite 7.5 times improvement in GBW, and 1.33 times improvement in SR, only 1.5 times improvement in the average settling-time is reported, and the worst-case settling-times are not reported for NCMs. In fact, the technique presented in [1] improves the small-signal settling-time, and not the large-signal speed, and the overall settling-time of the amplifier, is limited by the limitation of the SR. It is considerable that the input signal for the buffer amplifiers in a typical LCD column driver, are normally sampled signal [9]. Therefore, to have a fair merit evaluation, the worst-case settling-time (normally large-signal transition), considering the both rising and falling edges, should be used to evaluate the performance of the amplifiers, and not only the average settling-time which is used in the [1] and [2].

Figure 1 shows the proposed 4-step NCM amplifier in this work with SR enhancer circuit. For simplicity, the bias current generator device (Mb) in [1], is split into two different devices in this work (Mb0 and Mb1). As depicted in Fig. 1, when a large transition in the input signal happens, despite the Ib0, the bias current of Mb1 (Ib1), does not have a role in the SR of the NCM, since there is no path for Ib1 to contribute in the charging or discharging process of the CL. So the SR of the original 4-step NCM in [1], is limited to [(2K7.(1 + K6).Iu/CL)], as calculated in [1]. The same scenario happens for the 3-step NCM, as discussed in [2]. Indeed, during the slew phase, the bias current of Ib1, dissipates, without having any positive role on the charging or discharging of the CL, and this effectively slow down the transient process of the original NCMs. To speed up the NCM structure, during the large-signal transitions, a slew detector and enhancer is designed in this work [shown in Fig. 1(b)] which activates during the slew phase and feeds the bias current of Ib1, to Vcm1 or Vcm2 nodes, depends on the rising or falling transition. The total current of [Ib0 + Ib1], multiplies by the current-mirror ratio (K7) of the last current mirrors and feeds to CL. This technique significantly increases the SR and speed of the NCM, with only negligible extra current consumption (50nA), which dissipates in the designed SR detector circuit. In this case the SR increases to [2K7.(1 + K1 + K2 + K3 + K4 + K5 + K6).Iu/CL)]. Using the same current-mirror ratios (K), used in [1] for 4-step NCM (K1 = 2, K2 = 6, K3 = 1, K4 = 4, K5 = 2, K6 = 8, K7 = 6), proposed technique increases the SR of the original 4-step NCM, about 2.65 times. Also, applying the proposed technique for the 3-step NCM, with the same mirror ratio used in [2] (K1 = 2, K2 = 3, K3 = 1, K4 = 3, K5 = 5), the SR increases 2.5 times. Furthermore, for aggressive SR and speed boosting, the circuit shown in Fig. 1(c) is designed, which activates by SR detector circuit shown in Fig. 1(b), and feeds the current of Ibs1 to the Vcm1,2 node, and increases the total charging and discharging current of CL, more than 5 times, using the

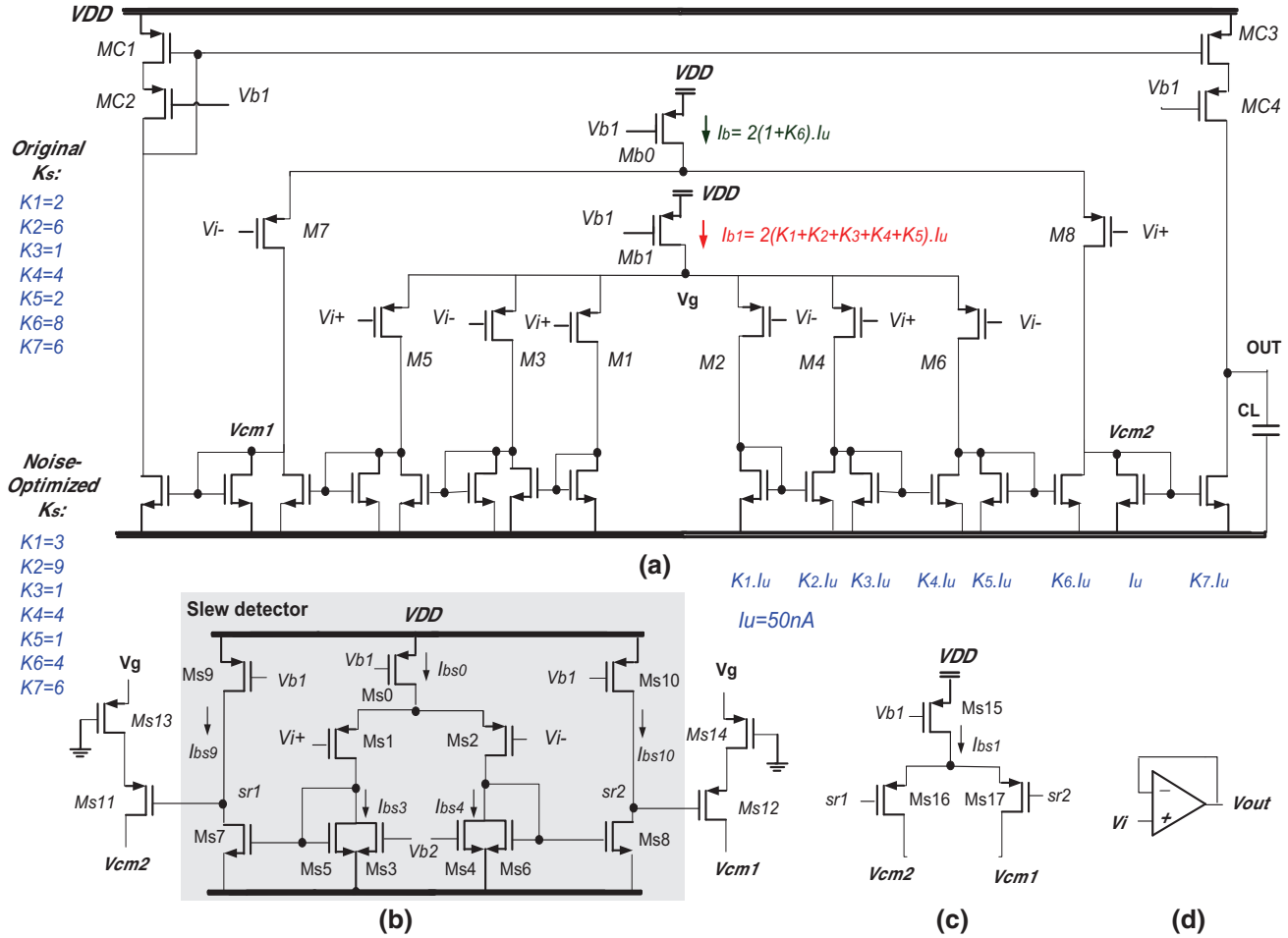

Fig. 1 Proposed 4-Step NCM. **a** Main amplifier, **b** SR enhancer, **c** aggressive SR enhancer, **d** unity-gain configuration

Ms16,17 devices which are normally OFF, during the small-signal operation of the NCMs.

The proposed low-power slew detector is shown in Fig. 1(b), and formed by Ms0-Ms10 devices. This circuit is partially not active during the small-signal operation of the amplifier and activates only when a large-signal transition happens. In the normal small-signal condition, only Ms0-Ms4 devices have static current. Hence the circuit does not affect the noise, DC-gain, and small-signal settling-time specification of the original NCM amplifier, to great extent. When a large-signal transition happens, Ms11,12 and Ms16,17 devices (depend on the rising or falling transition), activate by the slew detector circuit, and feed the bias current of [Ib1 + Ibs1] to Vcm1,2 node. During the small-signal operation of the amplifier the Ms5-Ms8 devices as well as Ms11-Ms14 devices, are turned off and become inactive, and the bias current of Ibs0, is carried by Ms3 and Ms4 devices. Therefore, for the small-signal operation mode, sr1 and sr2 nodes are pulled up to the supply voltage ($\sim$ VDD), by the bias current generator devices (Ms9 and Ms10). In the large-signal operation, depend on the rising or falling phase; Ibs0 directs to the either Ms1 or Ms2 devices. In this case, [Ibs0-Ibs3,4], flows throw Ms5,6 and amplifies by the current-mirrors formed by Ms5-Ms8. The current gain of these current-mirrors is set to 5. In this case, the current of Ms7,8 device becomes larger than the bias current of Ms9,10 (Ibs9,10), and the voltage of sr1,2 node, drops to the ground voltage ($\sim$ 0 V). Therefore, Ms11,12 and Ms16,17 devices, become ON and direct the bias current of [Ib1 + Ibs1], to Vcm2,1 node. This technique increases the total currents that charges or discharges CL, in the SR phase. Since the source of Ms13 and Ms14 devices are connected to the virtual ground node (Vg), they do not influence the frequency response of the amplifier, and the small-signal settling-time of the amplifier remain unaffected by these devices. Ms11 and Ms12 devices are used to separate the parasitic capacitance at the drain node of Ms13,14, from Vcm1,2 nodes. In this design, to have a higher area-efficiency, Ms0-Ms6, Ms11 and Ms12 devices, designed to have minimum dimension size (*W/L*). However, on the other side, Ms13,14 should have comparable size compared to those of M1-M6. The minimum

dimension value for Ms13,14, is determined by the worst-case transition in the input signal. In the slew phase, the worth-case transition, occurs when the input or output signal transits from/to the minimum value ($\sim$ 0.15 V). In this case, Ib1 flows throw M1, M4 and M5 devices in the falling mode, or throw M2, M3 and M6 devices, when a rising transition happens. Therefore, the size of Ms13,14 devices should be comparable to $\left[(W/L)_{M1,2}+(W/L)_{M4,3}+(W/L)_{M5,6}\right]$ to bypass the bias current of Ib1 to Vcm1,2 node. Ms13,14 designed with the minimum channel length to have higher area-efficiency.

In the NCM structure, the transistor's noise also amplifies by the mirror ratios, as discussed in [1] and [2]. The 4-step NCM structure designed in [1], tradeoffs noise performance for a higher SR, by utilizing larger bias currents and mirror ratios in the last current-mirrors (K6 and K7), for the higher SR, and using smaller bias currents (Ib1) for the M1-M6 devices. Since the noise generated by M1-M4 devices, amplify with the maximum gain, noise of these devices, dominates the overall noise performance of the amplifier. This issue relaxed in the proposed 4-step NCM, by increasing K1, K2, and the bias currents and feature sizes of the M1-M4 devices, in one hand, and decreasing K5, K6, and the bias currents and feature sizes for the M5-M8 devices, in the other hand, as shown in Fig. 1 (K1 = 3, K2 = 9, K3 = 1, K4 = 4, K5 = 1, K6 = 4, K7 = 6). Since the proposed 4-step NCM, benefits from the SR enhancer circuit, it is not necessary to have large value for K6, and at the same time, other performance metrics of 4-step NCM (Dc-gain, GBW, SR), remain unchanged to great extent.

Using cascode PMOS current-mirror, formed by the Mc1-Mc4 devices, the output impedance of the amplifier is increased 2 times, and DC-gain of the circuit is improved 6 dB compared to [1], which uses simple PMOS current-mirror. Since the amplifier is used in the unity-gain configuration of Fig. 1(d), the Vi- node is connected directly to the output node. Therefore, the output voltage swing range, is limited by the threshold voltages and the overdrive voltages of the input differential pair devices (Mb0,1, M1–M8) rather than the PMOS cascode devices. In addition, using the cascode structure for the PMOS current-mirror, improves the linearity of the current mirror and the NCM amplifiers, since it minimizes the drain-source voltage variations for the Mc1 and Mc3 devices and the current-mirror ratio, does not affect by the large voltage variations at the output node.

3 Results and discussion

In this section, the simulation results of the proposed 3-Step and 4-Step NCM amplifiers are shown and the proposed NCM amplifiers are compared with the original NCMs. A prototype for the designed amplifiers has been laid out in the 90 nm CMOS technology. The original NCMs and proposed 3-Step and 4-Step NCM amplifiers have been designed under the same power consumption and the same power supply, and finally the characteristics for the different capacitor loads are compared in Table 1. The total bias current (3μA) is divided into 60 unit currents (Iu = 50nA) in 4-step NCMs and is divided to 30 in 3-step NCMs (Iu = 100nA) and designs has the same current-mirror ratios (K) as in [1] and [2]. Transient simulations for the different amplitudes in the input signal, proposed NCMs achieves higher speed comparing to the original one, thanks to the SR enhancer circuit. Figure 2 shows the step response, for the proposed NCM amplifiers comparing to the original NCMs, for the different step amplitudes. The worst-case settling-time of the proposed 4-step NCM, is 9 times shorter than that of the original one, without significant extra static current consumption (only 50nA), as predicted before by the circuit analyzing. Simulations shows the 9 times speed increase for the proposed 3-step NCM comparing to the original 3-step NCM, as shown in Fig. 2, for the different capacitor loads. Figure 3 shows the AC response for the proposed 3-step and 4-step NCMs. Simulations confirm that the proposed NCMs in this work achieve the same UGBW, as the original NCMs, and the SR booster does not reduce the UGBW of the NCMs to great extent. For the proposed 4-Step NCM, AC simulation shows 0.014-to-2 MHz GBW, and for the proposed 3-Step NCM, 2.8-to-419 kHz GBW, linearly scalable with CL from 15 to 0.1nF, which are equal to those of the original NCM amplifiers. Furthermore, the proposed NCMs achieve 6 dB higher DC-gain thanks to the cascode structure at the PMOS current-mirror (MC1-MC4) for the both 3-step and 4-step NCMs. Three different FOMs are used to compare the performance of the amplifiers. FOM1 and FOM2 are used as small-signal and large-signal performance evaluation factors in [1] and [2], respectively. As mentioned before, in this work, a new FOM (FOM3 = [(CL)/(Tst.-max.Power.Area)]) is defined to compare the performance of the amplifiers, in which the worst-case settling-time (*Tst.max*) of the amplifiers (considering both falling and rising edge), in the unity gain configuration, is used as a main speed determining factor instead of the only GBW or SR parameters used in [1, 2]. Simulation results show that the proposed NCM amplifiers in this work achieves slightly smaller FOM1 comparing to the original NCM amplifiers in [1] and [2] for both 3-step and 4-step NCMs, due to

Table 1 Specifications comparison

	Three-stage amplifier						Single-stage NCMs							
	[3]	[4]	[5]	[6]	[7]	[8]	Original [1, 2]				Proposed			
							3-step		4-step		3-step		4-step	
CL(nF)	0.15	15	1	4.4	0.5	0.5	0.1	15	0.1	15	0.1	15	0.1	15
UGBW (KHz)	440	950	560–2140	1008	2000	1340	419	2.8	2000	14	419	2.8	2000	14
DC-gain (dB)	110	> 100	63–80	> 100	> 100	> 100	54	54	69	69	60	60	75	75
1% worst-case settling-time (μS)	–	–	–	–	–	–	15	2300	12	1770	1.6	240	1.3	184
Phase margin (°)	57	52.3	88	55.4	52	53	83	90	63	90	83	90	63	90
SRav (V/mS)	1.8	0.22	5.8	0.233	0.65	0.62	39	0.25	56	0.37	390	2.5	560	3.7
Input-referred noise (nV/$\sqrt{\text{Hz}}$) @ 10 kHz	–	172	116	–	–	–	68	68	81	81	68	68	71	71
CL-drivability	–	15	–	∼ 4	–	5	150x>				150x>			
Area (mm^2)	0.02	0.016	0.0066	0.007	0.0088	0.007	0.0008				0.00085			
CMOS technology (μm)	0.35	0.35	0.5	0.18	0.065	0.18	0.09							
Power (μW)	3.6f	144	160	36.5	20.4	6.3	3.6							
Power supply (V)	1.5	2	5	1.8	1.2	0.9	1.2							
FOM1 [(MHz.nF)/(μW mm^2)]	1.1	6.185	0.53	18.6	5.5	15.2	14.5	14.6	69	73	13.7	13.7	65	69
FOM2 [(V/nS.pF)/(μW mm^2)]	0.45	1.43	5.5	4	1.8	7	1.35	1.3	1.94	1.91	12.7	12.2	18.3	18.1
FOM3 [(pF)/(μW μS mm^2)]	–	–	–	–	–	–	2.31	2.26	2.9	2.94	20.4	20.4	25.1	26.6

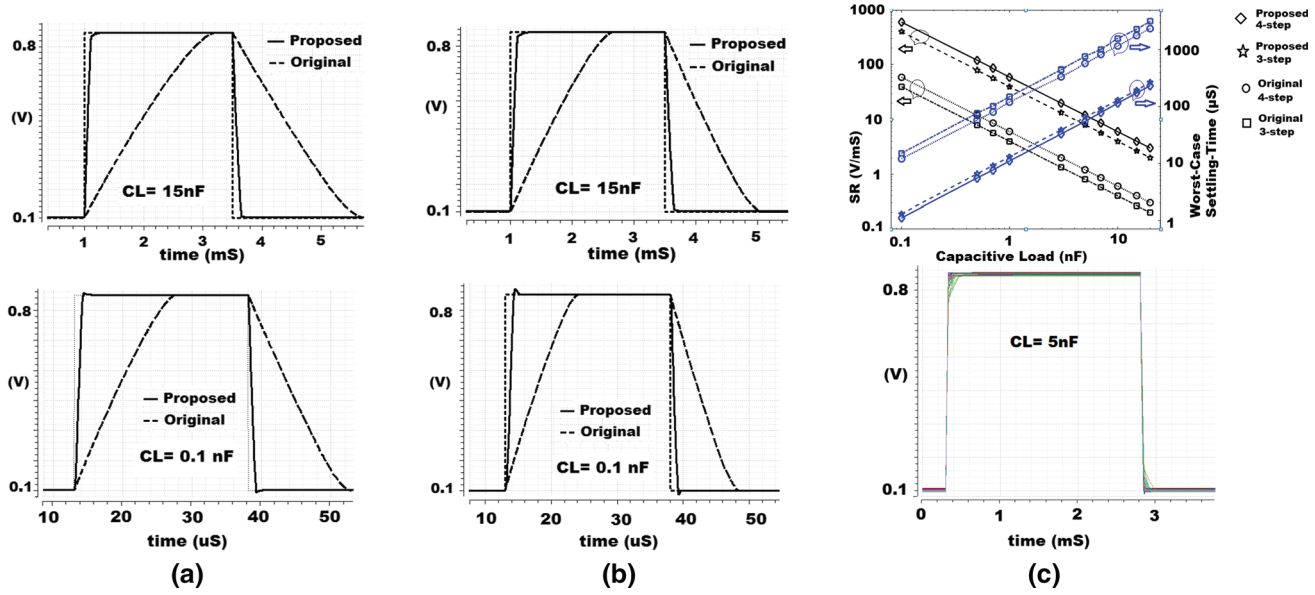

Fig. 2 Step-response of the NCMs. **a** 3-step, **b** 4-step, **c** top: SR and worst-case settling-time for different CL. bottom: Monte-Carlo simulations result (4-step)

increasing the area. The simulations confirm that, for the both 3-step and 4-step designs in this work, FOM2 is improved more than 9 times comparing to the original NCMs, thanks to the designed SR enhancer. In the same time, since the worst-case settling-time, is limited by the SR, the proposed NCMs achieves 9 times higher FOM3 comparing to the original NCMs. Noise simulation confirms that in the proposed NCMs, the input-referred-noise, is not increased by the SR enhancer structure, comparing to the original NCMs. Furthermore, noise simulations for the proposed SR-enhanced and noise-optimized 4-step NCM, (with K1 = 3, K2 = 9, K3 = 1, K4 = 4, K5 = 1, K6 = 4,

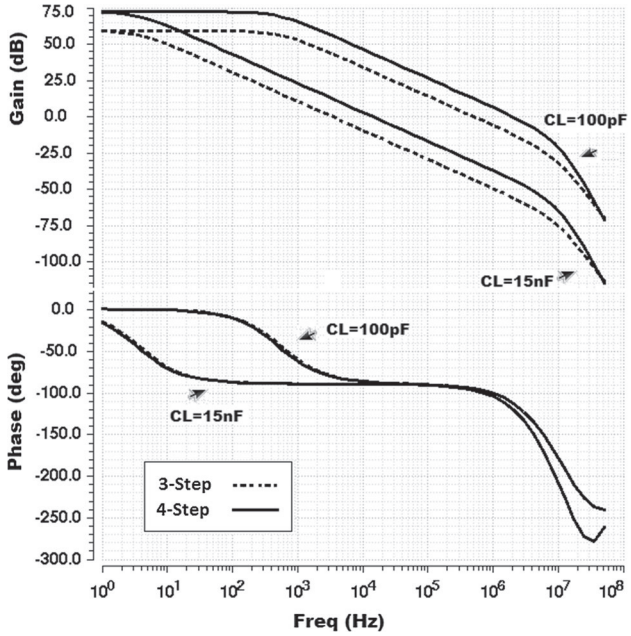

Fig. 3 AC response of the proposed NCM amplifiers

K7 = 6), confirms that, while the amplifier still benefits from 10 times higher SR, and 8 times shorter settling-time, the input-referred-noise reduces 12%, comparing to that of the original 4-step NCM. The robustness of the proposed NCM amplifiers against process and temperature variation, is evaluated by post-layout corner simulations at − 25, 0, 25 and 100 °C. For the proposed 4-step NCM, with CL = 10nF, the worst-case settling-time occurs at FS corner and at 100 °C, which still is 9 times shorter than that of the original 4-step NCM which has worst-case settling-time at SS corner and at − 25 °C. At 5nF CL, and under 100 × Monte-Carlo simulations (for both process and mismatch variations), the mean values for the SR of the both 3-step and 4-step, is still 10 times higher than those of original NCMs and the results confirm that the relative standard deviation of the SR is lower than 20%. The results are relatively robust, especially for applications in which the settling-time dominates by the SR. Finally, the characteristics of the designed NCMs are summarized in Table 1 for comparison.

4 Conclusion

This Paper introduced a new NCM amplifier, which improves the SR, settling-time, noise, and Dc-gain of the original NCM amplifier. Thanks to the designed SR enhancer circuit, the worst-case settling-time of the NCM amplifier, is improved more than 8 times, while preserving the power consumption, output swing, UGBW, Phase margin, and wide CL drivability without entailing any compensation capacitor or resistor, at the cost of increased complexity and negligible area. Rigorous simulations for implemented 3-step and 4-step NCM amplifiers confirmed the theoretical study and performance claims.

References

1. Yan, Z., Mak, P.-I., Law, M.-K. Martins, R., Maloberti, F. (2014). A 0.0013mm2 3.6 μW nested-current-mirror single-stage amplifier driving 0.15-to-15nF CLs with > 62° phase. In Solid-state circuits conference, digest of technical papers (ISSCC), pp. 288–289.
2. Yan, Z., Mak, P.-I., Law, M.-K., Martins, R. P., & Maloberti, F. (2015). Nested-current-mirror rail-to-rail-output single-stage amplifier with enhancements of DC gain, GBW and slew rate. *IEEE Journal of Solid-State Circuits, 50*(10), 2353–2366.
3. Peng, X., et al. (2011). Impedance adapting compensation for low-power multistage amplifiers. *IEEE Journal of Solid-State Circuits, 46,* 445–451.
4. Yan, Z. et al. (2012). A 0.016mm2 144 μW three-stage amplifier capable of driving 1-to-15nF capacitive load with > 0.95 MHz GBW. In *ISSCC Dig. Tech. Papers*, pp. 368–369.
5. Grasso, A. D., Marano, D., Esparza-Alfaro, F., Lopez-Martin, A. J., Palumbo, G., & Pennisi, S. (2014). Self-biased dual-path push-pull output buffer amplifier for LCD column drivers. *IEEE Transactions on Circuits and Systems I, 61*(3), 663–670.
6. Mak, K. H., & Leung, K. N. (2014). A signal- and transient-current boosting amplifier for large capacitive load applications. *IEEE Transactions on Circuits and Systems I, 61*(10), 2777–2785.
7. Chong, S., et al. (2012). Cross feedforward cascode compensation for low-power three-stage amplifier with large capacitive load. *IEEE Journal of Solid-State Circuits, 47,* 2227–2234.
8. Qu, W., Im, J.-P., Kim, H.-S., Cho, G.-H. (2014). A 0.9 V 6.3 μW multistage amplifier driving 500 pF capacitive load with 1.34 MHz GBW. In *IEEE ISSCC Dig. Tech. Papers*, pp. 290–291.
9. Lu, C.-W., Yin, P.-Y., Hsiao, C.-M., Chang, M.-C., & Lin, Y.-S. (2012). A 10-bit resistor-floating-resistor-string DAC (RFR-DAC) for high color-depth LCD driver ICs. *IEEE Journal of Solid-State Circuits, 47*(10), 2454–2466.

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Bibliography

[1] Marcus A.G. Santos, Roberto Munoz, Rodrigo Olivares, Pedro P. Rebouças Filho, Javier Del Ser, Victor Hugo C. de Albuquerque, “Online heart monitoring systems on the internet of health things environments: A survey, a reference model and an outlook, “, Volume 53, 2020, Pages 222-239, ISSN 1566-2535, https://doi.org/10.1016/j.inffus.2019.06.004.

[2] Shirvanimoghaddam, M., K. Shirvanimoghaddam, M. M. Abolhasani, Majid Farhangi, Vahid Zahiri Barsari, Hangyue Liu, M. Dohler and M. Naebe. “Paving the Path to a Green and Self-Powered Internet of Things.” (2017), Computer Science, Engineering, https://www.semanticscholar.org/paper/Paving-the-Path-to-a-Green-and-Self-Powered-of-Shirvanimoghaddam-

[3] H. Nakazawa, K. Sano, T. Abe, M. Baba, and N. Kumagai, “Charge–discharge characteristics of all-solid-state thin-filmed lithium-ion batteries using amorphous Nb2O5 negative electrodes,” *J. Power Sources*, vol. 174, no. 2, pp. 838–842, Dec. 2007.

[4] P. Harpe, H. Gao, R. v. Dommele, E. Cantatore and A. H. M. van Roermund, " A 0.20 mm2 3 nW Signal Acquisition IC for Miniature Sensor Nodes in 65 nm CMOS " in IEEE Journal of Solid-State Circuits, vol. 51, no. 1, pp. 240-248, Jan. 2016, doi: 10.1109/JSSC.2015.2487270.

[5] M. Wahbah, M. Alhawari, B. Mohammad, H. Saleh, and M. Ismail, “Characterization of human body-based thermal and vibration energy harvesting for wearable devices,” *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 4, no. 3, pp. 354–363, Sep. 2014.

[6] Patrick P Mercier, et. al “Energy extraction from the biologic battery in the inner ear” nature biotechnology 30, 1240-1243,2012, https://www.nature.com/articles/nbt.2394

[7] C. Himes, E. Carlson, R. J. Ricchiuti, B. P. Otis and B. A. Parviz, "Ultralow Voltage Nanoelectronics Powered Directly, and Solely, From a Tree," in IEEE Transactions on Nanotechnology, vol. 9, no. 1, pp. 2-5, Jan. 2010, doi: 10.1109/TNANO.2009.2032293.

[8] G. K. Fedder, R. T. Howe, T.-J. King Liu and E. P. Quevy, "Technologies for cofabricating MEMS and electronics," Proc. IEEE, vol. 96, no. 2, pp. 306-322, 2008.

[9] Shouri CHATTERJEE, Yannis TSIVIDIS, Peter KINGET, "Ultra-Low Voltage Analog Integrated Circuits" IEICE TRANSACTIONS on Electronics Vol.E89-C No.6 pp.673-680.

[10] P. R. Kinget, "Ultra-low Voltage Analog Integrated Circuits for nanoscale CMOS," 2007 IEEE Bipolar/BiCMOS Circuits and Technology Meeting, Boston, MA, 2007, pp. 144-148, doi: 10.1109/BIPOL.2007.4351856.

[11] B. Razavi, “Design of Analog CMOS Integrated Circuits”, McGraw- Hill, 2001.

[12] P. Harpe, H. Gao, R. van Dommele, E. Cantatore and A. van Roermund, "A 3nW signal-acquisition IC integrating an amplifier with 2.1 NEF and a 1.5fJ/conv-step ADC," 2015 IEEE International Solid-State Circuits Conference - (ISSCC) Digest of Technical Papers, San Francisco, CA, 2015, pp. 1-3, doi: 10.1109/ISSCC.2015.7063086.

[13] M. Liu, K. Pelzers, R. van Dommele, A. van Roermund and P. Harpe, "A106nW 10 b 80 kS/s SAR ADC With Duty-Cycled Reference Generation in 65 nm CMOS," in IEEE Journal of Solid-State Circuits, vol. 51, no. 10, pp. 2435-2445, Oct. 2016, doi: 10.1109/JSSC.2016.2587688.

[14] A. Liendo, D. Morche, R. Guizzetti and F. Rousseau, "Efficient Bluetooth Low Energy Operation for Low Duty Cycle Applications," 2018 IEEE International Conference on Communications (ICC), Kansas City, MO, 2018, pp. 1-7, doi: 10.1109/ICC.2018.8423011.

[15] W. Chen, Y. Su, Y. Lee, C. Wey and K. Chen, " 0.65V-input-voltage 0.6V-output-voltage 30ppm/°C low-dropout regulator with embedded voltage reference for low-power biomedical systems," 2014

IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC), San Francisco, CA, 2014, pp. 304-305, doi: 10.1109/ISSCC.2014.6757445.
[16] M. Aguirre-Hernandez and M. Linares-Aranda, "CMOS Full-Adders for Energy-Efficient Arithmetic Applications," in IEEE Transactions on Very Large-scale Integration (VLSI) Systems, vol. 19, no. 4, pp. 718-721, April 2011, doi: 10.1109/TVLSI.2009.2038166.
[17] R. H**.** Krambeck et.al "High-speed Compact Circuit with CMOS," IEEE JSSC, vol. 17, lune 1982.
[18] R. Kundu and R. D. Blanton, "ATPG for noise-induced switch failures in domino logic," ICCAD-2003. International Conference on Computer Aided Design (IEEE Cat. No.03CH37486), San Jose, CA, USA, 2003, pp. 765-768, doi: 10.1109/ICCAD.2003.159763
[19] Y. Tsividis, Operation and Modeling of the MOS Transistor, 2nd ed. New York: McGraw-Hill, 1999.
[20] M. Alioto, "Ultra-Low Power VLSI Circuit Design Demystified and Explained: A Tutorial," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 59, no. 1, pp. 3-29, Jan. 2012, doi: 10.1109/TCSI.2011.2177004.
[21] Rabaey, J.M., Chandrakasan, A. and Nikolic, B. (2003) Digital Integrated Circuits: A Design Perspective.
[22] Harris, D. (2004) Introduction to CMOS VLSI Design—Lecture 9: Circuit Families (Lecture Notes on the Subject). Harvey Mudd College, Claremont.
[23] Arthurs, A., *et al.* (2012) Ultra-Low Voltage Digital Circuit Design: A Comparative Study. *IEEE Faible Tension Faible Consommation* (*FTFC*), June 2012, 1-4.
[24] Ijjada, S.R., Ayyanna, G., Reddy, G.S. and Rao, D.V.M. (2011) Performance of Different CMOS Logic Styles for Low Power and High Speed. *International Journal of VLSI Design & Communication Systems* (*VLSICS*), **2**, No. 2.
[25] N. Paydavosi, et. al "BSIM4v4.8.0 MOSFET Model" Department of Electrical Engineering and Computer Sciences University of California, Berkeley, CA 94720. http://www.srware.com/xictools/docs/model_docs/bsim4.8.0/BSIM480_Manual.pdf.
[26] Heald, R. (2000) A Third-Generation SPARC V9 64-b Microprocessor. *IEEE Journal of Solid-State Circuits*, **35**, 1526-1538. http://dx.doi.org/10.1109/4.881196
[27] Sreenivasa Rao.Ijjada, Ayyanna.G, G.Sekhar Reddy, Dr.V. Malleswara Rao," Performance of Different CMOS Logic Styles for Low Power and High Speed" International Journal of VLSI design & Communication Systems (VLSICS) Vol.2, No. 2, June 2011.
[28] Bearden, D.R. (2000) A 780 MHz PowerPC/Sup TM/Microprocessor with Integrated L2 Cache. *International Solid-State Circuits Conference*, August 2000, 90-91.
[29] Silberman, J., *et al.* (1998) A 1.0-GHz Single-Issue 64-Bit Power PC Integer Processor. *IEEE Journal of Solid-State Circuits*, **33**, 1600-1607. http://dx.doi.org/10.1109/4.726542
[30] Sung, R.J.-H. and Elliott, D.G. (2007) Clock-Logic Domino Circuits for High-Speed and Energy-Efficient Microprocessor Pipelines. *IEEE Transactions on Circuits and Systems II*: *Express Briefs*, **54**, 460-464.http://dx.doi.org/10.1109/TCSII.2007.892212
[31] Kumar, R. (2001) Interconnect and Noise Immunity Design for Pentium 4 Processor. *Intel Technology Journal*, **Q1**, 1-12.
[32] Kundu, R. and Blanton, R.D. (2003) ATPG for Noise-Induced Switch Failures in Domino Logic. ICCAD-2003. *International Conference on Computer Aided Design* (IEEE Cat. No.03CH37486), San Jose, CA, 765-768.
[33] V. Kursun and E. G. Friedman, "Sleep switch dual threshold Voltage domino logic with reduced standby leakage current," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 12, no. 5, pp. 485-496, May 2004, doi: 10.1109/TVLSI.2004.826198.
[34] V. Kursun and E. G. Friedman, "Forward body biased keeper for enhanced noise immunity in domino logic circuits," 2004 IEEE International Symposium on Circuits and Systems (IEEE Cat. No.04CH37512), Vancouver, BC, Canada, 2004, pp. II-917, doi: 10.1109/ISCAS.2004.1329422.
[35] V. Kursun and E. G. Friedman, "Domino Logic with Variable Threshold Voltage Keeper", *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 11, no. 6, pp. 1080-1093, December 2003.

[36] V. Kursun and E. G. Friedman, "Node Voltage Dependent Subthreshold Leakage Current Characteristics of Dynamic Circuits", *Proceedings of the IEEE/ACM International Symposium on Quality Electronic Design*, March 2004.
[37] A. Alvandpour et al., "A Sub-130-nm Conditional Keeper Technique", *IEEE Journal of Solid-State Circuits*, vol. 37, no. 5, pp. 633-638, May 2002.
[38] Lee, Charles M., and ellen W. Szeto. "Zipper CMOS". IEEE Circuit and Device Magazine, 8755-3996/86/0500-0010, 1986.
[39] Shibata, T. and Ohmi, T. (1992) A Functional MOS Transistor Featuring Gate-Level Weighted Sum and Threshold Operations. *IEEE Transactions on Electron Devices*, **39**, 1444-1455.
[40] Berg, Y., Lande, T.S. and Næss, Ø. (2001) Programming Floating-Gate Circuits with UV-Activated Conductances. *IEEE Transactions on Circuits and Systems*, **48**, 12-19.
[41] T. S. Lande, D. T. Wisland, T. Soether and Y. Berg, "FLOGIC-Floating-gate logic for low-power operation," Proceedings of Third International Conference on Electronics, Circuits, and Systems, Rodos, Greece, 1996, pp. 1041-1044 vol.2, doi: 10.1109/ICECS.1996.584565.
[42] S. M. Mahmood and Y. Berg, "Ultra-low voltage and high speed NP domino carry propagation chain," 2013 IEEE Faible Tension Faible Consommation, Paris, 2013, pp. 1-4, doi: 10.1109/FTFC.2013.6577759.
[43] Mirmotahari, O. and Berg, Y. (2013) Robust Low-Power CMOS Precharge Logic. *Proceedings of the* 11*th Edition of IEEE Faible Tension Faible Consommation*, Paris, June.
[44] Berg, Y. and Mirmotahari, O. (2012) Ultra Low-Voltage and High Speed Dynamic and Static Cmos Precharge Logic. *FTFC* 2012: *The* 11*th International Conference of Faible Tension Faible Consommation* (*FTFC*), IARIA, Paris, 6-8 June 2012, 1-4. http://dx.doi.org/10.1109/ftfc.2012.6231718
[45] Berg, Y. (2011) Novel High Speed Differential CMOS Flip-Flop for Ultra Low-Voltage Applications. *Proceedings of the* 9*th Edition of IEEE New Circuits and Systems Conference* (*NEWCAS*), Bordeaux, 26-29 June 2011, 241-244. http://dx.doi.org/10.1109/newcas.2011.5981300
[46] Berg, Y. and Mirmotahari, O. (2012) Ultra Low-Voltage and High-Speed Dynamic and Static Precharge Logic. *Proceedings of the* 11*th Edition of IEEE Faible Tension Faible Consommation*, June 2012, Paris.
[47] Berg, Y. and Mirmotahari, O. (2012) Novel High-Speed and Ultra-Low-Voltage CMOS NAND and NOR Domino Gates. *Proceedings of the* 5*th international Conference on Advances in Circuits, Electronics and Micro-Electronics*, Rome, 19-24 August 2012.
[48] H. S. Bechmann, Master Thesis "High-Speed Digital Ultra-Low Voltage Floating Gate Design", 2014, University of oslo.
[49] L. Heller, W. Griffin, J. Davis and N. Thoma, "Cascode voltage switch logic: A differential CMOS logic family," 1984 IEEE International Solid-State Circuits Conference. Digest of Technical Papers, San Francisco, CA, USA, 1984, pp. 16-17, doi: 10.1109/ISSCC.1984.1156629.
[50] O. Mirmotahari, A. Dadashi, M. Azadmehr and Y. Berg, "Novel high-speed dynamic differential ultra low voltage logic for supply-voltage below 300 mV," 2015 IEEE International Conference on Electronics, Circuits, and Systems (ICECS), Cairo, 2015, pp. 53-56, doi: 10.1109/ICECS.2015.7440247.
[51] O. Mirmotahari, A. Dadashi, M. Azadmehr and Y. Berg, "High-speed dynamic dual-rail ultra low voltage static CMOS logic operating at 300 mV," 2016 International Conference on Design and Technology of Integrated Systems in Nanoscale Era (DTIS), Istanbul, 2016, pp. 1-4, doi: 10.1109/DTIS.2016.7483898.
[52] P. Meher and K. K. Mahapatra, "A technique to increase noise-tolerance in dynamic digital circuits," 2012 Asia Pacific Conference on Postgraduate Research in Microelectronics and Electronics, Hyderabad, 2012, pp. 229-233, doi: 10.1109/PrimeAsia.2012.6458660.
[53] Meher, Preetisudha and Mahapatra, K. K. (2013) "A New Ultra Low-Power and Noise Tolerant Circuit Technique for CMOS Domino Logic," International Journal of Computer and Communication Technology: Vol. 4: Iss. 3 , Article 6. Available at: https://www.interscience.in/ijcct/vol4/iss3/6

[54] J. Lin and C. Hsieh, "A 0.3 V 10-bit 1.17f SAR ADC With Merge and Split Switching in 90 nm CMOS," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 62, no. 1, pp. 70-79, Jan. 2015, doi: 10.1109/TCSI.2014.2349571.
[55] J. Steensgaard, "Bootstrapped Low-Voltage Analog Switches", IEEE Proc. Int. Symp. Circuits and Systems. Vol.2, pp. II 29- II 32, 1999.
[56] Seo, I. & Fox, R.M. "Comparison of Quasi-/Pseudo-Floating Gate Techniques and Low Voltage Applications" Analog Integrated Circuits and Signal Processing (2006) 47: 183. https://doi.org/10.1007/s10470-006-4818-0.
[57] J. Hyde, T. Humes, C. Diorio, M. Thomas, and F M. igueroa, "A floating-gate trimmable, 14-bit, 250 Ms/s digital-to-analog converter in standard 0.25 um CMOS." 2002 Symp. on VLSI Circuits Digest of Technical Papers vol. 23.3, pp. 328–331, 2002.
[58] A. J. Lopez-Martin, A. Carlosena and J. Ramirez-Angulo, "D/A Conversion Based on Multiple-Input Floating-Gate MOST," IEEE 42nd Midwest Symposium on Circuits and Systems, Vol. 1, pp. 149-152, 1999.
[59] K. Kotani, T. Shibata, M. Imai and T. Ohmi. "Clocked- Neuron-MOS Logic Circuits Employing Auto-Threshold-Adjustment", In IEEE International Solid-State Circuits Conference, pp. 320-321,388, 1995.
[60] T. Shibata and T. Ohmi. "A Functional MOS Transistor Featuring Gate-Level Weighted Sum and Threshold Operations", In IEEE Transactions on Electron Devices, vol 39, 1992.
[61] I. Seo, "Low-voltage low-power analog circuit techniques using floating-gate MOS transistors." Ph.D Dissertation, University of Florida, August 2004.
[62] J. Ramirez-Angulo, A.J. Lopez-Martin, R.G. Carvajal, and F.M. Chavero, "Very low voltage analog signal processing based on quasi-floating gate transistors." IEEE J. Sol.State Circuits vol. 39, pp. 434–442, 2004.
[63] F. Munoz, A. Torralba, R. G. Cavajal, J. Tombs, and J. Ramirez-Angulo, "Floating-Gate Based Tunable Low-Voltage Linear Transconductor and Its Application to HF GM-C Filter Design," IEEE Transactions on Circuits and Systems II, Vol. 48, No. 1, pp. 106-1 10, January 2001.
[64] Paul Hasler, Chris Diorio, Bradley A. Minch, "A four-quadrant floating-gate synapse", IEEE International Symposium on Circuits and Systems, 1998.
[65] Y. Berg, O. Mirmotahari, J. G. Lomsdalen, and S. Aunet, "High Speed Ultra Low Voltage CMOS inverter," in *Symposium on VLSI, 2008. ISVLSI '08. IEEE Computer Society Annual*, 2008, pp. 122-127.
[66] Yngvar Berg: Novel ultra-low-voltage and high-speed domino CMOS logic. VLSI-SoC 2010: 225-228
[67] J. M. Rabaey, A. Chandrakasan and B. Nikolic, "Digital Integrated Circuits: A Design Perspective", 2003.
[68] Yngvar Berg, Omid Mirmotahari: Low voltage precharge CMOS logic. DDECS 2009: 140-143.
[69] Yngvar Berg, Omid Mirmotahari, Snorre Aunet: High speed and ultra-low voltage CMOS latch. ICECS 2008: 153-156
[70] Yngvar Berg, Omid Mirmotahari, Snorre Aunet: Ultra low voltage and, nor and XOR CMOS gates. ICECS 2008: 846-849
[71] Yngvar Berg, Omid Mirmotahari, Johannes Goplen Lomsdalen, Snorre Aunet: High Speed Ultra Low Voltage CMOS inverter. ISVLSI 2008: 122-127
[72] Omid Mirmotahari, Yngvar Berg: Ultra Low Voltage High Speed Differential CMOS Inverter. PATMOS 2008: 328-337
[73] Yngvar Berg, Omid Mirmotahari, Per Andreas Norseng, Snorre Aunet: Ultra low voltage CMOS gates. ICECS 2006: 818-821
[74] Y. Berg, Tor S. Lande and Ø. Næss. "Programming Floating-Gate Circuits with UVActivated Conductances", IEEE Transactions on Circuits and Systems –II, vol 48, no. 1,pp 12-19, 2001

[75] Y. Berg “Novel high speed differential CMOS flip-flop for ultra low-voltage appications ”, In proc. of the 9th Edition of IEEE New Circuits and Systems Conference (NEWCAS), June, 2011, Bordeaux France.
[76] Y. Berg and O.Mirmotahari. “Novel High-Speed and Ultra-Low-Voltage CMOS NAND and NOR Domino Gates”, In proc. of the 5th international Conference on Advances in Circuits, Electronics and Micro-electronics, August 19-24, 2012, Rome, Italy.
[77] D. Harris, Introduction to CMOS VLSI Design—Lecture 9: Circuit Families (Lecture Notes on the Subject). Claremont, CA, USA: Harvey Mudd College, 2004.
[78] J. M. Rabaey, A. Chandrakasan and B. Nikolic, “Digital Integrated Circuits: A Design Perspective”, 2003.
[79] B. A. Wang and A. Chandrakasan, “A 180mV FFT processor using subthreshold circuit techniques”, IEEE ISSCC, pp.292-529, 2004.
[80] H. Soeleman and K. Roy, “Ultra-low power digital subthreshold logic circuits”, IEEE ISLPED, pp.94-96, Aug. 1999.
[81] Chandrakasan A.P. Sheng S. Brodersen R.W.: “Low-power CMOS digital design” IEEE Journal of Solid-State Circuits, Volume 27, Issue 4, April 1992 Page(s):473 – 484
[82] Verma N. Kwong J. Chandrakasan A.P.: “Nanometer MOSFET Variation in Minimum Energy Subthreshold Circuits”, IEEE Transactions on Electron Devices, Vol. 55, NO. 1, January 2008 Page(s):163 – 174
[83] S. Narendra, J. Tschanz, J. Hofsheier, B. Bloechel, S. Vangal, Y.Hoskote, S. Tang, D. Somasekhar, A. Keshavarzi, V. Erraguntla, G.Dermer, N. Borkar, S. Borkar, and V. De, “Ultra-low voltage circuits and processor in 180 nm to 90 nm technologies with a swapped-body biasing technique,” in IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers, Feb. 2004, pp. 156–157.
[84]] Y. Berg and O.Mirmotahari. “Novel Static Ultra Low-Voltage and High Speed CMOS Boolean Gates”, North atlantic university union: International Journal of Circuits, Systems and Signal Processing. ISSN 1998-4464. 6(4), s 249- 254.
[85] A. Dadashi, Y. Berg and O. Mirmotahari, "High-Speed, Modified, Bulk stimulated, Ultra-Low-Voltage, Domino Inverter," 2015 IEEE Computer Society Annual Symposium on VLSI, Montpellier, France, 2015, pp. 86-90, doi: 10.1109/ISVLSI.2015.100.
[86] A. Dadashi, O. Mirmotahari and Y. Berg, "An ultra-low-voltage, semi-floating-gate, domino, dual-rail, NOR gate," 2015 IEEE International Conference on Electronics, Circuits, and Systems (ICECS), Cairo, Egypt, 2015, pp. 61-64, doi: 10.1109/ICECS.2015.7440249.
[87] Dadashi, A., Mirmotahari, O. and Berg, Y. (2016) NP-Domino, Ultra-Low-Voltage, High-Speed, Dual-Rail, CMOS NOR Gates. *Circuits and Systems*, **7**, 1916-1926. doi: 10.4236/cs.2016.78166.
[88] A. Dadashi, O. Mirmotahari and Y. Berg, "Domino dual-rail, high-speed, NOR logic, with 300mV supply in 90 nm CMOS technology," 2016 IEEE International Symposium on Consumer Electronics (ISCE), Sao Paulo, Brazil, 2016, pp. 117-118, doi: 10.1109/ISCE.2016.7797398.
[89] O. Mirmotahari, A. Dadashi, M. Azadmehr and Y. Berg, "Novel high-speed dynamic differential ultra low voltage logic for supply-voltage below 300 mV," 2015 IEEE International Conference on Electronics, Circuits, and Systems (ICECS), Cairo, Egypt, 2015, pp. 53-56, doi: 10.1109/ICECS.2015.7440247.
[90] O. Mirmotahari, A. Dadashi, M. Azadmehr and Y. Berg, "High-speed dynamic dual-rail ultra low voltage static CMOS logic operating at 300 mV," 2016 International Conference on Design and Technology of Integrated Systems in Nanoscale Era (DTIS), Istanbul, Turkey, 2016, pp. 1-4, doi: 10.1109/DTIS.2016.7483898.
[91] Chandrakasan AP, Verma N, Daly DC. Ultralow-power electronics for biomedical applications. Annu Rev Biomed Eng. 2008;10:247-74. doi: 10.1146/annurev.bioeng.10.061807.160547. PMID: 18647116.
[92] P.R. Gray, P.J. Hurst, S.H. Lewis, and R.G. Meyer, Analysis and Design of Analog Integrated Circuits, Wiley, New York, 2001.
[93] B. Razavi, Design of Analog CMOS Integrated Circuits, McGraw- Hill, 2001.

[94] Razavi, "The Low Dropout Regulator [A Circuit for All Seasons]," in IEEE Solid-State Circuits Magazine, vol. 11, no. 2, pp. 8-13, Spring 2019, doi: 10.1109/MSSC.2019.2910952.
[95] F. Maloberti, *Analog Design for CMOS VLSI Systems*, Kluwer Academic Publishers, Dordrecht, 2001.
[96] Sh.CHATTERJEE, et al. "Ultra-Low Voltage Analog Integrated Circuits", IEICE TRANS. ELECTRON., VOL.E89–C, NO.6 JUNE 2006.
[97] P. P. Mercier, S. Bandyopadhyay, A. C. Lysaght, K. M. Stankovic and A. P. Chandrakasan, "A Sub-nW 2.4 GHz Transmitter for Low Data-Rate S94ensing Applications," in IEEE Journal of Solid-State Circuits, vol. 49, no. 7, pp. 1463-1474, July 2014, doi: 10.1109/JSSC.2014.2316237.
[98] K. E. Kuijk, "A precision reference voltage source," IEEE J. Solid-State Circuits, vol. SC-8, pp. 222–226, June 1973.
[99] H. Banba et al., "A CMOS bandgap reference circuit with sub-1-V operation," in IEEE Journal of Solid-State Circuits, vol. 34, no. 5, pp. 670-674, May 1999, doi: 10.1109/4.760378.
[100] M. Seok, G. Kim, D. Blaauw and D. Sylvester, "A Portable 2-Transistor Picowatt Temperature-Compensated Voltage Reference Operating at 0.5 V," in IEEE Journal of Solid-State Circuits, vol. 47, no. 10, pp. 2534-2545, Oct. 2012, doi: 10.1109/JSSC.2012.2206683.
[101] D. Albano, F. Crupi, F. Cucchi and G. Iannaccone, "A Sub-kT/q voltage reference operating at 150 mV" in *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 23, no. 08, pp. 1547-1551, 2015. doi: 10.1109/TVLSI.2014.2340576
[102] B. Baker and M. Oljaca "How the voltage reference affects ADC performance, Part 1, 2, and 3". https://www.ti.com/lit/an/slyt339/slyt339.pdf?ts=1610057262621&ref_url=https%253A%252F%252Fwww.google.com%252F, https://www.ti.com/lit/an/slyt331/slyt331.pdf?ts=1610094939671&ref_url=https%253A%252F%252Fwww.google.com%252F, https://www.ti.com/lit/an/slyt355/slyt355.pdf?ts=1610121587147&ref_url=https%253A%252F%252Fwww.google.com%252F.
[103] W. Chen, Y. Su, Y. Lee, C. Wey and K. Chen, " 0.65V-input-voltage 0.6V-output-voltage 30ppm/°C low-dropout regulator with embedded voltage reference for low-power biomedical systems," 2014 IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC), San Francisco, CA, 2014, pp. 304-305, doi: 10.1109/ISSCC.2014.6757445.
[104] M. Liu, K. Pelzers, R. van Dommele, A. van Roermund and P. Harpe, "A106nW 10 b 80 kS/s SAR ADC With Duty-Cycled Reference Generation in 65 nm CMOS," in IEEE Journal of Solid-State Circuits, vol. 51, no. 10, pp. 2435-2445, Oct. 2016, doi: 10.1109/JSSC.2016.2587688.
[105] A. Paidimarri and A. P. Chandrakasan, "A Wide Dynamic Range Buck Converter With Sub-nW Quiescent Power," in IEEE Journal of Solid-State Circuits, vol. 52, no. 12, pp. 3119-3131, Dec. 2017, doi: 10.1109/JSSC.2017.2747217.
[106] S. Bandyopadhyay, P. P. Mercier, A. C. Lysaght, K. M. Stankovic and A. P. Chandrakasan, "A 1.1 nW Energy-Harvesting System with 544 pW Quiescent Power for Next-Generation Implants," in IEEE Journal of Solid-State Circuits, vol. 49, no. 12, pp. 2812-2824, Dec. 2014, doi: 10.1109/JSSC.2014.2350260.
[107] K. Kadirvel et al., "A 330nA energy-harvesting charger with battery management for solar and thermoelectric energy harvesting," 2012 IEEE International Solid-State Circuits Conference, San Francisco, CA, 2012, pp. 106-108, doi: 10.1109/ISSCC.2012.6176896. (duty cycled reference)
[108] C. Lu, P. Yin, C. Hsiao, M. F. Chang and Y. Lin, "A 10-bit Resistor-Floating-Resistor-String DAC (RFR-DAC) for High Color-Depth LCD Driver ICs," in IEEE Journal of Solid-State Circuits, vol. 47, no. 10, pp. 2454-2466, Oct. 2012, doi: 10.1109/JSSC.2012.2206684.
[109] J. Nakamura "Image Sensors and Signal Processing for Digital Still Cameras" 2006 by Taylor & Francis Group, LLC.
[110] K, Ashish et al., "A 0.065-mm2 19.8-mW Single-Channel Calibration-Free 12-b 600-MS/s ADC in 28-nm UTBB FD-SOI Using FBB." IEEE J. Solid-State Circuits 52 (2017): 1927-1939.

[111] H. H. Boo et al., “A 12 b 250 MS/s pipelined ADC with virtual ground reference buffers,” IEEE J. Solid-State Circuits, vol. 50, no. 12, pp. 2912–2921, Dec. 2015.
[112] K. Bult and G. J. G. M. Geelen, “A fast-settling CMOS Op Amp for SC circuits with 90-dB DC gain,” *IEEE J. Solid-State Circuits*, vol. 25, no. 6, pp. 1379–1383, Dec. 1990.
[113] E. Sackinger et al., “A High-Swing, High-Impedance MOS Cascode Circuit,” IEEE J. Solid-State Circuits, vol. 25, no. 1, pp. 289–298, Feb 1990.
[114] B. J. Hosticka, "Improvement of the gain of MOS amplifiers," in IEEE Journal of Solid-State Circuits, vol. 14, no. 6, pp. 1111-1114, Dec. 1979, doi: 10.1109/JSSC.1979.1051324.
[115] Assaad, R. et al., “The recycling folded cascode: A general enhancement of the folded cascade amplifier” IEEE J. Solid-State Circuits, 44(9), 2535–2542. 2009.
[116] B. Nauta, "A CMOS transconductance-C filter technique for very high frequencies," in IEEE Journal of Solid-State Circuits, vol. 27, no. 2, pp. 142-153, Feb. 1992, doi: 10.1109/4.127337.
[117] C. A., & Gray, P. R. (1988). A positive-feedback transconductance amplifier with applications to high-frequency, highQ CMOS switched-capacitor filters. IEEE Journal of Solid-State Circuits, 23(6), 1370–1378
[118] A. Dadashi, Sh. Sadrafshari, Kh. Hadidi and A. Khoei "Fast- settling CMOS Op-Amp with improved DC-gain", Analog Integrated Circuits and Signal Processing,Vol. 70, No. 3, pp. 283-292, February 2012.
[119] A. Dadashi, Sh. Sadrafshari, Kh. Hadidi and A. Khoei "An enhanced folded cascode OpAmp using positive feedback and bulk amplification in 0.35 um CMOS process", Analog Integrated Circuits and Signal Processing, November, 2010.
[120] J.Ramirez-Angulo, B.Calvo, R.Carvajal, A.Lopez-Martin "Low-Voltage gm-Enhanced CMOS Differential Pairs Using Positive Feedback ", IEEE ISCAS 2010, Paris, France May 29-June 2, pp. 773-776.
[121] A. Dadashi “Modified Telescopic Amplifier with Improved Dc-Gain in 0.18 μm CMOS Process”. Int. J. Circ. Theor. Appl.. doi: 10.1002/cta.819
[122] Y. Chae and G. Han, "Low Voltage, Low Power, Inverter-Based Switched-Capacitor Delta-Sigma Modulator," in IEEE Journal of Solid-State Circuits, vol. 44, no. 2, pp. 458-472, Feb. 2009, doi: 10.1109/JSSC.2008.2010973.
[123] H. Luo, Y. Han, R. C. C. Cheung, X. Liu and T. Cao, " A 0.8-V 230-μ W 98-dB DR Inverter-Based ΣΔ Modulator for Audio Applications," in IEEE Journal of Solid-State Circuits, vol. 48, no. 10, pp. 2430-2441, Oct. 2013, doi: 10.1109/JSSC.2013.2275659.
[124] Y. Lim and M. P. Flynn, "A 100 MS/s, 10.5 Bit, 2.46 mW Comparator-Less Pipeline ADC Using Self-Biased Ring Amplifiers," in IEEE Journal of Solid-State Circuits, vol. 50, no. 10, pp. 2331-2341, Oct. 2015, doi: 10.1109/JSSC.2015.2453332. “
[125] B. Hershberg, S. Weaver, K. Sobue, S. Takeuchi, K. Hamashita and U. Moon, "Ring Amplifiers for Switched Capacitor Circuits," in IEEE Journal of Solid-State Circuits, vol. 47, no. 12, pp. 2928-2942, Dec. 2012, doi: 10.1109/JSSC.2012.2217865.
[126] E. K. F. Lee, "A sub-0.5V, 1.5μW rail-to-rail constant gm opamp and its filter application," 2012 IEEE International Symposium on Circuits and Systems (ISCAS), Seoul, 2012, pp. 197-200, doi: 10.1109/ISCAS.2012.6271662.
[127] Z. Qin, A. Tanaka, N. Takaya and H. Yoshizawa, "0.5-V 70-nW Rail-to-Rail Operational Amplifier Using a Cross-Coupled Output Stage," in IEEE Transactions on Circuits and Systems II: Express
Briefs, vol. 63, no. 11, pp. 1009-1013, Nov. 2016, doi: 10.1109/TCSII.2016.2539081.
[128] S. Chatterjee, Y. Tsividis, and P. Kinget, “0.5-V analog circuit techniques and their application in OTA and filter design,” Solid-State Circuits, IEEE Journal of, vol. 40, no. 12, pp. 2373–2387, Dec 2005. Body diff
[129] K.-P. Pun, S. Chatterjee, and P. Kinget, “A 0.5-V 74-dB SNDR 25-kHz Continuous-Time Delta-Sigma Modulator With a Return-to-Open DAC,” Solid-State Circuits, IEEE Journal of, vol. 42, no. 3, pp. 496–507, March 2007. Bodu bulk

[130] Musah, T. et al., “Parallel correlated double sampling technique for pipelined analogue-to-digital converters”, Electron. Lett., 2007, 43, (23), pp. 1260–1261. (CDS)
[131] Gregoire, B. R. et al., “An over-60 dB true rail-to-rail performance using correlated level shifting and an opamp with only 30 dB loop gain”, IEEE J. Solid-State Circuits, 43(12), 2620–2630. 2008.
[132] B. Hershberg, S. Weaver, and U. K. Moon “Design of a Split-CLS Pipelined ADC With Full Signal Swing Using an Accurate But Fractional Signal Swing Opamp”, IEEE J. SolidState Circuits, Vol. 45, No. 12, pp. 2623-2633, DECEMBER 2010.
[133] W. Chou, S. Yeh, C. Chiu and C. Hsieh, "A Linear-Logarithmic CMOS Image Sensor With Pixel-FPN Reduction and Tunable Response Curve," in IEEE Sensors Journal, vol. 14, no. 5, pp. 1625-1632, May 2014, doi: 10.1109/JSEN.2013.2294740.
[134] D. Lee, K. Cho, D. Kim and G. Han, "Low-Noise In-Pixel Comparing Active Pixel Sensor Using Column-Level Single-Slope ADC," in IEEE Transactions on Electron Devices, vol. 55, no. 12, pp. 3383-3388, Dec. 2008, doi: 10.1109/TED.2008.2006735.
[135] C. Lu, P. Yin, C. Hsiao, M. F. Chang and Y. Lin, "A 10-bit Resistor-Floating-Resistor-String DAC (RFR-DAC) for High Color-Depth LCD Driver ICs," in IEEE Journal of Solid-State Circuits, vol. 47, no. 10, pp. 2454-2466, Oct. 2012, doi: 10.1109/JSSC.2012.2206684.
[136] H. -. Le, X. -. Do and S. -. Lee, "Compact low-power high-slew-rate buffer for LCD driver applications," in Electronics Letters, vol. 46, no. 20, pp. 1370-1371, 30 September 2010, doi: 10.1049/el.2010.2236.
[137] J. Woo, D. Shin, D. Jeong and S. Kim, "High-Speed 10-bit LCD Column Driver with a Split DAC and a Class-AB Output Buffer," in IEEE Transactions on Consumer Electronics, vol. 55, no. 3, pp. 1431-1438, August 2009, doi: 10.1109/TCE.2009.5278010.
[138] Xia, Ming; Huang, Zunkai; Tian, Li; Wang, Ning; Zhu, Yongxin; Wang, Hui; Feng, Songlin. 2020. "An Area-Efficient 10-Bit Buffer-Reused DAC for AMOLED Column Driver ICs" *Electronics* 9, no. 2: 208. https://doi.org/10.3390/electronics9020208.
[139] Yan, Z., Mak, P.-I., Law, M.-K. Martins, R., Maloberti, F. (2014). A 0.0013mm2 3.6 µW nested-current-mirror single-stage amplifier driving 0.15-to-15nF CLs with >62° phase margin. In Solid-state circuits conference, digest of technical papers (ISSCC), pp. 288–289.
[140] Yan, Z., Mak, P.-I., Law, M.-K., Martins, R. P., & Maloberti, F. (2015). Nested-current-mirror rail-to-rail-output single-stage amplifier with enhancements of DC gain, GBW and slew rate. IEEE Journal of Solid-State Circuits, 50(10), 2353–2366.
[141] Ali Dadashi, Yngvar Berg, and Omid Mirmotahari. 2018. Energy-efficient, fast-settling, modified nested-current-mirror, single-stage-amplifier for high-resolution LCDs in 90-nm CMOS. Analog Integr. Circuits Signal Process. 97, 2 (November 2018), 253–259
[142] C.-W. Lu and L.-C. Huang, “A 10-bit LCD column driver with piecewise linear digital-to-analog converters,” IEEE J. Solid-State Circuits, vol. 43, no. 2, pp. 371–378, Feb. 2008. (cite in introduction)
[143] C.-W. Lu and K. J. Hsu, “A high-speed low-power rail-to-rail column driver for AMLCD application,” IEEE J. Solid-State Circuits, vol. 39, no. 8, pp. 1313–1320, Aug. 2004. (cite in text)
[144] J.-S. Kim, D.-K. Jeong, and G. Kim, “A multi-level multi-phase charge recycling method for low-power AMLCD column drivers,” IEEE J. Solid-State Circuits, vol. 35, no. 1, pp. 74–84, Jan. 2000.
[145] Peng, X., et al. (2011). Impedance adapting compensation for low power multistage amplifiers. IEEE Journal of Solid-State Circuits, 46, 445–451.
[146] Yan, Z. et al. (2012). A 0.016mm2 144 l W three-stage amplifier capable of driving 1-to-15nF capacitive load with 0.95 MHz GBW. In ISSCC Dig. Tech. Papers, pp. 368–369.
[147] Grasso, A. D., Marano, D., Esparza-Alfaro, F., Lopez-Martin, A. J., Palumbo, G., & Pennisi, S. (2014). Self-biased dual-path push pull output buffer amplifier for LCD column drivers. IEEE Transactions on Circuits and Systems I, 61(3), 663–670.
[148] Mak, K. H., & Leung, K. N. (2014). A signal- and transient-current boosting amplifier for large capacitive load applications. IEEE Transactions on Circuits and Systems I, 61(10), 2777–2785.
[149] Chong, S., et al. (2012). Cross feedforward cascode compensation for low-power three-stage amplifier with large capacitive load. IEEE Journal of Solid-State Circuits, 47, 2227–2234.

[150] Qu, W., Im, J.-P., Kim, H.-S., Cho, G.-H. (2014). A 0.9 V 6.3 μW multistage amplifier driving 500 pF capacitive load with 1.34 MHz GBW. In IEEE ISSCC Dig. Tech. Papers, pp. 290–291.
[151] H. Nakazawa, K. Sano, T. Abe, M. Baba, and N. Kumagai, "Charge–discharge characteristics of all-solid-state thin-filmed lithium-ion batteries using amorphous Nb2O5 negative electrodes," J. Power Sources, vol. 174, no. 2, pp. 838–842, Dec. 2007
[152] Patrick P Mercier, et. al "Energy extraction from the biologic battery in the inner ear" nature biotechnology 30, 1240-1243,2012.
[153] S.-W. Chen and R. W. Brodersen, "A 6-bit 600-MS/s 5.3-mW asynchronous ADC in 0.13μm CMOS," IEEE J. Solid-State Circuits, vol.41, no. 12, pp. 2669–2680, Dec. 2006.
[154] M. van Elzakker, E. van Tuijl, P. Geraedts, D. Schinkel, E. Klumperink, and B. Nauta, "A 1.9 μW 4.4 fJ/conversion-step 10b 1 MS/s charge redistribution ADC," in IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers, Feb. 2008, pp. 244–245.
[155] P. Harpe et al., "A 26 μW 8 bit 10 MS/s asynchronous SAR ADC for low energy radios," IEEE J. Solid-State Circuits, vol. 46, no. 7, pp. 1585–1595, Jul. 2011.
[156] P. Harpe, E. Cantatore, and A. van Roermund, "A 10b/12b 40 kS/s SAR ADC with data-driven noise reduction achieving up to 10.1b ENOB at 2.2 fJ/conversion-step," IEEE J. Solid-State Circuits, vol. 48, no. 12, pp. 3011–3018, Dec. 2013.
[157] P. Harpe, H. Gao, R. v. Dommele, E. Cantatore and A. H. M. van Roermund, " A 0.20 mm2 3 nW Signal Acquisition IC for Miniature Sensor Nodes in 65 nm CMOS " in IEEE Journal of Solid-State Circuits, vol. 51, no. 1, pp. 240-248, Jan. 2016, doi: 10.1109/JSSC.2015.2487270.
[158] M. Yip, and A. Chandrakasan, "A Resolution-Reconfigurable 5-to-10-Bit 0.4-to-1 V Power Scalable SAR ADC for Sensor Applications," IEEE J. Solid-State Circuits, vol. 48, no. 6, pp. 1453–1464, June. 2013.
[159] L.Chen, X. Tang, A. Sanyal, Y. Yoon, J. Cong and N. Sun, "A 0.7-V 0.6- μW 100-kS/s Low-Power SAR ADC With Statistical Estimation Based Noise Reduction," in IEEE Journal of Solid-State Circuits, vol. 52, no. 5, pp. 1388-1398, May 2017.
[160] *Ali Dadashi, Yngvar Berg, and. Omid Mirmotahari.* "A High-Performance CMOS Modified Amplifier" *IEEE Proceedings, ISCE 2016, Sao Paolo, Brasil.*
[161] *Ali Dadashi, Yngvar Berg, and. Omid Mirmotahari* "Fast-Settling, Energy-Efficient, Amplifier for High-Resolution LCD Displays". *IEEE Proceedings, AM-FPD 2017, Kyoto, Japan.*