Integrated hybrid coupler for monopulse radar and biomedical sensors applications

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Abstract

The 180-degree hybrid coupler was designed to miniaturize in the frequency range from 5 to 10 GHz with a 0-degree phase shift in the summation port and a 180-degree phase shift in the differential port. Miniaturization can minimize the power dissipation, and a passive component can solve the microstrip lines substrate materials' complex accessibility problem! The metal layer of the inductor will be chosen and designed in Cadence with the corresponding permeability and permittivity of the metal. The design process started from rat-race hybrid coupler microstrip line in Advanced Design Systems (ADS) to lumped passive component and further active 65nm CMOS implementation in Cadence. Simulation result shown via material from center-tapped inductor has created a parasitic inductance which shifts the frequency of interest bandwidth 1GHz to the left after EMX simulation. The passive circuit has a forward gain of -10dB and a return loss of around -6dB. Literature studies have been carried out to miniaturize the hybrid coupler and its performance parameter analysis. The final result has shown that only four passive components were used, which covered the frequency band of interest, 5GHz.

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Chapter 1

Introduction

180-degree hybrid couplers or rate race hybrid couplers have existed for decades. They have been widely used in signal splitting and combining low-power amplifiers, high-frequency circuits, and antenna beam-forming networks, their working frequency covers a broad band from 1GHz to more than 20 GHz depending on the implementation purposes. They also inhibit a multiple input- multiple output structure. Hybrid couplers are passive components that either split or combine two input signals. The electromagnetic waves propagate toward four ports as the input signals pass through the hybrid coupler. Three central excitation ports and one isolation port, or lag the one input signal to a different proportion of phase shift to the output port by signal delay or phase shift of inductor and capacitor. The ratio between the split signals may not be symmetrical. A particular case is a 4-port rat race hybrid coupler called the 3dB hybrid coupler, where the signals are split equally between the ports. Depending on the planar geometry, the electrical phase difference between the power outputs maybe 0 or 180 degrees. The hybrid coupler can be used in a mono-pulse radar or biomedical sensing system for signal processing. Depending on the input configuration, it can also be used as an interface, both as even-mode and odd-mode. The inputs can have identical incident waves of equal amplitude and phase (even mode excitation) or equal amplitude but phase-shifted by 180 degrees (odd mode excitation). The two different modes are called differential or common-mode configurations. Using passive component technology, emulating a hybrid coupler has power consumption and portability advantages compared with the transmission line. This thesis aims to implement a hybrid coupler using passive components to improve the physical design. Our physical design of a hybrid coupler will be tested and simulated by applying two equal amplitude 5 to 10 GHz signals to the two input ports and analyzing the scatter parameter of the reflected signal.The miniaturization of a hybrid coupler can reduce the size of the circuit containing it, thus possibly reducing the manufacturing cost and increasing portability. The challenge of this geometry design is to miniaturize the circuit without reducing the bandwidth. Traditional hybrid couplers are challenging to build because of their large dimensions and often narrow bandwidths. As a result,

using more sections in the hybrid coupler is a common way to increase bandwidth while reducing size. Nonetheless, there are numerous methods for minimizing hybrid couplers. Transmission lines can be configured in a T-shaped topology to reduce their size. Multilayered designs, meander lines, and multisection branch line couplers are also possibilities. Other examples include shunt lumped capacitors and lines with short, high impedance transmission; two-step stubs with high and low impedance; stub lines with stepped impedance; synthetic transmission lines; capacitors distributed inside the branch-line hybrid coupler; and microstrip lines with discontinuities in the branch-line hybrid coupler. Our problem statement is "How to miniaturize the hybrid coupler and achieve required bandwidth." Miniaturizing the hybrid coupler from microstrip line to lumped elements and further implementing TSMC 65 nm technology. The big size will occupy a large area in the circuit board, which creates unnecessary power consumption, so miniaturizing the hybrid coupler without affecting the working bandwidth is essential. Previous literature study [1] demonstrates reducing the hybrid coupler size by using Π shaped or H shaped structure. A cascade topology suppresses output amplitude mismatch and sustains differential output phases, thus facilitating the addition of coupler bandwidth. Also, a cascade topology center tapped inductor can shrink the hybrid coupler geometric structure, but material with parasitic capacitance will limit the bandwidth. [2]

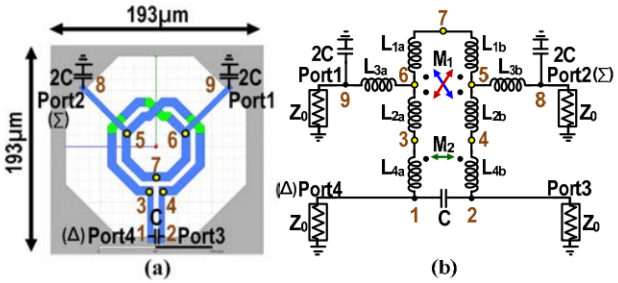


Figure 1.1: Size shrinking by using folded inductor

Folded inductor has a cascaded equivalent circuit structure shown in Figure 1.1 (b). Article [3] has presented a method for miniaturizing the hybrid coupler by using mathematical formula. Based on the previous studies master thesis will first make a conventional microstrip line-based hybrid coupler, further developed to a lumped passive component composed circuit board and compared with TSMC 65nm CMOS technology implementation in Cadence.

Chapter 2

Method

Several hybrid coupler topologies have various advantages and constraints; thus, inevitable trade-offs must be considered. A rat-race hybrid coupler has four ports, two inputs, and two outputs signal ports. In order to form an even mode signal without phase shift in the output and an odd mode with a 180-degree shift in the output, three alternative implementation methods can be applied: either implement active components like transistors or passive components like inductor and capacitor. The passive component has shown the advantage of reciprocal bidirectional and low power dissipation. Traditional transmission line, like microstrip line or strip-line, was first designed in ADS (Advanced Design System) based on the Maxwell equation and principle: changing in electrical field will create a magnetic field. Because of the non-reciprocal disadvantage of active components, the passive component design will be chosen for our circuit. EMX (High-Frequency Electrical Magnetic Simulator) simulation will be carried out after parasitic extraction. An equivalent lumped circuit for the topology must be established, and then adjustments are made to achieve the desired characteristics of the hybrid coupler. The circuit uses fewer components with compact geometry topology to miniaturize.

2.1 Design and simulation of proposed implementation using appropriate simulators (CST, ADS, Cadence)

The length and width parameter of the microstrip line is first calculated, and its momentum generated by the circuit will be simulated in ADS. Then passive component parameters such as inductance and capacitance will be calculated and simulated in ADS. The implemented design requires a suitable pad frame consisting of pads for probing or wire bonding that needs to be implemented with interconnects to the hybrid coupler. Both the pads and interconnects can significantly influence the characteristic impedance, affecting the Voltage Standing Wave Ratio (VSWR). The implemented design of the passive component in Cadence will be sent for fabrication. Therefore a post layout extraction and simulation are necessary

to conduct and measure the influence of the pads, interconnects, and other parameters.

Chapter 3

Theoretical background

3.1 Litterateur studies

The critical issue for designing a hybrid coupler is impedance matching to minimize insertion loss and return loss and enhance the reflection coefficient with a desired high bandwidth with fewer components. The literature study was typed with the research keywords "rate race hybrid coupler" and "180 directional hybrid couplers" in IEEE. According to this article, [4], performance analysis is done by analyzing VSWR at their desired frequency band: 2.4GHz. VSWR should be as low as possible to avoid insertion loss. In the article, [5] states that the isolation between the difference and summation ports was better in the two-layer microstrip structure with via holes. However, in a high-frequency design, the via holes are not recommended. It reminds us of our center-tapped inductor. The via holes in the inductor has an impediment effect in high frequency, which leads to lower bandwidth. To enhance bandwidth, discontinuity of transmission line between Ports 1 and 4 and an H-shaped coupled line between Ports 2 and 3 were utilized and recommended by the author. This hybrid coupler provided significant isolation between the difference and summation ports. Utilizing S42 and S24 are supposed to be -40 dB. According to the article, [6], the author states that the power incident upon Port 1 is partially coupled to Port 3. In a 10 dB coupler, the power at Port 3, referenced to the input will be -10 dB (1/10 the power). So S32 and S34 should be -10dB which is the same as our experiment. The remaining 9/10 of the power (.46 dB loss) will pass through the coupler to the output port (Port 2). Thus the return loss to Port 2, S22, should be around -3dB. Since it is a direction hybrid coupler, the parameter result is not relevant to our rat race hybrid coupler. The search keyword has been changed to "H shaped rat coupler." In the article, [7] T shaped structure will decrease the chip size and increase the operating frequency, but the return loss will increase. Authors [8] have shown that π shaped hybrid couplers have better isolation than T shaped hybrid couplers. Another way [9]for miniaturization is introducing additional resonance with open stubs on the inside of the rat-race coupler's ring, made of multiple lines, which can be used as inductance. Thus, the footprint can be reduced thanks to the added

resonances. The advantage is easy, low-cost fabrication, as their design does not have to use vias or lumped elements.

3.2 Principle of rat race coupler

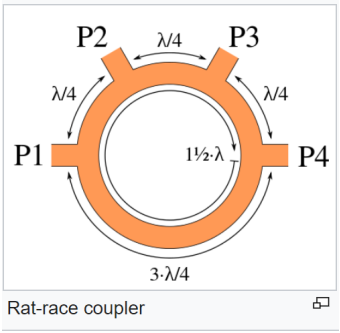


Figure 3.1: Rat Race hybrid coupler

In a four-port network, a 3dB rat-race hybrid coupler, or 180-degree hybrid coupler, has the following properties: when two 5GHz signals are injected into two input ports P1 and P3, and if these signals are in-phase, then the output should be summarized in port P2. If the two input signal is out of phase 180-degree, the output should be the difference in port P4. The two output ports have a 180-degree phase shift between each other. Therefore, it is also be called a 180-degree hybrid coupler. In addition, because of the symmetric design, the input port, and output port should also be reciprocal (input-output is bi-directional)[10]. The annular arrangement of ring lines has characteristic impedance of

$$Z = \sqrt{2}Z_0[11, P.231] \tag{3.1}$$

Suppose all ports have the same impedance Z_0. The phase shift of the output port is different from the geometry of the layout; the electrical 270-degree phase shift from P1 to P4 has a 180-degree geometry phase shift because the wave signal traveled through a transmission line, and the permittivity of the substrate made the signal arrive later (delay transmission).

Chapter 4

Microstrip implementation

4.1 Hand calculation on microstrip line

The propagation velocity depends on the microstrip line's impedance. The permeability and permittivity vary depending on the material. Overall, working in the GHz band sets requirements for both the components used and the laminate. Rogers ro4350b materials are tested to guide high-frequency wave signals. Rogers ro4350b 1.54 mm thickness microstrip line is implemented [12], as transmission line in rat race hybrid coupled with a characteristic impedance of

$$Z_0 = 50\Omega$$

We found the dielectric constant

$$\epsilon_r = 3.66$$

from the datasheet of R04350b[12, p. 0] In order to minimize power dissipation, the operating frequency impedance should be very close to the impedance in free space.

$$Z_f = 377\Omega.$$

Property	Typical Value		Direction	Units	Condition	Test Method
	RO4003C	RO4350B				
Dielectric Constant, ε_r Process	3.38 ± 0.05	[1] 3.48 ± 0.05	Z	--	10 GHz/23°C	IPC-TM-650 2.5.5.5 Clamped Stripline
[2] Dielectric Constant, ε_r Design	3.55	3.66	Z	--	8 to 40 GHz	Differential Phase Length Method

Figure 4.1: RO4350b data sheet dielectric constant.

From the book[13, p. 69] Figure 2-20 lookup table, the w/h ratio is found when the characteristic impedance is 50 Ω, and the dielectric constant is 3.66. The w/h ratio is between 2 and 3, which is above 1. For the convenience of calculation, 2.4 is chosen in our case. To calculate the w/h ratio, the B factor need to be calculated.

$$B = \frac{Z_f * \pi}{2 * Z_0 \sqrt{\epsilon_r}} = \frac{377 * 3.14}{2 * 50 * \sqrt{3.66}} = 6.188$$

The w/h ratio is then been calculated, because this ratio from the lookup table is bigger than 2, using this formula below:

$$\frac{w}{h} = \frac{2}{\pi}\{B - 1 - ln(2B-1) + \frac{\epsilon_r - 1}{2\epsilon_r}\left[ln(B-1) + 0.39 - \frac{0.61}{\epsilon_r}\right]\}$$

$$= \frac{2}{3.14}\{6.188 - 1 - ln(2*6.188-1) + \frac{3.66-1}{23.66}\left[ln(6.188-1) + 0.39 - \frac{0.61}{3.66}\right]\}$$

$$= 2.196$$

Substitute this ratio to the equation: Dielectric constant will be used to calculate the effective dielectric constant by using the formula below:

$$\epsilon_{eff} = \frac{\epsilon_r + 1}{2} + \frac{\epsilon_r - 1}{2} * (\frac{1}{\sqrt{(1 + 12 * \frac{h}{w})}})$$

$$= \frac{3.66+1}{2} + \frac{3.66-1}{2} * (\frac{1}{\sqrt{(1 + 12 * \frac{1}{2.196})}}) = 2.85$$

After finding effective dielectric constant ϵ_{eff} a specific expression will be used to calculate characteristic line impedance which is designed for a wide line W/H>1, which is:

$$Z_0 = \frac{Z_f}{\sqrt{\epsilon_{eff}} * (1.393 + \frac{w}{h} + \frac{2}{3}ln(\frac{w}{h} + 1.444))}$$

$$= \frac{377\Omega}{\sqrt{2.85} * (1.393 + 2.196 + \frac{2}{3}ln(2.196 + 1.444))}$$

$$= 50.13\Omega[13, P.68]$$

which is close to the target impedance of 50Ω, and therefore our design is correct. Because the thickness of the microstrip line is 1.54mm, and substitute this figure to get the width thickness. the trace width is

$$\frac{w}{h} * 1.54mm => w = 2.196 * 0.0154 = 3.4mm.$$

Phase velocity of the microstrip is

$$v_p = \frac{x}{\sqrt{\epsilon_{eff}}}[13, P.70] = \frac{3 * 10^8}{\sqrt{2.85}} = 177,514,792.899$$

Further the wavelength will be calculated

$$\lambda = \frac{v_p}{f} = \frac{c}{f * \sqrt{\epsilon_{eff}}} = \frac{3 * 10^8}{5 * 10^9\sqrt{2.85}} = 3.554mm$$

4.2 Schematic, layout of rat race coupler in ADS/CST

Simulated circuit is designed in ADS: Designing parameter setup in LineCalcu:

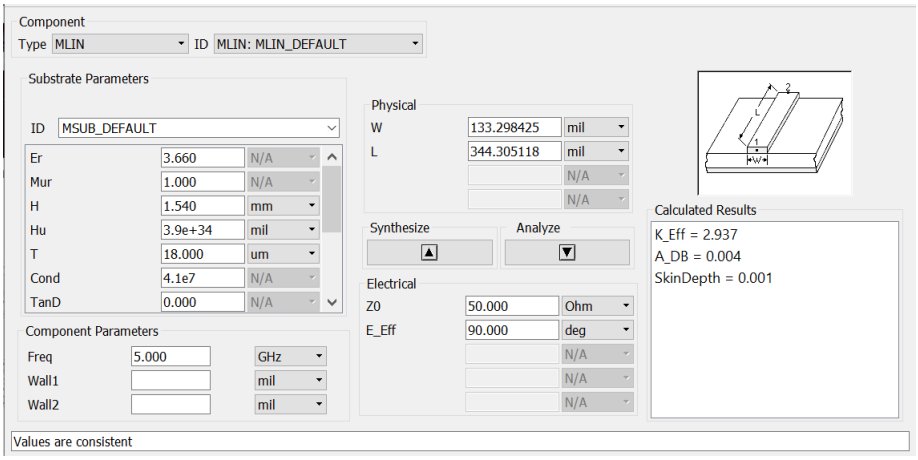


Figure 4.2: Microstrip and strip line parameter setup

where H =1.524mm (thickness of the substrate, which we set to 1.524mm), Er = 3.66 (electrical permittivity of the substrate, which we can find from the ro4350b datasheet). T = 18um (metal thickness). R= 1um (roughness of the copper). Mur = 1 (magnetic permeability of substrate, which is equal to 1 for all nonmagnetic materials as Ro4350b). First calculate port line: 90-degree, 50 ohm impedance then we get width: 3.35815mm, length: 8.76169mm. Then calculate the $1/4\lambda$ at 90 degree with impedance $50\sqrt{2} = 70.7ohm$ then we get width: 1.8098mm, length: 9.00493mm. Radius= 9mm/ (3.14/6) = 17.2mm. Finally calculate the $3/4\lambda$ at 270 degree, $50\sqrt{2} = 70.7ohm$ then we get width: 1.8098mm, length: 27.0148mm. Radius= 27mm/ (3.14/2)= 17.2mm. It is the same radius as $1/4\lambda$ The schematic and layout look like below:

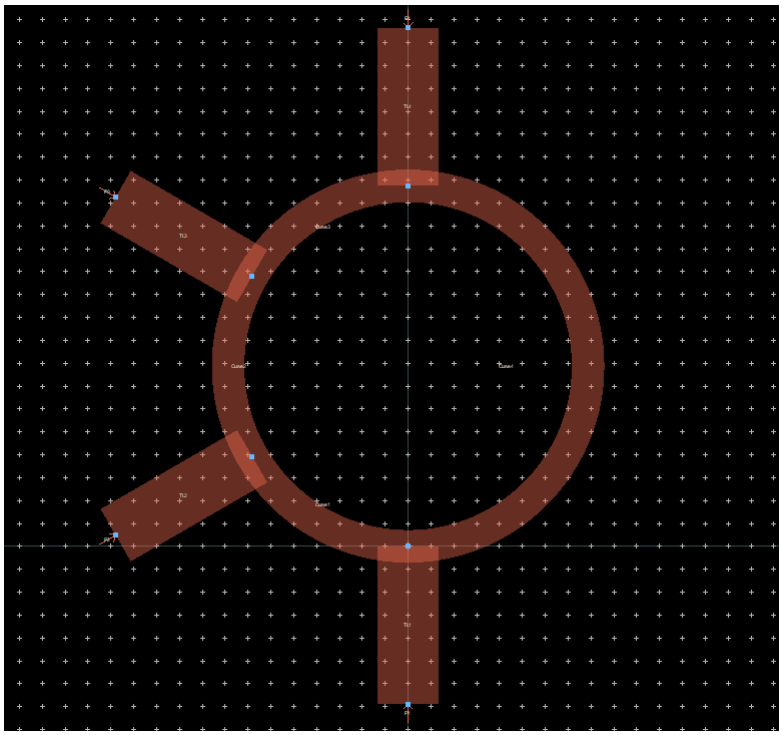


Figure 4.3: Microstrip Layout

4.3 Simulation of rat race coupler in ADS/CST

In this section we will make microstrip line phase shift, amplitude and with substrate as a whole (EM) simulation.

4.3.1 Sweep radius as ww parameter

In simulation a two group equation is setup, see figure 4.5:

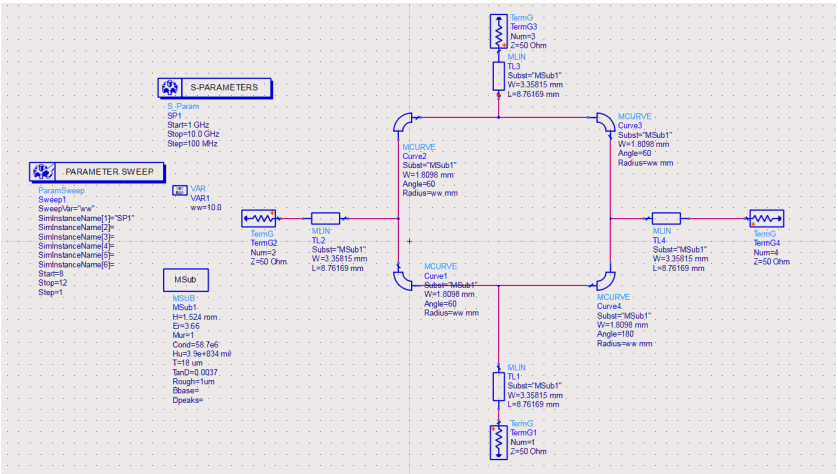


Figure 4.4: Rat race couple schematic sweep

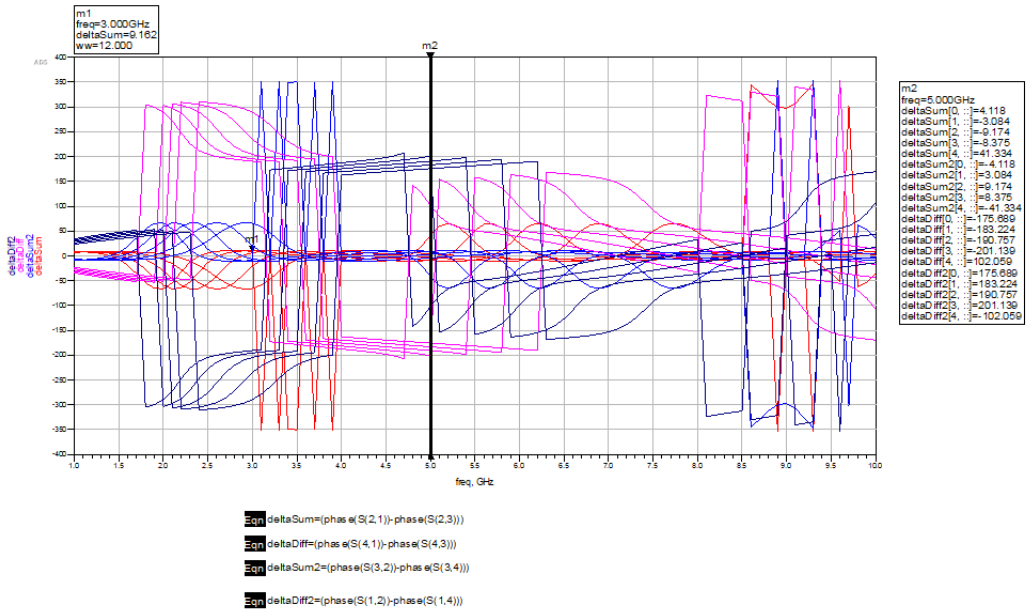


Figure 4.5: Simulation sweep width result

The tolerant interval for deltaSum/deltaSum2 is approximately zero degrees, and for deltaDiff/deltaDiff2, it is 180 degrees. In order to find the correct result, a standard parameter for the width of the ring coupler "ww" is set up. Then use a function called parameter sweep. Connect to s parameter simulation sp1: when sweeping the radius from 8m to 12mm, the simulation result is obtained in 1 linear step, as shown in Figure 4.5. The lookup table shows that the second sweep step approximately has a 9mm radius. From 5GHz to 10GHz, the phase shift is doubled, which means it will apply the exact proportional change at every harmonic frequency.

4.3.2 Amplitude analysis as S parameter

Amplitude relation for input and output port equation set up for the second part of the simulation. From the figure 4.6, we can see that:

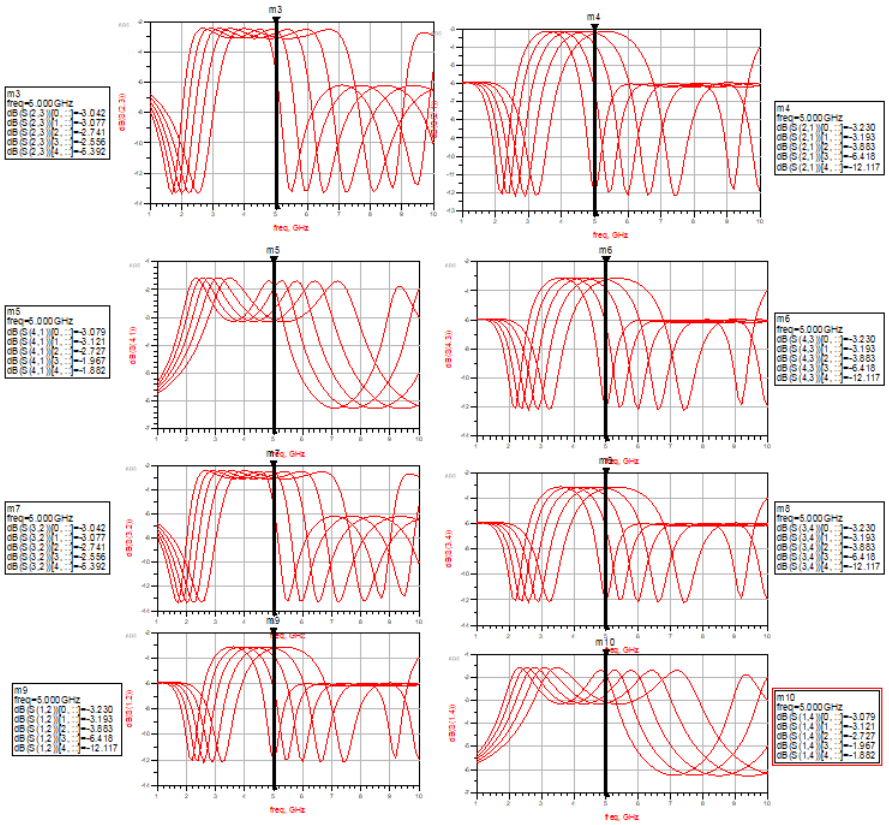


Figure 4.6: Amplitude Sweep result

If at 5GHz, S(2,3) or S(2,1), S(4,1), S(4,3) is not -3dB, but more than -3dB like -4dB, then there will be a power dissipation in transmission line. So put back the parameter radius =8.6mm to schematic again:

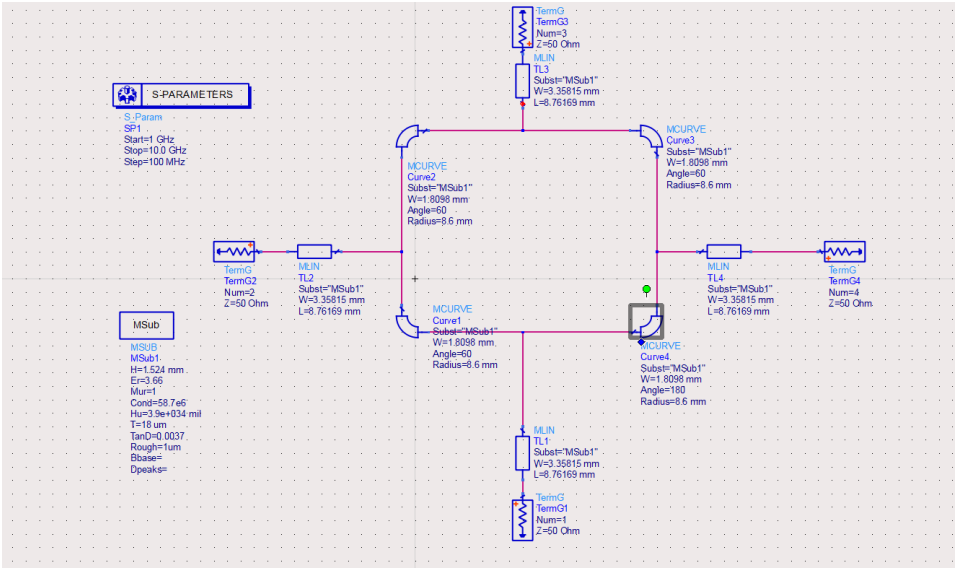
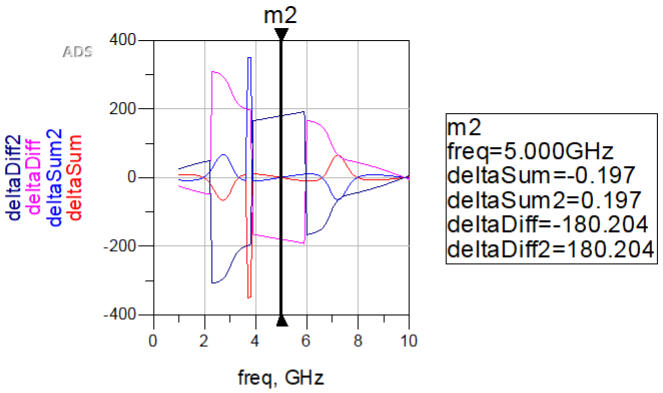


Figure 4.7: Radius=8.6mm schematic setup

The simulation results redone:



Eqn deltaSum=(phase(S(2,1))-phase(S(2,3)))

Eqn deltaDiff=(phase(S(4,1))-phase(S(4,3)))

Eqn deltaSum2=(phase(S(3,2))-phase(S(3,4)))

Eqn deltaDiff2=(phase(S(1,2))-phase(S(1,4)))

Figure 4.8: Simulation final phase result

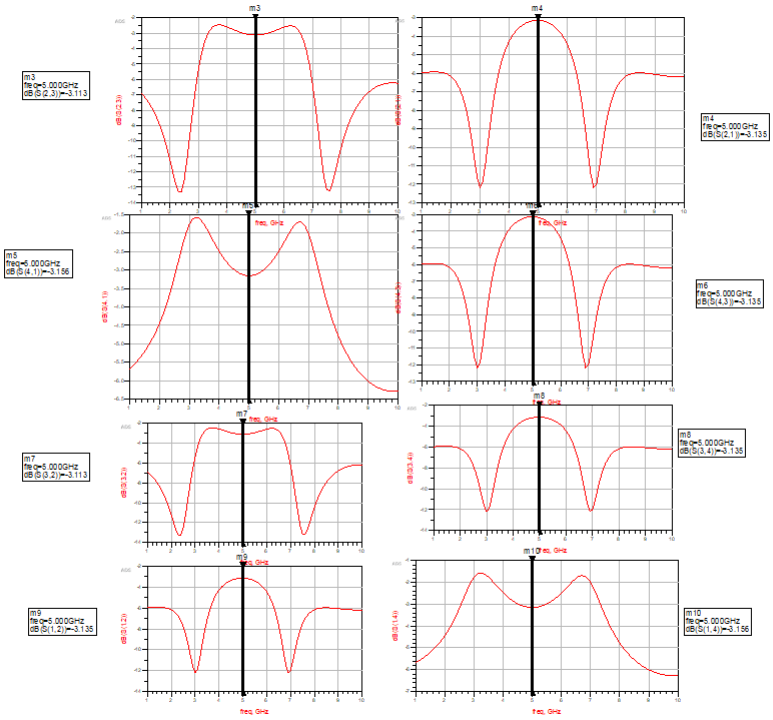


Figure 4.9: Simulation Magnitude final result

4.3.3 EM simulation

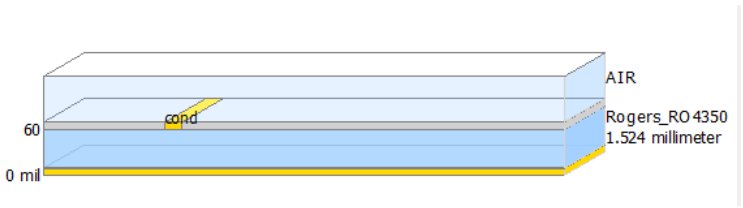


Figure 4.10: Substrate setup in EM simulation

The above substrate will be added to our simulation setup in this section. (For ADS substrate creating tutorial check the Nano Wiki of UiO)[14]. As explained in the theoretical background, this substrate will be used for momentum simulation in ADS. In order to see a larger scale of frequency changes impact the simulation result, the frequency range is set to be from 0 to 100 GHz with ten steps. Similarly, a corresponding sweep analysis is applied for EM momentum as well. The sweep parameter is radius. The simulation does not show the sweep result, the sweep parameter setup is given up in EM simulation: The EM simulation result when choose radius=8.6mm is below:

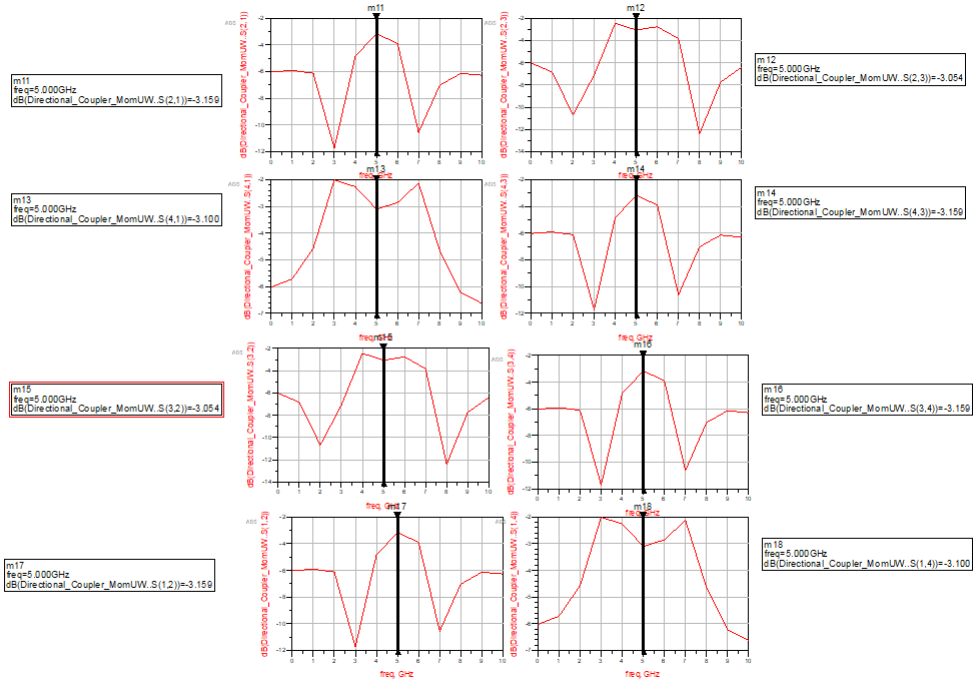


Figure 4.11: Electromagnetic Simulation S para result

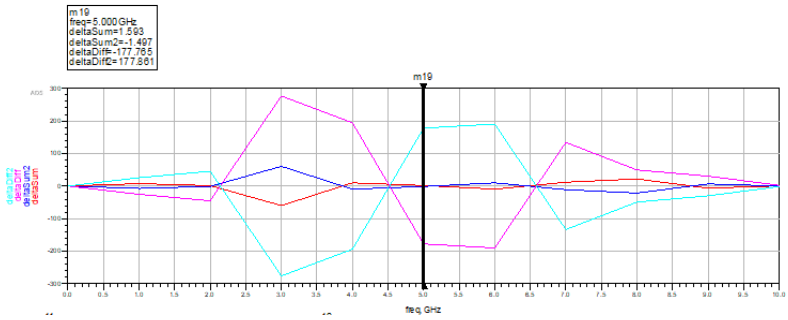


Figure 4.12: Electromagnetic Simulation delta result

There is a 3-degree variation in phase shift, but the magnitude shows there is no power dissipation during the transmission.

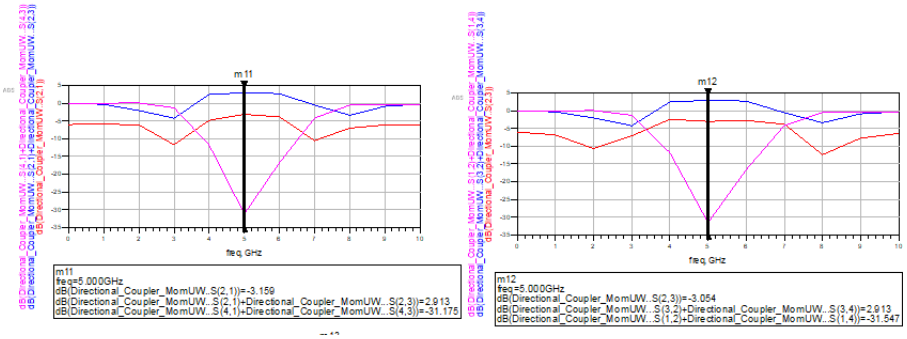


Figure 4.13: Electromagnetic Simulation momentum result

By making summation for the delta diff, power has reached a minimum peak -30dB!

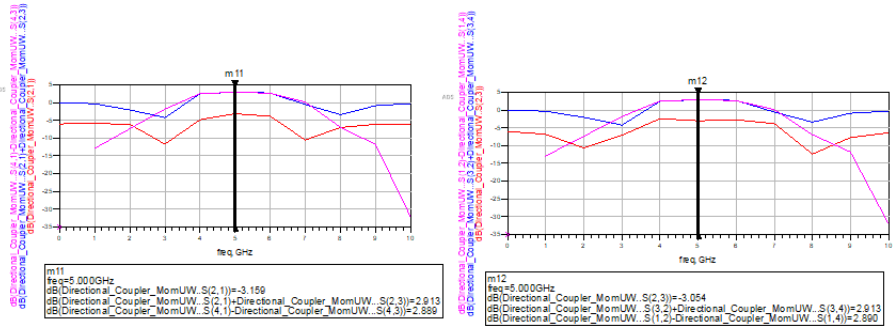


Figure 4.14: Electromagnetic Simulation reverse momentum result

In contrary, by making subtraction of for the delta sum, the power reached its top -3dB at 5 GHz.

Chapter 5

Passive component implementation

5.1 Component in Low frequency AC

The above chapter has designed a rat race microstrip line-based geometry structure. The lumped component structure has the advantage of size miniaturizing. This chapter will design a primary LC lumped circuit based on the calculations. Only passive components like capacitors and inductors without resistors are used. First, the passive components in series connection in low frequency are analyzed: Assume that the waveform in a circuit is a 2D sinus form of alternating current(AC). Only the imaginary part of the waveform is considered: The current will be

$$i = \hat{\imath} sin\omega t$$

The voltage will be

$$u = \hat{u} sin(\omega * t + \phi)$$

$$\hat{u} = Z * i$$

The impedance is:

$$Z = \sqrt{R^2 + (X_L - X_C)^2}$$

$$tan\phi = \frac{X_L - X_C}{R}$$

5.2 Component in High frequency AC

In high frequency, the impedance will decrease because of stray capacitance.[13, p. 19] Therefore, resistors are skipped but use capacitors and inductors instead. The voltage across an inductor has a 90-degree phase shift relative to the current, and the voltage across the capacitor has a -90-degree phase shift relative to the current. Schematic set up below and sweep inductor value from 10 to 200 in size of 50, but it gives the same result:

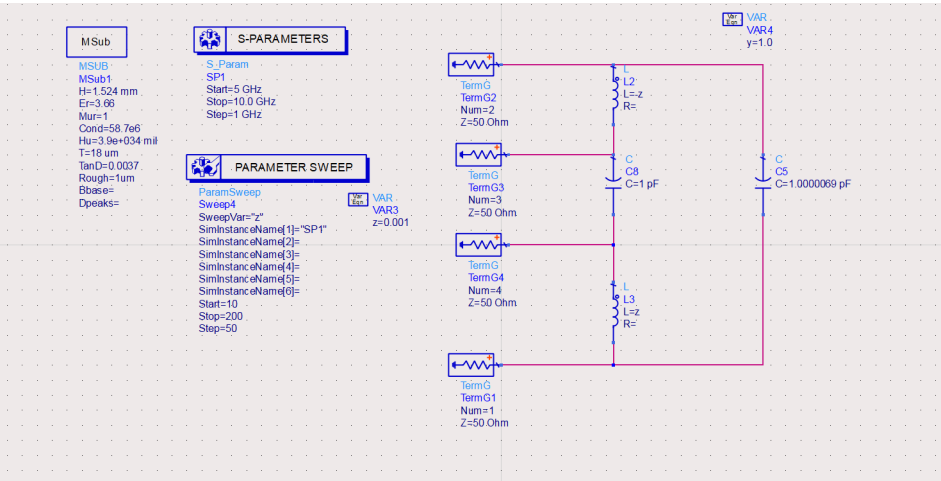


Figure 5.1: Sweep inductor schematic setup

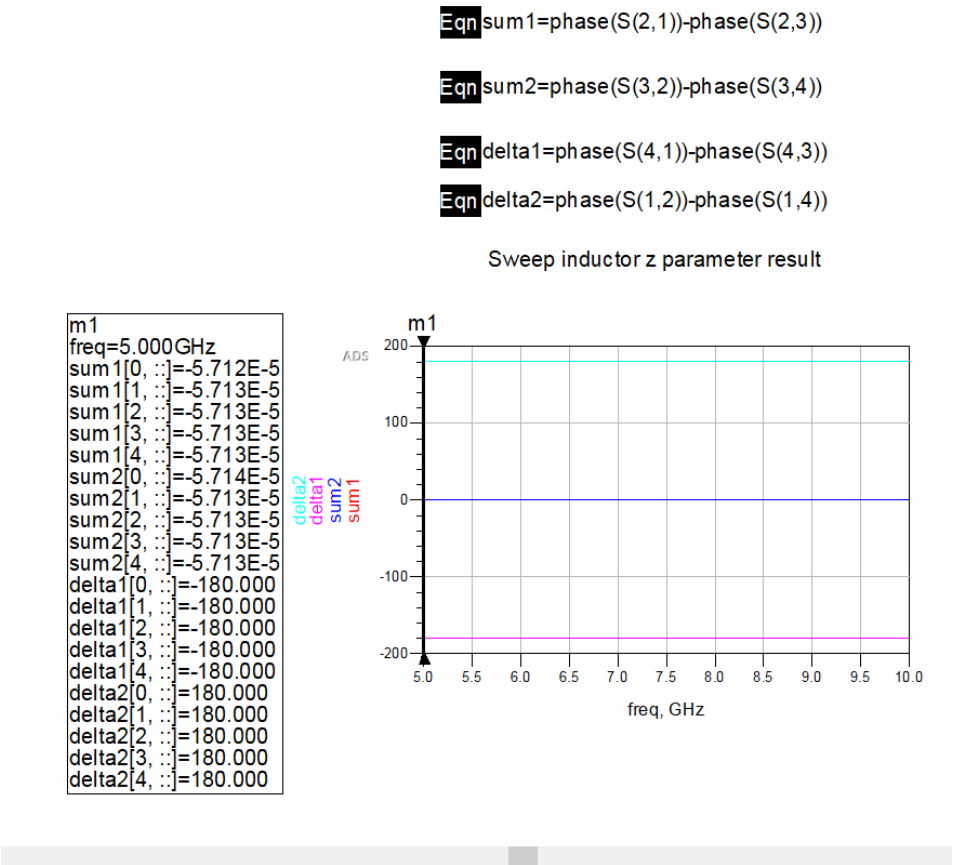


Figure 5.2: Sweep inductor z parameter result

By fine tuning capacitor C5 value to 1.0000069 pF the result is obtained. Then put back the parameter z: so L2=-200nH, L3=200nH, C8=1pF The simulation result is shown below:

Component	Value
C1	15fF
L11	5.5nH
L13	6nH
L14	5.5nH

Table 5.1: Final values of components applied to Cadence.

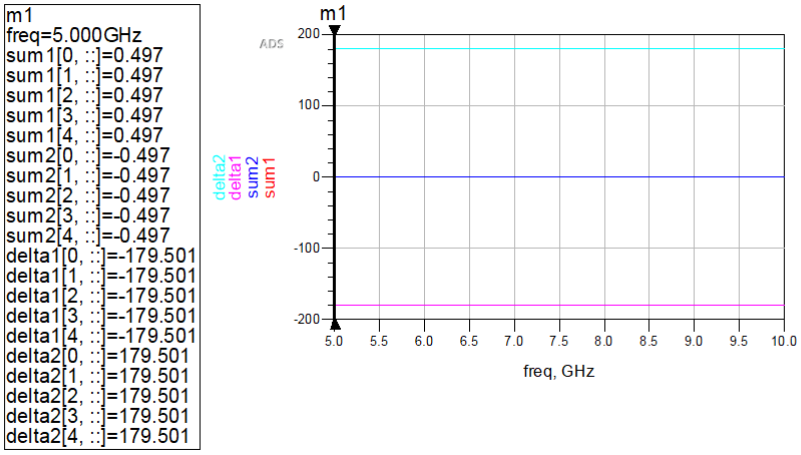


Figure 5.3: PCB simulation final result

In principle the -200 nH is mathematically possible, so after the adjusts of the schematic the following result is given:

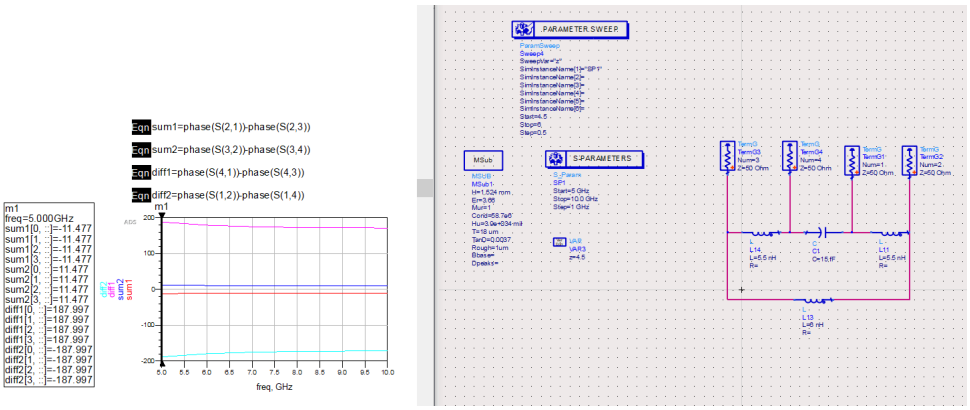


Figure 5.4: PCB schematic

The final value of capacitor and inductor is C1=15fF, L14=5.5nH, L11=5.5nH, L13=6nH. So, those values will be applied to Cadence. In order to know whether those values are reliable in the TSMC65nm library, the maximum and minimum value range for capacitor and inductor is founded below.

	Max	*Min*
crtmom_rf	10fF	500fF
spiral_sym_ct_mu_z	78pH	15nH

Table 5.2: Capacitor and inductor value range

All values are within the real component value range so the reliable component test bench setup in ADS below:

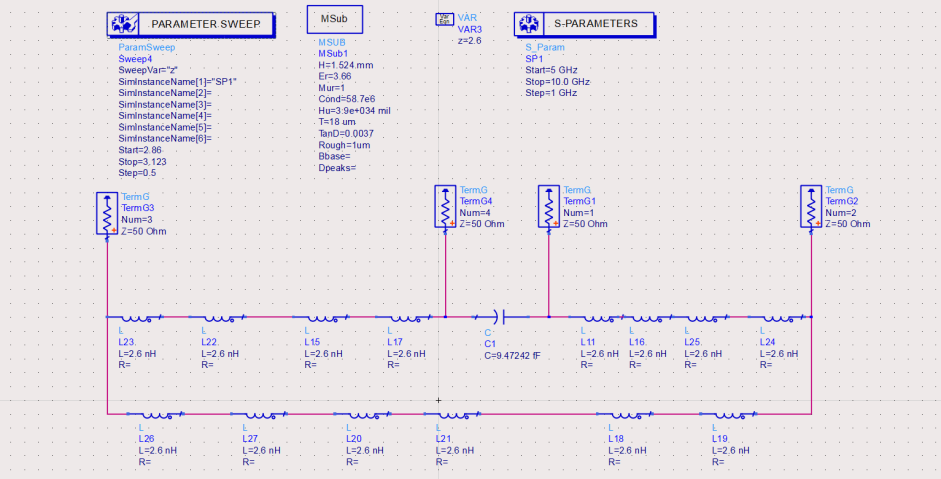


Figure 5.5: ADS schematic with divides reliable component value

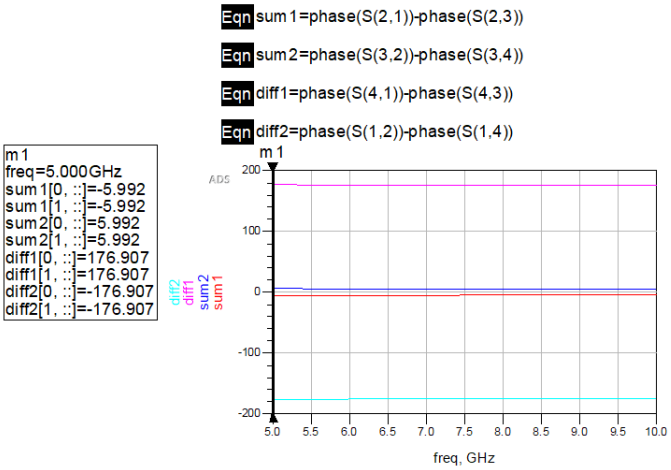


Figure 5.6: Simulation result with divided reliable component value

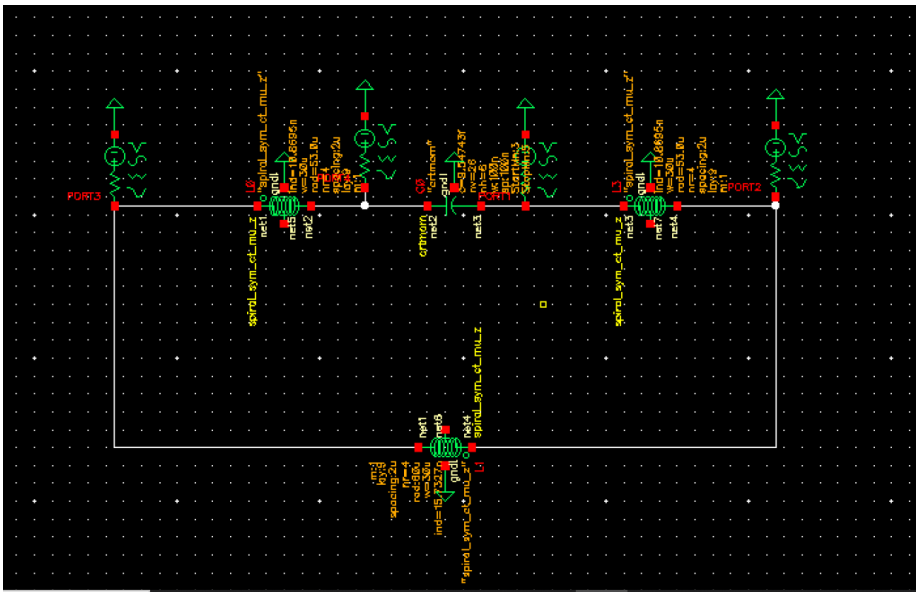


Figure 5.7: Cadence schematic setup with Tsmc65nm library

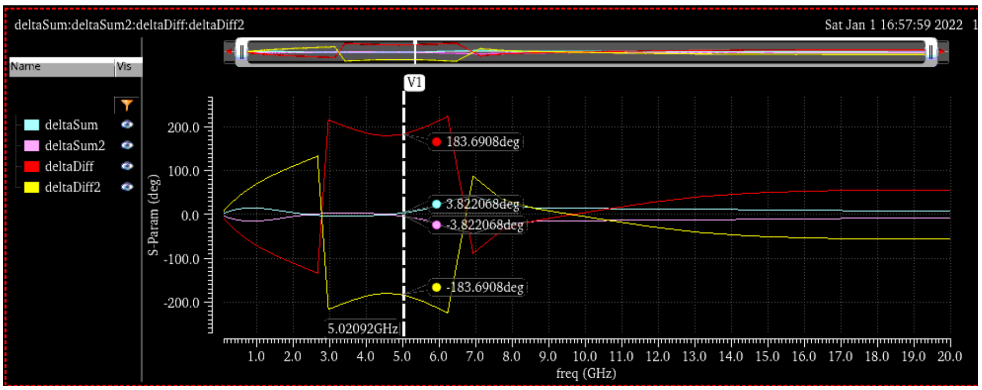


Figure 5.8: Simulation result cadence

The maximum value of Cap= 9.5fF has been used between Port 4 to 1, and inductor value 2.6nH*4 =10.6nH has been used between Port 3 to 4 and Port 1 to 2, between port 3 to 2, 2.6nH*8=20.8nH has been used. The bulk is grounded! The schematic is manipulated to create a hybrid coupler symbol and connect it to the test bench to generate the layout. After minimizing the number of inductors, the resonance curve has some significant swing after 6GHz. The smaller identical inductor has increased the signal bandwidth with constant dc feed, but after minimizing the size to a single one, the bandwidth decreases with less dc feed.

Chapter 6

Discussion

6.1 Performance Analysis

The performance analysis of our hybrid coupler is by analyse S11 and S22 (return loss), S14(insertion loss), S12 (reverse isolation), S21(forward gain).

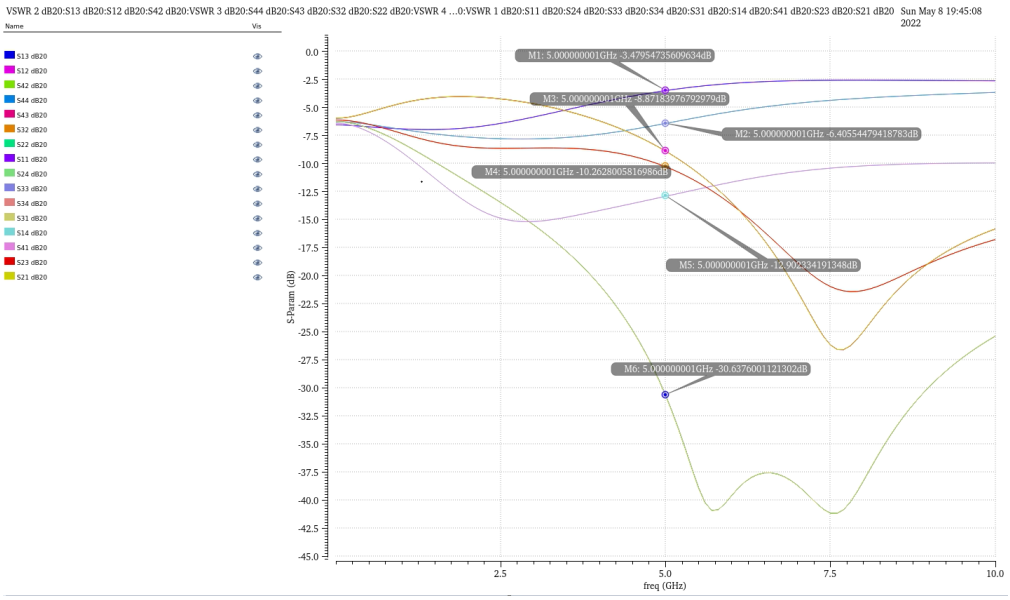


Figure 6.1: Simulation result S parameter

Parameter: Rat Race Coupler at 5GHz	
Reverse Isolation (S32)	$-10dB$
Reverse Isolation (S31)	$-30dB$
Reverse Isolation (S34)	$-6.4dB$
Reverse Isolation (S12)	$-8.87dB$
Reverse Isolation (S14)	$-8.87dB$
Insertion Loss (S41)	$-12dB$
Insertion Loss (S12)	$-10dB$
Return loss (S11)	$-3.48dB$
Return loss (S22)	$-6.4dB$
Reverse Isolation (S24)	$-30.8dB$
Reverse Isolation (S42)	$-30dB$
Return loss (S33)	$-6.4dB$
Return loss (S44)	$3.7dB$
Forward gain (S21)	$-8.87dB$
Forward gain (S23)	$-10.26dB$
Forward gain (S41)	$-8.87dB$
Forward gain (S43)	$-8.87dB$
VSWR1	$13.7dB$
VSWR2	$2.9dB$
VSWR3*	$2.9dB$
VSWR3	$9.2dB$
VSWR4	$13.7dB$
Gd23	$63ps$
Gd21	$63ps$
Gd41	$99ps$
Gd43	$63ps$
Gd42	$-20ps$

Table 6.1: S parameters, *= Hand calculated.

According to [15] performance analysis, forward gain S21 attenuation should be approximately -3dB, reverse isolation S32 and S34 are supposed to be less than -20 dB, which is -10 dB in our case. Return loss is supposed to be less than -15dB. The bandwidth should be more than 78 percent of the total working frequency, to reduce the unnecessary power loss. Phase tolerance interval should be plus or minus 10 degrees. Another article [16] has demonstrated similar results as our simulations. In our case, the isolation attenuation of S32 and S34 should be as high as possible to keep the two input signals isolated. The absolute attenuation of forward gain S21 should be as high as possible. The absolute attenuation of S11 is supposed to be as low as possible for an ideal hybrid coupler design. As depicted in Figure 6.1, at the frequency of interest, 5 GHz, which is the middle frequency of our actual bandwidth of hybrid coupler(4 GHz to 6.8 GHz) partly, a pretty satisfactory result is reached. The return loss is less than 7dB. Forward gain S21 is almost the same as reverse isolation S12, around -8.87dB, since it is a bidirectional structure. Group delay for G42 has a negative time delay -20ps, which is entirely reasonable between

two output ports. Because the purpose of our hybrid coupler is to have the correct phase shift in output port 2 and port 4, the requirement of reflecting attenuation S21 might relax to -10dB. Compared to the literature studies [17] forward gain result is approximately 7dB. Group delay is, by definition, the rate of changing of phase. The inductor has a jwL inductance utilizing forward phase shift, and the capacitor has 1/jwC capacitance, lagging the signal. There are two identical inductors between ports 1 and 2 and ports 3 and 4. Between ports 2 and 3 is another larger inductor. Between ports 4 and 1 is a capacitor. All four components are grounded. All the design values are decreased to reduce the parasitic effect. (Table simulation before and after). The signals from two input ports 1 and 3 are supposed to cancel each other out by the two inductors when going to port 2. Signals coming from port 1 are supposed to be 270 degrees delayed by the capacitor, and port 3 signals should be forwarded by the inductor 90 degrees. The delta between them will be 270-90=180 degree phase shift.

$$\begin{pmatrix} S_{11} = -3.48dB & S_{12} = -8.87dB & S_{13} = -39dB & S_{14} = -12dB \\ S_{21} = -8.87dB & S_{22} = -6.4dB & S_{23} = -10.26dB & S_{24} = -30.8dB \\ S_{31} = -30dB & S_{32} = -10dB & S_{33} = -6.4dB & S_{34} = -6.4dB \\ S_{41} = -12dB & S_{42} = -30dB & S_{43} = -8.87dB & S_{44} = 3.7dB \end{pmatrix} \tag{6.1}$$

The s-parameter matrix above shows excellent reverse isolation between the two output ports. This matrix is very symmetric. S11=S44, S41=S14, S23=S32, S21=S12=S43, S42=S24, S22=S34=S33, forward gain of S21 and S43 has a tolerance interval of minus 6 dB energy loss. S21 and reverse isolation S12 are the same, and S23 and reverse isolation S32 are the same. S31=S42=S24, S13 is very uniquely high, which is reasonable because it is between two output ports.

VSWR (Voltage standing wave ratio) for port 1 is defined as (1+S11)/(1-S11)= (1+(-3.48))/(1-(-3.48))= -1.8065, VSWR for port 2 is defined as (1+S22)/(1-S22)= (1+(-6.4))/(1-(-6.4)) = -1.3704, VSWR for port 3 is defined as (1+S33)/(1-S33)= (1+(-6.4))/(1-(-6.4)) = -1.3704, VSWR for port 4 is defined as (1+S44)/(1-S44)= (1+(-3.7))/(1-(-3.7)) = -1.7407. The voltage standing wave ratio is the ratio between maximum and minimum voltage reflected on the port. When the impedance is perfectly matched there will be no power loss, by means of the S11 S22 S33 S44 will be as close as -3dB as possible. When the VSWR is 1, there are no reflected power and the voltage have a consistent magnitude. A negative VSWR means there is a power loss at the port, the reflected negative voltage is higher than the positive. The noise contribution of each port is shown in result browser:

```
# value( VNP("/PORT2") 5G)

sweep             value(VNPP("/PORT2" "??") 5e+09) (V^2/Hz)
ext_file_noise        0
rn                  380.145e-21
total               380.145e-21

# value( VNP("/PORT1") 5G)

sweep             value(VNPP("/PORT1" "??") 5e+09) (V^2/Hz)
ext_file_noise        0
rn                   29.8666e-21
total                29.8666e-21

# value( VNP("/PORT4") 5G)

sweep             value(VNPP("/PORT4" "??") 5e+09) (V^2/Hz)
ext_file_noise        0
rn                  974.606e-24
total               974.606e-24

# value( VNP("/PORT3") 5G)

sweep             value(VNPP("/PORT3" "??") 5e+09) (V^2/Hz)
ext_file_noise        0
rn                   17.536e-21
total                17.536e-21
```

Figure 6.2: Noise analysis

The two output ports, port 2 and port 4 contribute the most noise. The two input ports, ports 1 and 3, have minimal noise contribution. Delta port 4 has the most noise contribution among others.

6.2 Smith Chart

Impedance matching network is applied to Smith Chart by a unity circle around 50 Ohms (yellow circle). Since the VWSR is negative, the unity circle may overlap more than 180 degrees. Beyond the left edge will approach the short circuit, and the right side will approach the open circuit. We add series L from port 1 to port2 jw*7.5nH, adding one more series inductor jw*8.92924nH from port2 to port3. Adding a series/ parallel inductor will elevate the inductance along the real axis, adding a series/parallel capacitor crash down through the real axis.

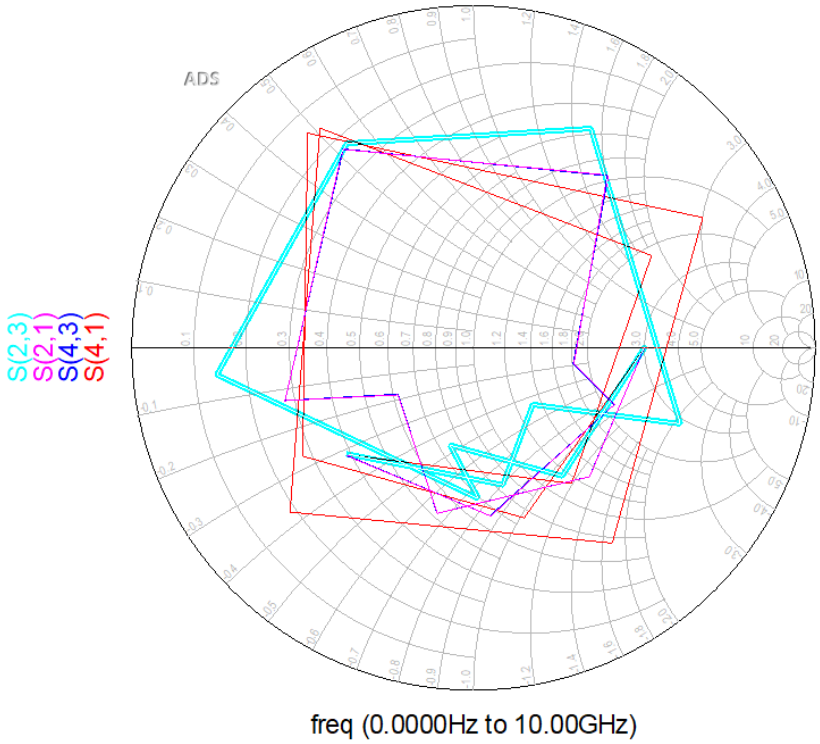


Figure 6.3: Smith chart analysis

6.3 Miniaturization

The physical dimension of the passive circuit is the first inductor: width=538.66um, length=466.02um. capacitor: width=100nm. Second inductor: width=538.66um, length=466.02um. Third inductor: width=457.445um, length=406.02um. The dimension of the layout is: width:1291 um, around 1.291 mm, length:1100 um, around 1.1 mm. The tiny aspect is designed to be compact for biomedical purposes. It is handy for blood sugar measurement, for example. Another perspective to reduce the size is to use a resonance circuit. Two LC tank series connections might reduce the size because the capacitor is smaller than the center-tapped inductor. At our frequency of interest 5GHz, the ft=2*pi*1/$\sqrt{LC}$, $LC = 6.3390e + 09$.

Chapter 7

Active component implementation

7.1 Active component design in Cadence

The active hybrid coupler has the advantage of miniaturizing to nanometer level but has the disadvantage of non-reciprocal. Size mismatching between the upper NMOS transistor and down NMOS transistor will cause some phase shift between the input signal (gate) and the output signal from the source-drain side. So the active component design will be based on the principle of two NMOS_rf_6x connected as an inverter. By having a diverse width and length in the upper NMOS transistor and the bottom NMOS transistor, the phase will be shifted 180 degrees or 90 degrees. Since every transistor in the cutoff region can be treated as a resistor, even though all the transistors are not in saturation, it still can fulfill the requirement. Four inverters are used. Their parallel connection makes them an equal voltage divider of 1 Volt, which will be 250mV for each inverter, and each NMOS transistor is half of 250mV, which is 125mV (source-drain voltage), since the gm=125mV/25=5 siemens, because gm=2*Id/Veff => Id=gm*veff/2=0.005*0.2/2=0.5mA. Then the width over length $=\sqrt{0.0005} = 0.02236$, the minimum length 60nm is used, and the total width will be 1.3416nm*5fingers=6.708nm. Since a width over length percentage is used by means, the total width would be around 670nm. Then the above parameter will be put back into the schematic and set up test bench in Cadence.

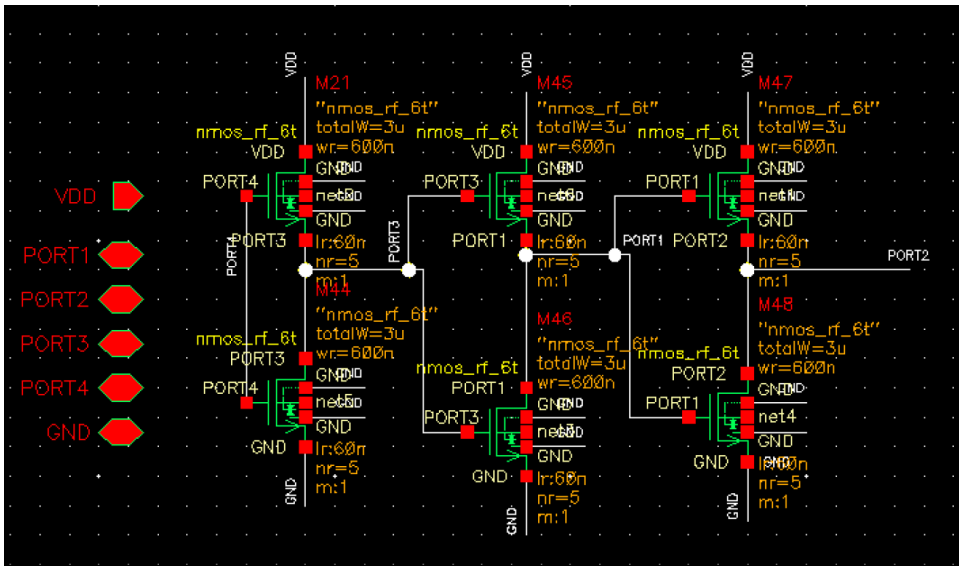


Figure 7.1: Serie inverter setup in cadence

After some fine tuning, the final width of 600nm will be used for Nmos. The final simulation result is shown below:

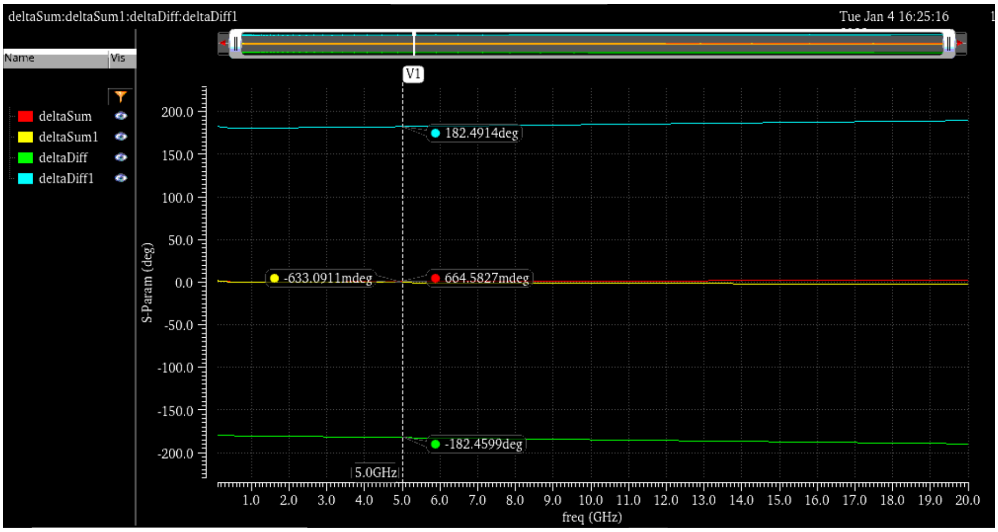


Figure 7.2: Result of serie inverter

Nmos hybrid coupler gives better phase response without any phase shift through all frequency ranges, and it is bidirectional. It shows its advantage by miniaturizing the whole circuit. However, the NMOS circuit constructs a latch that causes a bi-directional problem because deltaDiff is supposed to be positive 180 degrees. The simulation of Nmos in one direction is succeeded!

Chapter 8

Verification

8.1 Passive component layout in Cadence

The final step is to make a layout and do EMX simulation to verify the simulation result before send to fabrication.

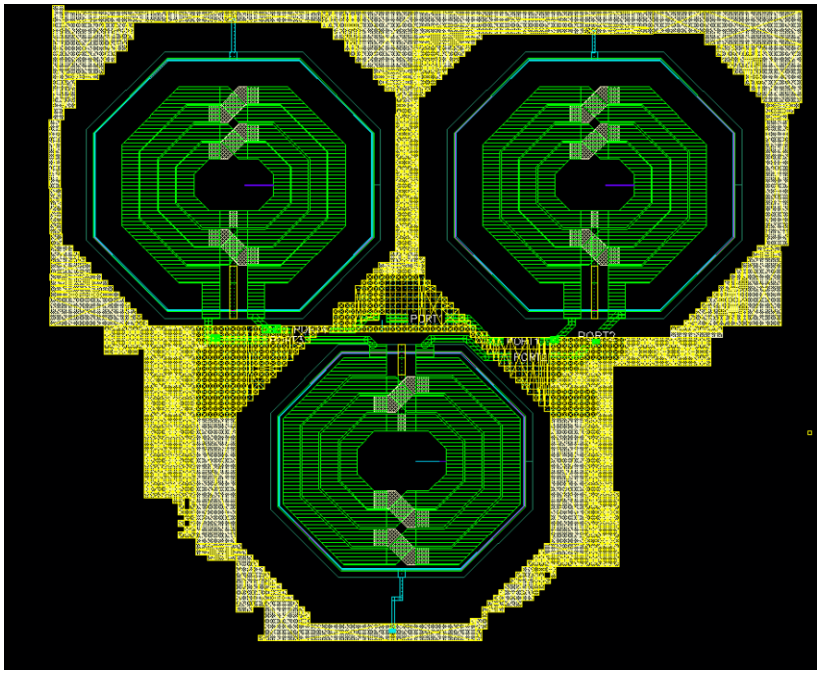


Figure 8.1: Layout

Center tapped inductor has 8 metal layers M1 to M8. All even layers are powered, and odd layers are grounded. M9 is used for routing and M8 is used for shielding for ports.

Model name	$spiral_s ym_c t_m u_z$
Inductor width, M	$30u$
Inner radius, M	45.0
Number of turns	4
Spacing, M	$2u$
Guard ring distances, M	$50u$
Temp, C	27
Freq, Hz	$5G$
Approx. inductance, H	$7.50883n$
Q factor	5.223697
Inductor area width, M	$538.66u$
Inductor area length, M	$466.02u$
Top metal	9
Hard constrain	*Yes*

Table 8.1: Twin inductors' parameters.

Model name	$spiral_s ym_c t_m u_z$
Inductor width, M	$30u$
Inner radius, M	52.0
Number of turns	4
Spacing, M	$3u$
Guard ring distances, M	$10u$
Temp, C	27
Freq, Hz	$5G$
Approx. inductance, H	$8.92924n$
Q factor	4.997419
Inductor area width, M	$457.445u$
Inductor area lenght, M	$406.02u$
Top metal	9
Hard constrain	*Yes*

Table 8.2: Third inductor parameters.

Model name	*crtmom*
Description	*MOMcapacitor*
Fingers width, M	30*u*
Fingers space, M	45.0
Number of horizontal fingers	4
Number of vertical fingers, M	2*u*
RTMOM bottom metal layer, M	50*u*
CapValue@0V, F	27
Create OD dummy	5*G*
OD width, H	7.50883*n*
Create OD2 layer	5.223697
DFM rule, M	538.66*u*
Well type, M	466.02*u*
Adding DMEXCL layer	9
Hard constrain	*Yes*
Register number	*IMEC* − 2218561833

Table 8.3: Capacitor parameters.

Parasitic inductance will be generated by many factors, such as mosaics tiles and copper wires. VDD net is floating in layout since it is a passive circuit. After EMX simulation the new generated N-Port symbol is implemented to testbench and the results are shown below:

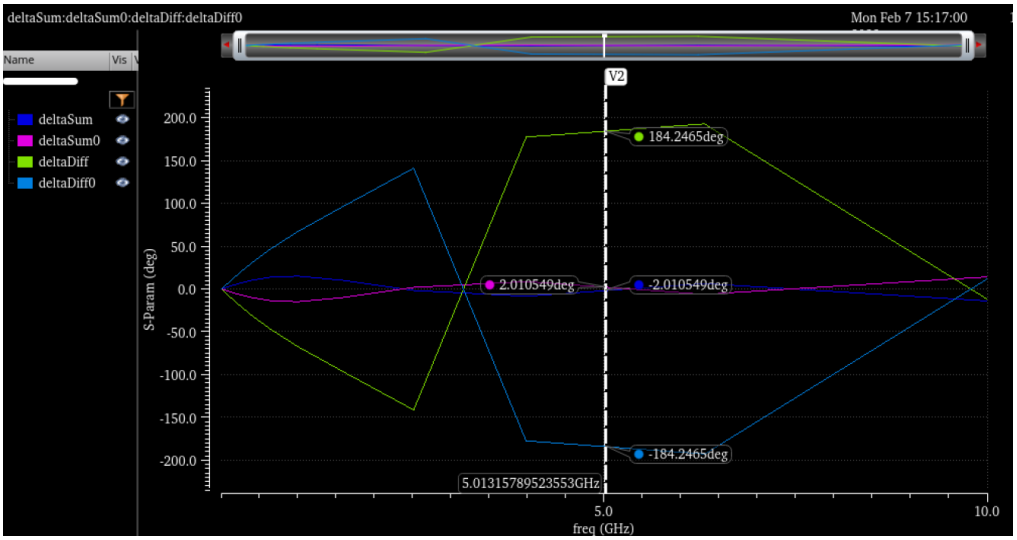


Figure 8.2: Final result in cadence

To the difference of ideal cap (9.7 f), ten times the value is used in layout to reduce the parasitic inductance and drive the deltaSum and deltaSum0 to approximately 0 degrees. Two symmetric inductor values have controversially decreased from ideal 10nH to real component 7.5nH The corresponding last one has reduced from 15nH excellent value to non-ideal value 8.9nH, to counterpart the other inductor and capacitor effect.

Compared to Figure 4.12, the parasitic inductance and capacitance have shifted the frequency bandwidth a little to the left from 5 - 6 GHz to 4 - 6.5 GHz. The tolerance interval is tweaked with plus and minus 1 degree. Compared to Figure 5.8, the frequency bandwidth has shifted slightly from 3 - 6.5 GHz to 4 - 6.5 GHz. The via material in the center tapped inductor and another parasitic factor from the copper line has minimized the frequency bandwidth! The last step is to send the layout-generated GDS file to fabrication.

Chapter 9

Conclusion

The 180-degree hybrid coupler is used for biomedical or mono-radar purposes. It works by splitting or combining two equal amplitude high-frequency input signals. The required phase shift will be the reference for analyzing the desired pattern, such as a change in blood sugar level. The blood sugar level will be detected without vessel penetration by further categorizing the desired pattern of two input signals with the original pattern. This master thesis uses Advanced Design System (ADS) and Cadence to design a hybrid coupler focusing on passive components. The active component shows a trade-off in miniaturizing but not reciprocal. Our hybrid coupler has a working frequency spanning between 4GHz and 6.5GHz after the EMX simulation, which covers the resonant frequency of the center-tapped inductor, usually around 6GHz plus parasitic. Compared to the ideal component design in Cadence, the bandwidth has shifted to the left and minimized 4GHz, which might be caused by the via in the inductor, which can create parasitic inductance to the circuit. From the performance analysis, the reverse isolation and the return loss have to be further improved to 0(-40dB), and the reflection coefficient has to be minimized depending on the requirement. Still, there is a 10dB hybrid couple on the market, so the 10dB reflection coefficient is entirely reasonable! The noise contributed from each port can be reduced by connecting a decoupling capacitor for each port in layout to the ground, but it might affect the phase shift of our result. Many litterateur studies have been carried out for rat race hybrid coupler with different geometric and π shape geometry has shown its advantage over T-shape geometric when considering reflection coefficient and return loss. However, since it is not a phase-shifting rat race hybrid coupler, it is irrelevant to our circuit design since the size is miniaturized to only four components, so our experiment succeeded! A more complex structure should be considered between the excitation port and the isolation port to improve bandwidth. Due to the limited time and lack of theoretical support from the company, we have stopped our work here.

Chapter 10

Appendix

Meeting on Zoom: 18-12-2020 Basic instruction on principle of hybrid coupler Book reference ... Meeting on Zoom: 01-15-2021 Schematic design in ADS /CST. Meeting on Zoom: 1-25-2021: simulation in ADS Meeting on Zoom: 1-27-2021: T-strip setup and equation correction. Meeting on Zoom: 1-30-2021: simulation setup. Meeting on Zoom: 02-04-2021: EM simulation and phase and amplitude sweep discussion. Meeting on Zoom: 03-08-2021 : On alternative hybrid coupler design Meeting on zoom: 04-21-2021: On PCB design Meeting on zoom: 05-05-2021: justify the max value of cap and inductor Meeeting on zoom: 18-10-2021: ADS component recap. and EM simulation in cadence.

Bibliography

[1] Edgar Garay, Min-Yu Huang and Hua Wang. 'A cascaded self-similar rat-race hybrid coupler architecture and its compact fully integrated Ka-band implementation'. In: *2018 IEEE/MTT-S International Microwave Symposium-IMS*. IEEE. 2018, pp. 79–82.

[2] Mahmoud Moubadir et al. 'Miniaturized design of rat-race coupler by utilizing T-shape stubs'. In: *Procedia Manufacturing* 22 (2018), pp. 79–84.

[3] Amjad Omar, Nihad Dib and Abdullah AlBdrashiny. 'Miniaturized CPW Rat-Race Coupler Using the Superformula'. In: *2018 18th International Symposium on Antenna Technology and Applied Electromagnetics (ANTEM)*. IEEE. 2018, pp. 1–2.

[4] Young-wan Kim et al. 'Performance analysis for various structures of six-port phase correlator using hybrid coupler, power divider and rat-race ring coupler'. In: *International Symposium on Computer Science and Its Applications*. IEEE. 2008, pp. 243–246.

[5] Fatemeh Babaeian and Nemai Chandra Karmakar. 'A planar ultra-wide band asymmetric rat-race hybrid coupler'. In: *International Journal of RF and Microwave Computer-Aided Engineering* 30.6 (2020).

[6] RF Directional Couplers. *3dB Hybrids Overview*. URL: https://www.ieee.li/pdf/essay/directional_couplers.pdf.

[7] B Pavithra and S Maheswari. 'Design of Compact 180 degree Hybrid Coupler Using T-Shaped Structure'. In: *Advances in Engineering Research (AER)* 142 (2018). URL: https://www.researchgate.net/publication/355422070_Design_Of_Compact_180_Degree_Hybrid_Coupler_Using_T-shape_Structure.

[8] Hani Ghali and Tarek A Moselhy. 'Miniaturized fractal rat-race, branch-line, and coupled-line hybrids'. In: *IEEE Transactions on Microwave Theory and Techniques* 52.11 (2004), pp. 2513–2520. URL: https://ieeexplore-ieee-org.ezproxy.uio.no/stamp/stamp.jsp?tp=&arnumber=1353534&tag=1.

[9] He-Xiu Xu, Guang-Ming Wang and Ke Lu. 'Microstrip rat-race couplers'. In: *IEEE Microwave magazine* 12.4 (2011), pp. 117–129.

[10] *Master Thesis Instruction*. URL: https://www.mn.uio.no/fysikk/studier/master/masteroppgaver/Elektronikk-informatikk%5C%20og%5C%20teknologi/mikroelektronikk-og-sensorteknologi/hybrid-coupler.html.

[11] Frank Gustrau. *RF AND MICROWAVE ENGINEERING. FUNDAMENTALS OF WIRELESS COMMUNICATIONS*. A John Wiley Sons, Ltd., Publication, 2012. ISBN: 978-1-119-95171-1.

[12] *RO4000® Series*. URL: https://rogerscorp.com/-/media/project/rogerscorp/documents/advanced-connectivity-solutions/english/data-sheets/ro4000-laminates-ro4003c-and-ro4350b---data-sheet.pdf.

[13] Gene Bogdanov Renhold Ludwig. *RF circuit design*. Pearson International Edition, 2009, p. 704.

[14] *ADS substrate*. URL: https://nano.wiki.ifi.uio.no/ADS_Substrate_definition.

[15] Hiroshi Okabe, Christophe Caloz and Tatsuo Itoh. 'A compact enhanced-bandwidth hybrid ring using an artificial lumped-element left-handed transmission-line section'. In: *IEEE Transactions on Microwave theory and Techniques* 52.3 (2004), pp. 798–804.

[16] Mazhar B Tayel and Hani S Alhakami. 'An optimized lumped element improved performance hybrid Directional Couplers'. In: *2012 8th International Conference on Computing Technology and Information Management (NCM and ICNIT)*. Vol. 1. IEEE. 2012, pp. 489–494.

[17] GL Stevens. 'A high-performance hybrid RF isolation amplifier'. In: *The Telecommun. and Data Acquisition Rept.* (1984), pp. 1–8.