

# Investigation into the Implementation of a Frequency-to-digital $\Sigma\Delta$ Modulator ADC based on 3D Sequential Integration

Zhijian Zhou



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Department of Physics  
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Implementation of a  
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# Abstract

Continuous MOSFET dimensional scaling is a challenge in semiconductor device fabrication. 3D integration is a possible solution for further reduction of integrated circuit area. The 3D-MUSE project explores a specific high density 3D integration technology, 3D sequential integration (3DSI), for 'systems-in-cube' (SinC) circuit designs in a 2-tier 3D stack combining 28nm FDSOI and 65nm SOI CMOS technologies.

With the benefit from the extraordinary increase in vertical connection density in 3DSI technology, analog and digital devices can be designed respectively in two different tiers connected by a monolithic inter-tier via (MIV). Therefore, mixed signal circuits are highly recommended such as analog-to-digital converters which are important in almost any electronic system.

In this thesis, the theory, design and analysis about a 1st order 8-bit frequency-to-digital  $\Sigma\Delta$  modulator (FDSM) ADC are illustrated. Compared with the conventional  $\Sigma\Delta$  ADC, the FDSM ADC is a non-feedback  $\Sigma\Delta$  ADC which does not need a DAC. The integrated circuit is designed with 3DSI PDK. The analog devices are implemented in the top tier with the 28nm FDSOI process transistor while the digital devices in the bottom tier based on the 65nm SOI CMOS process transistor. This ADC employs a 1.0V supply voltage and the maximum power consumption is 1.161  $\mu\text{W}$  for 8-bit resolution. The FSR is [0 nA, 102.52nA]. The clock frequency is 100 MHz and the sampling frequency is 172.17 kHz.

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# Preface

It is an unforgettable experience for the past two years I have spent in University of Oslo. My gratitude to the people who have given me help and support cannot be fully expressed with a few words in the preface.

Firstly of all, I wish to express my great gratitude to my supervisor Professor Philipp Dominik Häfliger for offering me such an opportunity to work on my thesis on 3DMuse project. It was him who had patiently guided me through the whole project.

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I wish to thank many of my friends for contribution in each of their own ways, though not directly related to my work, but no one will be forgotten, though no one is mentioned here.

Finally, I wish to thank my family for their patience, understanding and encouragement over the years.

# Chapter 1

## Introduction

### 1.1 3D Sequential Integration

3D integration is a broad term that includes the technologies which stack silicon wafers and interconnect them vertically. The integration density is, therefore, enhanced by adding more functionality to an integrated circuit without increasing area. The small distance between stacked tiers can reduce the resistance and the parasitic capacitance in vertical interconnections. 3D sequential integration (3DSI), as one of the 3D integration technologies, provides a very high density of vertical interconnections. The reason for this is that the pre-patterned device tiers are connected by the monolithic inter-tier vias (MIVs) which can be processed as same as any other metal-to-metal via in the 3DSI. [10]

### 1.2 Motivation

3D-MUSE wants to spearhead the progression from classical 'Systems-in-stack' to true 'Systems-in-cube'(SinC) which will be realized by 3DSI.[1]

The former is known as a 3D system where functional blocks are located in a single plane in the 3D integration stack, while the latter takes advantage of the full emancipation of interconnect density in the third dimension of 3DSI and implements functional blocks in a volume with multiple tiers. Compared with the conventional 3D system, the significant difference in 3DSI is that the vertical connection density is on par with the horizontal connection density. As a result, system structures can now completely encompass the placement of each individual system component in a volume.[1]

Thus, transistors of a circuit module can be placed freely in any tier with no significant disadvantages. This provides new chances to make tiers with different types of transistors, e.g. transistors optimized for the digital signal domain in one and transistors optimized for the analog signal domain in another tier. As a consequence, mixed signal circuits can be designed with highly optimized components, as the frequency-to-digital  $\Sigma\Delta$  modu-

lator ADC designed is illustrated in this thesis.

4DSpace is a Strategic Research Initiative at the Faculty of Mathematics and Natural Sciences of the University of Oslo [2]. Its objective is to figure out how plasma instabilities and turbulence affect energy transfer, transport and coupling at different scales in the near Earth space.

Bekkeng Tore Andre's master thesis [8] is based on this project. In his thesis, he designs a prototype of a novel fixed-bias multi-Needle Langmuir Probe system to be used on sounding rockets and satellites. The instrument collects current from four needle probes placed in front of the rocket/satellite's shock front and measures it separately. The frequency-to-digital  $\Sigma\Delta$  modulator ADC demonstrated in this thesis implements converting an input current into digital output signal and can be applied in the prototype designed by Bekkeng Tore Andre to measure the current.

### **1.3 Objectives**

In this thesis, the main goal is to investigate an implementation based on the emerging CMOS 3DSI in 3D with a 3DSI PDK instead of the classical 2D integrated circuit by designing a specific circuit, a 1st order 8-bit frequency-to-digital modulator  $\Sigma\Delta$  ADC that can convert input current into digital output signal.

## Chapter 2

# Background

### 2.1 3D-MUSE

3D-MUSE is a Horizon 2020 EU research project that began on January 1, 2018 and will last for four years, aiming on developing 3DSI in state of the art 28nm CMOS technology to allow 3D integrated circuit designs with the same order of magnitude of vertical inter-tier via density as horizontal wire density. A schematic diagram of 3DSI is shown in Figure 2.1.1. The 3DSI consists of two device tiers connected by a Monolithic Inter-tier Via (MIV). One tier is the top tier which utilizes the SOI 65nm process technology. The other tier is the bottom tier which is based on the 28nm FDSOI process technology. [1] [10]

#### 2.1.1 Silicon on Insulator

The silicon on insulator (SOI) refers to the fabrication technology which employs a layered silicon-insulator-silicon substrate in semiconductor manufacturing. The silicon junction is above an electrical insulator, which is significantly different from that for the traditional silicon-built devices. The insulator isolates the body from the substrate, significantly reducing the parasitic capacitance. [22]

#### 2.1.2 Fully Depleted Silicon on Insulator

The fully depleted silicon on insulator (FDSOI) is a planar process technology that combines the advantage of decreased silicon geometries with the ease of production. This technology is established on two major breakthroughs. One is that an ultra-thin layer of insulator, known as the buried oxide (BOX), is placed on the top of the base silicon, the other is that the transistor channel can be built by a very thin silicon film. By virtue of the thin film silicon structure, it is unnecessary to dope the channel, resulting in a "fully depleted" transistor.[14]

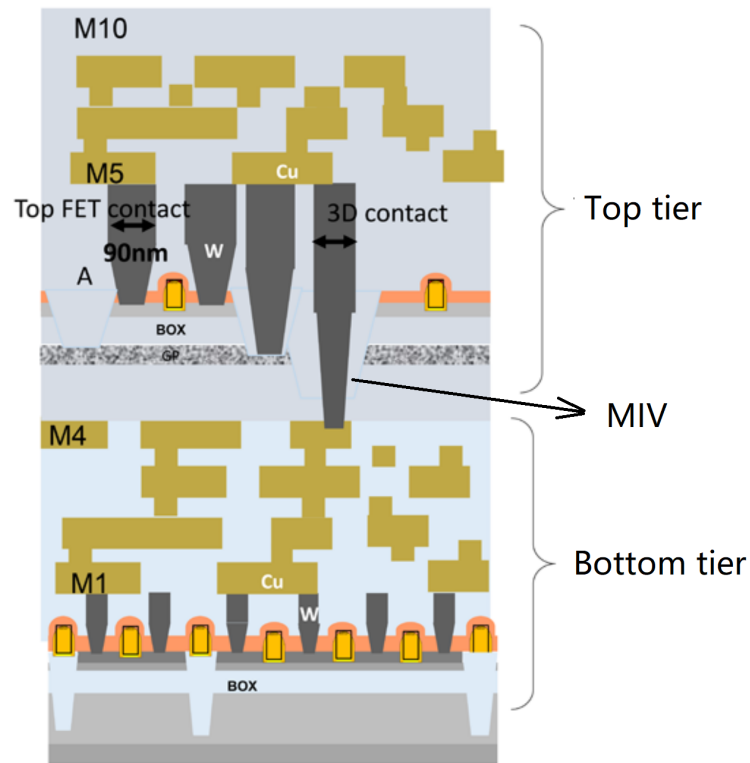


Figure 2.1.1: A schematic diagram of 3DSI [1]

## 2.2 Analog-to-digital Converter (ADC) Application

Analog-to-digital converter (ADC) is a system that converts an analog signal (continuous form) to a digital signal (discrete form). A simple ADC symbol is shown in Figure 2.2.1.

As a vitally important integral to connect the real-world with digital system, ADCs are utilized in many fields. For instance, they play an significant role in music recording. People frequently make music on computer by means of analog recordings, necessitating the use of analog-to-digital converters to create the pulse-code modulation(PCM) data streams that are used in CDs and digital music files. ADCs are also extensively used in digital signal processing to produce the quantized signal such as TV tuner cards, microcontrollers and digital storage oscilloscopes. In addition, ADCs are of vital importance in scientific instruments as in the readout circuits of the CMOS image sensor design. There are various sensors such as temperature sensors, pressure sensors, accelerometer and etc., which produce analog signals. These signals can be amplified and sent into an ADC, providing a digital number proportionate to the input signal.



Figure 2.2.1: An ADC symbol [6]

## 2.3 Analog-to-digital Converter Architectures

### 2.3.1 Integrating ADCs

Integrating ADC is a form of analog-to-digital converter that principally uses an integrator to convert an unknown input voltage into a digital representation. This type of converters is ideal for realizing high-accuracy data conversion in a very slow speed. It provides high resolution and are commonly used in the measurement instruments such as digital multimeters. A schematic diagram for a dual-slope integrating ADC is shown in Figure 2.3.1 and its "dual slope" conversion plotted in Figure 2.3.2. The integrator input is connected to the minus input ( $-V_{in}$ ) to ramp up in a fixed time ( $t_{int}$ ) and reach a certain voltage dependent on the magnitude of the input voltage. Then the input is connected to a constant reference voltage ( $V_{ref}$ ) to ramp down to zero, resulting in a constant slope and a time variable. The dual-slope integrating ADC solves the accuracy problem in single-slope integrating ADC because its output is independent of the resistor (R) and the capacitor (C).

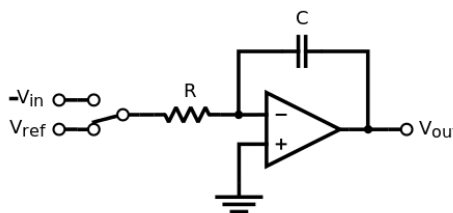


Figure 2.3.1: Integrating(dual slope) ADC [16]

### 2.3.2 Successive-Approximation ADCs

Successive-approximation ADCs primarily use the binary search algorithm to find the closest digital number to match an input signal. A schematic diagram for a D/A converter-based successive-approximation ADC is illustrated in Figure 2.3.3. In the first period, the most significant bit (MSB) will be determined. Then in each following period, a lower significant bit will be determined until the lowest significant bit (LSB) is determined in the last period. Therefore, to finish an N-bit conversion, the successive-

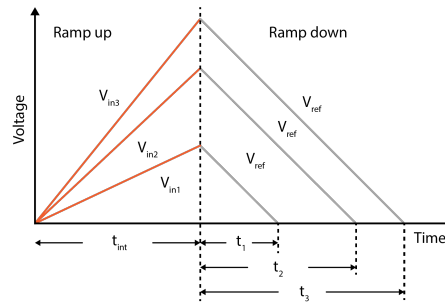


Figure 2.3.2: Operation of the integrating ADC for 3 inputs [27]

approximation ADCs will take an  $N$ -clock-cycle time. As a whole, successive-approximation ADCs are very versatile, providing a moderately high accuracy, low power consumption and low circuit complexity.[9]

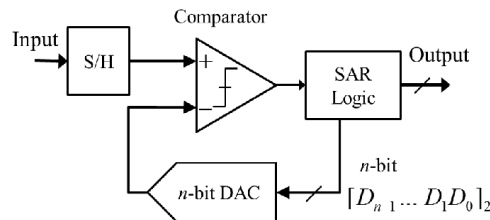


Figure 2.3.3: A D/A converter-based successive-approximation ADC [24]

### 2.3.3 Algorithmic ADCs

Algorithmic ADCs are much the same as successive-approximation ADCs. In place of dividing the reference by 2 in every period, algorithmic ADCs multiply the input voltage by 2 in every cycle while the reference voltage remains constant. Here is a schematic diagram of an algorithmic ADC in Figure 2.3.4. The input voltage ( $V_i$ ) will be sampled first and compared with the reference voltage ( $V_{FS}/2$ ) to generate 2 different results in two different cases. Then the results will be amplified by 2 to generate new inputs, which will be sampled again. The combination of these functions can be realized by a multiplying digital-to-analog converter (MDAC) stage. These operations are repeated in  $N$  clock cycles and one bit is produced in every cycle. This repetition of using the same circuitry in every conversion results in high resolution and relatively low power consumption, however, due to the cyclical conversion the speed is not very fast.

### 2.3.4 Pipelined ADCs

Pipelined ADCs are similar to successive-approximation ADCs and algorithmic ADCs, but there are multiple circuits working on consecutive input samplings at the same time. Pipelined ADCs divide the whole conversion task into  $k$  sequential subtasks as schematically shown in Figure



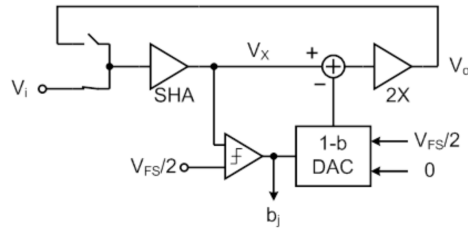


Figure 2.3.4: An algorithmic ADC [7]

2.3.5. Each stage is made up of a single independent analog circuit to execute one subtask.

In the first stage, the input signal ( $V_{in}$ ) is sampled and held. It will also be digitized into  $n_1$  bits and these bits will be converted into an analog voltage by a digital-to-analog converter (DAC). The voltage generated by the DAC is subtracted from the input voltage and the result is further amplified by a residue amplifier to create a residue for the next stage. In the next stage, the incoming residue is regarded as the input signal and a similar sequence of operations are performed while the next sampling starts to be processed in the previous stage. In the last stage, the last few least significant bits (LSB) are resolved and no more residue will be generated since no adjacent stage takes place after the last one. Due to this pipeline technique all of the stages can work concurrently so pipelined ADCs are able to finish one conversion on every clock cycle. Thus, these kind of ADCs can provide a comparatively higher speed versus successive-approximation ADCs and algorithmic ADCs.

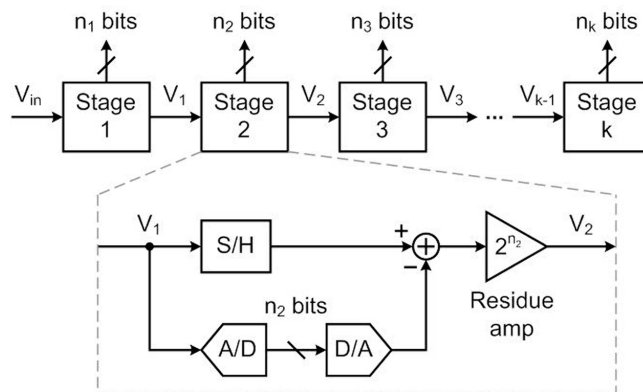


Figure 2.3.5: A schematic diagram of the pipelined ADCs [19]

### 2.3.5 Flash ADCs

Flash ADCs have the fastest speed among all ADCs. Flash ADCs take advantage of a resistor string (voltage divider circuit) with a huge number of comparators connected to different nodes of the resistor string to

compare the input voltage with the voltage at the nodes. A typical diagram of a 3-bit flash ADC is shown in Figure 2.3.6. For an N-bit conversion,  $2^N - 1$  comparators are always required. A priority encoder is used in a flash ADC in order to solve the problem that two or more inputs of encoder are logic high simultaneously. Therefore, in this case, the output code is determined by the highest priority input. Ideally, there should be  $2^N$  input corresponding to the N-bit output, so the remaining input is connected to the logic high with the lowest priority, which means that the output code will be all zeros ( $(00\dots0)_2$ ) if all of the comparator output are logic low. In addition, this ADC also requires the sample and hold circuits to sample and hold the input signal during the conversion since this ADC is a combinatory logic. However, the large number of comparators also gives rise to some drawbacks like high power consumption, limited resolution and large die area.

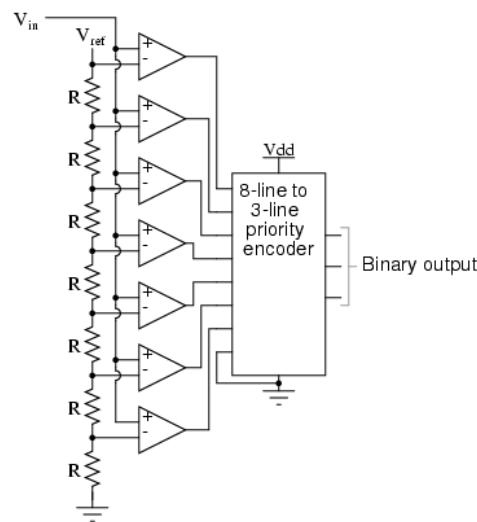


Figure 2.3.6: A 3-bit flash ADC [13]

### 2.3.6 Delta-Sigma ADCs

Delta-sigma ADC is one of the modern advanced ADCs. A basic diagram of a delta-sigma ADC is shown in Figure 2.3.7. A delta-sigma ADC fundamentally consists of a delta-sigma modulator, a digital filter and a decimator. An analog input signal will be first digitized by a delta-sigma modulator into a serial bit-train called sampling frequency. The pulse width is corresponding to the magnitude of the input signal.

The work principle of the 1st order delta-sigma modulator is illustrated in Figure 2.3.8. An input signal will be sent into a difference amplifier together with the output of feedback loop to either add or subtract a constant  $V_{ref}$ , the reference voltage of the 1-bit digital-to-analog converter (DAC). Then output of the difference amplifier is integrated by an integrator which is an averaging over time. Next, the result is further sent into a comparator regarded as an 1-bit ADC to produce an 1-bit output with a feedback loop

through an 1-bit DAC connected to the difference amplifier. The 1-bit output is converted into a high bit word by a digital filter. This high bit word will be finally decimated by a decimator to slow down the data rate.

### Decimation Filter

The purpose of the decimation is to decrease the sample rate of a signal by removing samples from the data stream, realized by a digital low pass filter followed by a decimator. The decimation filter converts the oversampled low-resolution digital signal into a high resolution digital signal. The decimation is usually used to decrease the ADC data rate to reasonable levels for data caption, to maintain high output sampling rate for more flexible frequency planning and to take advantage of decimation filtering for improving spectral performance.

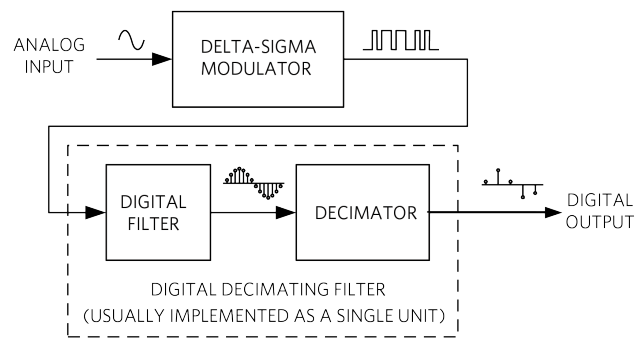


Figure 2.3.7: A basic diagram of a delta-sigma ADC [28]

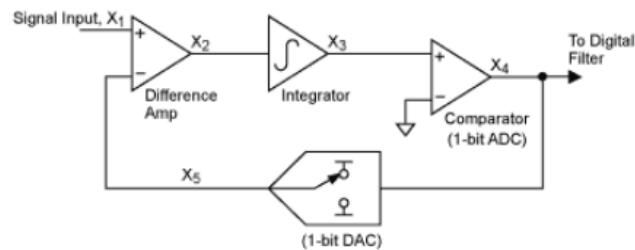


Figure 2.3.8: A simple diagram of a delta-sigma modulator [26]

## 2.4 The Performance Metrics of Analog-to-digital Converters

### 2.4.1 Sampling Rate

In order to convert a continuous analog signal to discrete digital signal, sampling and quantizing the analog signal is required. A fixed time frame

$T_s$  named sampling period is chosen to sample the input signal. The relationship between  $T_s$  and sampling rate  $f_s$  can be expressed by Equation 2.1,

$$f_s = \frac{1}{T_s} \quad (2.1)$$

so it is easy to understand that sampling rate  $f_s$  define the number of samples taken in every second. Additionally, there is always a constraint on the sampling rate  $f_s$ , the so-called Nyquist's theorem that the sampling rate  $f_s$  should be not less than twice of the highest frequency component of the input signal.

### 2.4.2 Resolution

The resolution of an ADC is generally defined by the number of digital outputs the ADC produces to represent the granted range of analog inputs. For example, an N-bit ADC indicates that it can express a maximum of  $2^N$  distinct analog inputs.

#### Effective number of bits (ENOB)

Since the real signal contains noise and real circuits also introduce additional noise and distortion, an N-bit ADC usually provides an actual resolution less than N-bit. Therefore, a term, effective number of bits (ENOB) is introduced to describe the effective resolution afforded practically by the ADC.

### 2.4.3 Transfer Curve

The transfer function for a system illustrates the relationship between the input and the output of the system. In the field of analog-to-digital converters, the transfer function is always demonstrated by a mapping curve consisting of the values of the analog inputs and their digital counterparts. The transfer curve for an ideal ADC is a monotonic linear function. However, due to the defined finite number of the output digital codes for an real ADC, each output code is associated with a certain range of the input analog values. Thus, the ideal transfer function is actually a staircase function. [11, 25]

An example of the ideal transfer curve for an 3-bit ADC is shown in Figure 2.4.1. The staircase function is the actual transfer curve for the perfect 3-bit ADC because of quantization while the straight dash line adopting the middle points of every step width is the ideal transfer curve.

### 2.4.4 Offset and Gain Error

The offset error in an ADC is defined as the difference between the actual transfer curve and the ideal transfer curve at the point where the input value produces zero output value. The offset error is measured in the Least

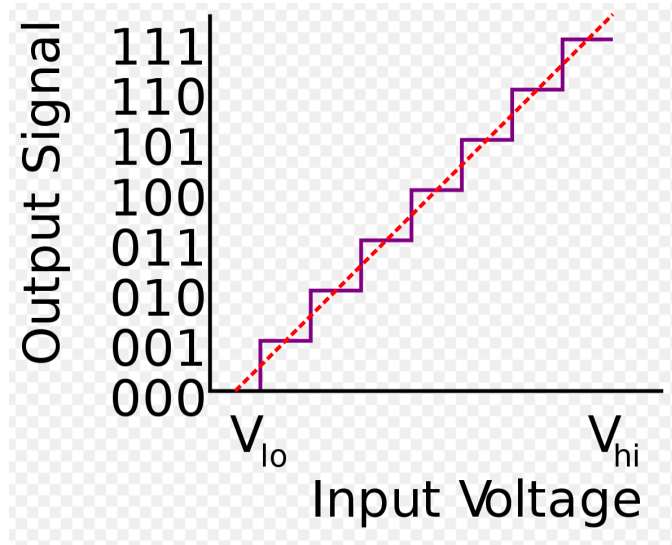


Figure 2.4.1: Ideal transfer curve for an 3-bit ADC [12]

Significant Bit (LSB). It can be driven by Equation 2.2,

$$LSB = \frac{FSR}{2^N} \quad (2.2)$$

where the FSR is the full-scale range of the ADC and the N corresponds to the resolution of the ADC. [5, 9, 18]

With the offset error being reduced to zero, the gain error represents the deviation from the actual transfer curve to the ideal transfer curve at the middle point of the last step of the staircase function, measured in LSB. [5, 9]

In addition, the full-scale error is regarded as the sum of the offset error and the gain error. [9]

### 2.4.5 Differential and Integral Non-linearity

Differential non-linearity (DNL) is a popular measure of performance for analog-to-digital converters. It is a term to describe the difference between the least significant bit (LSB) and the deviation between two analog values corresponding to two adjacent digital numbers. The DNL of each quantization step can be express by Equation 2.3 [5, 9, 12],

$$DNL(i) = \frac{V_{out}(i+1) - V_{out}(i)}{ideal\ LSB\ step\ width} - 1 \quad (2.3)$$

As shown in Figure 2.4.2, this transfer curve has a maximum DNL of +0.5 LSB and a minimum DNL of -0.5 LSB.

Integral non-linearity (INL) is also a commonly used measure of performance for analog-to-digital converters. It is a term to define the difference between the analog value of the midpoint of the quantization

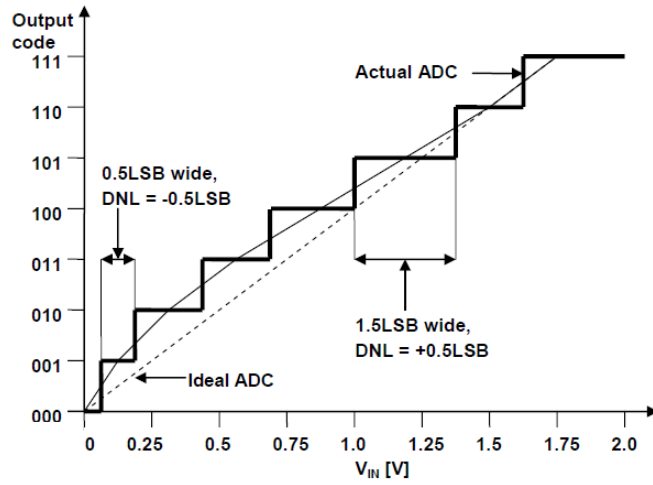


Figure 2.4.2: An example for DNL [5]

steps and the corresponding analog value of the ideal transfer curve. The INL of each quantization step is driven in Equation 2.4 [5, 9, 12],

$$INL(c) = | V_{M,ideal}(c) - V_{M,real}(c) | \quad (2.4)$$

An example for calculating INL is schematically shown in Figure 2.4.3. The transfer curve results in a max INL of +0.75 LSB.

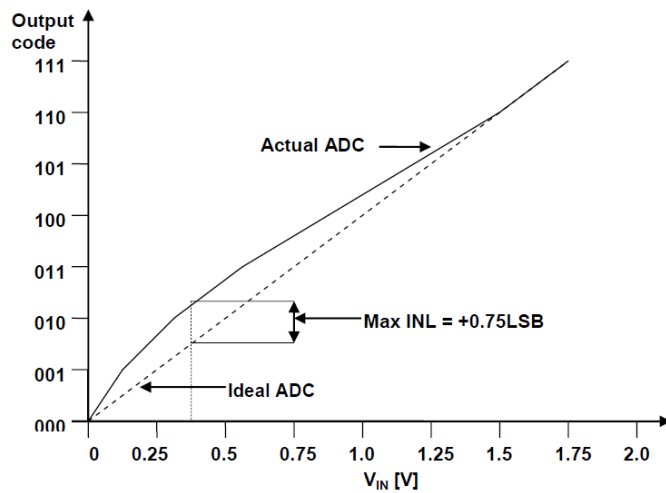


Figure 2.4.3: An example for INL [5]

## 2.5 PVT Variations

It is of vital importance to take into consideration what different corners the chips might face in fabrication. Thus, the PVT variations are introduced.

PVT variations are inter-chip variations caused predominantly by external factors such as the ambient temperature, the supply voltage and the process of the chip fabricating. [20, 21] In the term PVT, the letters P, V and T represent respectively the variations of process, supply voltage and operating temperature.

### **2.5.1 Process Variation**

There are thousands of chips manufactured everyday, on which billions of transistors are packaged. It cannot be expected that all of the transistors should be identical. During the fabrication process of integrated circuits, there has been naturally occurring variance in the attributes of transistors, named process variation. The process variation will result in deviations among transistor sizes throughout a whole chip, leading to different propagation delay all over the chip because small transistors are faster. [20, 21] Additionally, the deviations among transistor sizes can have an impact on the open circuit voltage [17].

### **2.5.2 Supply Voltage Variation**

Almost all of chips require a power supply to provide supply voltage, which can be realized by making use of either DC source or voltage regulator. However, the voltage regulator will not always provide the same voltage and hence the current might change, which consequently leads to the changes of propagation delay. The placements of different cells with respect to their distance from the power supply can also affect the supply voltage because of the parasitic resistance. Since the delay of a cell is determined by the saturation current dependent on the power supply, the power supply affects the propagation delay of a cell. [20, 21]

### **2.5.3 Operating Temperature Variation**

Temperature variation is an unavoidable problem for integrated circuit design. There are 3 dominant factors causing the temperature fluctuation. They are switching, short-circuiting and the leakage power consumption. The switching power consumption, which accounts for the majority of the power consumption, results from the required energy to charge up the parasitic and load capacitances. The short-circuiting power consumption is due to finite falling and rising time. Besides, the sub threshold currents and the reverse biased diodes in a CMOS transistor give rise to the leakage power consumption. As a result of the dissipation of power, the operating temperature rises up so that the electron and hole mobility is influenced. Thus, the propagation delay will change. [20, 21]

## Chapter 3

# Theory and Components

In this thesis, a first order 8-bit frequency-to-digital  $\Sigma\Delta$  modulator (FDSM) ADC is presented. Based on 3DSI technology, the analog devices in this ADC are designed on the top tier while the digital devices on the bottom tier in order to reduce the area of the whole circuit. The first order 8-bit FDSM ADC is composed of a FDSM and an 8-bit ripple counter. The ring current-controlled oscillator (RCCO) of the first order FDSM is the analog device to be implemented with the 65nm process transistors on the top tier. The rising and falling edge detector of the first order FDSM and the 8-bit ripple counter are the digital devices to be implemented with the 28nm process transistors on the bottom tier.

### 3.1 Frequency-to-digital $\Sigma\Delta$ Modulator

Unlike conventional  $\Sigma\Delta$  modulator, which use operational amplifiers and are therefore reliant on a supply voltage sufficiently higher than the MOS threshold voltage, the frequency-to-digital  $\Sigma\Delta$  modulator (FDSM) does not have feedback, thus the maximum amplitude of the input signal is not limited as in feedback-based  $\Sigma\Delta$  converters. And the noise requirements in the internal circuit are not directly related to the usable supply voltage since the input signal is frequency-modulated [30].

The general FDSM consists of an integrator, a phase detector and a differentiator. A block diagram of this type modulator is shown in Figure 3.1.1. The input signal to the FDSM will first be integrated by the integrator. The output of the integrator is a phase signal and will be detected by the phase detector and further compared by the differentiator to produce a 1-bit code as the output of the FDSM [15].

In this thesis, the integrator is implemented with a 3-stage current-controlled ring oscillator which produces the integrated signal of the input current. The phase detector and the differentiator are combined into one block. The integrated signal will be then sent into the block. The block is made up of a 2-input XOR gate and two D flip-flops. It detects the falling and rising edge of the input signal, generating a 1-bit stream whose frequency is double the phase signal. A new block diagram of the 1st-order FDSM is shown in Figure 3.1.2.



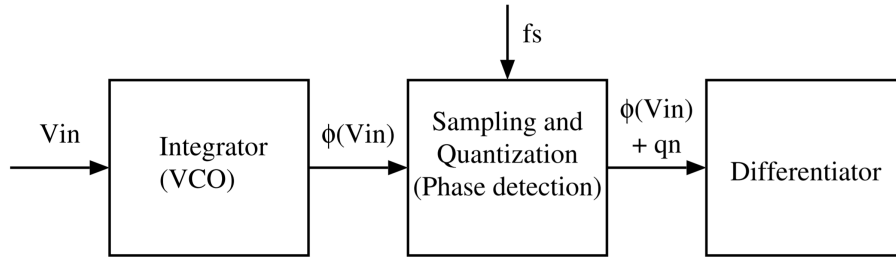


Figure 3.1.1: Block diagram of the FDSM [30]

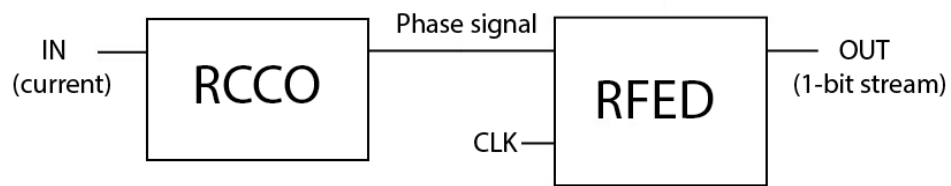


Figure 3.1.2: Schematic of the 1st-order FDSM

## 3.2 Current Starved Inverter

Current starved inverter is an inverter biased by 2 current sources. One is, implemented with a pMOS transistor, connected between the VDD and the source of the pMOS transistor of the inverter, and the other is, implemented with a nMOS transistor connected between the source of the nMOS transistor and the ground. In this way, the inverter can be biased by changing the gate voltages of the two current source transistors. Moreover, it is easier to bias the two current sources by a current mirror circuit and its circuit schematic can be seen in Figure 3.2.1. All of the transistors are 65nm process transistors. The transistors  $M_2$  and  $M_3$  operate as an inverter and the  $M_1$  and  $M_4$  operate as current sources respectively. These current sources will limit the current available to the inverter. The drain current of the transistors  $M_5$  is set by the input control current ( $I_{ctrl}$ ). The currents in the transistor  $M_5$ ,  $M_6$  and  $M_4$  are mirrored and so are the currents in the transistors  $M_7$  and  $M_1$ .

## 3.3 Current Starved Ring Oscillator

### 3.3.1 Ring Oscillator

The definition of the ring oscillator is that an odd number of inverters are connected in series with positive feedback. And in order to obtain sufficient oscillations and gain, the ring oscillator starts with three stages, which means that three inverters are connected in series with a positive feedback. The inverter gives delay to input signal and if the numbers of inverters

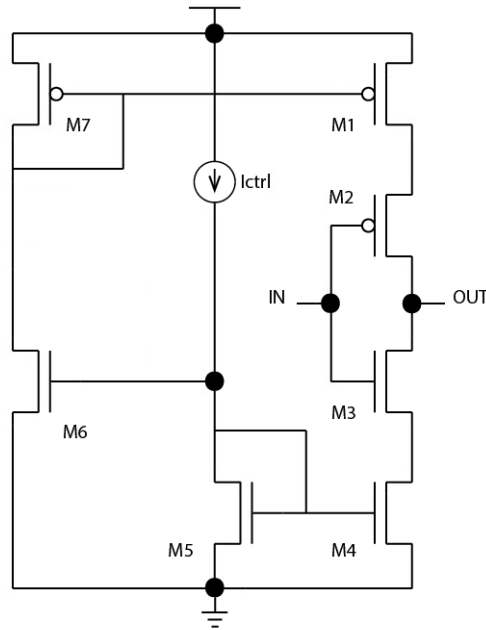


Figure 3.2.1: Schematic of the current starved CMOS inverter

increase then the oscillator frequency will decrease. Therefore, the desired oscillator frequency depends on the number of inverter stages of the ring oscillator.

The frequency of the ring oscillator can be calculated by Equation 3.1,

$$f = \frac{1}{2n\tau} \quad (3.1)$$

where the  $n$  is the number of inverters and the  $\tau$  is the time delay of a single inverter. [29]

### 3.3.2 Current Starved RCCO

In the current starved ring oscillator, we control the amount of current available to charge or discharge the capacitive load of each stage in order to control the delay.

In Figure 3.3.1, the schematic of a three-stage current starved ring current-controlled oscillator (RCCO) is shown. All of the transistors are the 65nm process transistor. The ring oscillator is current-controlled because the input of the 1st order 8-bit FDSM ADC is a current. Such ADC can be applied in the prototype of a novel fixed-bias multi-Needle Langmuir Probe system designed by Bekkeng Tore Andre [8]. As illustrated in the current starved inverter, the control current  $I_{ctrl}$  modulates the current of the pull-down and pull-up network by the technique of current mirror. The current available to charge or discharge the load capacitances is controlled by these

Parameter	In load and decoupling inverters	Others
$W_p/L_p(\text{nm})$	200/70	240/268
$W_n/L_n(\text{nm})$	100/70	120/268

Table 3.3.1: Transistor Parameter Table of RCCO

current source transistors.

A large  $I_{ctrl}$  value will allow a large current to flow through the inverter, leading to small delay. The frequency range and linearity of the RCCO are regulated by the variation of ( $I_{ctrl}$ ). The slower voltage swing of the RCCO brings about a longer rising/falling edge, which might be a major short-coming when bias current is quite small. [23]

In addition, the output load capacitance of each stage can be much different especially for the last stage, thus, as is shown in Figure 3.3.1, the first two stages are loaded by a inverter respectively and a inverter as decoupling is added to the output of RCCO. The reason for using an inverter instead of an explicit capacitor is that there is no capacitor available in the top tier. The parameters of the transistors in RCCO is shown in Table 3.3.1.

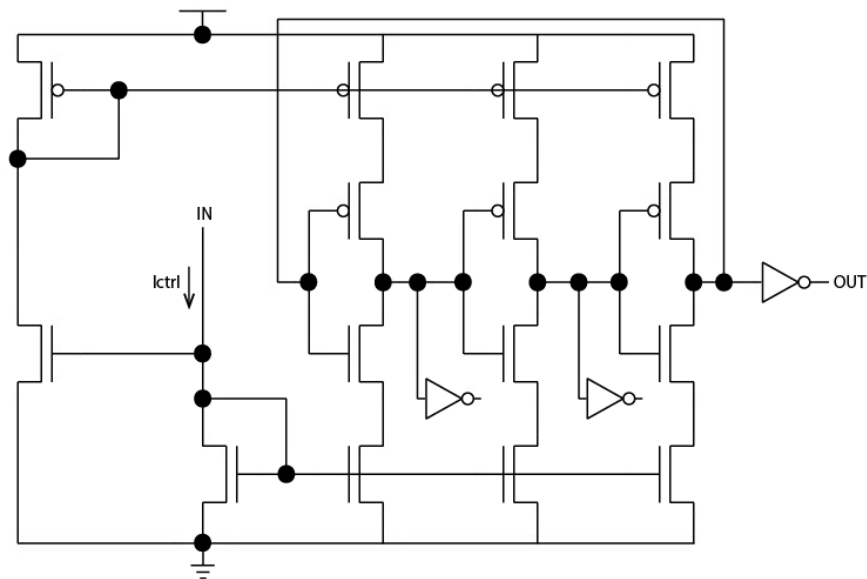


Figure 3.3.1: Schematic of the three-stage RCCO

### 3.4 D Flip-flop

The D flip-flop is a memory circuit which captures the value of the D-input at a definite portion of the clock cycle (such as the rising edge of the clock).

The schematic of a D flip-flop is in Figure 3.4.1. All of the transistors are the 28nm process transistor. This D flip-flop adopts 14 transistors. The transistors  $M_1$  and  $M_3$  are nMOS transistors while the transistors  $M_2$  and  $M_4$  are pMOS transistors. All inverters are made up of one nMOS transistor and one pMOS transistor.

The inverter  $I_5$  is used to generate the inverted clock signal  $clk\_non$  and the inverter  $I_6$  is utilized to generate the delayed clock signal  $clk\_d$ . When the delayed clock signal  $clk\_d$  is logic low, the transistor  $M_1$  is on to let input signal pass while the transistor  $M_2$  is off. The two inverters  $I_1$  and  $I_2$  work as delay components to delay the input signal. The transistor  $M_3$  is off to stop the current input signal from the input node of inverter  $I_3$ . The transistor  $M_4$  is on so that it becomes a feedback loop to constantly generate the previous input signal for output together with the two delay inverters  $I_3$  and  $I_4$ . When  $clk\_d$  is logic high, the transistor  $M_1$  is off to stop the current input signal from the input node of the inverter  $I_1$ . The transistor  $M_2$  is on so that it becomes a feedback loop to constantly generate the previous input signal together with the two delay inverters  $I_1$  and  $I_2$ . The transistor  $M_3$  is on to let the previous input signal pass through the two delay inverters  $I_3$  and  $I_4$  for the output while the transistor  $M_4$  is off.

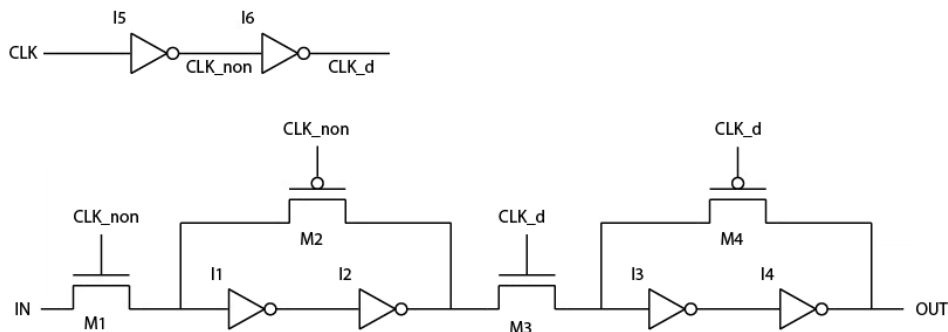


Figure 3.4.1: Schematic of the D flip-flop without a asynchronous reset

### 3.4.1 D Flip-flop with an Asynchronous Reset

An asynchronous reset should make sure that the output of the D flip-flop will keep logic low while the asynchronous reset is active.

Thus, in the circuit shown in Figure 3.4.1, it is necessary to clear the left and right loops once the asynchronous reset signal is high. The left loop is made up of the transistor  $M_1$  while the two inverters  $I_1$  and  $I_2$  and the right loop consists of the transistor  $M_4$  and the two inverters  $I_3$  and  $I_4$ . In order to clear left and right loops, a logic low signal must be constantly forced into both the two loops. This can be realized by applying an AND gate between the transistor  $M_1$  and the inverter  $I_1$  and between the transistor

$M_3$  and the inverter  $I_3$  respectively. Once the asynchronous reset signal is active, a logic low signal will be sent into the other inputs of the two AND gates to steadily force a logic low output of the two AND gates to feed up the inverters  $I_1$  and  $I_3$ .

A D flip-flop with an asynchronous reset is shown in Figure 3.4.2. All of the transistors are the 28nm process transistor. The asynchronous reset  $arst$  is an active high reset in this case. The inverter  $I_5$  is used to generate the inverted clock signal  $clk\_non$  and the inverter  $I_6$  is utilized to generate the delayed clock signal  $clk\_d$ . The inverter  $I_8$  is to generate the inverted asynchronous reset signal  $arst\_non$  so that an active high reset for the D flip-flop is realized. In addition, since an AND gate followed by an inverter is equivalent to a NAND gate, instead of adding the two AND gates before the two inverters, two NAND gates  $N_1$  and  $N_2$  are applied to simplify the circuit. The inverted asynchronous reset signal  $arst\_non$  acts as the other input of the two NAND gates to clear the left and right loops when the D flip-flop is reset. In addition, inverter  $I_7$  is added to generate the inverted output signal.

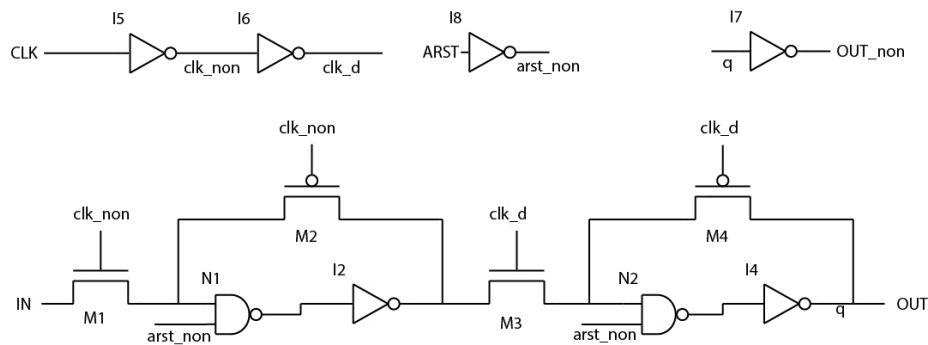


Figure 3.4.2: Schematic of the D flip-flop with an asynchronous reset

### 3.5 T Flip-flop

T flip-flop works as a toggle switch. If the input T is logic high, the T flip-flop changes the state in every rising or falling edge of the clock input. If the input T is logic low, the T flip-flop holds the previous state. So the T flip-flop can be easily implemented by a NOR gate and a T flip-flop. A schematic diagram of a T flip-flop with an asynchronous reset is shown in Figure 3.5.1.

### 3.6 XOR Gate

XOR gate is a digital gate that gives a logic high output when the number of true inputs (logic high) is odd. In Figure 3.6.1, the schematic diagram of a 2-input XOR gate implemented with 12 CMOS transistors can be seen. All

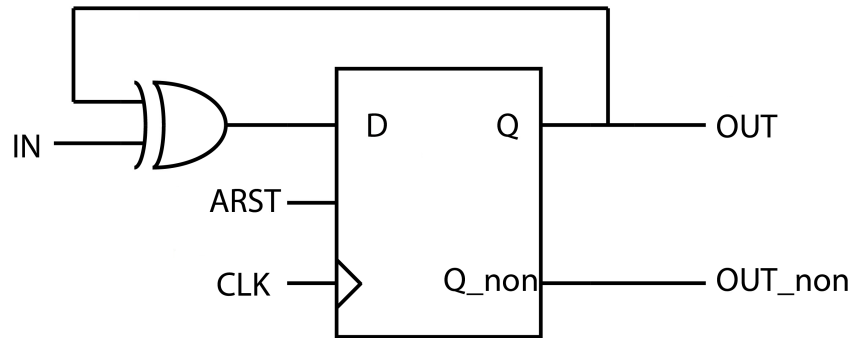


Figure 3.5.1: Schematic of a T flip-flop with an asynchronous reset

of the transistors are the 28nm process transistor. As it shows, two inverters are utilized to generate the inverted input signals.

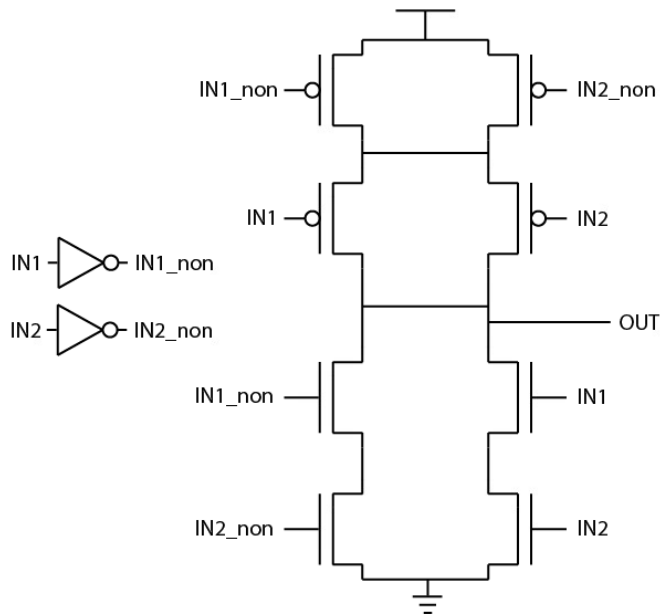


Figure 3.6.1: Schematic of a 2-input XOR gate

### 3.6.1 NAND Gate

NAND gate is a digital gate that gives a logic low output when all of the inputs are logic high. In Figure 3.6.2, the schematic diagram of a 2-input NAND gate implemented with 4 CMOS transistors can be seen. All of the transistors are the 28nm process transistor.

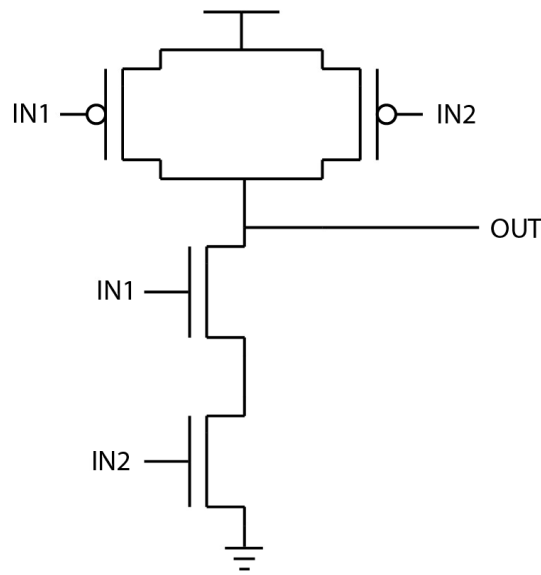


Figure 3.6.2: Schematic of a 2-input NAND gate

### 3.7 Rising and Falling Edge Detector

The block named rising and falling edge detector (RFED) composed of the phase detector and the differentiator is schematically shown in Figure 3.7.1. All of the transistors are the 28nm process transistor. The parameters of the transistors in RFED is shown in Table 3.7.1. The RFED consists of two D flip-flops and a 2-input XOR gate. The input signal of the RFED is sampled and quantized by the first D flip-flop, resulting a 1-bit stream output signal. Then a signal differentiation is implemented with the second D flip-flop and the 2-input XOR gate.

To be specific, the first D flip-flop delays the input signal for one clock cycle and the second D flip-flop further delays the input signal for one more clock cycle. And the outputs of the two D flip-flops will be sent into a 2-input XOR gate for comparison. In other words, the RFED makes a comparison between the current signal level and the signal level one clock cycle before. Thus, after every rising or falling edge of the signal, there will be a pulse occurring in the output bit-stream with the pulse width equal to one clock cycle. As a result, the period of the phase signal is quantized into the amount of clock period. Moreover, the frequency for the output signal of the RFED is approximately double that for the input signal, which increases the resolution.

In addition, it is worth noticing that the clock frequency  $f_{clk}$  is actually the oversampling frequency for the input signal and need to be much higher than double the maximum input frequency  $f_{max}$ . If the  $f_{clk}$  is just twice as much as the  $f_{max}$ , the output signal of the RFED will remain logic high all

Parameter	All
$W_p/L_p(\text{nm})$	160/30
$W_n/L_n(\text{nm})$	80/30

Table 3.7.1: Transistor Parameter Table of RFED

the time once the RFED detects a rising or falling edge of the  $f_{max}$ .

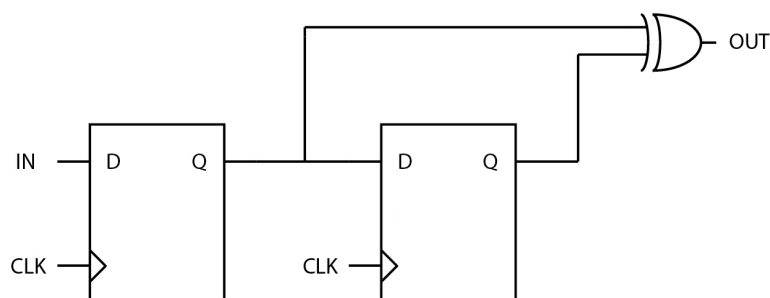


Figure 3.7.1: Schematic diagram for the RFED

### 3.8 8-bit Ripple Counter

In order to convert the 1-bit stream output of the rising and falling edge detector to an 8-bit number, an 8-bit ripple counter is required. The ripple counter is a type of the Asynchronous counter. The "ripple" means that the clock pulse ripples through all of the subsequent D flip-flops, therefore, only the first D flip-flop is clocked with an external clk. The number of unique states of an n-bit ripple counter is  $2^n$  and n D flip-flops are demanded to form the n-bit ripple counter. The ripple counter takes advantage of the toggle mode of flip-flops. Thus, it is easy to build the ripple counter with T flip-flops. A schematic diagram of an 8-bit ripple counter is shown in Figure 3.8.1. All of the transistors are the 28nm process transistor. The parameters of transistors used in the counter is shown in Table 3.8.1. The first T flip-flop is clocked by an external input signal. The input of each T flip-flop is connected to VDD for the toggle mode. The inverted output of each T flip-flop becomes the clock signal for the subsequent T flip-flop while the non-inverted output of each T flip-flop becomes the 8-bit number. Thus, this ripple counter has a rising edge toggle, which means it counters for every rising edge of the input signal. [4] [3]



	All
$W_p/L_p(\text{nm})$	160/30
$W_n/L_n(\text{nm})$	80/30

Table 3.8.1: Transistor Parameter Table of the 8-bit ripple counter

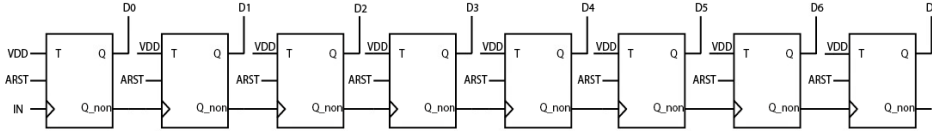


Figure 3.8.1: Schematic diagram for the 8-bit ripple counter

### 3.9 Operating Principle of the 1st Order 8-bit FDSM ADC

In Figure 3.9.1, a schematic diagram of the 1st order FDSM ADC is illustrated. First, the input current is sent into RCCO where the input current is integrated into a phase signal. Second, the phase signal goes into a rising and falling edge detector which implements the sampling, quantization and differentiation. It results in a 1-bit stream that contains the information about the phase signal. The frequency for the 1-bit stream is actually double that for the phase signal. The clock frequency to the D flip-flop should be much higher than the double of the frequency of the phase signal. Third, in order to convert the 1-bit stream to an 8-bit stream, an 8-bit ripple counter is proposed. The 8-bit counter is controlled by an asynchronous reset signal ARST. To determine the ARST, it is important to know that there must be  $2^8 = 256$  transitions after an reset pulse occurring in the beginning since the 8-bit ripple counter need to count up to  $(11111111)_2$  for the highest frequency of the 1-bit stream. Thus, the transition period is defined by the period of the highest frequency of the 1-bit stream which is double the highest frequency of the phase signal. Due to the rising edge toggle of the counter, the transition period starts from the beginning of the pulse to the beginning of the subsequent pulse. And the pulse width plus 256 transition periods defines the sampling period of the 1st order 8-bit FDSM ADC.

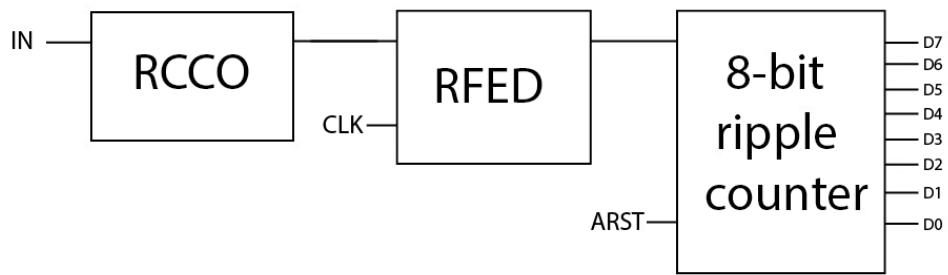


Figure 3.9.1: Schematic diagram for the 1st order 8-bit FDSM ADC

## Chapter 4

# Results and Discussion

### 4.1 Input-output(IO) Relationship for the 3-stage Current-controlled Ring Oscillator

First and foremost, the input-output(IO) relationship for 3-stage current-controlled ring oscillator (RCCO) needs to be ascertained because it helps to determine the input range of the first order FDSM ADC. After testing, the input range is determined to be approximately [50 pA, 60 uA] and the corresponding output range is [16.7 kHz, 807.75 MHz]. The IO transfer curve is shown in Figure 4.1.1. It can be certain that there will be no oscillation if the input current is lower than 50 pA while the FDSM will go into saturation if the input current exceeds 60 uA. Since the linearity of the FDSM ADC predominantly depends on the linearity of the RCCO, the range [0, 102.656 nA] is chosen because of the relatively high linearity and the corresponding output range is [0, 22.12 MHz]. The corresponding part of IO transfer curve is shown in Figure 4.1.2.

### 4.2 Transfer Curve for the 1st Order 8-bit FDSM ADC

The full-scale range (FSR) of the 1st order 8-bit FDSM ADC is [0, 102.52 nA] as illustrated in Section 4.1. The Least Significant Bit in current  $I_{LSB}$  can be driven by Equation 2.2 and it is approximately equal to 0.400 nA. Since the maximum frequency of the RCCO output is  $f_{max}=22.12$  MHz, as discussed in Section 3.7, the clock frequency  $f_{clk}$  must be much higher than  $2f_{max}=44.24$  MHz. Accordingly, the  $f_{clk}$  chosen is 100 MHz. The transition period  $T_{2f_{max}}$  referred to in Section 3.9 can be driven by Equation 4.1

$$T_{2f_{max}} = \frac{1}{2f_{max}} = \frac{1}{44.24 \text{ MHz}} \approx 22.6\text{ns} \quad (4.1)$$

The asynchronous reset signal ARST is designed to be a periodic signal. In each period, ARST is logic high for one transition period first. Then it goes to logic low and lasts for 256 transition periods. Thus, the sampling period  $T_s$  for the 1st order 8-bit FDSM ADC is  $22.6 \text{ ns} * (1 + 256) = 5.8082 \mu\text{s}$  and the corresponding sampling rate  $f_s$  is approximately equal to 172.17 kHz.

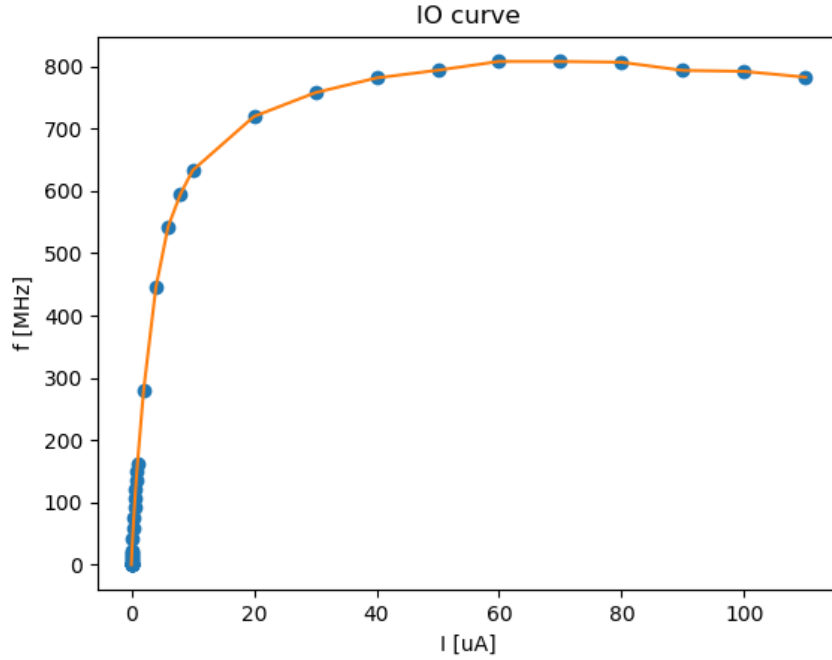


Figure 4.1.1: The IO curve of the FDSM

The transfer curve for an ADC is very helpful to characterize the performance of the ADC. However, due to the long time duration of the simulation, it is impossible to obtain the transfer curve for the full-scale range at high resolution, but for reference, a low resolution plot is shown in Figure 4.2.1. Therefore, only a section of the transfer curve is focused with relatively high resolution. The chosen section is [49 nA, 51 nA], and its corresponding plot shown in Figure 4.2.2. To get the staircase plot, some test points are required. So a bigger step size, 0.05 nA, is chosen at the beginning. Then, between every two adjacent stairs, a smaller step size, 0.002 nA, is chosen. In the input range [49 nA, 51 nA], the minimum differential non-linearity  $DNL_{min} \approx -0.03$  LSB and the maximum differential non-linearity  $DNL_{max} \approx -0.02$  LSB. Apparently, the 1st order FDSM ADC has a relatively small differential non-linearity in the input range [49 nA, 51 nA]. In addition, by simulation, some test points near the start or the end of the FSR are obtained. As a result, the range of the input generating the highest output number  $(11111111)_2 = 255$  is found to be approximately [102.486 nA, 102.52 nA] while the range of the input producing the lowest output number  $(00000000)_2 = 0$  is approximately [0, 0.092 nA]. The two ranges are shorter than  $1I_{LSB}$ . So the 1st order 8-bit FDSM ADC has offset gain and may have gain error also. By calculating the standard deviation  $RMS$  in the section [49 nA, 51 nA] chosen an attempt to estimate the ENOB is

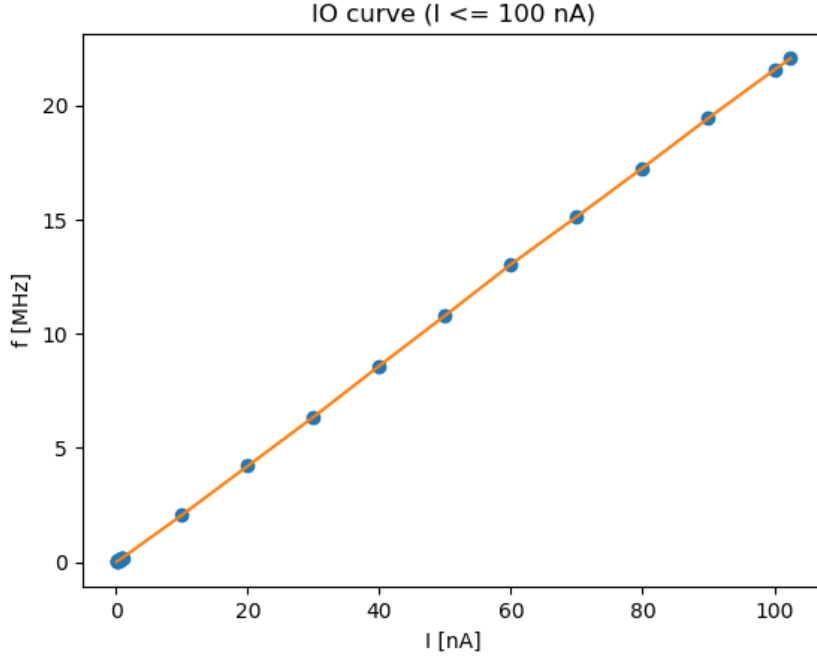


Figure 4.1.2: The IO curve from 50p to 102.656 nA

made. The RMS in this case is defined by Equation 4.2,

$$RMS = \sqrt{\frac{1}{n} \sum_{i=1}^n (D_{Ideal} - D_{Staircase})^2 |_{when I_i}} \quad (4.2)$$

where the D is the digital number, the I is the current value. Since the test points obtained are not homogeneous, more points are filled by reasoning so that there are 1001 points between 49 nA and 51 nA with the step size 0.002 nA. The corresponding plot is shown in Figure 4.2.1. The RMS for the ideal staircase curve is approximately equal to 0.289 while the RMS for the real staircase curve is approximately equal to 0.570. The RMS for the real staircase is less than 1 in the section. If the standard deviation of the FSR remains around 0.570, the ENOB of the 1st order 8-bit FDSM ADC can be estimated to be between 7-bit and 8-bit. With the 102.52 nA input, the power consumption calculated is approximately equal to 1.161  $\mu$ W. So the maximum power consumption for 8-bit conversion is 1.161  $\mu$ W.

### 4.3 Metastability in RCCO

When starting a simulation on RCCO, it takes time for the RCCO to oscillate at a stable frequency. The simulation of the RCCO output with 10 nA input is shown in Figure 4.3.1. It can be seen that the metastability problem. The reason for this is that the signals between every two stages of the RCCO are at an unknown state. There are 3 stable states which

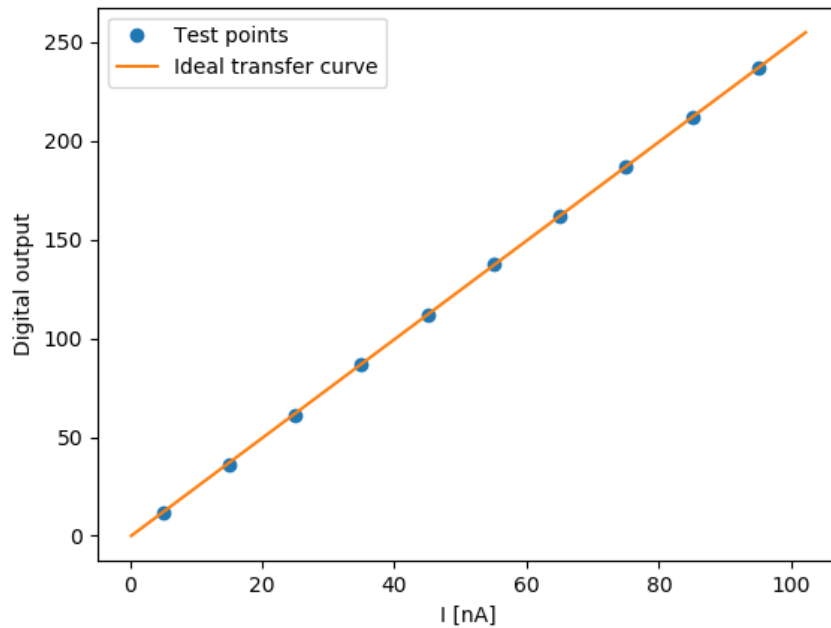


Figure 4.2.1: The full transfer curve for the 1st order 8-bit FDSM ADC at low resolution.

are 0,  $V_{DD}/2$  and  $V_{DD}$ . 0 and  $V_{DD}$  are attractive fixed points while the  $V_{DD}/2$  is repulsive fixed points. An unknown state will be attracted to the attractive fixed points if the unknown state is near the attractive fixed points and will be repulsed from the repulsive fixed points if the unknown state is near the repulsive fixed points. These processes take time. If the metastability problem appears during the sampling period of the 1st order 8-bit FDSM ADC, an incorrect digital output will take place. To solve this problem, an initial condition operation can be applied, for example, the input signal of the first stage in RCCO can be forced to be 0 in the beginning. Another solution is to discard the result for the first sampling of the FDSM ADC.

#### 4.4 Deviation caused by Quantization

The period of the output signal of the RCCO is quantized into the amount of the clock period. In other words, the frequency of the output 1-bit stream to the FDSM is not accurately double the frequency of the output phase signal for the RCCO. In Figure 4.4.1, a timing diagram for the FDSM with 100 nA input current is shown. It can be observed that the distance between every two pulses in the RCCO output bit-stream is non-uniform. Therefore, it may occur that the number of the pulses collected by one sampling period will increase or decrease by one every time. This might give  $\pm 1$  LSB deviation to the output number. A possible solution to avoid this deviation

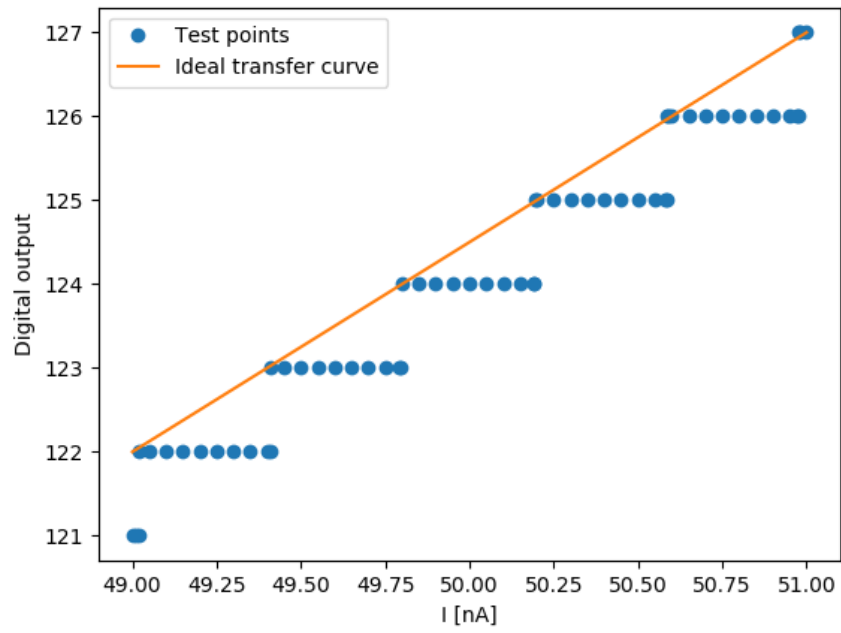


Figure 4.2.2: The transfer curve for the 1st order 8-bit FDSM ADC

is to increase the clock frequency  $f_{clk}$  even more. However, this will result in more power consumption.

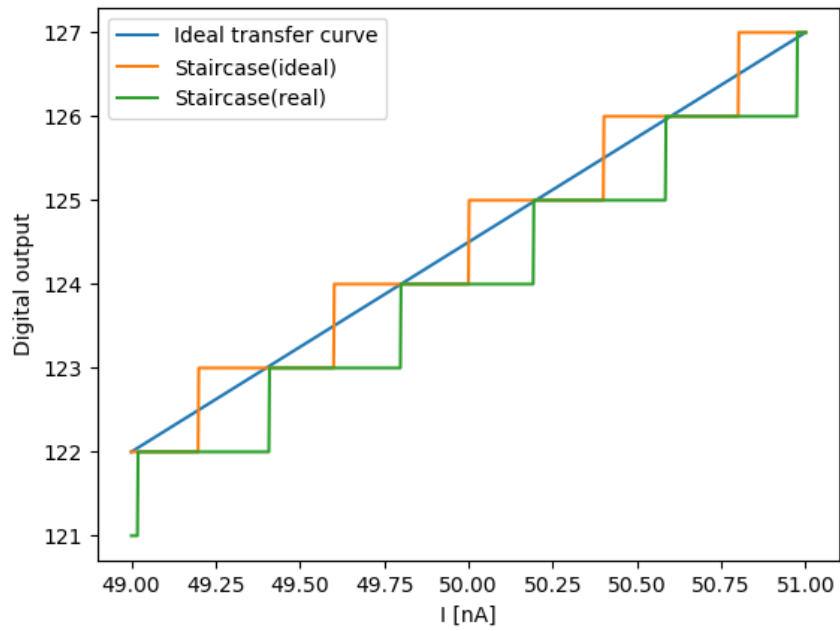


Figure 4.2.3: The transfer curve for the 1st order 8-bit FDSM ADC with points filled

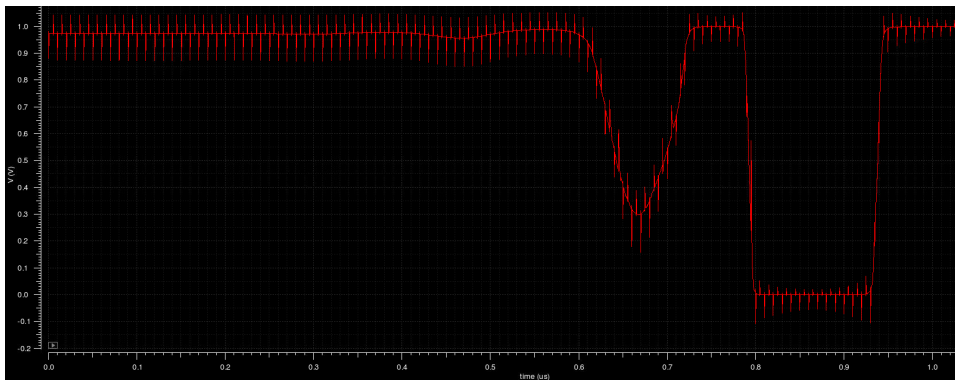


Figure 4.3.1: Metastability problem



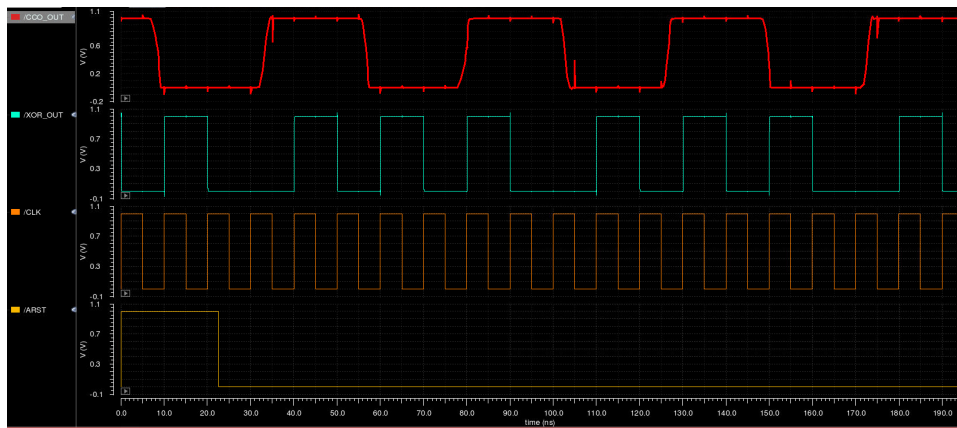


Figure 4.4.1: The timing diagram of the FDSM with 100 nA input current

## Chapter 5

# Conclusions and Future Work

In this thesis, the theory of the frequency-to-digital  $\Sigma\Delta$  modulator ADC has been presented. A novel 3DSI implementation of the 1st order 8-bit FDSM ADC has been performed. The 1st order 8-bit FDSM ADC is composed of a 3-stage RCCO, a RFED and an 8-bit ripple counter. The input current is firstly integrated into a phase signal, and then the phase signal is sampled, quantized and differentiated by the RFED which generates a 1-bit stream containing the information about the frequency for the phase signal. Finally, the 1-bit stream is converted into an 8-bit digital number by the 8-bit ripple counter. The 1st order 8-bit FDSM ADC uses a 1.0V supply voltage and the maximum power consumption 1.161  $\mu\text{W}$  for 8-bit resolution. The FSR is [0 nA, 102.52nA]. The clock frequency is 100 MHz and the sampling frequency is 172.17 kHz. The specification of the 1st order FDSM ADC is shown in Table 5.0.1.

According to the simulation, it is deduced that the 1st order 8-bit FDSM ADC can have a relatively good linearity. However, since the linearity of this ADC dominantly depends on the linearity of the 1st order FDSM, the FSR of this ADC is small. A small FSR also limits the sampling frequency, so the speed of this ADC is slow. A high clock frequency is required in this ADC, which can give rise to more power consumption. The metastability problem can be solved by initial condition operation or discarding the result of the first sampling of the FDSM ADC. In addition, since this ADC does not need a DAC for feedback, the circuit complexity is reduced. However, due to lone time duration of simulation, only the DC performance is

Property	Value
FSR	[0 nA,102.52 nA]
Resolution	8 bits
Clock frequency	100 MHz
Sampling frequency	172.17 kHz
Supply voltage	1.0 V
Power consumption	$\leq 1.161 \mu\text{W}$

Table 5.0.1: Specification of the 1st order FDSM ADC

investigated.

The integrated circuit has been implemented with 3DSI PDK. All of the analog devices are implemented in the top tier with the the 65nm process transistor while all of the digital devices are implemented in the bottom tier with the 28nm process transistor. Therefore, compared with the conventional 2D version, it can be deduced that the 3D version of the 1st order 8-bit FDSM ADC should have a smaller area. And the interconnecting wiring is reduced, resulting in less parasitic capacitance and resistance. Additionally, since the analog domain is insulated from the digital domain by a ground plane between the tiers, the cross-talk noise in the 3D version can be much smaller.

Since the 1st-order FDSM ADC is only investigated in schematic level, it is also worth investigating the performance of the ADC in layout level in the future work so that the influence by the parasitic capacitance and resistance can be investigated and the actual area of the ADC can be calculated. Besides, to design the ADC in 2D version, for example, to design all of the devices in the top tier with the 65nm process transistor or in the bottom tier with the 28nm process transistor and then to make a comparison between 2D version and 3D version with respect to the performance are significant as well.

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