electronics

MDPI

Article

Memristive and Memory Impedance Behavior in a Photo-Annealed ZnO–rGO Thin-Film Device

Gian Carlo Cardarilli [1], Gaurav Mani Khanal [1,*], Luca Di Nunzio [1], Marco Re [1], Rocco Fazzolari [1] and Raj Kumar [2]

[1] Laboratory of Microelectronics and VLSI Architectures For DSP, Department of Electronics Engineering, University of Rome "Tor Vergata", Via Del Politechnico 1, 00133 Rome, Italy; g.cardarilli@uniroma2.it (G.C.); di.nunzio@ing.uniroma2.it (L.D.N.); marco.re@uniroma2.it (M.R.); rocco.fazzolari@uniroma2.it (R.F.)

[2] Department of Physics, Centre for Materials Science and Nanotechnology, Faculty of Mathematical and Natural Sciences, University of Oslo, 0316 Oslo, Norway; r.kumar001@unibs.it

* Correspondence: Gauravmani.khanal@uniroma2.it; Tel.: +39-9175-7921-1514

Received: 6 December 2019; Accepted: 5 February 2020; Published: 7 February 2020

Abstract: An oxygen-rich ZnO-reduced graphene oxide (rGO) thin film was synthesized using a photo-annealing technique from zinc precursor (ZnO)–graphene oxide (GO) sol–gel solution. X-ray diffraction (XRD) results show a clear characteristic peak corresponding to rGO. The scanning electron microscope (SEM) image of the prepared thin film shows an evenly distributed wrinkled surface structure. Transition Metal Oxide (TMO)-based memristive devices are nominees for beyond CMOS Non-Volatile Memory (NVRAM) devices. The two-terminal Metal–TMO (Insulator)–Metal (MIM) memristive device is fabricated using a synthesized ZnO–rGO as an active layer on fluorine-doped tin oxide (FTO)-coated glass substrate. Aluminum (Al) is deposited as a top metal contact on the ZnO–rGO active layer to complete the device. Photo annealing was used to reduce the GO to rGO to make the proposed method suitable for fabricating ZnO–rGO thin-film devices on flexible substrates. The electrical characterization of the Al–ZnO–rGO–FTO device confirms the coexistence of memristive and memimpedance characteristics. The coexistence of memory resistance and memory impedance in the same device could be valuable for developing novel programmable analog filters and self-resonating circuits and systems.

Keywords: memristive device; resistive switching; ZnO–rGO memristor; memory impedance

1. Introduction

Metal–oxide-based memristive devices have attracted much attention due to their ability to process and store information with minimum power requirements, and for this reason, soon, they could replace transistor-based flash memory [1–7]. Memristors can be integrated into a highly dense crossbar network array to implement the interconnection of a high number of CMOS neurons emulating spike-based learning [8–15].

A Memory Resistor, or Memristor, is a two-terminal device theoretically postulated by L. Chua in 1971 [16]. Memristors are variable resistors with the ability to store/memorize their previous resistive value. The resistance of a memristor, known as Memristance, can be controlled by varying the polarity and/or magnitude of the input (voltage or current). Correspondingly, we obtain a voltage or current-controlled memristor. The most important characteristic of the memristor is the pinched hysteresis loop in its current–voltage (I–V) curve, when the device is connected to a varying input voltage or current, pinched hysteresis makes a memristor a passive and fourth fundamental circuit element besides the resistor, capacitor, and inductor [9,10,17].

The voltage-controlled memristor is described by Equations (1) and (2) [18]:

$$I_{MR} = M_G(w, V_{MR}, t)V_{MR} \tag{1}$$

$$w = f(w, V_{MR}, t) \tag{2}$$

where I_{MR} and V_{MR} are the input current and voltage to the memristor, respectively. M_G and M_R represent the memconductance and the memristance, respectively. Finally, w is a parameter that takes into account the internal structure of the memristor. Similarly, the current-controlled Memristor is described by Equations (3) and (4) [18].

$$V_{MR} = M_R(w, I_{MR}, t)I_{MR} \tag{3}$$

$$w = f(w, I_{MR}, t) \tag{4}$$

Recently, many reports [19–24] have experimentally demonstrated that memristive, memcapacitive, and meminductive behavior coexist in the same single nano-sized memristive device. Published reports have shown and argued that it is possible to achieve memristive and memimpedance behavior on a single nano-device by varying the frequency of the input signal or by varying the input sweep rate (V/s).

The memristor is a Metal–Insulator–Metal (MIM) structure device, as shown in Figure 1. A thin layer of insulator or semiconductor material (also called active layer or storage layer) is sandwiched between the two metal electrodes. Memristive devices with a layer thickness of few nanometers and low operating voltages with switching energy of few femtojoule (fJ) have been successfully implemented [25,26].

Among the available materials for memristor and memristive devices, zinc oxide (ZnO) and its composite has some unique advantages: nontoxic and easy synthesis, high ion mobility, excellent resistance switching property, and relatively low set and reset voltages. In recent years, ZnO and its composites have been extensively used to fabricate memristive devices [19,22,27,28]. In previous works, the high-temperature thermal annealing process was used for creating vacancies within the ZnO thin film [29–31]. This approach limits the applications of ZnO and ZnO composite thin film for the development of ReRAM (Resistive RAM) and flexible memristive devices.

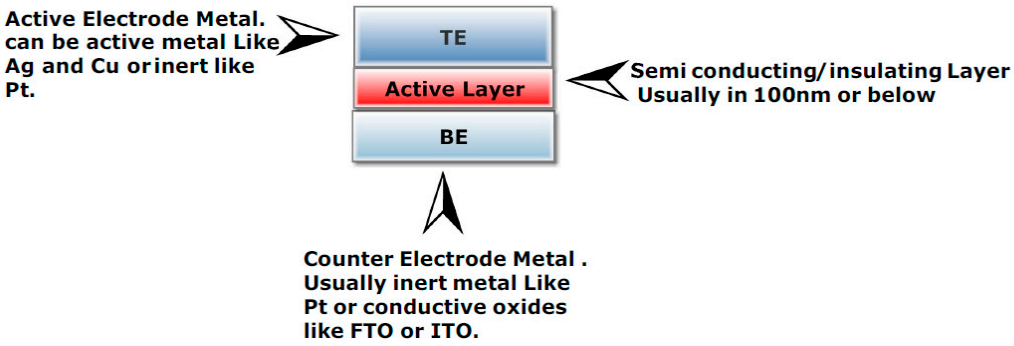

Figure 1. Memristor device structure. TE, top electrode; BE, bottom electrode; FTO, fluorine-doped tin oxide; ITO, Indium-doped tin oxide.

In this work, we propose a low-temperature, low-cost, facile- and electro-forming-free memristive device based on zinc precursor (ZnO)–reduced graphene oxide (rGO) composite thin film sandwiched between aluminum (Al) as a top electrode (TE) and fluorine-doped tin oxide (FTO) as a bottom electrode (BE).

The experimental results show the presence of memimpedance behavior in the ZnO–rGO thin film memristive device. Memreristive and memimpedance behavior can be simultaneously controlled

by varying the input stimulus sweep rate. These results could open a way for the fabrication of new low-cost nano-devices that can be used as memristor, as well as memimpedance, devices for developing adaptive analogue circuits applications.

2. Materials and Methods

The thin film used for this work is the same as described in [32,33]. The required chemical zinc acetate dehydrate, ethanol, and ethanolamine were obtained from Sigma Aldrich. Graphene oxide powder (1 gm) was received from Abalonyx (Norway). All of the reagents were of analytical grade and used as such. Zinc acetate dehydrate and ethanolamine in equal fraction were added to ethanol and stirred at 60 °C for 30 min. Graphene oxide (GO) (0.1 mg/ml) was added to the as-prepared solution and kept under constant stirring for 24 h. ZnO sol–gel solution was prepared in a similar way, without the addition of graphene oxide.

The dip-coating technique was used for the deposition of the as prepared ZnO–rGO composite onto the FTO-coated glass substrate. The thickness and uniformity of the thin film were supervised by controlling the dipping speed and repetition of the coating process. In our work, we repeated the coating process twice to obtain a uniform thin film of about 80 nm. After the deposition process, the devices were exposed to deep UV irradiation with the main line at 254 nm (90%) and secondary line at 185 nm (10%) for about 5 h.

A Scanning Electron Microscopic image of the prepared ZnO-rGO thin film is shown in Figure 2. The photo-annealed ZnO–rGO composite thin film shows a wrinkled surface structure evenly distributed in the entire film surface area. The formation of wrinkles in the composite film is suggested due to the removal of epoxy and hydroxyl groups during the annealing process [34–36].

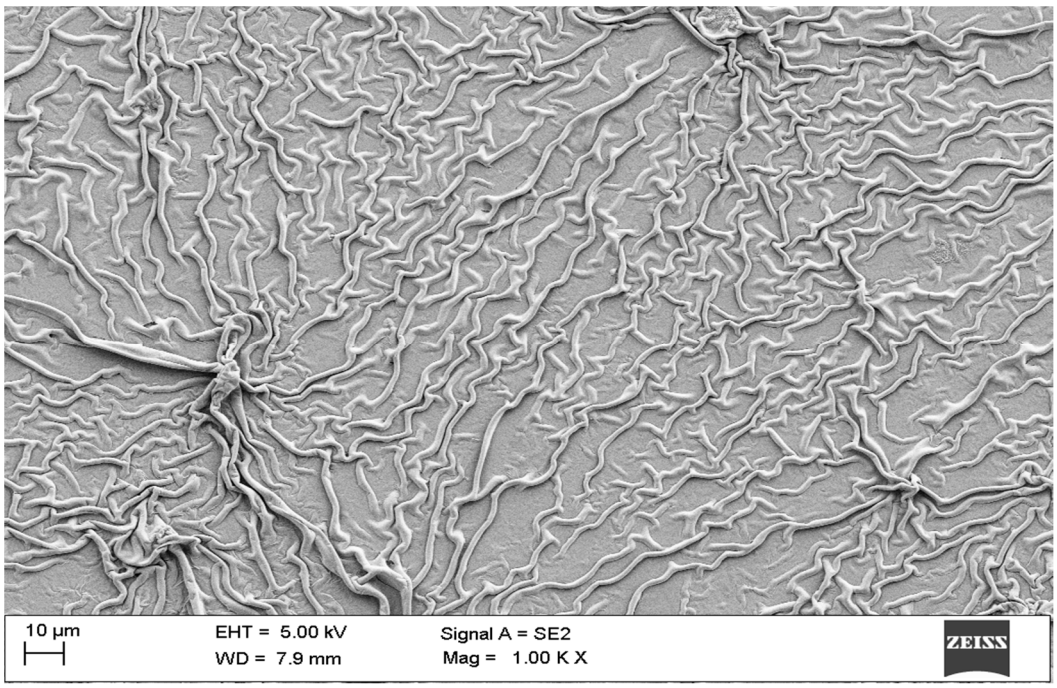

Figure 2. SEM image deep UV prepared zinc precursor (ZnO)–rGO thin film. rGO: reduced graphene oxide.

The crystallinity of pure ZnO and ZnO–rGO composite thin film was studied via an X-ray diffraction (XRD) pattern. XRD was performed on both the thin films by using a RIGAKU−Geigerflex diffractometer with a copper (Cu) anode to generate Cu Kα radiation (α = 1.5406 A°). The diffraction pattern was studied in the 2θ range of 10–80°. Figure 3a,b shows the diffraction patterns for the two prepared thin films, (a) ZnO and (b) for ZnO–rGO film. The observed characteristic peaks for the

ZnO sample, as shown in Figure 3a, correspond to (002), (101), and (103) crystal planes at 34.4°, 36.3°, and 62.9° (2θ), respectively, while the diffraction peaks for the crystal plane (002) at 34.4° of a sample ZnO–rGO is shown in Figure 3b. This suggests that the crystalline ZnO in both of the samples has a hexagonal wurtzite crystal structure with a c-axis orientation [24]. The widespread peak at 34.4° (2θ) in Figure 3 is most probably due to the small grain size of the nanoparticles. Moreover, in Figure 3b, another peak is visible at 24.4° (2θ); this characteristic peak corresponds to the (002) crystal plane of rGO. Since, in Figure 3b, there are no other diffraction peaks. Therefore, it is used to convey that the GO has been fully reduced to rGO [36].

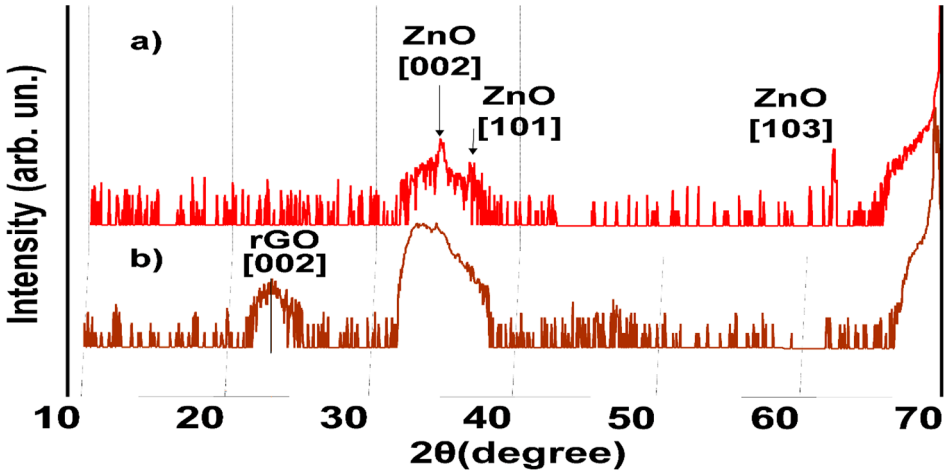

Figure 3. XRD pattern of (**a**) ZnO thin film and (**b**) ZnO–rGO thin film.

A 1 × 1 mm and 150-nm-thick Al top electrode was deposited by RF magnetron sputtering. The substrate was not heated during the top contact deposition process. The Al/ZnO–rGO/FTO device structure and device's memristive switching phenomenon is discussed and explained in Section 4. FTO forms an ohmic contact with the ZnO–rGO film. Hence, FTO-coated glass is used as the BE.

3. Electrical Characterization

The electrical characterization was done using a Keithley 2612 source meter. The Al TE electrode was connected to the HI connector and the FTO BE electrode was connected to the LO connector of the source meter. The experiment measurement setup is shown in Figure 4.

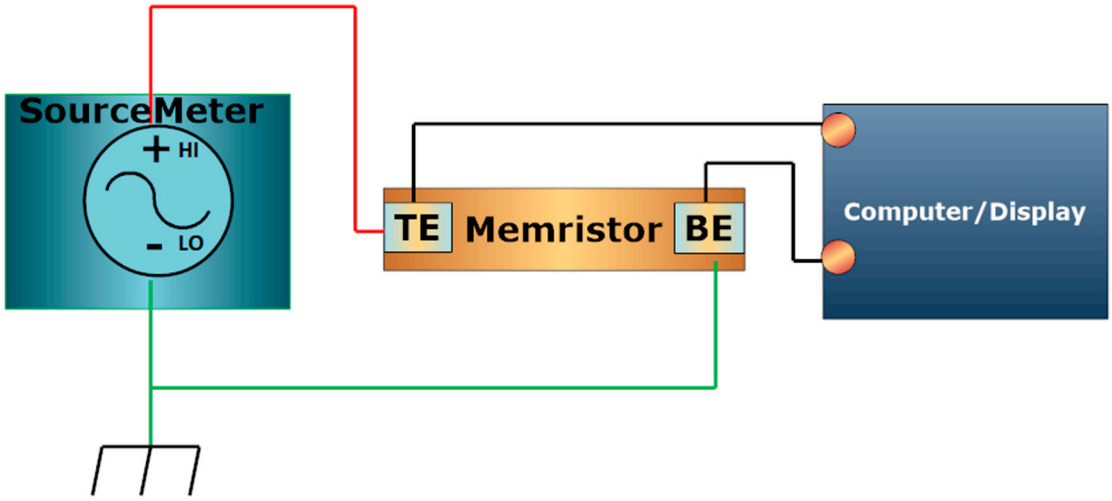

Figure 4. Setup block diagram for current–voltage (I–V) measurements.

Firstly, to measure the parasitic effects of the measurement setup (due to the probe or source meter non-ideal input stage), I–V measurement was done for the purely FTO-coated conductive sample. The obtained result is shown in Figure 5; the I–V curve confirms that the parasitic effects due to the experimental measurement set up and FTO substrate are negligible and will not considerably affect the memristor I–V measurements results.

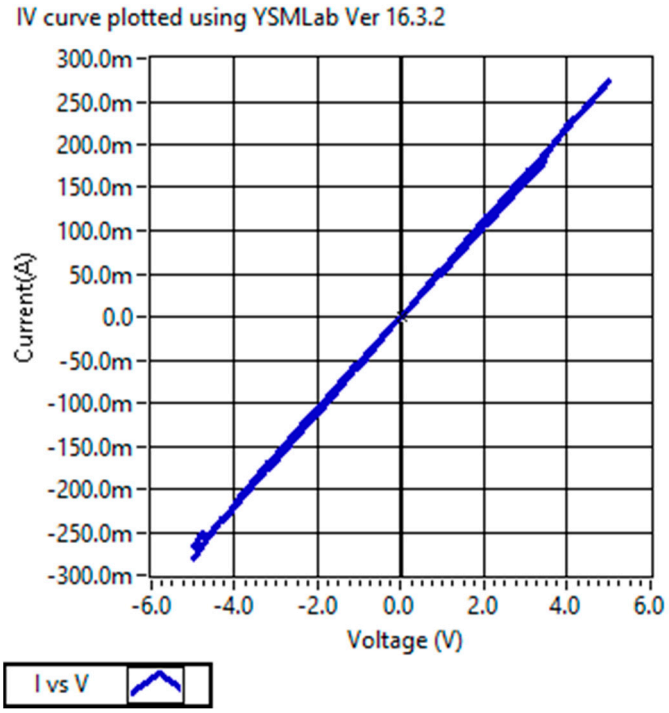

Figure 5. Benchmark test result for parasitic effects due to the -V measurement set-up: I–V curve for the FTO sample.

Voltage sweeps in the range ±5 V were applied to the device with a voltage step size of 0.1 V (current limit 100 mA) at a sweep rate of 0.5 V/s. The I–V characteristic curve of the device is summarized in Figure 6. The change in the device resistance regions are the following:

1. The source meter starts to increase the voltage from −5 V toward 0 V, and the output current is very small.
2. After passing 0 V, the output current starts to increase linearly.
3. At V_{set} = +4.5 V, the device switches to the low resistive state (LRS), and after 4.5 V, the output current increases sharply (up to 5 V).
4. Voltage starts reducing from +5 V toward 0 V, and the output current decreases linearly.
5. Then, the polarity of the input voltage (below 0 V toward −5 V) is changed, and the output current decreases sharply.
6. At V_{reset} = −2.5 Vm, the device switches to a high resistive state (HRS).

To test the stability of the device, I–V measurements were recorded for 100 consecutive ±5 V voltage cycles. The multiple voltage sweeps' I–V measurement result is shown in Figure 7; the device shows good stability and very little variation in switching characteristics.

The I–V curve is not a perfect pinched hysteresis curve, which suggests that the device has some energy stored at 0 V. Replotting of the I–V curve in semilog scale shows more clearly a picture for non-zero crossing of the I–V curve (Figure 8). Due to the non-zero crossing hysteresis loop, this device falls into the non-ideal or extended memristor class, as detailed in [20,21,37–39].

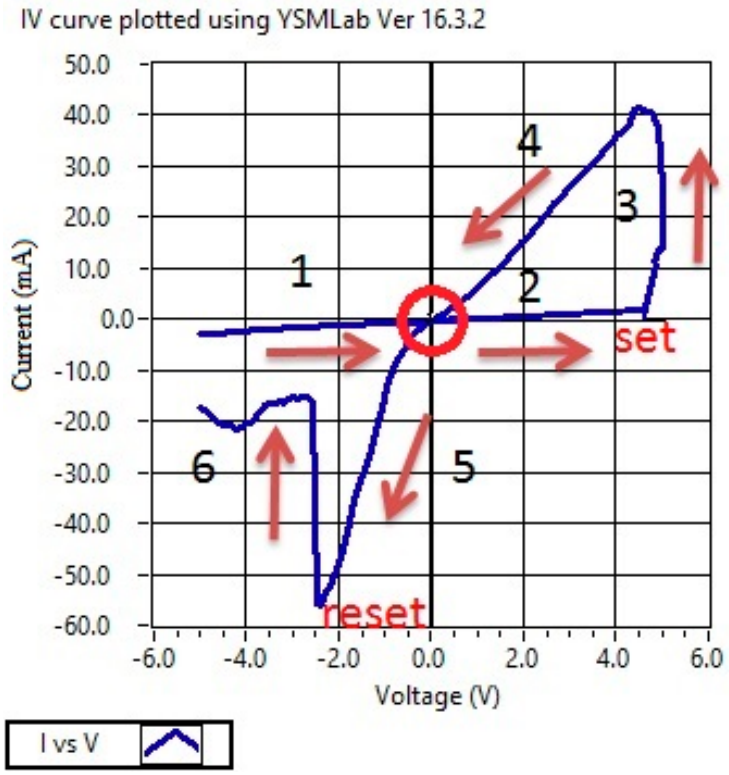

Figure 6. Device I–V plot, for a DC sweep cycle in the range ±5 V at a sweep rate of 0.5 V /s. The arrow shows the direction of the current.

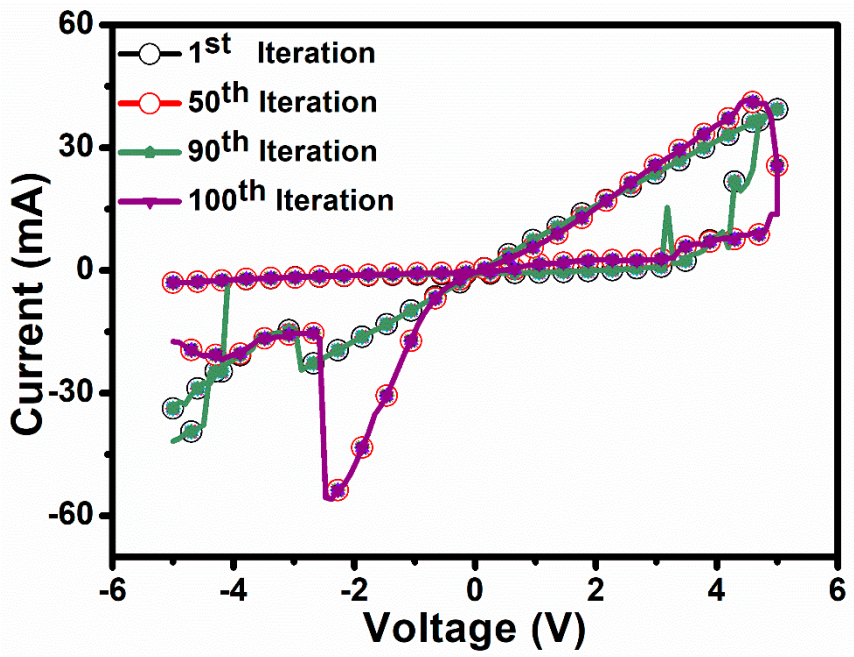

Figure 7. Device I–V plot, for a 100 continuous DC sweep cycle in the range of ±5 V at a sweep rate of 0.5 V/s.

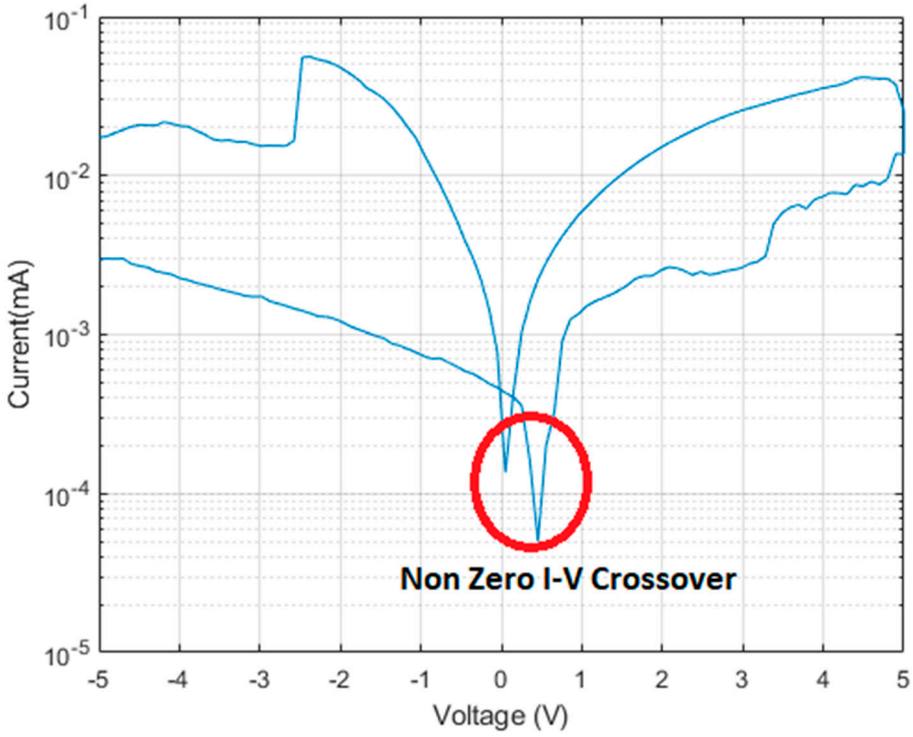

Figure 8. I–V curve in semilog scale.

The I–V curve for the ZnO–rGO device at different input voltage sweep rates (1.5, 2.5, 3.5, and 5 V/s) are summarized in Figure 9a–d, respectively. The following observations were made based on the results obtained during our experiment.

1. With the increment in voltage sweep rate from 0.5 to 1.5 V/s (Figure 9a), the crossover point of the I–V curve shifts from the origin and moves slightly into the first quadrant of the I–V plane.
2. With further increment in the sweep rate to 2.5 V/s, the I–V crossover point moves higher into the first quadrant (Figure 9b).

This shift of the crossover point from the origin toward the first quadrant is related to the simultaneous occurrence of a memristive and memcapacitive effect in the nano-device, as reported in [20,21,40].

3. Continuing the increase in the voltage sweep rate from 2.5 to 3.5 V/s, the I–V crossover point now drifts down toward the third quadrant of the I–V plane (Figure 9c).
4. Finally, increasing the scan rate to 5 V/s, the crossover points move completely into the third quadrant, and the curve also shows a second crossover point at around −2.5 V (Figure 9d) near to V_{reset} of Figure 6.

This behavior is related to the simultaneous existence of a memristive and meminductive effect occurring within the nano-device, as also reported in [20,21,40].

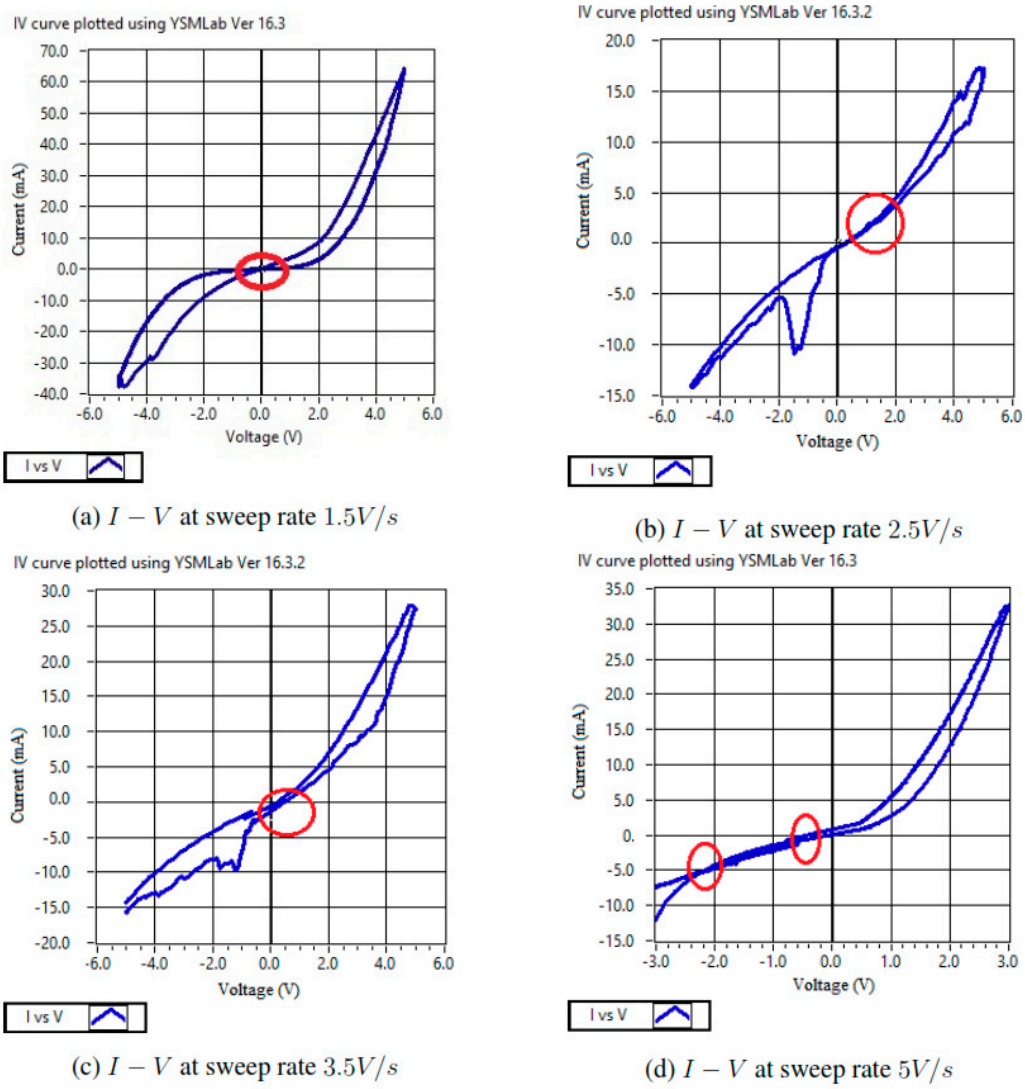

Figure 9. I–V plot at different sweep rates. (**a**) I–V at a sweep rate of 1.5 V/s. (**b**) I–V at a sweep rate of 2.5 V/s. (**c**) I–V at a sweep rate of 3.5 V/s. (**d**) I–V at a sweep rate of 5 V/s.

4. Resistive Switching Mechanism

The switching mechanism of a memristive device depends heavily on the selected material for the sandwiched active layer and for the metal electrode.

The operating mechanism of the ZnO–rGO thin film memristive device is filamentary (i.e., the formation and breaking of conductive filaments (CFs) between TE and BE). The filamentary-based switching in ZnO devices has been reported previously in different works in the literature [40–46].

The bipolar switching response of the Al–ZnO–rGO–FTO device can be attributed to the formation and rupture of CFs consisting of oxygen vacancies created during the photo-annealing process.

The vacancies move along the thin film under the influence of the applied electric field, thereby creating or dissolving the current conduction paths between TE and BE, as shown in Figure 10. With TE positive and BE connected to the ground, oxygen vacancies move toward BE and create a conduction path between BE and TE, turning the device ON (low resistive state (LRS)). Whereas, reversing the polarity of the applied voltage (i.e., making BE positive with respect to TE), the vacancies drift away from BE toward the TE, thereby disturbing the conduction path and turning the device OFF (high resistive state (HRS)).

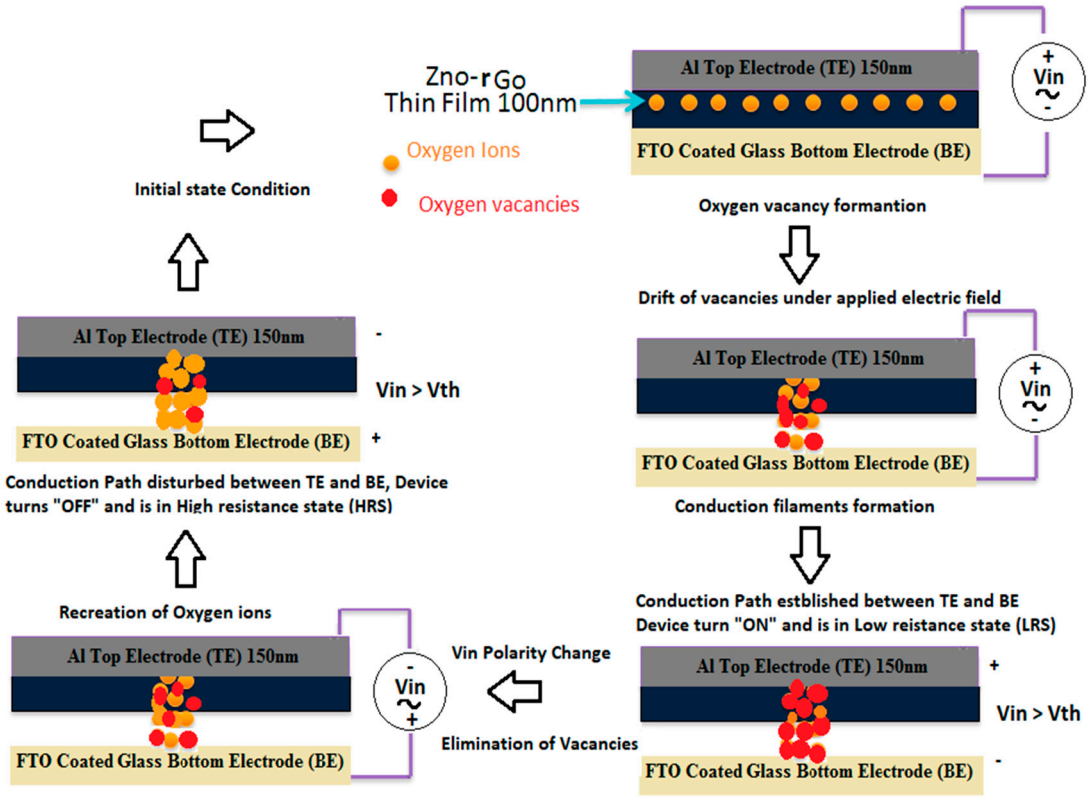

Figure 10. Switching mechanism for the Al–ZnO–rGO–FTO device.

In many of the oxide-based memristive devices, an added process known as electro-forming is used to activate the device. This is because pristine state oxide materials generally have a low density of defects such as vacancies or interstitials. In the electro-forming process, a high voltage with suitable compliance current is first given to the device to create the free vacancies in the active layer. This forming process is an undesirable process, especially for neuromorphic and non-volatile memory applications [28,46,47]. In our device, this electro-forming step is not needed because enough vacancies for initiating the switching operation are created in the thin film via photo annealing.

As discussed, the formation or dissolution of the CFs is due to the input voltage-controlled movement of the oxygen vacancies. Therefore, the resistive state of the device can easily be controlled by applying a different voltage within the range of V_{set} and V_{reset}; for an input voltage value, the device will capture a unique resistive state between LRS and HRS. These multiple resistive values are attributed to the strength of the CF formation. A strong conductive path between TE and BE will switch the device into its LRS. Similarly, a weak conductive path will make the device switch to its HRS.

Therefore, for our device, it is safe to say that the distance between the filament and the bottom electrode edge determines the resistive state of the device.

The formation and dissolution of CFs between TE and BE is a reconfigurable process. Hence, simply by changing the polarity or magnitude of the input voltage, it is possible to control the instantaneous state of the memristive device.

5. Results and Discussion

The stable bipolar switching characteristic can be explained by the movement of the oxygen ions within the oxide bulk under the influence of the applied electrical field. During positive bias (i.e., TE connected to a positive voltage), oxygen ions from the bulk are attracted toward TE, creating free oxygen vacancies in the bulk film that form the CFs. As the positive voltage at TE increases, more ions

are pulled up from the oxide bulk, leaving behind enough vacancies to complete the conduction path and forcing the device to its LRS.

During the negative biasing phase (i.e., when the TE electrode is connected to a negative voltage), oxygen ions from the TE interface are pushed back into the oxide bulk. The further increment in negative potential pushes the oxygen ions to recombine with the oxygen vacancies. Assisted by joule heating, more ion–vacancy recombination takes place disturbing the CF bridge, forcing the device to nonconductive HRS.

In our device, the best R_{off}/R_{on} ratio is approximately 40, which is measured at 4.7 V (Figure 7). The output current is relatively high (i.e., 0.04 A for 4 V) for the discrete device. This high current could be due to the large TE area; indeed, the dependency of memristive device operation on the top electrode material and area is well studied and documented [34,45–49]. The I–V characteristics of the device depend on the input voltage sweep rate [22]. The non-zero crossing I–V implies that there is some charge stored in the device, suggesting that the device has memory impedance at the nano scale, which naturally coexists with memristive behavior. The frequency-dependent behavior of memristive devices and systems has been well studied. It is a well-known phenomenon that could be explained based on the charge equilibration process [17,19–21]. At the microscopic level, when a current flow in a resistor, charge accumulation occurs on one side of the resistor, with the corresponding depletion layer at the other end due to the scattering of the carriers at the interfaces, thereby creating resistive dipoles. The dipole formation process is dynamic and appears as a resistance change [50]. The dipole formation process takes some time and is associated with some energy storage with respect to the capacitance of the system.

Therefore, at high frequency (for frequencies greater than or equal to the inverse of time of charge equilibrium process), the system does not get enough time to create the stable local resistive dipoles, and hence, does not show an apparent resistive change or a pinched hysteresis loop [10]. This behavior is attributed to the coexistence of memristive, memcapacitive, and meminductive effects occurring simultaneously in the device, as also reported [20,21].

Note also that at a low scan rate, the hysteresis loop area is large, and a clear switching is observed in Figure 6. The hysteresis area reduces significantly with an increase of the scan rate, while at higher sweeping rates, the resistive switching (memristive) behavior is affected by the appearance of memory impedance (capacitive or inductive) effects, as shown in Figure 8.

As discussed before, the time-dependent state of a memristor device changes in response to the alternating input signal, and is accompanied by time-dependent resistive, as well as a reactance change. Therefore, in reference [51], the authors have suggested a more general equation 5, 6, 7, and 8 for the change in the state of nanoparticle memristive systems.

The positive and negative regions of the I−V curve are re-plotted in the double log coordinates to understand the memristive behavior of our device. Figure 11 displays the positive voltages, while Figure 12 shows the negative voltages. Different carrier transport models were used to fit the double log curve. Primary models that were used were Fowier–Nordheim (F–N) tunneling, thermionic emission, Poole–Frenkel emission, Schottky emission, and space-charge-limited conduction (SCLC).

The above-mentioned conduction mechanism (SCLC) ($I \propto aV^2$, where a is the slope of the curve) is a better fit for our device I–V. Ohmic conduction ($I \propto V$) is dominant for the low voltage region between 0 and ±3 V of the device I–V curve for both positive and negative sweep voltages. The conduction mechanism for voltages beyond ±3 V is different. The high voltage conduction region can be divided into three different regions of SCLC conduction theory.

Initially, the conduction is linear ($I \propto V$) ($a = 1$) until all of the open traps in the active layer are filled up by the injected carries (linear region in Figures 11 and 12).

The current starts to increase slowly ($I \propto V^{1.3}$), until the deep traps are also filled. This corresponds to a SCLC region in Figures 11 and 12.

Lastly, all the trap centers are filled with the injected carriers and space charge accumulates, which sharply increase the current, and the response follows a strong SCLC, which is known as trapped charge-limit current (TCLC) slope a = 2.5 (TCLC region in Figures 10 and 11).

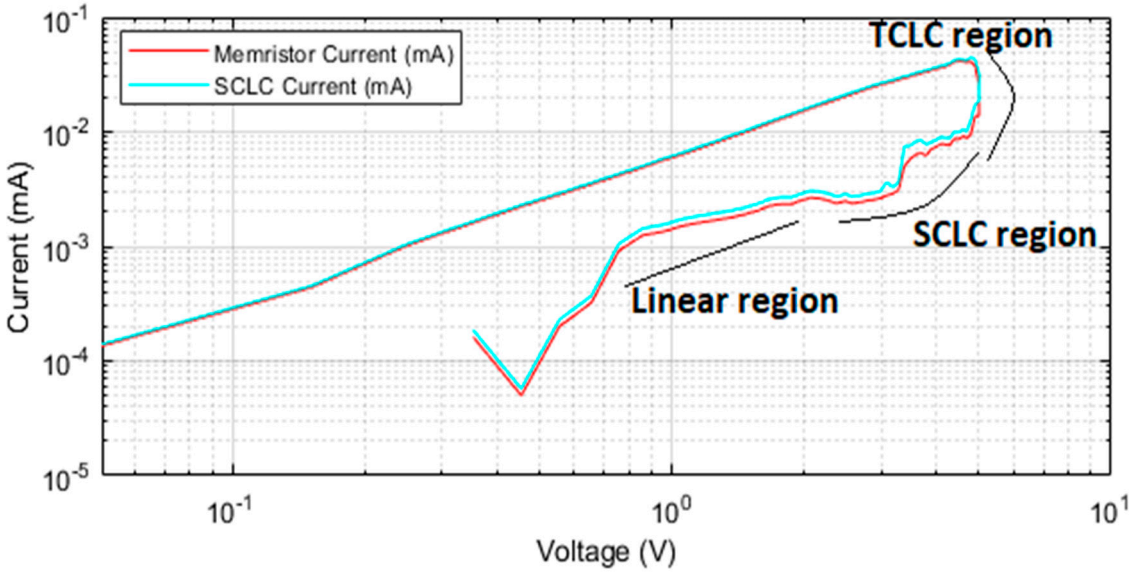

Figure 11. I–V curve double log scale for positive voltage 0 V → 5 V → 0 V.

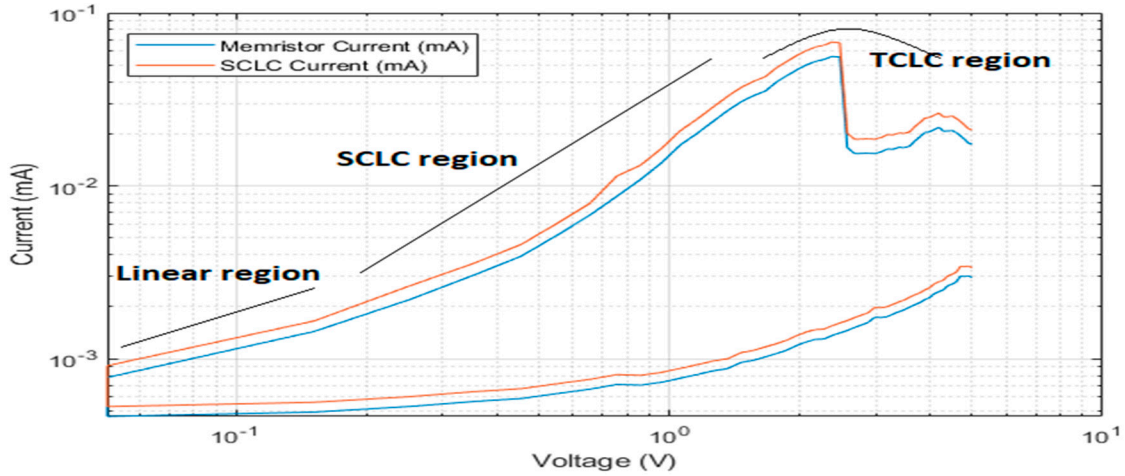

Figure 12. I–V curve double log scale for negative voltage −5 V → 0 V → −5 V.

The increase and decrease of the current with respect to the change in the input voltage, as shown in Figures 10 and 11, indicate the process of charge carriers trapping and releasing. Therefore, the bipolar switching behavior of the device can be attributed to the charge trapping–detrapping process, which is commonly known as the trap-controlled SCLC conduction mechanism. The SCLC conduction mechanism has been observed in many ZnO-based memristive devices [44,52–54].

6. Conclusions

In this work, we fabricated a low-cost, facile, and photo (UV)-activated ZnO–rGO thin film memistive device. The device exhibits symmetric bipolar re-configurable resistive change behavior with an OFF–ON ratio of 40. The SCLC was established to be the current conduction mechanism for the ZnO–rGO device. It is argued based on the experimental results (via the electrical characterization)

that memristive, memcapacitive, and meminductive effects coexist naturally in the ZnO–rGO thin film memristive device.

Since the device shows a re-configurable coexistence of memresistive and memimpedance effects, it could be useful for making adaptive analogue circuits. Moreover, we believe that the device performance at high frequency could be further enhanced by choosing high-electron-mobility materials such as pure graphene as the active layer between the two electrodes and/or by reducing the thickness of the ZnO–rGO thin film to <40 nm [20,55].

Author Contributions: G.M.K. conceptualized, investigated, resourced, and wrote the original draft; G.C.C. supervised the work; L.D.N., R.F., and M.R. supported in performing the electrical measurements, and reviewing and editing of the written work; finally, R.K. analyzed and validated the material properties. All authors have read and agreed to the published version of the manuscript.

Funding: This research received no external funding.

Acknowledgments: We are thankful to Abalonyx AS, Norway, for providing the high-quality graphene oxide used in this work.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Patil, S.R.; Chougale, M.Y.; Rane, T.D.; Khot, S.S.; Patil, A.A.; Bagal, O.S.; Jadhav, S.D.; Sheikh, A.D.; Kim, S.; Dongale, T.D. Solution-Processable ZnO Thin Film Memristive Device for Resistive Random Access Memory Application. *Electronics* **2018**, *7*, 445. [CrossRef]
2. Cheng, T.; Rao, J.; Tang, X.; Yang, L.; Liu, N. Analog Memristive Characteristics and Conditioned Reflex Study Based on Au/ZnO/ITO Devices. *Electronics* **2018**, *7*, 141. [CrossRef]
3. Zhao, X.; Li, Y.; Ai, C.; Wen, D. Resistive Switching Characteristics of Li-Doped ZnO Thin Films Based on Magnetron Sputtering Materials. *Materials* **2019**, *12*, 1282. [CrossRef] [PubMed]
4. Simanjuntak, F.M.; Panda, D.; Wei, K.H.; Tseng, T.Y. Status and Prospects of ZnO-Based Resistive Switching Memory Devices. *Nanoscale Res. Lett.* **2016**, *11*, 368. [CrossRef] [PubMed]
5. Romero, F.J.; Toral-Lopez, A.; Ohata, A.; Morales, D.P.; Ruiz, F.G.; Godoy, A.; Rodriguez, N. Laser-Fabricated Reduced Graphene Oxide Memristors. *Nanomaterials* **2019**, *9*, 897. [CrossRef] [PubMed]
6. Lian, X.; Shen, X.; Lu, L.; He, N.; Wan, X.; Samanta, S.; Tong, Y. Resistance Switching Statistics and Mechanisms of Pt Dispersed Silicon Oxide-Based Memristors. *Micromachines* **2019**, *10*, 369. [CrossRef] [PubMed]
7. Villena, M.A.; Roldán, J.B.; González, M.B.; González-Rodelas, P.; Jiménez-Molinos, F.; Campabadal, F.; Barrera, D. A new parameter to characterize the charge transport regime in Ni/HfO2/Si-n+-based RRAMs. *Solid-State Electron.* **2016**, *118*, 56–60. [CrossRef]
8. Zamarreño-Ramos, C.; Camuñas-Mesa, L.A.; Pérez-Carrasco, J.A.; Masquelier, T.; Serrano-Gotarredona, T.; Linares-Barranco, B. On spike-timing-dependent plasticity, memristive devices, and building a self-learning visual cortex. *Front. Neurosci.* **2011**, *5*, 26. [CrossRef]
9. Khanal, G.M.; Acciarito, S.; Cardarilli, G.C.; Chakraborty, A.; Nunzio, L.D.; Fazzolari, R.; Cristini, A.; Re, M.; Susi, G. Synaptic behavior in ZnO-rGO composites thin film memristor. *Electron. Lett.* **2017**, *53*, 296–298. [CrossRef]
10. Bi, G.-Q.; Poo, M.-M. Synaptic modifications in cultured hippocampal neurons: Dependence on spike timing, synaptic strength, and postsynaptic cell type. *J. Neurosci.* **1998**, *18*, 10464–10472. [CrossRef]
11. Likharev, K.K. Cross nets: Neuromorphic hybrid cmos/nano electronic networks. *Sci. Adv. Mater.* **2011**, *3*, 322–331. [CrossRef]
12. Indiveri, G.; Linares-Barranco, B.; Hamilton, T.J.; van Schaik, A.; Etienne-Cummings, R.; Delbruck, T.; Liu, S.-C.; Dudek, P.; Häfliger, P.; Renaud, S.; et al. Neuromorphic silicon neuron circuits. *Front. Neurosci.* **2011**, *5*, 73. [CrossRef] [PubMed]
13. Serrano-Gotarredona, T.; Masquelier, T.; Prodromakis, T.; Indiveri, G.; Linares-Barranco, B. STDP and STDP variations with memristors for spiking neuromorphic learning systems. *Front. Neurosci.* **2013**, *7*, 2. [CrossRef] [PubMed]

14. Snider, G.S. Spike-timing-dependent learning in memristive nanodevices. In Proceedings of the IEEE International Symposium on Nanoscale Architectures, Anaheim, CA, USA, 12–13 June 2008; pp. 85–92. [CrossRef]
15. Acciarito, S.; Cristini, A.; Nunzio, L.D.; Khanal, G.M.; Susi, G. An avlsi driving circuit for memristor-based stdp. In Proceedings of the 12th Conference on Ph.D. Research in Microelectronics and Electronics (PRIME), Lisbon, Portugal, 27–30 June 2016. [CrossRef]
16. Chua, L.O. Memristor—The missing circuit element. *IEEE Trans. Circuit Theory* **1971**, *18*, 507–519. [CrossRef]
17. Di Ventra, M.; Pershin, Y.V.; Chua, L.O. Circuit elements with memory: Memristors, memcapacitors, and meminductors. *Proc. IEEE* **2009**, *97*, 1717–1724. [CrossRef]
18. Chua, L.O.; Kang, S.M. Memristive devices and systems. *Proc. IEEE.* **1976**, *64*, 209–223. [CrossRef]
19. Li, L.; Zhang, Y.; Chew, Z. A Cu-ZnO nanowire-Cu resistive switching device. *Nano-Micro Lett.* **2013**, *5*, 159–162. [CrossRef]
20. Qingjiang, L.; Khiat, A.; Salaoru, I.; Papavassiliou, C.; Hui, X.; Prodromakis, T. Memory impedance in TiO2 based metal-insulator-metal devices. *Sci. Rep.* **2014**, *4*, 4522. [CrossRef]
21. Valov, I.; Linn, E.; Tappertzhofen, S.; Schmelzer, S.; van den Hurk, J.; Lentz, F.; Waser, R. Nanobatteries in redox-based resistive switches require extension of memristor theory. *Nat. Commun.* **2013**, *4*, 1771. [CrossRef]
22. Khanal, G.M.; Cardarilli, G.C.; Chakraborty, A.; Acciarito, S.; Mulla, M.Y.; Nunzio, L.D.; Fazzolari, R.; Re, M. A ZnO/rGO composite thin film discrete memristor. In Proceedings of the 2016 IEEE International Conference on Semiconductor Electronics (ICSE) (IEEE-ICSE2016), Kuala Lumpur, Malaysia, 17–19 August 2016. [CrossRef]
23. Song, J.; Zhang, Y.; Xu, C.; Wu, W.; Wang, Z.L. Polar charges induced electric hysteresis of ZnO nano/microwire for fast data storage. *Nano Lett.* **2011**, *11*, 2829–2834. [CrossRef]
24. Sarma, S.; Mothudi, B.M.; Dhlamini, M.S. Observed coexistence of memristive, memcapacitive and meminductive characteristics in polyvinyl alcohol/cadmium sulphide nano composites. *J. Mater. Sci. Mater. Electron.* **2016**, *27*, 4551–4558. [CrossRef]
25. Lewis, D.L.; Lee, H.-H.S. Architectural evaluation of 3D stacked ReRam caches. In Proceedings of the IEEE International Conference on 3D System Integration, San Francisco, CA, USA, 28–30 September 2009; pp. 1–4. [CrossRef]
26. Kudithipudi, D.; Merkel, C.E. Reconfigurable memristor fabrics for heterogeneous computing. In *Advances in Neuromorphic Memristor Science and Applications*; Springer: Dordrecht, The Netherlands, 2012; pp. 89–106. [CrossRef]
27. Macaluso, R.; Mosca, M.; Costanza, V.; D'angelo, A.; Lullo, G.; Caruso, F.; Calì, C.; DiFranco, F.; Santamaria, M.; DiQuarto, F. Resistive switching behaviour in ZnO and VO2 memristors grown by pulsed laser deposition. *Electron. Lett.* **2014**, *50*, 262–263. [CrossRef]
28. Kumar, A.; Rawal, Y.; Baghini, M.S. Fabrication and characterization of the ZnO-based memristor. In Proceedings of the IEEE International Conference on Emerging Electronics, Mumbai, India, 15–17 December 2012; pp. 1–3. [CrossRef]
29. Sekhar, K.C.; Kamakshi, K.; Bernstorff, S.; Gomes, M.J.M. Effect of annealing temperature on photoluminescence and resistive switching characteristics of ZnO/Al2O3 multilayer nanostructures. *J. Alloys Compd.* **2015**, *619*, 248–252. [CrossRef]
30. Sawa, A. Resistive switching in transition metal oxides. *Mater. Today* **2008**, *11*, 28–36. [CrossRef]
31. Yang, Y.C.; Pan, F.; Zeng, F.; Liu, M. Switching mechanism transition induced by annealing treatment in nonvolatile Cu/ZnO/Cu/ZnO/Pt resistive memory: From carrier trapping/detrapping to electrochemical metallization. *J. Appl. Phys.* **2009**, *106*, 123705. [CrossRef]
32. Chakraborty, A.; Khanal, G.M. Study of sol-gel based synthesized ZnO-rGO composite thin film. In Proceedings of the NGPT Conference, Rome, Italy, 15–17 June 2016.
33. Chakraborty, A.; Pizzoferrato, R.; Agresti, A.; de Matteis, F.; Orsini, A.; Medaglia, P.G. Wet-chemical synthesis of ZnO nanowires on low-temperature photo-activated ZnO-rGO composite thin film with enhanced photoconduction. *J. Electron. Mater.* **2018**, *47*, 5863–5869. [CrossRef]
34. Scherer, G.W. Sintering of sol-gel films. *J. Sol-Gel Sci. Technol.* **1997**, *8*, 353–363. [CrossRef]
35. Kwon, S.J.; Park, J.H.; Park, J.-G. Wrinkling of a sol-gel-derived thin film. *Phys. Rev. E* **2005**, *71*, 011604. [CrossRef]

36. Uddin, A.S.M.I.; Phan, D.T.; Chung, G.S. Synthesis of ZnO nanoparticles-reduced graphene oxide composites and their intrinsic gas sensing properties. *Surf. Rev. Lett.* **2014**, *21*, 1450086. [CrossRef]
37. Chua, L. Everything you wish to know about memristors but are afraid to ask. *Radioengineering* **2015**, *24*, 319–368. [CrossRef]
38. Biolek, D.; Biolek, Z.; Biolkova, V.; Ascoli, A.; Tetzlaff, R. About v-i Pinched Hysteresis of Some Non-Memristive Systems. *Math. Probl. Eng.* **2018**, *2018*, 1747865. [CrossRef]
39. Mouttet, B. Memresistors and non-memristive zero-crossing hysteresis curves. *arXiv* **2012**, arXiv:1201.2626.
40. Kamble, G.U.; Shetake, N.P.; Yadav, S.D.; Teli, A.M.; Patil, D.S.; Pawar, S.A.; Karanjkar, M.M.; Patil, P.S.; Shin, J.C.; Orlowski, M.K.; et al. Coexistence of filamentary and homogeneous resistive switching with memristive and meminductive memory effects in Al/MnO_2/SS thin film metal–insulator–metal device. *Int. Nano Lett.* **2018**, *8*, 263. [CrossRef]
41. Dongale, T.D.; Khot, K.V.; Mali, S.S.; Patil, P.S.; Gaikwad, P.K.; Kamat, R.K.; Bhosale, P.N. Development of Ag/ZnO/FTO thin film memristor using aqueous chemical route. *Mater. Sci. Semicond. Process.* **2015**, *40*, 523–526. [CrossRef]
42. Chew, Z.J.; Li, L. A discrete memristor made of ZnO nanowires synthesized on printed circuit board. *Mater. Lett.* **2013**, *91*, 298–300. [CrossRef]
43. Gul, F.; Efeoglu, H. Bipolar resistive switching and conduction mechanism of an Al/ZnO/Al-based memristor. *Superlattices Microstruct.* **2017**, *101*, 172–179. [CrossRef]
44. Tan, C.; Liu, Z.; Huang, W.; Zhang, H. Non-volatile resistive memory devices based on solution-processed ultrathin two-dimensional nanomaterials. *Chem. Soc. Rev.* **2015**, *44*, 2615–2628. [CrossRef]
45. Yang, J.J.; Borghetti, J.; Murphy, D.; Stewart, D.R.; Williams, R.S. A Family of Electronically Reconfigurable Nanodevices. *Adv. Mater.* **2009**, *21*, 3754–3758. [CrossRef]
46. Pan, F.; Gao, S.; Chen, C.; Song, C.; Zeng, F. Recent progress in resistive random-access memories: Materials, switching mechanisms, and performance. *Mater. Sci. Eng. R Rep.* **2014**, *83*, 1–59. [CrossRef]
47. Miao, F.; Yi, W.; Goldfarb, I.; Yang, J.J.; Zhang, M.X.; Pickett, M.D.; Strachan, J.P.; Ribeiro, G.M.; Williams, R.S. Continuous electrical tuning of the chemical composition of TaO(x)-based memristors. *ACS Nano* **2012**, *6*, 2312–2318. [CrossRef]
48. Sun, Y.; Yan, X.; Zheng, X.; Liu, Y.; Zhao, Y.; Shen, Y.; Liao, Q.; Zhang, Y. High on–off ratio improvement of ZnO based forming-free memristor by surface hydrogen annealing. *ACS Appl. Mater. Interfaces* **2015**, *7*, 7382–7388. [CrossRef] [PubMed]
49. Gale, E.; Pearson, D.; Kitson, S.; Adamatzky, A.; de Lacy Costello, B. The effect of changing electrode metal on solution-processed flexible titanium dioxide memristors. *Mater. Chem. Phys.* **2015**, *162*, 20–30. [CrossRef]
50. Sai, N.; Bushong, N.; Hatcher, R.; di Ventra, M. Microscopic current dynamics in nanoscale junctions. *Phys. Rev. B* **2007**, *75*, 115410. [CrossRef]
51. Kim, T.H.; Jang, E.Y.; Lee, N.J.; Choi, D.J.; Lee, K.J.; Jang, J.T.; Choi, J.S.; Moon, S.H.; Cheon, J. Nanoparticle assemblies as memristors. *Nano Lett.* **2009**, *9*, 2229–2233. [CrossRef]
52. Yang, Y.C.; Pan, F.; Liu, Q.; Liu, M.; Zeng, F. Fully room-temperature-fabricated nonvolatile resistive memory for ultrafast and high-density memory application. *Nano Lett.* **2009**, *9*, 1636–1643. [CrossRef]
53. Huang, Y.; Luo, Y.; Shen, Z.; Yuan, G.; Zeng, H. Unipolar resistive switching of ZnO-single-wire memristors. *Nanoscale Res. Lett* **2014**, *9*, 381. [CrossRef]
54. Lampert, M.A. Simplified theory of space-charge-limited currents in an insulator with traps. *Phys. Rev.* **1956**, *103*, 1648–1656. [CrossRef]
55. Mouttet, B. A Memadmittance Systems Model for Thin Film Memory Materials. *arXiv* **2010**, arXiv:1003.2842.