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Exploring Single Event Effects in the ALICE (A Large Ion Collider Experiment) SAMPA chip

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To all mystic seekers

"The scientific observer of Nature is a kind of mystic seeker in the act of prayer."

— Dr. Muhammad Iqbal (1877-1938)

Abstract

Since the 1980s, the High Energy Physics (HEP) experiments employ Application Specific Integrated Circuits (ASICs) for data readout purposes. This is achieved by the remarkable evolution of the Complementary Metal Oxide Semiconductor (CMOS) technology in terms of speed, area, and cost. It allows for higher custom integration density, enhanced circuit performance, lower power consumption as well as better temperature and radiation tolerance performance than the commercial ICs or discrete components.

After the second long shutdown (LS2) ending in 2021 at the Large Hadron Collider (LHC), improved resolution requirements of the tracking detectors in the HEP experiments demand a higher number of readout channels and more compact front-end electronics. Due to strict area requirements, both analog and digital circuitries are integrated on a single silicon die, turning into mixed-signal readout ASICs. In this context, the "SAMPA" chip is developed to fulfill the readout requirements for multiple detectors at the ALICE (A Large Ion Collider Experiment) experiment.

With the increased interaction rate expected after the LS2, the radiation load on the SAMPA chip will consequently also increase. The work presented in this thesis evaluates the radiation tolerance of the SAMPA chip, with the main focus on the single event effects (SEE) qualification of the SAMPA chip for the foreseen radiation levels at the ALICE detectors after the LS2.

As the SAMPA chip is fabricated in a commercial CMOS technology, the radiation hardness assurance of the SAMPA chip was imperative for ensuring its reliable and acceptable operation in the ALICE radiation environment. This is accomplished by conducting high-energy protons, heavy-ions, and pulsed-laser irradiation campaigns on various prototypes of the SAMPA chip. During the proton campaigns, the extracted soft error σ values was in the order of $\sim 10^{-14}\text{cm}^{-2}$/bit for various memory elements, which is consistent with the results from comparable technologies in literature. In the V2 and final versions of the SAMPA chip, most of the critical configuration registers are protected by the triple modular redundancy (TMR) technique, while the essential (header) information of the data packets is protected with the hamming coding.

During protons exposure of the second "V2" prototype, frequent and significant jumps in the current consumption were detected on the digital power domain of the SAMPA chip. The subsequent heavy-ions campaign confirmed that the current jumps were associated with the single event latch-up (SEL) events in the V2 prototypes. Dedicated collimator tests with the heavy-ions and pulsed-laser tests showed that one of the commercial SRAM IPs was the primary source for triggering SEL events in the V2 prototypes. Since the expected failure rates of the SEL events were unacceptable for the ALICE detectors, the SEL sensitive

SRAM IP blocks were substituted with the SEL tolerant SRAM IP blocks in the final versions of the SAMPA chip. A heavy-ions campaign on the final versions of the SAMPA chip confirmed robustness against SEL events. Conclusively, the final versions of the SAMPA chip is expected to operate successfully in the ALICE radiation environment.

Preface

"With faith, discipline and selfless devotion to duty,
there is nothing worthwhile that you cannot achieve."
— Muhammad Ali Jinnah (1876-1948)

This dissertation is submitted for the degree of Doctor of Philosophy at the University of Oslo. The research described herein is conducted under the supervision of Associate Professor Ketil Røed (Department of Physics, University of Oslo), Associate Professor Johan Alme (Department of Physics and Technology, University of Bergen), and Professor Philipp Dominik Häfliger (Department of Informatics, University of Oslo) at the Department of Physics, Faculty of Mathematics and Natural Sciences, University of Oslo, between September 2013 and October 2018.

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Acronyms

6T	Six Transistors
ADC	Analog to Digital Converter
AGORFIRM	AGOR Facility for IRradiation of Materials
ALICE	A Large Ion Collider Experiment
ALTRO	ALice Tpc ReadOut
ASET	Analog Single Event Transient
ASIC	Application Specific Integrated Circuit
BC	Baseline Calculation
BIM	Beam Intensity Monitor
BIST	Built-In-Self-Test
BJT	Bipolar Junction Transistors
Bx	Bunch-crossing
CERN	European Organization for Nuclear Research
CHARM	CERN High energy Accelerator Mixed-field
CMOS	Complementary Metal Oxide Semiconductor
CRU	Common Readout Unit
CSA	Charge Sensitive Amplifier
CTP	Central Trigger Processor
Cu	Copper
DAC	Digital to Analog Converter
DAQ	Data AcQuisition
DAS	Direct ADC Serialization
DD	Displacement Damage
DFT	Design-For-Test

DICE	Dual-Interlocked-Storage-Cell
DP	Dual-Port
DSP	Digital Signal Processor
DUT	Device Under Test
e-h	electron-hole
EDAC	Error Detection And Correction
ENC	Equivalent Noise Charge
eV	Electron Volt
fb	femtobarn
FEC	Front-End Card
FEE	Front-End Electronic
FF	Flip-Flop
FPD	Fixed PeDestal
FPGA	Field-Programmable Gate Array
GBT	Gigabit Transceiver
GEM	Gas Electron Multiplier
GPIO	General Purpose Input/Output
hb	heart-beat
HEH	High-Energy Hadrons
HEP	High Energy Physics
HI	Heavy-Ion
HIF	Heavy-Ion Facility
HPS	Hard Processor System
HSMC	High-Speed Mezzanine Card
HV	High Voltage
I2C	Inter-integrated Circuit
IC	Integrated Circuit
IIR	Infinite Impulse Response

IP	Intellectual Property
KVI	Center of Advanced Radiation Technology
LAN	Local Area Network
LEO	Low Earth Orbit
LET	Linear Energy Transfer
LHC	Large Hadron Collider
LS	Long Shutdown period
LSB	Least Significant Bit
LVDS	Low Voltage Differential Signaling
MCH	Muon CHamber
MPW	Multi-Project Wafer
MSB	Most Significant Bit
MTBF	Mean Time Between Failure
MUX	Multiplexer
MWPC	Multi-Wire Proportional Chamber
NB	Neighbour
NCCA	Naked Chip Carrier to Altera readout
NFS	Network File System
NIEL	Non-Ionizing Energy Loss
nMOS	N-channel Metal Oxide Semiconductor
O^2	Online-Offline computing system
PASA	PreAmplifier ShAper
PCCA	Package Chip Carrier to Altera readout
PedMem	Pedestal Memory
PID	Proportional-Integral-Derivative
PL	Pulsed-Laser
pMOS	P-channel Metal Oxide Semiconductor
POR	Power-On Reset

QCD	Quantum Chromo Dynamics
QGP	Quark-Gluon Plasma
R.Pi	Raspberry Pi
R2E	Radiation To Electronics
RB	Ring Buffer
RCU	Readout Control Unit
RPP	Rectangular ParallelePiped
RTL	Register-transfer level
RX	Receiver
SAR	Successive Approximation Register
SC	Scan Chain
SECDED	Single-Error-Correction-Double-Error-Detection
SEE	Single Event Effect
SEL	Single Event Latchup
SET	Single Event Transient
SEU	Single Event Upset
SF2	Smart-Fusion2
Si	Silicon
SiO_2	Silicon dioxide
SLVS	Scalable Low-Voltage Signaling
SO	Serial Output
SP	Single-Port
SR	Shift Register
SRAM	Static Random Access Memory
ssh	Secure SHell
SV	Sensitive Volume
TFBGA	Thin Fine Ball Grid Array
Ti	Titanium

TID	Total Ionizing Dose
TMR	Triple Modular Redundancy
TPC	Time Projection Chamber
TSL	The Svedberg Laboratory
TSMC	Taiwan Semiconductor Manufacturing Company
TTC	Timing, Trigger and Control
TW	Time Window
TX	Transmitter
UART	Universal Asynchronous Receiver/Transmitter
UCL	Universitè Catholique de Louvain
VL	Versatile Link
W	Tungsten

Chapter 1

Introduction

The last century has been a remarkable era for cosmology, astrophysics, technology, and high energy physics. Particle accelerators are at the forefront of attempts to resolve mysteries related to the creation of the universe: the existence of the super-symmetry, the nature of dark matter, and the existence of extra dimensions. A Particle accelerator recreates the stages which initially took place a fraction of seconds after the Big Bang.

1.1 The Large Hadron Collider

The Large Hadron Collider (LHC) is one of the world's largest and most powerful high-energy particle accelerators, delivering center-of-mass energies up to 13 TeV for proton-proton collisions. The LHC is a massive machine with two adjacent beam pipes contained in a circular tunnel with a circumference of 27 km. It is located roughly 100 meters below ground level at the border of Switzerland and France. Figure 1.1 presents a bird's eye view of the LHC, highlighting the physical locations of the various experiments. Inside the tunnel, particles

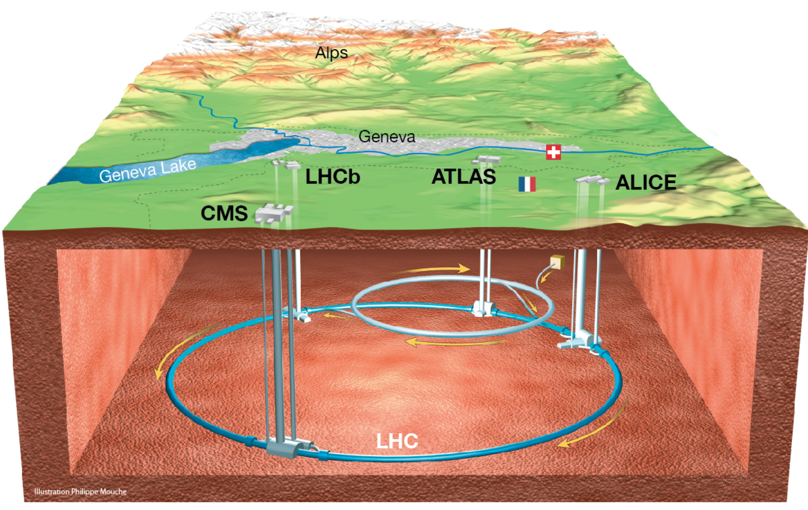


Figure 1.1: An overview of Large Hadron Collider, highlighting various experiments at the beam intersection points. ©2014-2020 CERN [1].

accelerate in opposite directions within the beam-lines and collide together at

multiple intersection points. The four main LHC experiments are installed at the intersection points: ALICE, ATLAS, CMS, and LHCb. These experiments are dedicated to explore different theories within the field of particle physics.

1.1.1 Luminosity

the unit barn (b) expresses the cross-sectional area of nuclei and nuclear reactions. One barn is equivalent to 10^{-28}m^2. For a particle accelerator, the valuable cross-section areas are often within picobarn and femtobarn of range. In order to detect collisions with such small cross-sections, a significant amount of collisions is required within a reasonable amount of time. The *luminosity* $\mathscr{L}$ parameter assesses the ability of a particle accelerator to produce the required number of interactions. $\mathscr{L}$ is further classified into the peak and integrated luminosity.

Peak and Integrated Luminosity

The peak luminosity $\mathscr{L}_{peak}$ is determined by the total number of collisions performed by a detector per cm^2 per second. The value of $\mathscr{L}_{peak}$ depends upon certain parameters presented in Equation 1.1:

$$\mathscr{L}_{peak} = \frac{f \cdot n_1 \cdot n_2}{4 \cdot \pi \cdot \sigma_x \cdot \sigma_y} \tag{1.1}$$

where n_1 and n_2 represents the total number of particles per bunch in beamline 1 and 2, respectively. f is the collision rate with opposite beams at the intersection point. σ_x and σ_y represents bunch transverse size at interaction point.

The integrated luminosity $\mathscr{L}_{int}$ is expressed by taking the integral of $\mathscr{L}_{peak}$ over time, as shown in Equation 1.2, where T is the data collection time of the detector with the delivered luminosity $\mathscr{L}$.

$$\mathscr{L}_{int} = \int_0^T \mathscr{L}(t)dt \tag{1.2}$$

The unit of $\mathscr{L}_{int}$ is cm^{-2}, which is typically expressed as inversed femto-barn (fb^{-1})[1]. $\mathscr{L}_{int}$ expresses the total number of events collected over the accelerator's lifetime, as presented in Equation 1.3, where N is the number of interested events and the σ value is the cross-section of these interested events.

$$N = \mathscr{L}_{int} \cdot \sigma \tag{1.3}$$

For instance to collect 1000 events with a cross-section of 8 fb, the expected $\mathscr{L}_{int}$ is 125 fb^{-1}. To achieve this, the accelerator with $\mathscr{L}_{peak}$ of $1.5 \times 10^{34}\text{cm}^{-2}\text{s}^{-1}$ requires a lifetime of $8.3{\times}10^6$ seconds. Accidental beam-dumps are among the significant causes which minimize the lifetime of the LHC. One of the reasons for the beam-dumps is the radiation-induced Single Event Effects (SEE) within the electronics. The plot in Figure 1.2 represents annual beam-dumps of the LHC due to SEEs on the electronics equipment installed inside the tunnel, as

[1] 1 fb^{-1} is 10^{39} cm^{-2}.

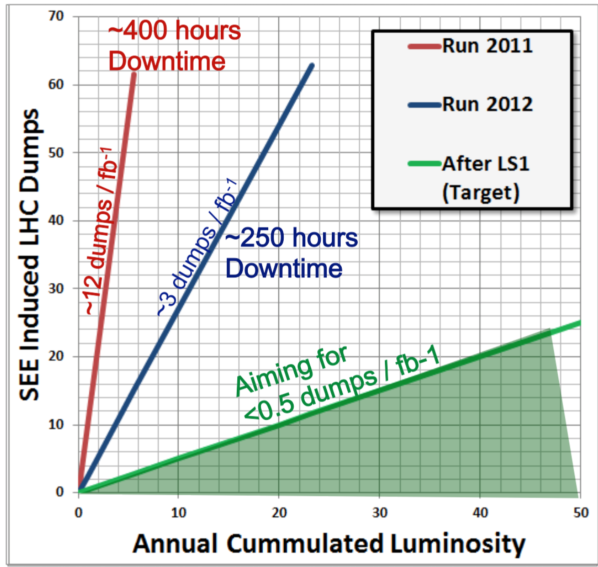


Figure 1.2: LHC beam-dumps due to single event effects against beam luminosity. ©2015-2019 CERN. Reprinted with permission from A.Bignami et al. [2].

a function of beam luminosity. During 2011, the radiation-induced effects on the electronic equipment of the LHC provoked ∼70 beam-dumps, which resulted in ∼400 hours of downtime for the accelerator. Since then, several mitigation techniques have been employed by the Radiation To Electronics (R2E) group at CERN to minimize beam dumps, which are mainly caused by the SEEs on the electronics. The SEE hardness assurance of the LHC electronic equipment is essential to enhance the overall lifetime of the accelerator.

1.2 A Large Ion Collider Experiment

A Large Ion Collider Experiment (ALICE) experiment resides at one of the intersection points of the LHC beam-lines. It studies the outcome of lead-lead, proton-lead and proton-proton collisions, to characterize the properties of strongly interacting matter at extreme energy densities, where a phase of matter called Quark-Gluon Plasma (QGP) is formed [3].

1.2.1 Physics goals

In today's universe, every ordinary matter consists of atoms. Each atom contains a nucleus composed of neutrons and protons, which is surrounded by a cloud of electrons. Both the protons and neutrons are made up of quarks that are vigorously bounded by gluons in a confined state.

The higher temperatures achieved during heavy-ion collisions at the ALICE experiment release quarks from their gluons and transforms them into a state called QGP. The existence of the QGP state and its properties are the key

issues in the theory of Quantum Chromo Dynamics (QCD), which is a strong interaction sector of the Physics Standard Model [4]. The QGP expands and cools, and transforms into a hadronic matter. Due to its short lifetime, the observation of this plasma transition is not directly possible. The ALICE detectors can successfully track footprints of the hadronic state, which contains various properties of the QGP. More details about the physics goals of the ALICE experiment can be found in reference [3, 5].

1.2.2 An overview of the ALICE sub-detectors

The overall dimension of the detector is $16 \times 16 \times 20$ m^3 with a total weight of approximately 10,000 tons. Figure 1.3 represents a schematic layout of all sub-

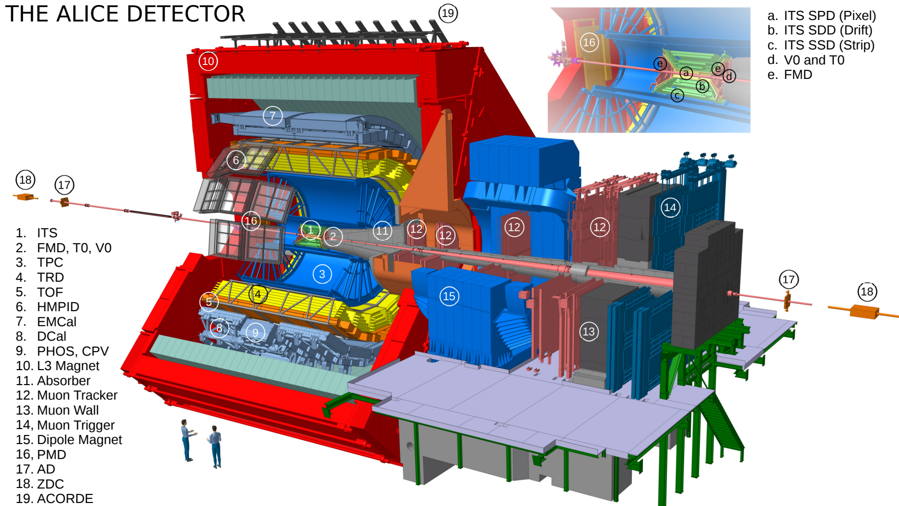


Figure 1.3: A schematic layout of the ALICE sub-detectors. ©2017 CERN, for the benefit of the ALICE Collaboration [6].

detectors of the ALICE experiment. The ALICE experiment consists of a central barrel part which measures hadrons, electrons and photons, and a forward muon spectrometer. From the collision point outwards, the detector layout consists of various tracking detectors, followed by the particle identification detectors, calorimeters, and the muon spectrometer.

1.2.3 The Time Projection Chamber

The Time Projection Chamber (TPC) detector is one of the leading tracking detectors of the central barrel, located close to the beam collision point. It is a gaseous detector with a cylindrical shape. It has an overall length of 510 cm along the beamline, with an inner and outer radius of about 85 cm and 250 cm, respectively. Figure 1.4 presents the layout of the TPC detector, which mainly consists of a field cage and the readout chambers. The detector has an active

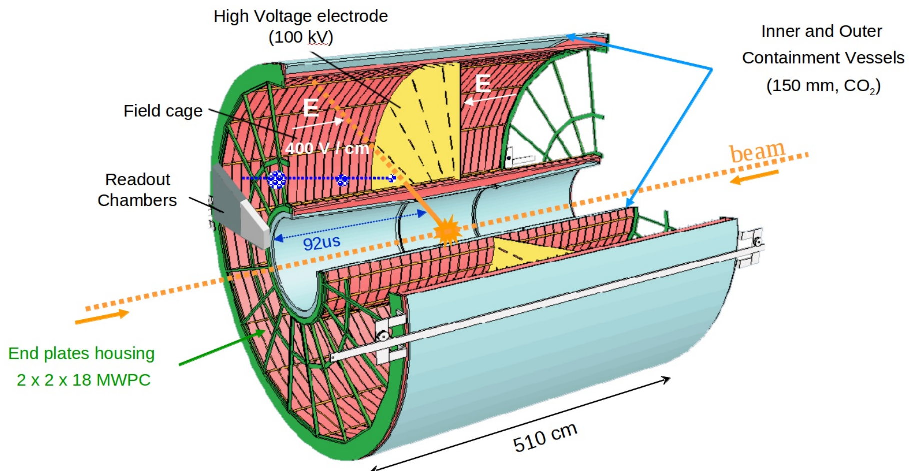


Figure 1.4: A schematic overview of the TPC detector[7].

gas volume of 88 m^3, which is filled with an ionizing gas mixture and serves as a drift medium for the electrons. Inside the field cage, a 30 μm High Voltage (HV) electrode is located in the middle of the detector, dividing the active volume into two halves of equal sizes. In the presence of an electric field, the HV electrode conducts as the positive electrode while the end-plates (readout chambers) act as the negative electrodes.

When a charged particle transverse through the gas volume of the detector, it ionizes gas atoms, leaving a trail of ionization along its track. This ionization trail assists in predicting the trajectory of the particle. When an electric field applies to the gas volume inside the detector, most of the free ions and electrons drift oppositely towards the high voltage electrode and the end-plates, respectively. The interpreting position of electrons at the end-plates provides a two-dimensional information of the transversing particle. Since electrons move towards the end-plates with a constant speed in medium, measuring the arrival time of electrons between the ionization trail and the end-plates provides the third dimension of track. It allows the TPC detector to precisely construct a 3-D trajectory of all charged particles.

Current readout electronics of the TPC detector

The charge of the ionized particles is sensed by 72 Multi-Wire Proportional Chamber (MWPC) based readout chambers, with a total of 557,658 readout cathode pads at the end-plates [8]. The flexible caption cables further transmit the sensed signals (charge) to 4356 Front-End Cards (FEC). The typical distance between the pad plane and the FECs is about 10 cm. Each TPC FEC is populated with 8 PreAmplifier ShAper (PASA)[9] chips and 8 ALice Tpc ReadOut (ALTRO)[10] chips where each chip supports 16 concurrent channels. Thereby, one FEC can simultaneously process signals from 128 pads (channels).

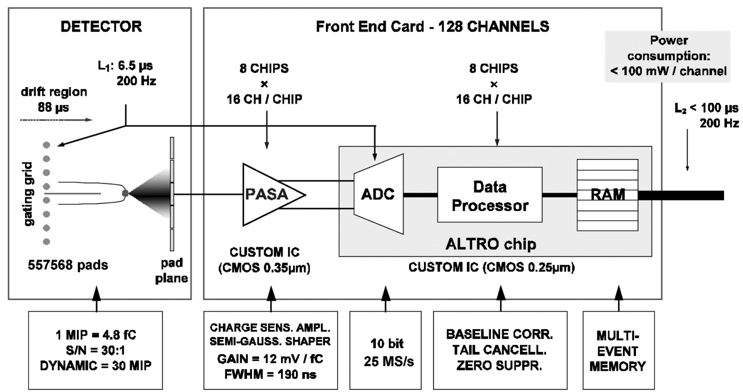


Figure 1.5: An overview of current ALICE TPC Front-End Electronics. Copyright ©2010 CERN for the benefit of the ALICE collaboration. Published by Elsevier B.V. [11].

Figure 1.5 presents an individual channel readout of the ALICE TPC electronics where the PASA chip transforms the induced charge on the detector pads into a voltage signal that transmits further to the ALTRO chip. The PASA chip is a custom-made analog integrated circuit manufactured in Austria Micro Systems 350 nm CMOS technology. The main objective of the PASA chip is to integrate, amplify as well as shape the collected charge from the TPC detector pad.

The ALTRO chip is a mixed analog-digital custom integrated circuit that is designed and optimized for the ALICE TPC readout electronics detector. It can process data from 16 concurrent channels simultaneously, where each channel consists of a commercial 10-bits 25-MSPS Analog to Digital Converter (ADC) from the ST microelectronics, followed by a pipelined Data Processor and the multi-acquisition data memory. The ALTRO chip is operated at 2.5 V of nominal supply voltage and manufactured in the ST 250 nm HCMOS-7 technology.

The ALTRO chip requires two levels of triggers from the Central Trigger Processor (CTP) in order to process data to the Readout Control Unit (RCU). Level 1 (L1) trigger arrives 6.5 μs after the interaction, which initiates the readout activity of the TPC detector. The event data is sampled, processed, and stored in the data memory of a Multi-Event Buffer. The maximum readout speed of the ALTRO chip is 40 MHz, where the data is transmitted on a 40-bits wide bus, providing a total bandwidth of 200 MByte/s [5].

1.3 LHC after LONG SHUTDOWN 2

The LHC started its initial RUN 1 phase in 2009, which completed in January 2013. During this period, an integrated luminosity of 30 fb^{-1} accumulated with a peak luminosity of 7.7×10^{33}cm^{-2}s^{-1}. This data set is valid for the ATLAS and CMS experiments at 8 TeV center-of-mass proton collisions. Smaller data sets are achieved for the LHCb and ALICE experiments.

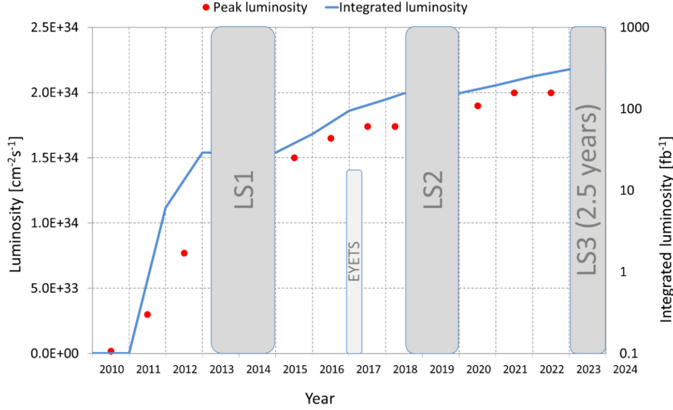


Figure 1.6: LHC luminosity plan from RUN 1 to RUN 3 [12]. RUN 3 will start from 2021.

Figure 1.6 presents the roadmap of the LHC luminosity upgrade till 2023 where three main Long Shutdown periods LS1, LS2 and LS3 are emphasized, with the desired $\mathscr{L}_{peak}$ and $\mathscr{L}_{int}$ parameters. During RUN 2 phase, 13 TeV of center of mass energy was achieved during the pp collisions with $\mathscr{L}_{peak}$ of $10^{34}\mathrm{cm}^{-2}\mathrm{s}^{-1}$. The accumulated $\mathscr{L}_{int}$ was about 100fb $^{-1}$.

In 2019, the LHC planned another major upgrade during LS2, followed by a RUN 3 period in 2021. During RUN 3, the LHC will reach $\mathscr{L}_{peak}$ of 2-3$\times10^{34}\mathrm{cm}^{-2}\mathrm{s}^{-1}$ and deliver $\mathscr{L}_{int}$ of about 300 fb^{-1}. One of the primary objectives of the LS periods is to increase both the mass energy and the luminosity of the LHC to discover the universe beyond the Standard Model [4]. Consequently, the infrastructure of the LHC detectors requires several upgrades to achieve this goal.

1.3.1 The upgrade strategy for the ALICE experiment

During RUN 1 Pb-Pb collisions in the ALICE experiment, the $\mathscr{L}_{peak}$ reached up to $5\times10^{26}\mathrm{cm}^{-2}\mathrm{s}^{-1}$ at a center of mass energy of 2.76 TeV. Before LS2, the ALICE experiment collected 1 nb^{-1} Pb-Pb collisions at the peak luminosity up to 1×10^{27} - $4\times10^{27}\mathrm{cm}^{-2}\mathrm{s}^{-1}$ which corresponds to a collision rate of 8 kHz [13, 14]. For the Pb-Pb events, the maximum readout rate of the present ALICE detector is limited to 500 Hz. During RUN 3, the ALICE experiment is planning to acquire 10 nb^{-1} of Pb-Pb collisions, at a peak luminosity of $6\times10^{27}cm^{-2}s^{-1}$ and an interaction rate of 50 kHz. In contrast to RUN 1, the data collection rate for Pb-Pb collisions will increase by a factor 100 after these upgrades.

In order to fully utilize the high luminosity provided by the LHC after LS2, the ALICE collaboration has undertaken significant upgrades to enhance the data acquisition rate of the events by, for instance, allowing continuous readout of the detectors. This thesis has mainly contributed to the readout electronics upgrades of the ALICE TPC and MCH detectors for RUN 3.

TPC upgrade during RUN 3

The current readout chain of the ALICE TPC detector utilizes MWPC based technology. This is one of the limiting factors in achieving the desired readout rate of RUN 3. It leads to a drift time of 100 μs for electrons from the central electrode to the readout chambers, together with the ions drift time of 180 μs from the sense wires to the gating grid. This corresponds to a dead time of $\sim$280 μs (3.5 kHz) between each interaction.

With the expected interaction rate of 50 kHz during RUN 3, the present drift time is five times longer than the average time between interactions. In this context, the present MWPC based technology will be replaced by the Gas Electron Multiplier (GEM) based technology [15, 16]. The GEM based technology promises reliable operation in high-speed environments, which resolves the problem of longer drift time in the TPC readout electronics. However, it also implies a complete redesign of the TPC front-end electronics and the readout system.

Gas Electron Multiplier

Figure 1.7 illustrates the working principle of both MPWC and GEM based technology. In the MWPC based technology, the multiplication takes place closer to the anode wire that collects electrons and serves as the readout electrode. For

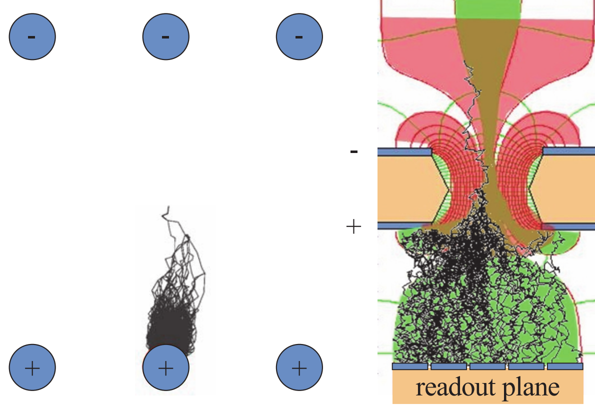


Figure 1.7: Working principle of MWPC (left) and GEM (right) illustrated. Black paths are electron trajectories, the drift of ions is not indicated. Copyright © 2013 by JACoW — cc Creative Commons Attribution 3.0 (CC-BY-3.0) [16].

the GEM foil, the energetic field is formed in millions of microscopic holes in a dielectric foil by biasing the top and bottom electrodes. A simulated field line pattern in one GEM hole is presented in Figure 1.7 which strongly focuses in the center of the hole. The GEM foil screens the drift of ions (above the GEM) from the readout plane (below), which eliminates the characteristic ion tails, compared to the MWPC based technology.

In the MPWC-based technology, ions generated in the avalanche remain in the gas for tens or hundreds of μs, reducing the field strength around the anode wires (and therefore the gas gain). The ions generated in a GEM avalanche leave the hole within a time window of 100 ns, resulting in a higher readout throughput. Reference [15, 16] presents more comprehensive details regarding the GEM-based topology.

ALICE Muon Chamber upgrade during RUN 3

To support an interaction rate of 50 Hz during RUN 3, the readout rate of the Muon CHamber (MCH) detector is set to 100 kHz, including a safety margin for the Pb-Pb collisions. However, the present triggering source (Muon Trigger) of the MCH detector only supports a maximum trigger rate of 1 kHz for data readout. Another limitation is the digitization of 64 analog channels only via two ADCs mounted on the FECs, which leads to a longer dead-time between interactions. More details about the current readout electronics of the MCH detector can be found in reference [17].

For RUN 3, the MCH readout adopts a new architecture where the signals will be sampled continuously. It consequently requires an upgrade of the present FECs and the readout electronics of the MCH detector.

1.4 Scope of this work

In order to overcome challenges for both the TPC and MCH detectors during RUN 3, a dedicated readout ASIC named "SAMPA" is developed to fulfill the requirements of both detectors. With the increased interaction rate expected during RUN 3, the radiation load on the new front-end electronics will consequently also increase. As the SAMPA chip is fabricated in a commercial CMOS process, it is imperative to assess radiation tolerance of the chip before the ALICE detectors can employ it. The work presented in this thesis has evaluated the radiation tolerance of the SAMPA chip, with the main focus on the single event effects (SEE) qualification of the SAMPA chip for the foreseen radiation levels at the ALICE detectors after the LS2. For instance, an unwanted change of state (bit-flip) in a memory element may interrupt the readout acquisition system of the ALICE detectors. For the worst-case scenario, it can require a complete halt of the ALICE experiment to remove and correct the state. The following points summarize the scope of this work:

- Evaluate radiation-induced soft error sensitivity of the SAMPA chip. It includes an in-depth understanding of both analog and digital blocks of the SAMPA chip as well as the radiation sensitivity analysis of these blocks.

- Identify possible mitigation actions that are required to ensure the correct and acceptable behavior of the SAMPA chip in the ALICE radiation environment. It also involves discussions on what is meant by the acceptable behavior. For instance, the consequences of radiation-induced errors within various parts of the SAMPA chip can help to conclude whether the system can tolerate a guaranteed rate of failure for these affected parts.

- The selection of appropriate irradiation facilities with a proton or neutron beams is essential to predict the expected failure rate for the ALICE detectors. Occasionally, other relevant sources (heavy-ions or pulsed-laser) are considered for characterizing a particular type of radiation-induced error.
- Conduct an irradiation campaign on the first SAMPA prototype to obtain an earlier radiation-induced error sensitivity indication of the technology node.
- Execute irradiation campaigns on the consecutive prototypes with the increased functionality and improvements against radiation-induced errors. It also involves the evaluation of implemented radiation-induced error mitigation techniques within the consecutive prototypes.

1.4.1 SAMPA Collaboration

Several institutes associated with the ALICE experiment were involved in the design and characterization of the SAMPA chip. FAPESP[2] primarily funded the development of the SAMPA chip. This has been a collaborative project between the Electrical Engineering, Polytechnic School of University (EPUSP), and the Institute of Physics (IPUSP) at the University of São Paulo, Brazil.

The initial design of the SAMPA chip started back in 2013 and spanned over five years with various prototypes. Hugo Daniel Hernandez Herrera (from EPUSP) designed the analog front-end of the SAMPA chip. On the digital side, the first SAMPA prototype was designed by Heitor Guzzo Neves (from EPUSP). Bruno Sanches (from EPUSP) and Arild Velure[3](from the University of Bergen) developed the digital design of the subsequent prototypes. The carrier boards of the SAMPA prototypes were developed by the IPN (Institut de Physique Nucleaire) group in Orsay, France.

1.4.2 Main contributions

It is essential to highlight that the work presented in this thesis concerning the general design of the SAMPA chip, and in particular, mitigation techniques to enhance the radiation tolerance of the SAMPA chip, is primarily performed by the SAMPA design team. Nonetheless, I was actively involved in discussions and suggestions to employ necessary mitigation techniques for the radiation tolerance enhancement of the SAMPA prototypes.

I have also anticipated in the design phase of the first two prototypes (MPW1 and V2) of the SAMPA chip in closer collaboration with the leading design team. Once the prototypes were fabricated, I performed post-silicon verification of the prototypes and shared results with the SAMPA collaboration during weekly

[2]FAPESP = Fundaccão de Amparo à Pesquisa do Estado de São Paulo/São Paulo State Research founding agency.

[3]Arild Velure also developed FPGA-based Data AcQuisition (DAQ) system for the SAMPA prototypes.

meetings. Since these tasks are not directly relevant to the Ph.D. research topic, they are not presented here[4].

During the campaigns, the communication with the SAMPA prototypes was performed via the FPGA-based Data AcQuisition (DAQ) system, primarily developed by Arild Velure. Nonetheless, I provided several functionality suggestions to optimize the DAQ system for the campaigns and executed several modifications for the final optimization of the DAQ system prior to the campaigns. I also proposed recommendations during the design and manufacturing of the SAMPA carrier boards.

I was entirely responsible for tasks related to the radiation hardness assurance of the SAMPA prototypes. It mainly consisted of: (i) planning various campaigns according to the projected submission deadlines of the prototypes, (ii) ensuring proper preparation and execution of the campaigns, and (iii) analysis of acquired results from the campaigns. A successful irradiation campaign involves several tasks, such as appropriate facility selection, equipment transport, physical setup preparation (reliable cables and connections), firmware development, and the ability to execute critical actions during the campaigns. The actual irradiation campaign is not the most time-consuming part by far, compared to all the preparations and data analysis tasks.

Outcomes of the campaigns were thoroughly analyzed to understand the consequences of radiation-induced errors in the ALICE radiation environment. The results were further shared and discussed with the SAMPA collaboration. Accordingly, design improvements were implemented in the consecutive prototypes. For instance, a potentially destructive radiation-induced failure was discovered during one of the campaigns. It triggered concern among the SAMPA collaboration as the failure interfered submission of the consecutive prototype. I urgently conducted subsequent campaigns to prevent further delays in the submission of the consecutive prototype. The objective of these campaigns was to identify the exact location of the radiation-induced failure in the prototype as well as to provide an appropriate remedy for the consecutive prototype.

In this thesis, all conclusions regarding the consequences of radiation-induced soft errors in the SAMPA prototypes were made with close interactions and discussions with the design team.

1.5 Chapter Organization and Overview

This thesis has eight chapters, including this introductory chapter. An overview of the rest of the thesis is as follows:

- Chapter 2 provides an overview of the fundamental radiation-matter interaction mechanisms, with a focus on radiation-induced failures in semiconductor devices. The particle composition of the LHC radiation environment is briefly discussed and compared with other relevant irradiation environments. It also presents foreseen irradiation levels for the readout electronics of the ALICE detectors after LS2.

[4]The presentations are available online at reference [18, 19, 20, 21].

- Chapter 3 presents an upgraded readout system of both TPC and MCH detector. An architectural overview of both analog and digital blocks of the SAMPA chip is presented with the main focus on the soft error handling mechanisms within the digital block.
- Chapter 4 describes the test setup for the irradiation campaigns. Two independent test setups were prepared to cover both the hard and soft SEE errors.
- Chapter 5 presents radiation-induced soft error results from the first two prototypes of the SAMPA chip. High energy proton campaigns were conducted at The Svedberg Laboratory (TSL) in Uppsala, and the AGOR Facility for IRradiation of Materials (AGORFIRM) in Groningen.
- Chapter 6 provides radiation-induced hard error results from both proton campaigns. The second prototype was susceptible to Single Event Latch-up (SEL) events, which was further investigated by conducting the heavy-ions campaign at the Heavy-Ion Facility (HIF) in Belgium. Two experimental methods were employed to localize the source of SEL events in the prototype: (i) Dedicated collimators were prepared during the heavy-ions campaign to identify the primary source of SEL events, and (ii) a pulsed-laser campaign was conducted to gain in-depth insight of the SEL sensitive regions with μm resolution.
- Chapter 7 discusses several design improvements to resolve the SEL issue in the final versions of the SAMPA chip. In addition, the results from the final heavy-ions campaign are presented.
- Chapter 8 summarizes the results from all campaigns and provides the expected failure rates of various kinds of SEEs in the ALICE radiation environment. It emphasizes some limitations of this work with suggestions for improvements in the future. The thesis concludes by providing the on-going status of the SAMPA project.

Chapter 2

Background

The objective of this chapter is to present the fundamental knowledge about radiation-induced effects in the semiconductor devices. This chapter contains several distinct, yet similar topics related to radiation-induced effects in the semiconductor devices, as well as the most common mitigation techniques to enhance the radiation tolerance of the devices.

2.1 Radiation interaction in matter

Radiation is the process of transmitting energy through space or matter in the form of energetic particles or electromagnetic waves. An overview of how radiation interacts with matter is essential to understand radiation-induced damage in electronics, mainly in the semiconductor devices. According to reference [22], radiation interactions with matter mainly classifies into electromagnetic, weak, and hadronic interactions. Reference [22] provides extensive details about the electromagnetic and weak interactions. The hadronic interactions are of utmost importance for this thesis since it can lead to the single event effects (SEEs) in the LHC environment.

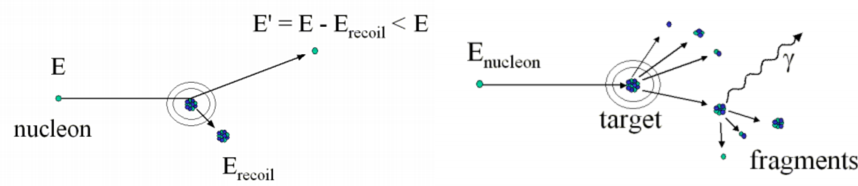
2.1.1 Hadronic interactions

A hadronic interaction is also known as a *nuclear* or *strong* interaction. It mainly occurs due to a significant closer distance between the trajectory of the incoming particle and the nucleus of the atom. Particles coupled to the strong force (such as protons, neutrons and pions) are subject to the hadronic interactions. An hadronic interaction occurs when the incident particle's energy is equal to or higher than the Coulomb barrier [22]. Since the neutrons have no charge, they do not frequently interact with the orbital electrons of the electric field. Nevertheless, while traversing close enough to the nucleus of an atom, they may initiate nuclear interactions in the matter. The hadronic interactions are further categorized into the elastic and inelastic interactions.

Elastic collisions

In elastic nuclear collisions, an incoming particle deflects from its original trajectory and deposits some fraction of its kinetic energy into the nucleus of the atom. No excitation or fragmentation takes place and the natural energy state remains unchanged. It leads to a local indirect ionization along the recoil path.

Most of the silicon recoils created by the elastic collisions have rather low energies. For instance, with an initial neutron energy of 125 MeV, 5% of the interactions deliver a recoil with an energy larger than 0.27 MeV, and only 0.1% of the interactions exhibit recoil energy above 1.5 MeV [23].



(a) Elastic nucleon nucleus collision. *(b) Inelastic nucleon-nucleus collision.*

Figure 2.1: Processes involved during the hadronic interactions with matter [22].

Inelastic collisions

A considerable amount of energy interchanges during an inelastic process, where a substantial amount of energy of the incident particle transforms into the excitation or break-up of the nuclei. The excited states may later decay by the gamma rays or experience further break-ups, as illustrated in Figure 2.1b.

An inelastic nuclear collision produces secondary protons, neutrons, and pions during the initial state. Additionally, an excited intermediate nucleus [24] is created. This intermediate nucleus subsequently de-excites by the emission of the gamma rays, and finally transforms into a stable and lighter residual nucleus. These particle generating processes take place at the expense of the binding energy of the parent nucleus. Secondary fragments from the second reaction stage consist of protons, neutrons, light ions (deuterons, tritons, and helium), and a heavy residual nuclei such as magnesium, oxygen, or carbon. Besides neutrons, all reaction products contribute to the electronic ionization energies.

2.2 Cumulative radiation effects in electronics

Cumulative effects occur due to long-term exposure of an electronic device in a radiation environment, which in turn creates or activates microscopic defects in the device. Over the time, the gradual accumulation of these microscopic defects degrades the electrical properties of the device, which can ultimately lead to failure when the device reaches its tolerance limits. Therefore, it is possible to foresee when the failure will happen for a particular device. The cumulative effects are mainly categorized in the total ionizing dose (TID) and displacement damage (DD) effects [25].

2.2.1 Total ionizing dose

Ionization of matter is caused by interaction between the atoms in the matter and high energy photons or charged particles, such as protons, electrons and heavy ions. Charged particles generate electron-hole (e-h) pairs when passing through the matter. This further leads to the ionization damage, where the density of generated e-h pairs is proportional to the energy transferred to the matter.

In semiconductor devices, the TID effect deposits energy in silicon dioxide (SiO_2). In the presence of an electric field, the recombination process of the

generated e-h pairs in SiO_2 is usually slower than in the substrate (Si) material, and both electrons and holes start to drift within the electric field. Due to higher mobility, electrons quickly leave the oxide. The holes can either be trapped in the defect centers of the oxide or migrate to the Si-SiO_2 interface traps via hydrogen reactions. Both these effects accumulate to degrade the long-term reliability of the semiconductor devices [25].

The TID effect can alter the threshold voltages of the modern Metal-Oxide-Semiconductor (MOS) transistors due to trapped charges (e-h pairs) in the SiO_2 gate insulator. The TID effect can also degrade the mobility and transconductance properties of the MOS transistors. It can also increase the leakage currents and result in higher noise and mismatch between the transistors.

Most of the commercial CMOS processes can typically withstand a dose of few kRad without significantly degrading the performance of the device. According to reference [26], most of the commercial components can accumulate 5 kRads of TID without performance degradation. Some components can even withstand up to 20 kRad or more, and a few may fail before 1 kRad. Hence, it is impossible to predict which category a commercial component may fall into without conducting a TID qualification campaign of the component. According to reference [27], some of the modern CMOS technologies can withstand a dose up to several hundred kRads, compared with the older technologies.

2.2.2 Displacement Damage

The DD effects are induced by the atomic displacement in the active layer of a semiconductor device, defecting the crystal lattice of the device. Non-Ionizing Energy Loss (NIEL) is the primary interaction mechanism of this effect [28], which is commonly expressed in the unit of particle fluence.

According to reference [25], the macroscopic effect of DD varies with the semiconductor technology. Typically, the CMOS technology is tolerant against the DD effects up to the particle fluences expected at the LHC environment. In the bipolar devices, the DD effect can increase the base current of the transistor, which can further impact the gain of the transistor. Reference [25] reports that the DD effect can be foreseen in the bipolar devices beyond 50 MeV protons fluence of about 3×10^{11} p/cm^2. The DD effect can also degrade the performance of other devices, such as photo-detectors and optocouplers.

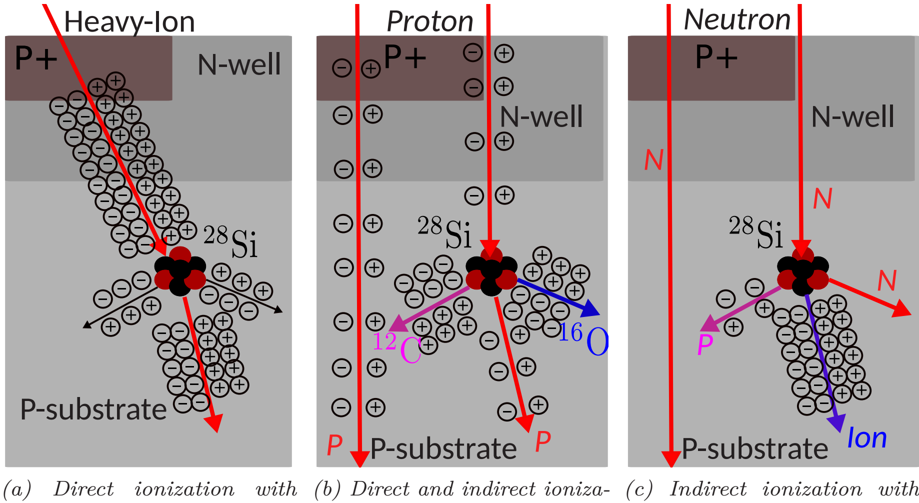
2.3 Single event effects mechanisms

In contrast to cumulative effects, the short-time response due to the energy transfer of an ionized particle within a semiconductor device causes the single event effects (SEEs). A SEE event can exhibit failure in a device at any time, and its probability expresses in terms of its cross-section (σ) value. When an energetic particle strikes the substrate of a semiconductor device, an electrical charge is deposited along its particle track, either by direct or indirect ionization.

2.3.1 Direct Ionization

Direct ionization occurs due to Coulomb interactions between the incoming charged particles and the atoms of the semiconductor device. The incoming charged particle frees e-h pairs along its path in the device as it loses energy. When all of its energy is lost, the particle comes at rest in the matter, having traveled a total path length, typically known as the particle's range. It is typically expressed as the linear energy transfer (LET)[1].

The direct ionization mechanism involves no intermediate steps, and the interaction occurs directly between the incoming particle and the semiconductor device. Figure 2.2a presents this mechanism, where an incoming heavy-ion creates a density of e-h pairs in the semiconductor device.



(a) Direct ionization with heavy-ions. *(b) Direct and indirect ionization with protons.* *(c) Indirect ionization with neutrons.*

Figure 2.2: Illustration of direct and indirect ionization in silicon by heavy-ions, protons and neutrons.

2.3.2 Indirect Ionization

While traversing through matter, most of the protons create e-h pairs through direct ionization mechanism. The density of these e-h pairs is insufficient to provoke SEEs, as illustrated in Figure 2.2b[2]. However, as the technology scaling trend decreases the critical charge threshold, the SEEs can also occur due to direct ionization mechanism of protons [30]. Since neutrons carry no charge, they only create e-h pairs due to nuclear reactions within the silicon nucleus, as illustrated in Figure 2.2c.

[1] The LET expression is used to describe the energy loss per unit path length of a particle as it passes through a matter.

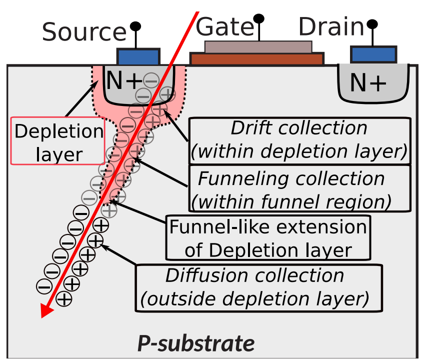
[2] According to reference [29], only 1 out of 10^5 protons will have a nuclear reaction in 4μm silicon device.

Both protons and neutrons may undergo inelastic collisions with the target nucleus. It can further lead to one of the following nuclear reactions [31]: (i) Interaction with the target material, leading to elastic collisions, which further produce Si recoils, (ii) the emission of alpha or gamma particles and the recoil of a daughter nucleus (e.g., silicon emits alpha particles and a recoiling Magnesium nucleus), and (iii) spallation reactions in which the target nucleus is broken into two fragments (e.g., Si breaks into Carbon and Oxygen ions), each of which can recoil.

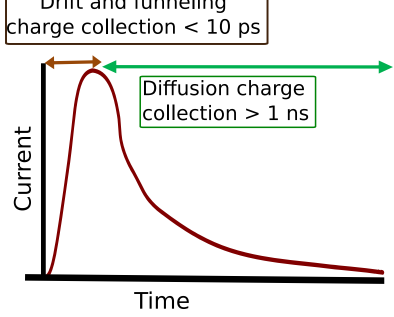
Any of these nuclear reactions can deposit sufficient energy along their paths by direct ionization mechanism, resulting in SEEs. Among these nuclear reactions, the spallation reaction creates the highest density of e-h pairs in which the compound nucleus breaks up into heavy fragments[3]. These nuclear reactions are energy-dependent of the incident particles, and the cross-section of all nuclear reactions is relatively constant above 60 MeV of incident energy [31].

2.3.3 Fundamental charge collection mechanism for Single Event Effects

Once the charge is deposited within the semiconductor device, either by direct or indirect ionization mechanism, the electric field in the device collects only a fraction of the created charge. In modern CMOS devices, the high electric



(a) Ionized particle interaction with p-n junction of CMOS structure.



(b) Resultant current pulse.

Figure 2.3: Charge collection mechanisms nearby the reverse-biased junction of a CMOS device.

field present in the depletion layer of the reverse-biased pn-junction is the most sensitive region for charge collection [33]. This region is often referred to as the Sensitive Volume (SV) of a device, and the density of e-h pairs in this region determines whether a SEE will take place or not. For instance, if particle-induced e-h pairs do not reach the pn-junction, an inferior amount of charge will be

[3] The maximum LET of these heavy fragments reported in reference [32] is about 16 $\mathrm{MeVcm^2mg^{-1}}$.

collected in the SV area, and the probability of inducing SEE will be much lower. Figure 2.3a demonstrates three main charge collection mechanisms near the p-n junction region [34]:

1. The drift mechanism is responsible for the charge collection within the depletion region.

2. The ionizing particle may cause a temporary funnel-like extension of the depletion region deeper into the substrate, due to concurrent distortion of the potential inside the depletion region [35]. The charge collection within this funnel region is known as the funneling collection.

3. The charge which is induced outside the depletion region but within the diffusion length of the charge carriers, which is collected by the diffusion process. Any additional charge can be collected as the electrons diffuse into the depletion region on a longer time scale until all excess carriers have been collected, recombined, or diffused away from the junction area.

The collected charge flows towards the electrodes in the presence of an electric field, resulting in a transient current at the junction node. Figure 2.3b demonstrates the response of the current pulse, which is dominated by a faster drift and funnel process time τ_β, followed by a slower diffusion process time τ_α. The resulted current pulse is traditionally defined as a double exponential function presented in equation 2.1 [36], where Q is the collected charge in femto coulomb unit at the sensitive node.

$$I(t) = \frac{Q}{\tau_\alpha - \tau_\beta} \cdot (e^{-\frac{t}{\tau_\alpha}} - e^{-\frac{t}{\tau_\beta}}) \tag{2.1}$$

The overall impact of the transient current depends upon its intensity and the number of impacted nodes within a circuit. This transient current is the fundamental for inducing almost all kinds of SEEs within the microelectronic devices.

2.4 Single Event Effects in microelectronic devices

The digital circuits are more sensitive to SEEs than their counterparts due to several reasons:

- The transistors of the digital circuits are usually smaller in size to enhance the speed performance. Therefore, less charge is required to flip the state of a transistor.

- Generally, digital circuits do not utilize particular layout techniques (Guard rings, triple N-well, and dummy components), and automatic routing is executed to connect several metal layers.

- The digital circuits occupies most of the areas in the modern ASIC designs, which increases the probability of SEEs.

The critical charge (Q_{crit}) is the main parameter to determine the soft error sensitivity of a circuit. It is the minimum amount of charge that must be collected at the sensitive node of the circuit to cause a soft error. If the collected charge Q_{coll} is higher than Q_{crit}, a soft error occurs. A simpler model to determine Q_{crit} is presented in equation 2.2 [37]:

$$Q_{crit} = C_n \cdot V_n + I_{rstr} \cdot t_{sw} \tag{2.2}$$

where C_n and V_n are the equivalent capacitance and voltage at the stuck node, I_{rstr} is the restoring current provided by the feedback, and t_{sw} is the time required to flip the state of the stuck node.

According to reference [38], the SEEs are divided into single event upset (SEU), multiple bit upset (MBU), multiple cell upset (MCU), single event functional interrupt (SEFI), single event latch-up (SEL), single event transient (SET), single event burnout (SEB), and single event gate rupture (SEGR). This thesis primary evaluates SEU, SET, and SEL events within the SAMPA prototypes.

2.4.1 Single Event Upset

SEU events in the CMOS integrated circuits are dominated by the storage elements such as static random access memories (SRAM) and sequential circuits such as latches and flip-flops (FFs). If the deposited charge exceeds the critical charge (Q_{crit}) at the respective sensitive node within a storage element, the stored value at that node may flip, which further alters the output state of the storage element. Both SRAM and sequential cells from the standard digital library typically utilize aggressive design rules, which are favorable for provoking SEU events[4].

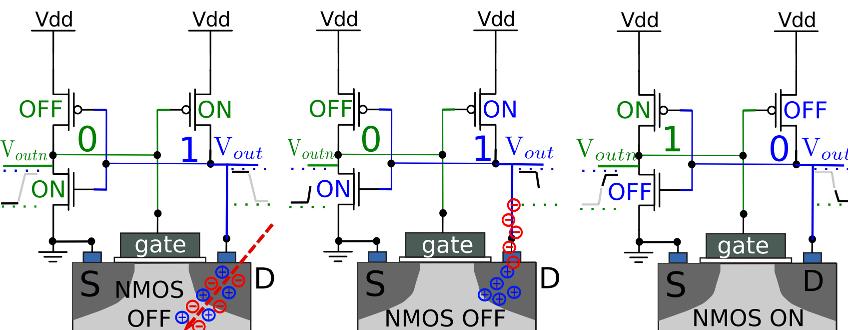
Single Event Upset in SRAM cell

For a conventional six-transistors (6T) SRAM cell, the most SEU sensitive nodes are the reverse-biased p-n junctions at the drain terminals of the non-conducting (OFF) transistors. The charge collected at the drain terminals of the conducting transistors enhances the ability to hold the stored value. The source terminals of the pMOS and nMOS transistors are often connected to the V_{DD} and GND power rails, respectively.

Figure 2.4 illustrates a series of stages involved in triggering SEU in an SRAM cell. For the sake of simplicity, the figure does not show the access pass transistors. A cross-sectional layout substitutes the nMOS transistor symbol at the right-hand in order to provide an in-depth understanding of the charge generation and collection mechanisms within the SRAM cell.

In Figure 2.4a, an ionizing particle strikes the reverse-biased drain junction of the non-conducting nMOS transistor. As a consequence, e-h pairs are generated, where the electrons start to migrate towards the positive terminal, as illustrated in Figure 2.4b. It induces a transient current which flows through the struck junction, while the conducting pMOS transistor in the same inverter sources

[4]Due to minimum transistor current drives and capacitance.



(a) Ion strikes drain of an OFF nMOS transistor. *(b) Charge is collected and voltage drop at V_{out}.* *(c) Feedback is triggered and SEU occurs.*

Figure 2.4: SEU mechanism in a CMOS SRAM cell.

the current in an attempt to balance the particle-induced current. However, since the conducting pMOS transistor has limited current driving strength, the voltage at V_{out} node starts to gravitate. If the voltage drops below the switching threshold of the cross-coupled inverter, and the drop lasts for a long enough time, the feedback inverter turns on. This causes the SRAM cell to change its initial stored state, creating an SEU event, as presented in Figure 2.4c.

Single Event Upset in flip flops

The typical master-slave structure of a conventional D-FF is presented in Figure 2.5. When the clock is high, the master latch holds the output value Q in its

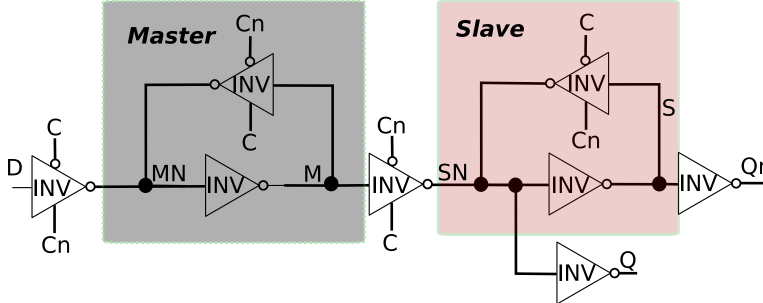


Figure 2.5: Simplified flip flop diagram presenting the SEU sensitive nodes [39].

feedback while the slave latch becomes transparent. When the clock is low, the master latch becomes transparent, and the slave latch holds the Q value in its feedback. Hence there is an even probability of capturing a bit-flip from either of the latches. Thereby, when the clock is high, an SEU can occur in the master latch, which can further propagate to the slave latch when the clock goes low. When the clock is low, the SEU can appear in the slave latch, which can further propagate to the output node.

Comparison of critical charge between SRAM and flip-flop

The critical charge Q_{crit} and the charge collection Q_{coll} efficiency of the sensitive nodes determine the soft error sensitivity of both the SRAM and FF cells. These values depend upon several parameters such as gate length, substrate structure, the bias of the circuit nodes, substrate's doping level, and the LET energy of the incident particle [38]. Additionally, Q_{crit} depends on the node capacity and the supply voltage, as presented in Equation 2.2. Since the structure of both SRAM and D-FF cells consists of an active feedback loop, Q_{crit} also depends upon the strength of the feedback transistors.

In an SRAM cell, Q_{crit} is mainly identical for both storage nodes since the physical dimensions of the cross-coupled inverters are identical, making the SRAM cell symmetrical. The inverters are sized differently in the FF latches, which provides different fan-out values and makes the FF cell asymmetric. Thereby, the individual storage nodes in the FFs have different Q_{crit}, and their soft error sensitivity can vary with several orders of magnitude [40]. This asymmetry forms a fundamental difference between the soft error sensitivity of both cells.

In reference [39], the Q_{crit} is determined for multiple internal soft errors sensitive nodes of a conventional FF cell. The simulations were performed in SPICE using 130 nm CMOS technology with 1.2 V of supply voltage, which is relatively comparable with the SAMPA chip specifications. The simulation results demonstrate that depending upon the location of the particle strike within the FF, the Q_{crit} can alter significantly. For instance, when storing the high logic values at sensitive nodes M and S, the Q_{crit} is respectively 11.6 fC and 15.5 fC, to flip the state. For low logic values, the Q_{crit} is only 2.8 fC and 3.2 fC for identical nodes. Hence, 1→0 bit-flip will acquire more charge from the incoming particle than 0→1 bit-flip.

The physical phenomena behind higher Q_{crit} values while holding high logic state can be related to the physical dimensions of the cross-coupled inverters. Additionally, since positive holes may also drift to P+ diffusion and P-substrate regions of the pMOS transistor, the collected charge can be lesser than the deposited charge at the pn junction for the respective transistor.

2.4.2 Single Event Transient

The SET is a voltage transient induced by the charge deposition of an ionizing particle path. The SETs can be temporary voltage fluctuations on the output of the analog circuits (amplifiers, buffers, shapers, comparators), known as Analog Single Event Transients (ASET). The duration of these ASET events is typically within the 10^{-12}s range and thereby does not impose any severe effect on the overall performance of the analog circuits. Nevertheless, when the output of an analog circuit is fed into an Analog to Digital Converter (ADC), the time window of the ASET event determines whether the ADC will sample the voltage fluctuation or not. For instance, if the ASET event occurs near the sampling window of the ADC, it can be sampled and digitized by the ADC. Reference [41] presents more comprehensive details about the ASET events.

The SET events can directly impact output or intermediate nodes of the digital gates due to lower node capacitance. Both sequential and combinational gates can suffer SET events. In sequential circuits, a SET event can cause bit-flips if it fulfills the following criteria [42]:

1. The incoming particle produces sufficient charge to induce a voltage/current transient to propagate in the circuit.

2. There is an open propagation path through active combinational logic paths for the SET event to reach the memory element.

3. The SET event has sufficient amplitude and duration to alter the output state of the latch/memory.

4. The SET event arrives during the active clock of the memory element. Hence, the probability of capturing a SET event is proportional to the clock frequency.

The overall impact of a SET event mainly depends upon the functionality of the affected digital gate. For instance, the memory elements might not capture a SET event from the combinational logic gates due to logical, electrical, or latching-window masking phenomena [43]. Nevertheless, SET events can cause system failure if induced within the clock or reset distribution networks of the digital circuits. Reference [44] reports that the SET events are capable of sinking through several levels of clock and resetting network trees after reaching the controlling FFs. Consequently, this can result in simultaneous bit-flips within multiple FFs, or even partial/complete reset of the chip.

2.4.3 Single Event Latch-up

The SEL is caused by the passage of a single energetic particle through the sensitive regions of s device structure. The SEL triggers the internal parasitic thyristor structure within a CMOS device, forming a low impedance path between the power rails. It further leads to an abnormal high-current state within the device and is typically corrected by power cycling the device. If the SEL event is left uncorrected for a more extended period, the high-current path can cause melting and permanent damage to the device. Hence, an SEL event is usually considered as a destructive event.

Figure 2.6 illustrates a typical configuration of N-type and P-type regions within a CMOS inverter, creating two parasitic bipolar junction transistors (BJTs). The nMOS source terminal (as an emitter) and the N-well region transforms the L_{npn} BJT, where the P-substrate region acts as the base terminal. The pMOS source terminal (as an emitter) and P-type substrate construct the V_{pnp} BJT, where the N-well region acts as the base terminal. The base terminals of both L_{npn} and V_{pnp} transistors are connected to the GND and V_{DD} taps, respectively. The parasitic resistances (R_{bs} and R_{bw}) create the across emitter-base junctions of both BJTs. R_{bw} is the substrate resistance that strongly depends upon the substrate structure, whereas R_{bw} is the parasitic resistance within the

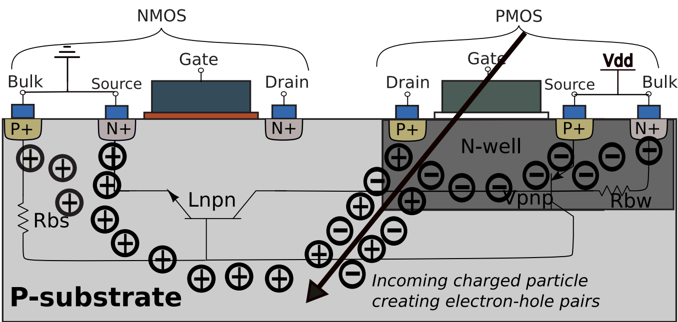
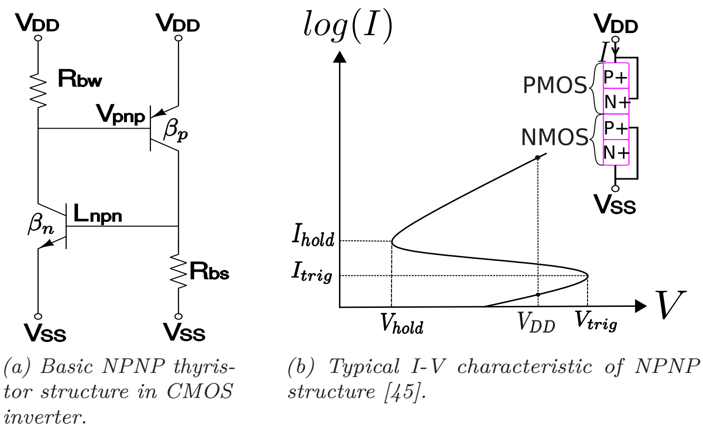


Figure 2.6: Single Event Latch-up in the CMOS inverter.

N-well structure. Figure 2.7a presents an equivalent npnp thyristor structure, where the collector terminal (output node) of each BJT is connected to the base terminal (input node) of its counter BJT.



(a) Basic NPNP thyristor structure in CMOS inverter.

(b) Typical I-V characteristic of NPNP structure [45].

Figure 2.7: Mechanism of npnp thyristor triggering in CMOS inverter.

Under normal circumstances, the middle junction of the npnp structure is reverse-biased, allowing only a small leakage current to pass through this high impedance structure [46]. If any additional current is induced within the structure, the feedback loop amplifies this current and cause it to sustain itself. The npnp structure can be forward-biased either by the V_{pnp} within the N-well region, or L_{npn} within the P-substrate region. However, in a typical CMOS process, more charge is required to trigger L_{npn} transistor than V_{pnp} transistor [46], which makes the V_{pnp} transistor more favorable to latch-up effect.

Figure 2.6 illustrates a particle strike scenario within a CMOS inverter, where the e-h pairs collected at the well-substrate junction region are favorable for the latch-up event. When a particle strikes through the N-well near the pn junction region, the electric field separates the generated e-h pairs, where the

majority carriers recombine most of the holes in the N-well. At the same time, the electrons drift toward the N+ well tap contact, connected to the V_{DD}. If a sufficient amount of electrons are collected, the potential distribution within the N-well is no longer uniformly equal to the V_{DD}, which results in a voltage drop within the N-well region. When this voltage drop is sufficiently high, the P+ source node of the pMOS starts to inject holes through the N-well to the P-substrate, which further turns on the V_{pnp} transistor. Excess holes in the P-substrate start drifting towards the P+ contact terminal of the nMOS, connected to the GND potential.

Since the substrate resistance R_{bs} is high enough, the current flow of the holes increases the base potential of the L_{npn} BJT [45]. When sufficient holes are collected at this P+ contact of the nMOS, the N+ source of nMOS starts injecting electrons through the P-substrate into the N-well region. The injected electrons are further collected by the N+ node of the pMOS, connected to the V_{DD}. At this point, both BJTs are injecting minority carriers into the other BJT's base terminal, creating a positive feedback loop that establishes a direct current flow path between the power rails.

Once the latch-up is initiated, it follows a typical current versus voltage ($I-V$) curve identical to the silicon controlled rectifier [47] device presented in Figure 2.7b, where the source terminals of pMOS and nMOS transistors act as the anode and cathode terminals, respectively. The transition from low to high impedance region is characterized by the points (V_{trig}, I_{trig}) and (V_{hold}, I_{hold}) from the $I-V$ curve presented in Figure 2.7b. The former point represents the transition from the high impedance region to the negative differential resistance region, and the latter marks the transition from the negative differential resistance region to the lower impedance region.

I_{trig} is the transient current for triggering latch-up event within the device, and V_{trig} is the voltage induced by I_{trig} over the parasitic resistance of the device. For the latch-up to sustain, a minimum voltage and current applied to the structure is required to keep the thyristor forward biased in the conducting state, known as V_{hold} and I_{hold}, respectively. In most cases, keeping the supply voltage V_{DD} lower than V_{hold} makes the circuit robust against latch-up events [48].

Following conditions should be fulfilled for the latch-up initialization: (i) The generated current from the incoming particle should exceed the trigger current ($I > I_{trig}$), (ii) the loop gain product of the BJTs must exceed the unity of the structure ($\beta_n \times \beta_p > 1$), and (iii) the holding voltage should be larger than the supply voltage ($V_{DD} > V_{hold}$) [48].

2.5 Single Event Effects mitigation techniques

The mitigation techniques employment either on the layout or circuit design level can suppress the SEE sensitivity of a device [49].

2.5.1 Layout level mitigation

Layout techniques can efficiently lower the SEL sensitivity of the CMOS devices. The loopback current generation in the BJTs is the underlying mechanism to

trigger SEL events in the CMOS devices. The reduction of the parasitic resistance values (R_{bs} and R_{bw}) and thus, the gain of BJT transistors, is an intuitive method to suppress SEL sensitivity. It is accomplished by placing adjacent CMOS transistors apart from each other, which increases the anode-cathode spacing between the CMOS transistors. Another method is to increase the well-contact frequency between the CMOS transistors. Multiple well-contacts suppress the voltage variations in the N-well region, which initially starts conducting the vertical BJT transistor within this region. Furthermore, guard ring techniques are generally employed for reducing the inter-device leakage currents. These techniques are also favorable in reducing SEL sensitivity of the circuits [48, 46, 50].

2.5.2 Circuit level mitigation

The soft error mitigation is achieved either by designing radiation-hard cells on the circuit level or implementing redundancy techniques on the standard cells.

Radiation-hard cells

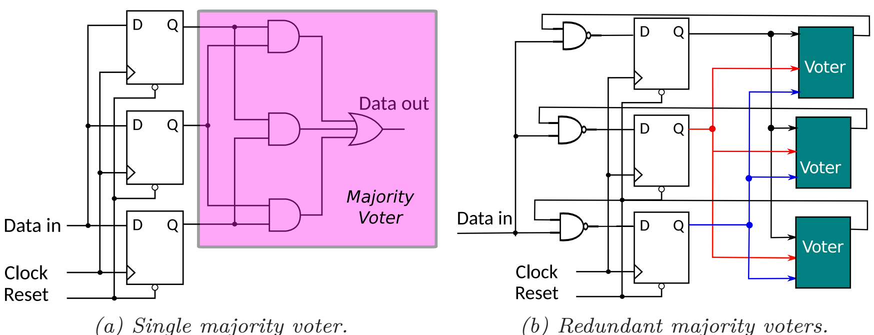
A common technique to reduce the soft error rate of a design is to develop custom cells by altering or including additional passive devices (resistors, transistors, and capacitance). These techniques either eliminate the collection of the injected charge or increase the critical charge threshold for soft errors. During the past 3 decades, various architectures are proposed in the literature to enhance the radiation-tolerance of the cells [51, 52, 53, 54, 55, 56].

Radiation-hardness by redundancy

The soft error sensitivity of a device can also be reduced by including additional redundancy to the existing stored information. It is accomplished either by triplicating memory elements with the Triple Modular Redundancy (TMR) technique or by encoding the data with the Error Detection And Correction (EDAC) techniques.

The TMR mitigation technique utilizes three FFs to store identical information in parallel, and a majority voter compares the outputs of all FFs, as presented in Figure 2.8a. This mitigation technique is only beneficial if the soft error occurs only in a single FF at a time instant, and the majority voter's output does not propagate the wrong result due to soft error transient within the voter. [57]. The latter scenario is typically restrained by triplicating majority voter instances, as presented in Figure 2.8b. The feedback of the voted result restores the internal states of the FFs and avoids error build-up [58]. Periodic or automatic refreshing of the stored data in the TMR-protected FFs can also prevent the accumulation of soft errors. This method is generally known as scrubbing in the digital design [59]. The HEP applications employ TMR mitigation scheme at CERN where it is often acceptable to offer area penalty[5] against soft error protection of critical (control and status) registers.

[5]The area penalty exceeds at least with a factor 3 by employing TMR mitigation technique.



(a) *Single majority voter.* (b) *Redundant majority voters.*

Figure 2.8: Triple Modular Redundancy using standard flip flops.

In comparison to the TMR redundancy, the EDAC techniques often require less information redundancy. There are various approaches to implement EDAC techniques in the data stream, ranging from the detection of a single bit error to the detection and correction of multiple bits/bytes within a data set[6]. The parity bit calculation is the fundamental of all EDAC techniques, which is typically executed by counting the number of logic high or low states within a data stream. The parity bits are usually embedded within the existing data stream on the transmitter side. On the receiver side, the acquired data stream is decoded and received parity bits are compared with the expected parity bits.

Hamming coding [60] is one of the most widely employed EDAC techniques. It can support the correction of the single-bit error and the detection of a double-bit error by using Single-Error-Correction-Double-Error-Detection (SECDED) algorithm. In the HEP applications, the SECDED algorithm is typically employed on the payload packets before the packets are transmitted from the detector electronics. It offers efficiency in terms of performance, redundancy bits, and area penalty. A typical notation of hamming coding is (12,8), which represents 12 bits in total, of which 8 are the data bits, and the remaining 4 are parity bits. The following equation usually calculates the number of parity bits:

$$2^K - 1 \geq M + K \tag{2.3}$$

where M represents the total number of data bits, and K expresses the required number of parity bits. Further details about the calculation and interleaving of the hamming bits are outside the scope of this thesis. The details can be accessed in Chapter 15 in reference [61].

Except for the first SAMPA prototype, redundancy techniques are employed to protect the performance of the prototypes against soft errors. For instance, the configuration registers are hardened with the TMR redundancy, whereas the header part of the packets is protected by employing SECDED algorithm of the hamming EDAC technique.

[6]The EDAC techniques come along with the storage overhead and increased data processing time.

2.6 Scaling trends and their impact on SEE

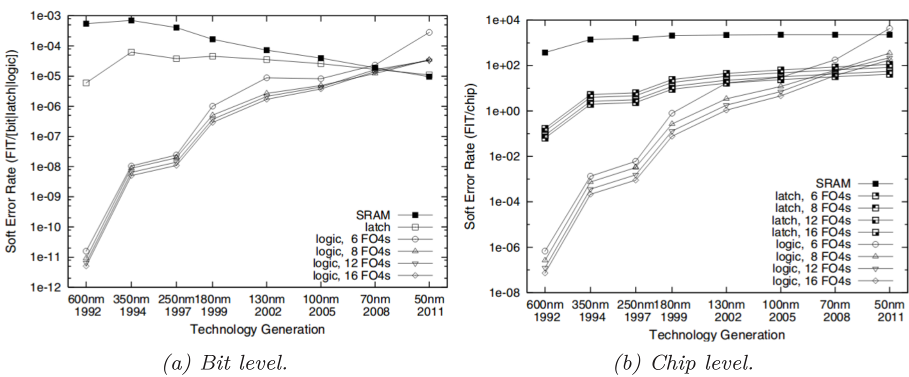
The fundamental existence of soft errors within the CMOS devices is due to constant technology scaling, which is mainly governed by Moore's law [62]. According to reference [63], the impact of technology scaling can be expressed by the following equation:

$$SER \propto F \times A \times exp(-\frac{Q_{crit}}{Q_s}) \qquad (2.4)$$

where F is the particle flux, A is the soft error sensitive area of the device, Q_{crit} is the critical charge, and Q_s is the charge collection efficiency at the sensitive node.

With technology downscaling, the supply voltage of the circuits consequently decreases. These two factors lower the node capacitance (C_n) and node voltage (V_n) (from Equation 2.2), which directly reduces the Q_{crit} of the device. However, the supply voltage scaling also imposes a favorable impact on the SER of a device as it reduces the electric field strength, which consequently reduces the charge collection efficiency of the device. As a result, both Q_{crit} and Q_s parameters (from Equation 2.4) reduces with feature size scaling. Additionally, the SER factor decreases proportionally to the square of the device area.

Reference [63] presents SER simulations for both the memory elements and the combinational logic. Figure 2.9 compares the results from various technology nodes. The results demonstrate that the Q_{crit} of individual SRAM and latch cells



(a) Bit level. *(b) Chip level.*

Figure 2.9: SER for SRAM, latches and combinational logic. ©2002 IEEE. Reprinted, with permission, from P.Shivekumar et al. [63].

decrease gradually with technology scaling, together with a relatively constant Q_s for all feature sizes. Since the exponential factor $\frac{Q_{crit}}{Q_s}$ remains comparative constant with the technology scaling, the primary technology scaling effect is the reduction in the sensitive area A, which gradually decreases the SER of the individual memory elements. However, as the number of memory elements increases per chip, the overall SER per chip is more or less constant for both the SRAM and latch cells, as presented in Figure 2.9b.

In contrast to the memory elements, the SER contribution of the combinational logic linearly increases with the downscaling of the technology [64]. It is mainly due to the diminishing of the masking effects in the combinational circuits. For instance, the impact of electrical masking reduces significantly with device scaling as the speed performance of individual transistors increases and will cause less attenuation impact on the SET pulses. The supply voltage reduction is another aspect which reduces the drive currents of the transistors. It results in slower recovery of the affected node and ultimately leads to longer durations of the SET pulses. Higher clock frequencies are the most critical factor which significantly reduces the temporal masking effect. As a consequence, the memory elements sample more frequently and the sampling probability for SET pulses increases.

In recent years, the charge sharing mechanism [65] has started to dominate due to technology scaling. As a consequence, multiple sensitive nodes can simultaneously collect charge, which is initially generated from a single charged particle hit. It mainly occurs due to reduced spacing between the sensitive nodes. The charge sharing mechanism has started to impose limitations on the traditional soft error redundancy techniques.

Technology scaling is favorable for the latch-up effects [66]. The increase in the substrate doping generally suppresses the resistivity, which reduces the parasitic resistance in the N-well and P-substrate regions. It further reduces the potential drop to forward-bias the emitter-base junctions of the BJT transistors. Additionally, the increased doping within the base regions of the parasitic transistors degrades their current gains, which diminishes positive feedback mechanisms. As the device supply voltage decreases with the technology, the threshold voltage (holding voltage) for latch-up may succeed below this threshold.

2.7 LHC radiation environment

The LHC is composed of a mixed-field radiation environment where each field imposes different radiation damage within the electronic components. The LHC radiation environment mainly originates from the following sources:

- The collision of particles at the experiment areas and the respective particle debris.
- Beam losses in the collimator and other beam intercepting devices.
- Beam interactions with residual gas.

The resulting radiation fields consist of a broad range of particles and energies. For a given location at the LHC, the contribution of the particles and the intensity of particles radiation field depend upon the operation conditions of the LHC as well as the gap/shielding between the interaction point and the respective location.

Figure 2.10 illustrates an example of the simulated particle energy spectra encountered at the tunnel location of the LHC. The simulations performed using

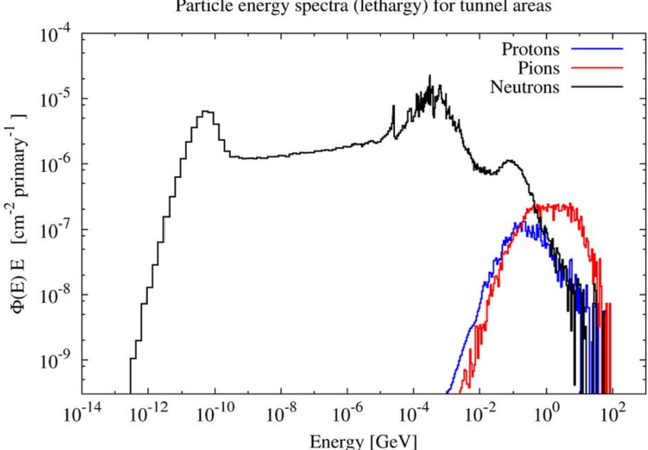


Figure 2.10: Simulated particle energy spectra for tunnel areas in the LHC. The radiation is due to the particle debris induced by the proton-proton beam collision in one of the CERN experiment points. ©2011 IEEE. Reprinted, with permission, from [67].

FLUKA Monte Carlo transport code[7] [68]. This spectra considers the hadrons relevant for inducing the SEEs, and their energies extend up to ∼100 GeV. In the context of LHC, the most relevant hadrons are protons, neutrons, charged pions, and kaons. The SEEs are typically induced by the indirect energy deposition events from the nuclear interactions between the hadrons and the nuclei in the sensitive regions of the semiconductor devices. Besides, other particles such as electrons, photons as well as muons are also present in the LHC environment. These can degrade the performance of the semiconductor devices due to the TID effects.

The SEE rate is proportional to the hadron fluence (integrated flux) with the kinetic energy above 20 MeV. Mainly, these hadrons are referred to as the high energy hadrons (HEH). The SEE relative radiation level of a particular LHC location can be expressed either as the HEH flux (particles/cm^2/s) or the integral HEH flux (particles/cm^2).

Table 2.1 compares the approximated annual HEH fluence values of the LHC irradiation environment with other relevant environments. It is worth mentioning that depending on the location within the LHC, the annual HEH fluences span over a wide range, extending from the values just above the ground level fluence to several orders of magnitudes more significant than those obtained for the typical Low Earth Orbit (LEO) missions. The last column in Table 2.1 presents the magnitude differences of various HEH flux environments relative to the ground level. The last row displays the annual HEH fluence expected at the

[7] FLUKA is a general-purpose tool for calculations of particle transport and interactions with matter. It is valid for a wide range of applications spanning from proton and electron accelerator shielding to target design, calorimetry, activation and dosimetry, cosmic ray studies, and radiotherapy. Among them, the prediction of radiation damage in electronics has always been a traditional field.

Environment	1 year fluence [hadrons/cm^2]	Factor
Ground level	1-2×10^5	1
Avionics	~2×10^7	~10^2
International Space Station orbit	~7×10^8	~3.5×10^3
Polar Low Earth Orbit (800km)	~3×10^9	~1.5×10^4
LHC	~10^6-10^{12}	~5×10^6
TPC and MCH (ALICE-LHC)	~1.07×10^{11}	~5.4×10^5

Table 2.1: Annual high energy hadron fluences for different radiation environments. The data is taken from reference [69, 13]

worst-case locations in the TPC and MCH detectors of the ALICE experiment where the SAMPA chip will operate.

2.8 Radiation levels at the ALICE experiment during RUN 3

To evaluate the severity of SEE induced errors on the electronic devices and to predict the expected failure rate, one must acquire adequate knowledge of the radiation levels the electronics will be exposed to. With the enhanced interaction

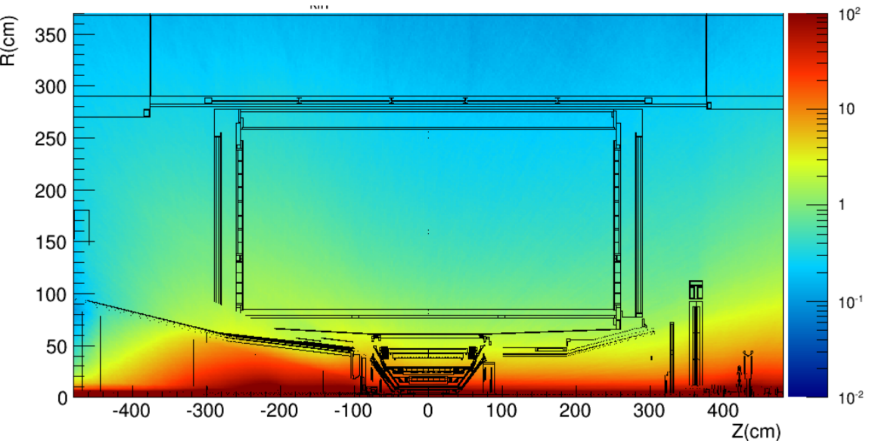


Figure 2.11: Rate of hadrons [kHz] with energy of >20MeV for a Pb-Pb collision rate of 50 kHz. Copyright ©2013-2019 CERN(License: CC-BY-3.0) [13].

rate at the ALICE TPC and MCH detectors during RUN 3, the radiation load on the new front-end electronics will consequently also increase. The HEH fluence and TID are the primary sources of radiation-induced errors in the readout electronics.

A contour plot of the expected HEH fluence rate at the ALICE experiment during RUN 3 is presented in Figure 2.11. The origo in the contour plot serves as the intersection point of the beam with the maximum magnitude of HEH fluence rate, which decreases gradually as moving farther from the intersection

point. Both end-plates of the TPC detector (see Section 1.2.3 on page 4) are outfitted with the readout chambers (readout electronics), where the innermost readout chambers consider as the worst-case scenario, experiencing a higher rate of HEH fluence.

			RUN 3		RUN 1	
Element	r(cm)	Z(cm)	TID (kRad)	>20MeV HEH (kHz/cm^2)	TID (kRad)	>20 MeV HEH (kHz/cm^2)
TPC In	79	[-260,260]	2.1	3.4	1.6	0.79
TPC Out	258	[-260,260]	0.3	0.7	0.022	0.18
MCH S1*	19	-536	0.42	3	-	-
MCH S2*	24	-686	0.19	1	-	-
MCH S3*	34	-983	0.14	0.9	-	-
MCH S4*	45	-1292	0.18	1	-	-
MCH S5*	50	-1422	0.91	0.7	-	-

* MCH S1-5 corresponds to various stations of the Muon Chamber detector.

Table 2.2: Comparison between the ALICE TPC and MCH radiation levels for RUN 1 and RUN 3. The data is taken from reference [70] and [13].

Table 2.2 compares the radiation level for the ALICE TPC and MCH detectors between RUN 1 and RUN 3, both simulated by using FLUKA Monte Carlo transport code [68]. There is no significant increase in the TID levels between RUN 1 and RUN 3. However for RUN 3, the HEH flux rate is at least a factor 4 higher than RUN 1 for the worst location scenario. As the HEH flux rate at the innermost part of the TPC and MCH S1 is relatively comparable, these numbers determine the radiation level requirements for the SAMPA chip. Conclusively, the SAMPA chip should withstand a dose of 2.1 kRad (including a safety factor 10) and 3.4 kHz cm^{-2} (including a safety factor of 2) of HEH flux to operate successfully in the ALICE radiation environment. Throughout this thesis, these numbers are employed to predict the failure rates for various kinds of SEEs of the SAMPA chip in the ALICE radiation environment.

2.9 SEE hardness assurance methodologies

An ideal way of assessing a device's sensitivity against SEEs is to monitor its performance in the actual radiation environment. However, it imposes several practical limitations: (i) intricate access to the actual radiation environment, (ii) a reasonable amount of SEE errors accumulation often requires several weeks of beam exposure, and (iii) hard to employ design improvements in the custom-made chips once the chips are fabricated and commissioned in the sensors (detectors).

Another approach is to develop models for every circuit within a chip individually and determine the regions which can be sensitive to SEE. These models are often process and technology-dependent, and these parameters are not accessible to the user. Therefore, it may result in assuming inaccurate sensitivity of the circuits, leading ultimately to unaccepted consequences.

One of the most adapted and widely used approaches for evaluating SEE sensitivity of an electronic device is the exposure of the device with relevant particles in an accelerator facility. It simulates the hostile radiation environment fairy well and overcomes uncertainties from the modeling approach. The limited beam time and cost are some of the drawbacks of this approach. With this approach, various kinds of SEE events (SEL, SEU, SET, SEFI) can coincide in more complex devices such as mixed-signal ASICs, FPGA, and microprocessors. Therefore, identifying an accurate source of error can be difficult.

Proper test planning and in-depth understanding of the Device Under TEST (DUT) is essential for a successful irradiation campaign. For instance, either one overlooks packing a simple test cable or chooses improper beam profile can result in dire consequences on the outcome of a remote site test trip.

2.9.1 High-energy proton campaigns

For SEE qualification at the LHC, the charged hadrons threshold is considered to be at the kinetic energy of ∼20 MeV. No SEE failures are expected below this threshold due to one of the following phenomena: (i) the charged hadrons lose a significant amount of energy while traversing through the component package, hence not reaching the sensitive region of the device, (ii) the hadrons penetrate to the sensitive region but do not have sufficient energy to produce inelastic events. Above 20 MeV of kinetic energies, hadrons (neutrons and protons) contribute to nearly identical SEE failure events[8]. Reference [71] experimentally proved this phenomenon. In other words, the SEE failure rate saturates at higher energies. The results from reference [71] demonstrate that the upset rate of 10 GeV protons is only slightly higher than for 200 MeV protons. It stems from the fact that the increase in the hadron's incident energy does not significantly increase the recoil energy generated inside the silicon during the collisions. In the central collisions at higher energies, the sensitive target is likely to break into small pieces, each having lower LET values.

The particle energy spectra of the LHC from Figure 2.10 demonstrates that the peak energy of the charged hadrons lies above 100 MeV. Hence, all charged hadrons above 20 MeV are considered equally efficient to induce SEE events. Reference [71] states that a proton beam irradiation campaign within the energy range of 60-200 MeV should provide a suitable means to qualify LHC electronics against SEEs. For SEL qualification, however, a mono-energetic proton beam with energies closer to 200 MeV is recommended [72]. It stems from the fact that the maximum LET produced by the nuclear recoils increase with the proton energy [32].

Although SEE qualification of the LHC electronics can be performed either by high energy proton or neutron beams, proton beams are widely utilized due to their broader availability. Contrary to the neutrons, high energy protons offer

[8]Since most abundant silicon isotope compounds of the equivalent number of protons and neutrons, making it isospin symmetric. At lower energies, the inelastic σ of proton decreases due to Coulomb repulsion [71].

a combined effect of SEEs, TID as well as the DD. A quick estimate of TID and DD from protons exposure at two distinct energies is summarized in Table 2.3.

Proton Energy	TID	NIEL
50 MeV	$\sim$ 14 kRad	1.8 $\times 10^{11}$ n/cm^2
200 MeV	$\sim$ 6 kRad	1.0 $\times 10^{11}$ n/cm^2

Table 2.3: Estimate of dose damage and displacement damage from 10^{11} protons/cm^2. Data is taken from reference [27]

For high energy proton campaign above 100 MeV, de-lidding of the DUT is usually not required as the hadrons can easily penetrate through the plastic material and reach the SV of the DUT. Proton campaigns are commonly performed in air. Hence the supporting equipment can be located closer to the DUT. It makes the proton campaign more straightforward compared to the heavy-ions or pulsed-laser campaigns. However, relatively high fluences are required to acquire a sufficient amount of SEE errors, consequently depositing the TID damage in the DUT over time.

Due to statistical nature, the most crucial figure of merit for the SEE events is the rate of occurrence (i.e., how many events take place per unit time). It mainly depends upon the SEE susceptibility of the DUT, the particle flux, and the nature of the particles. In the context of LHC, the failure rate is typically predicted by multiplying the extracted σ values from a proton campaign at an energy above 60 MeV, by the maximum hadron flux (above 20 MeV) foreseen at the expected location.

2.9.2 Heavy-Ions campaigns

Heavy-Ions (HI) irradiation campaigns are widely executed for SEE hardness assurance qualification of the devices for space applications. During the campaign, the σ_{SEE} curve is determined. This provides the σ_{SEE} region as a function of various LET values of the ions. The SEE sensitive region and the threshold limits of a particular event can further be identified from the σ_{SEE} curve.

In the context of LHC, the HI campaigns are not preferred for SEE qualification of the semiconductor devices. This is mainly due to different underlying mechanisms between the HEH and HI induced SEEs, demonstrated previously in Figure 2.2. The HI primarily triggers SEE events in the semiconductor devices via direct ionization mechanism. The HEH first undergoes a nuclear interaction, and the products of the interaction subsequently produce SEE events via direct ionization mechanism. Therefore, the SEE failure rate prediction for the LHC radiation environment is not straightforward from the σ_{SEE} curve, extracted from a HI campaign. Nevertheless, several σ_{SEE} curve parameters from the HI campaign, with some hypothesis about the SV of the DUT, can be used to estimate the SEE failure rate at the LHC [25].

According to reference [32], the maximum LET energy of nuclear recoils generated by HEH interactions with silicon is typically lower than 16 MeVcm^{2}mg^{-1}.

For SEE qualification of LHC electronics from a HI campaign, a general rule-of-thumb is that if the threshold of a SEE event is above ~16 $MeVcm^2mg^{-1}$, the device will most likely not experience the respective event in the LHC environment. According to reference [73], however, this rule-of-thumb is inadequate for the modern high-density ICs (e.g., SRAMS). It is due to the presence of high-Z materials to enhance circuit performance. For instance, Copper (Cu) and Titanium (Ti) is often utilized for the metalization. Additionally, ohmic contacts and interconnections are composed of Tungsten (W) [74]. Reference [73] suggests that 34 $MeVcm^2mg^{-1}$ is the maximum LET value, which can be generated from the nuclear recoils of protons and Tungsten interactions. Therefore, to qualify devices with high-Z materials, a supplementary rule-of-thumb is recommended in reference [73], stating that if the SEL threshold of the device is higher than the LET value of 40 $MeVcm^2mg^{-1}$, the DUT will not latch-up in the hadrons environment.

The HI campaign preparation is somehow distinct from the high energy proton campaign. To prevent energy loss or absorption of the charged particles in the air, the DUT is irradiated inside a vacuum chamber. It often requires dedicated preparation of cables, which should support the available feed-through connectors at the facility. Additionally, the energy of the incoming ions degrades in the package, which further imposes higher uncertainties in the energy spectrum at the sensitive regions. Therefore, the DUT often requires de-lidding or substrate thinning.

2.9.3 Pulsed-Laser campaigns

Due to random strike locations of the incoming particles at the DUT, particle accelerator campaigns are insufficient to provide temporal and spatial information about the SEE error. It is seldom required to localize the source of SEE error (e.g. SEL) within the sensitive region of the DUT. The Pulsed-Laser (PL) technique [75] can provide this information by depositing the charge into the sensitive regions of the DUT with μm of resolution. During a PL campaign, photons are responsible for creating e-h pairs via either photoelectric, Compton scattering, or pair production effect [22], where the photon energy transforms into the electric potential due to the photo-voltaic effect [76]. This conversion mainly depends upon the inversely proportional relationship between the deposited photon's energy and the wavelength (λ), as presented in Equation 2.5 [75].

$$E_{photon} = \frac{hc}{\lambda} \tag{2.5}$$

where h is the Planck's constant (6.626×10^{-34} Js or 4.135×10^{-15}eVs), and c is the speed of light ($3\times10^{8}ms^{-1}$).

In a semiconductor device, 1.12 eV is the minimum energy required to excite electrons from the valence to the conduction band. It corresponds to a threshold wavelength of 1110 nm. When photons exceed this threshold, the bandgap energy becomes more significant than the intrinsic photon energy, and the photons penetrate through the silicon substrate. Absorption coefficient of photons in

semiconductor is another critical parameter, which is inversely proportional to the wavelength parameter. Figure B.2 (see Appendix B.2 on page 157) presents this relation and demonstrates that photons can penetrate longer distances within the semiconductor substrate as the wavelength increases. During a PL SEE campaign, a typical wavelength value for the laser source is ~1064 nm, which is slightly lower than the wavelength threshold (1110 nm) for exciting electrons in the silicon bandgap. Likewise, it is sufficient to penetrate a distance of 900μm within the substrate.

One of the main challenges with the PL campaign is the prediction of failure rates as the function of energy or LET values for the relevant radiation environments. Reference [77] presents some models to extract ions-equivalent LET values from the deposited laser energy. These models require several process parameters that are not easily accessible. The prediction of failure rates from the PL campaign is even more complicated for the LHC electronics as the photons energy deposition mechanisms do not involve nuclear interactions within the semiconductor [75].

Similar to the HI campaigns, the PL campaigns require dedicated sample preparation. The modern ICs are often high density, where several metal layers overlay the top of the substrate. It imposes limitations for top-side laser exposure due to shadowing of the metal layers. Hence, dedicated carrier boards are required to access the sensitive regions from the rear of the DUT.

Despite all these limitations, the PL technique is gaining popularity for SEE hardness assurance testing due to its lower cost and higher availability. The PL campaign is often conducted in a laboratory and not in an accelerator facility. It offers a diagnostic feature to precisely localize the SEE sensitive regions within complex ICs, which is likely unachievable with the traditional particle accelerator campaigns.

2.9.4 Test scenarios and recommendations

In general, various test scenarios should be evaluated before an irradiation campaign. The user also requires a sufficient overview of the respective radiation source and remote site facility in advance, to accordingly prepare for the campaign. It is recommended to prepare for the worst-case scenarios during the campaign. This includes the soft error handling capabilities of both the DUT and the DAQ system as well as the control and communication interface with the DUT. For the soft error (SEU/SET) evaluation, minimum operating voltage and maximum operating frequency should be considered for the worst-case scenario. Maximum operating voltage and the expected temperature is essential for the SEL qualification.

During a proton campaign, the user often resides in a control room. Hence, the user should evaluate signals integrity and remote access to the DUT beforehand. The worst-case scenario for SEE is generally accomplished at the maximum energy of the protons. Therefore if time allows, the DUT exposure at all available proton energies at the facility is recommended.

During a HI campaign, the maximum LET value for the LHC electronics is 16 MeVcm^{2}mg^{-1}. Therefore, it is recommended to scan at different LET values within this range. To fully qualify against SEL effects, it is desirable to expose the DUT at higher LET values up to 40 MeVcm^{2}mg^{-1}.

During a PL campaign, the standard methodology is to laser scan the DUT both horizontally and vertically, meanwhile moving the laser source with reasonable step size and at a constant repetition rate. In this way, a single laser pulse is deposited at each grid point. Since laser scanning of the entire DUT can be time-consuming and impractical, the user should gain an overview of the physical location of the SEE suspected regions beforehand. Additionally, the user should assess the backside surface quality and substrate thickness of the DUT beforehand. For instance, a rough surface with dirt and bulks can lead to inaccurate energy loss due to photons scattering or absorbing mechanisms. Substrate thinning may also be required to reach the sensitive regions of the DUT, depending upon the wavelength of the laser source (penetration depth).

2.10 Irradiation campaigns of the SAMPA prototypes

To qualify the SAMPA chip for the ALICE radiation environment, a careful analysis is performed for the severity of various kinds of SEEs. Accordingly, appropriate mitigation techniques are implemented in the consecutive prototypes to reduce their SEE sensitivity. The SEE sensitivity is primarily evaluated by conducting five irradiation campaigns on various prototypes of the SAMPA chip from April 2015 to January 2018. Table 2.4 provides an overview of the period, prototype, facility, and the main objectives of every campaign.

#	Facility	Source	SAMPA prototype	Device Received	Device Tested	Objective(s)
1	TSL[1]	Proton	MPW1	Feb. 2015	April 2015	SEE and TID
2	KVI[2]	Proton	V2	Nov. 2016	March 2017	SEE and TID
3	CRC[3]	Heavy-Ions	V2	Nov. 2016	May 2017	SEL
4	CRC[3]	Heavy-Ions	V3 and V4	Nov. 2017	Nov. 2017	SEE
5	IES[4]	Pulsed-laser	V2 and V4	Nov. 2017	Jan. 2018	SEL

[1] The Svedberg Laboratory, Uppsala, Sweden.
[2] Center of Advanced Radiation Technology, Groningen, Holland.
[3] Cyclotron Resource Centre, Louvain-la-Neuve , Belgium.
[4] Institute of Electronics and Systems , Montpellier, France.

Table 2.4: An overview of the SAMPA irradiation campaigns.

Chapter 3

Upgrade of the Front-End Electronics

Improved resolution requirements for the tracking detectors of the high energy physics (HEP) experiments call for a higher number of readout channels as well as more compact front-end electronics. Currently, the CMOS technologies have gained a superior position in the development of ASICs for HEP readout systems due to the high integration density and low power consumption. New front-end ASICs are multi-channel systems that can often serve up to 1024 channels, simultaneously.

The latest trend in the ASIC projects for the HEP applications is the integration of both analog and digital circuitries on the same silicon die, turning into a mixed-signal readout chip. In this context, a new readout chip "SAMPA" is developed, which represents integration and modernization of presently used TPC PASA chip(analog) [9] and ALTRO chip (digital) [10].

3.1 The objective of the SAMPA ASIC

Among the planned upgrades of the ALICE TPC detector for RUN 3, existing MWPC based technology will be replaced by the GEM based technology. In the GEM based technology, an electron cloud induces negative signals at the readout plane. In the MWPC based technology, positively charged ions drift towards the readout plane. It imposes following limitations on the present readout electronics [8]:

- GEM based chambers should accommodate signals with negative polarity, while the current PASA chip only supports signals with positive polarity. The PASA chip also restricts noise requirement (ENC) of ∼670 e.
- The ALTRO chip is based on a triggered readout system. As the readout rate will increase during RUN 3, data sampling and acquisition of the TPC detector should execute concurrently. Hence, a continuous readout system is one of the requirements for new TPC readout electronics.
- As the collision rate increases, the readout system requires doubling of readout channels (from 16 to 32) per chip.

3.1.1 CERN/ALICE common projects

During RUN 3 at the LHC, data transmission links are upgraded to wider bandwidths as well as better radiation tolerance to handle an enormous amount

of physics data. Currently, optical data links are the most efficient means of data transmission over longer distances. This technique is widely employed by the LHC detectors. Typically, data transmission from the LHC detectors requires three concurrent systems: data acquisition (DAQ), timing trigger and control (TTC), and slow control (SC). All these systems have different bandwidth requirements. With the advancement of technology, it is possible to develop a general-purpose optical link that can simultaneously support data transmissions from all concurrent systems. Since data transmission protocols are identical for many of the LHC detectors, the CERN community has developed Gigabit Transceiver (GBT) [78] and Versatile Link (VL) [79] projects. They provide faster optical links that are qualified to operate in the LHC radiation environment.

During RUN 3, the ALICE detector will process a data flow of ~1 TB/s from all detectors to the online computing and data storage system. The Common Readout Unit (CRU) [80] will handle this processing, which is assisted by the high-performance FPGAs, equipped with multi-Gigabit optical input and output connectors. The CRU is a common functional interface between the on-detector systems, the Online-Offline computing system (O^2), and the Central Trigger Processor (CTP). The CRUs will reside in a counting room, outside the radiation zone.

3.1.2 ALICE detectors readout upgrade during RUN 3

To meet necessities of TPC detector readout during RUN 3 as well as to benefit from combined developed projects at CERN, new front-end cards (FECs) are designed[1] [8]. Each FEC contains a complete readout chain for amplifying, shaping, digitizing, processing and buffering of TPC signals. To profit from the existing mechanical and cooling structures, the size and power dissipation of the new FEC will remain unchanged.

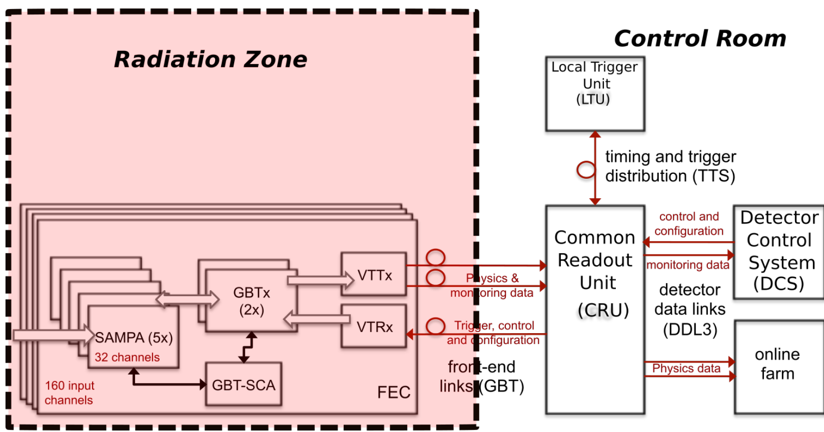


Figure 3.1: Schematic of TPC readout system with CRU as central part, connecting front-end electronics to trigger system, and online farm [8].

[1]The Oak Ridge National Laboratory (ORNL) group has designed new TPC FECs.

A schematic of the upgraded TPC readout system is presented in Figure 3.1, where readout equipment that will be placed within the radiation zone is highlighted. The detector signals propogate from the readout pads to the FECs via flexible Kapton cables. Each FEC accommodates five SAMPA chips, processing signals from 160 channels concurrently at a rate of 8 Gbit/s. The acquired data is further transferred to the dual GBTx chips, which multiplex and transmit the data to the CRU via versatile optical link cables. Each FEC hosts one bi-directional transceiver (VTRx) and one uni-directional transmitter (VTTx) chip, where the former also provides control and trigger configurations from the DCS and LTU units respectively, through the CRU. Altogether, the TPC detector will serve 3276 FECs, which will transmit data to the CRUs at a throughput of ~30 Tbit/s.

The GBT-SCA chip configures and monitors various parameters (temperature, current) of the FEC. It also features an I2C protocol for configuring and controlling numerous internal registers of the SAMPA chips. Table E.1 (on page 179) summarizes the total number of components and their required bandwidths for the complete readout system of the TPC detector during RUN 3.

The readout architecture of the ALICE Muon Tracking Chamber (MCH) detector will also be upgraded during RUN 3 to accommodate a higher readout rate up to 100 kHz. For the MCH detector, 34,000 SAMPA chips and 17,000 FECs will be installed and connected to various CRU [80] interface via ~500 GBT [78] optical links. Reference [81, 82] manifests more exceeding details about the MCH readout upgrade.

3.1.3 Technology choice for the SAMPA ASIC

In 2013 during the kick-off of the SAMPA project, IBM 130 nm CMOS technology was the first option for SAMPA prototypes fabrication since radiation tolerance of this foundry was well-known[2]. IBM decided to sell off its foundry business to GlobalFoundries, and the future of foundry became uncertain. The CERN collaboration commenced to examine alternative foundries for future HEP projects, and TSMC 130 nm foundry seemed to be the best substitution[3]. The SAMPA was among the initial projects of the HEP experiments, which adopted TSMC 130 nm CMOS technology node. In the meantime, the micro-electronics group (EP-ESE-ME) [83] at CERN fabricated various test chips with TSMC 130 nm technology to evaluate its tolerance with respect to the LHC radiation environment.

3.2 The SAMPA chip

The SAMPA chip is intended to fulfill requirements for both ALICE TPC and MCH detectors, by adapting different detector signals with programmable

[2]Several prototypes were already developed for the HEP applications with the IBM 130 nm technology.

[3]The TSMC technology provided long-term availability, reliable models, and excellent support. However, the radiation tolerance of the foundry was unknown.

parameters. Table 3.1 summarizes both general specifications of SAMPA chip and requirements dedicated to each of ALICE sub-detectors.

Parameter	ALICE TPC	ALICE MCH
Readout Chamber	GEM	MWPC
Signal polarity	Negative	Positive
Peaking time (ns)	160	300
Gain (mV/fC)	30	4
Detector capacitance (pF)	18.5	40-80
Equivalent Noise Charge (ENC)	< 600e @ 18.5pF	< 950e @ 40pF < 1600e @ 80pF
ADC sampling frequency	5,10 or 20 MSps	10 MSps
ADC resolution	10-bit	
Readout Mode	Continuous	Triggered
TID (KRad)	2.1	0.91
>20MeV HEH (kHz/cm^2)	3.4	3.0
Power consumption	< 32(mW/ch)	
Die size (mm^2)	84.5	

Table 3.1: The requirements of the new SAMPA chip [13].

3.2.1 Architecture overview of SAMPA chip

The SAMPA chip includes 32 identical data processing channels, each containing a Charge Sensitive Amplifier (CSA), a pulse shaper, an Analog to Digital Converter (ADC), followed by a Digital Signal Processor (DSP) block, as presented in Figure 3.2.

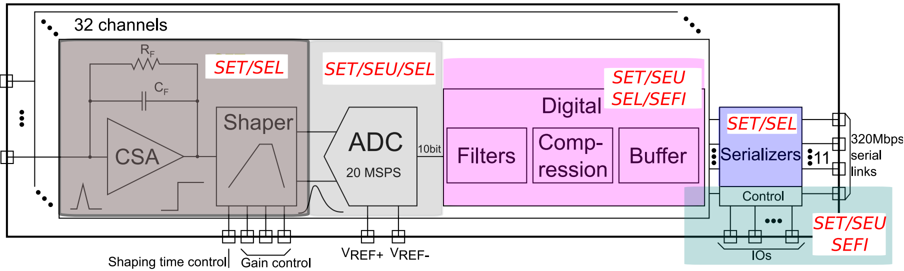


Figure 3.2: A simplified block diagram of the SAMPA chip illustrating possible SEE induced errors in the chip.

As both analog and digital blocks of the SAMPA chip are integrated on a single silicon die, radiation hardness assurance of the chip becomes complicated. For instance, several SEE induced errors can coincide, imposing challenges to identify the accurate source of the event. A thorough understanding of the chip is required to analyze the results from the irradiation campaigns precisely and

categorize soft errors from various domains of the chip accordingly. Figure 3.2 highlights the most foreseen SEE errors in the SAMPA chip.

3.2.2 Analog Front-End

Analog front-end of the SAMPA chip is composed of a charge sensitive amplifier (CSA) and a semi-gaussian pulse shaper. The CSA amplifies either positive or negative charge pulses from the detector pads, where the value of the feedback capacitor is tuned to achieve the desired peaking time of the pulse. The next stage is a pulse-shaper network that limits the bandwidth of output signals and optimizes the overall signal-to-noise ratio. Between the pulse-shaper and the ADC, an analog buffer regulates the DC voltage level of the shaper's output in accordance with the dynamic range of the ADC. Reference [84] presents comprehensive details about the analog front-end blocks of the SAMPA chip.

Analog blocks can potentially be sensitive to ASET events [85]. The severity of such events is quite low due to the typically shorter duration of the radiation-induced transient pulses. These pulses should occur closer to the sampling clock of the ADC to get sampled in the DSP block.

SEL event is another, potentially destructive SEE event for the analog blocks. Although the probability of triggering SEL events in analog blocks is quite low, it can still trigger, given inadequate layout techniques. Due to strict noise requirements of the analog front-end, the leakage currents are reduced by employing various noise suppressing layout techniques, such as guard rings and triple n-well. These techniques are equally favorable to reduce SEL sensitivity of the SAMPA analog front-end blocks [48].

3.2.3 SAMPA Analog to Digital Converter

The SAMPA chip has a differential 10-bit ADC, supporting multiple sampling frequencies (5, 10, or 20 MHz). The ADC utilizes the Successive Approximation Register (SAR) topology [86]. Reference [87] presents further design details of the SAMPA ADC, which is mainly composed of a charge redistribution Digital to Analog Converter (DAC), a comparator, and the SAR register logic. The core sampling frequency of the ADC is 10 MHz, whereas the SAR logic requires a conversion frequency of 80 MHz.

The SAMPA ADC can be prone to experience both SEL, SET as well as SEU events where SEL sensitivity can favorably be reduced by employing efficient layout techniques to meet strict linearity requirements[4]. ASET events on the analog comparator and the DAC block can imbalance capacitor array [88], leading to imprecise digital conversion. The SAR register logic executes comparison as well as shift operations and composed of 20 FFs from the standard digital library. It can experience both SET and SEU events, altering the output data stream for a single conversion. Such errors have considerably low severity due to fewer amount of FFs. Since a soft error will only confine within one single event, filters in the DSP block can likely discard such events. In the worst-case

[4]Integrated nonlinearity (INL) and differential nonlinearity (DNL) < 0.7 LSB.

scenario, it will result in loss of single hit or noise hit at the serialized output data of the chip.

3.2.4 DSP

The DSP is implemented as a single block, acquiring data from all 32 ADCs in parallel. It executes various filtration algorithms to eliminate signal perturbations, distortion of the pulse shape, offset as well as signal variations due to environmental conditions. In the DSP, the data stream is further compressed by eliminating all data samples below a programmable threshold, and data packets are constructed. Each data packet is marked with a unique timestamp and size, to be reconstructed afterwards. Data packets are buffered in the Ring-Buffer (RB) module until the reception of the acquisition signal. Once the acquisition signal is received, data packets are further serialized and transmitted from the chip. The data readout takes place either in continuous or triggered mode, by enabling up to eleven 320 Mbps Scalable Low-Voltage Signaling (SLVS) serial links, allowing a data throughput of up to 3.2 Gbps.

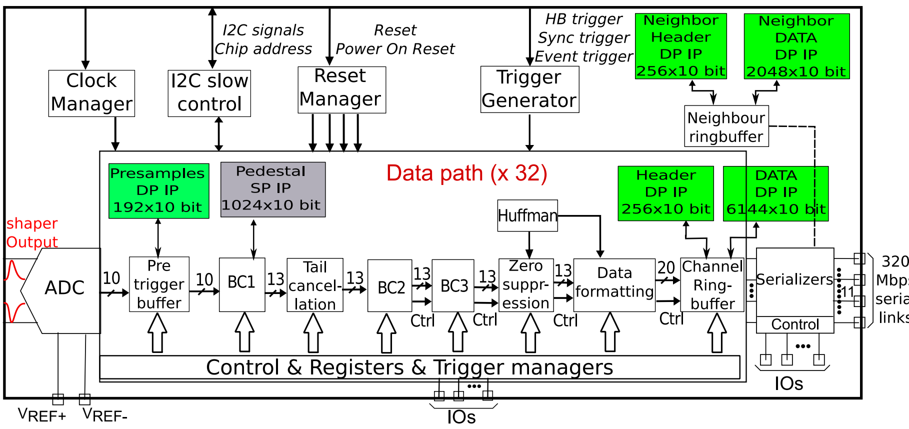


Figure 3.3: Simplified block diagram of SAMPA DSP block, presenting data path chain.

A simplified digital data path chain for a single channel of the SAMPA chip is presented in Figure 3.3. It emphasizes the placement of both single-port (SP) and dual-port (DP) embedded SRAM IPs, together with various control and configuration signals (clock, reset, trigger) of the SAMPA chip[5].

The DSP block is prone to various kinds of SEEs (SET, SEU, SEL, and SEFI), as the digital cells are implemented from the standard digital library. Due to aggressive design rules, these circuits are favorable to SEEs. Depending upon the severity of SEE induced error, it can potentially lead to failure in data readout, which in turn may only recover after complete halting and reconfiguration of the ALICE experiment.

[5]Figure 3.3 does not include several controlling blocks of the digital part for simplicity sake.

3.2.5 Soft error handling in the SAMPA registers

The suspected soft errors contribution in the registers (FFs) of the SAMPA chip are classified into three severity levels:

1. **Data path errors** are least severe, since the corrupted data only occurs within the internal data-path chain. The typical soft errors are: (i) SET events sampled from the analog front-end, (ii) SET and SEU events from the ADC, and (iii) bit-flips in the pipelined registers of the data path. Since data stream updates periodically in this path, these errors are commonly confined within one event, which results in loss of single hit or noise hit in the serialized output data.

2. **Configuration errors** usually occur in the configuration registers or the pedestal memories, and may lead to incorrect data flow control or configuration of the chip. These errors will likely sustain until reset or reconfiguration of the chip is initiated. Hence, the severity level for such errors is higher than the data-path errors. The SAMPA chip may usually operate with these errors, depending upon the affected configurations by the soft error.

3. **Functional errors** are most severe as they can malfunction the functionality of the SAMPA chip. They can occur in the critical state machines, memory pointers, as well as the clock or reset network trees.

Most of the configuration registers in V2 and consecutive prototypes of the SAMPA chip are hardened by employing the TMR mitigation technique. TMR protection is implemented at a low-level using standard FFs. Reference [89] provides further details about the design and implementation of TMR technique in the SAMPA chip.

In V2 and consecutive prototypes of the SAMPA chip, there are ∼125,000 FFs in total, including additional TMR registers. The amount of FFs (excluding TMR FFs) is ∼55,000, of which 20,700 (28%) are not TMR protected [89]. The exceptions are:

1. **Internal data path:** About ∼17,700 FFs are present in the data path chain between the ADCs and the Ring-Buffer (RB) memories. It corresponds to ∼ 1/3 of the total FFs in the DSP. To save area, FFs in the data path do not have any TMR protection, as the soft errors in this path are acceptable.

2. **Daisy chained data path:** Daisy chaining is an additional feature for low data throughput detectors (MCH), where a single eLink transmits serialized data from dual SAMPA chips. About 109 FFs are included between the daisy-chained input and the RB module. These FFs are not protected due to (setup/hold) timing concerns. The header data is already hamming-protected.

3. **Test structures:** The V2 and consecutive prototypes of the SAMPA chip include various test structures (ring oscillator, linear feedback shift register generator, JTAG). In total, 138 FFs are included in these test structures. These FFs are not TMR protected since the TMR protected configuration registers reset them.

4. **Memory BIST:** Memory Built-In-Self-Test is not protected, as it is kept in reset by an external pin. It contains ∼2700 FFs.

3.2.6 SRAM IPs in the SAMPA chip

In V2 and consecutive prototypes of the SAMPA chip, the DSP block utilizes both standard FFs and Artisan embedded SRAM IPs from ARM [90] for data storage purposes. The former primarily stores static information in the configuration registers, while the latter stores the periodically updated data in the data path chain. Embedded SRAM IPs were favored for their higher area density and lower power compared to conventional register-based memory arrays.

A single-port (SP) SRAM cell typically consists of six transistors and offers a single set of address and data interface. Thus, the SP SRAM cell can only perform a single operation (read or write) at a time [91]. The dual-port (DP) SRAM cell contains eight transistors, offering two sets of data and address paths. This can independently execute both write and read operations [91]. In the DSP, the DP SRAM IPs are utilized where buffering of the ADC data stream is of primary concern.

SP SRAM IPs were implemented for the pedestal memories in the BC1 filter of V2 prototype to save area as the ADC data stream does not buffer in these memories. Instead, the pedestal memories receive data stream from the slow control interface to perform various operations (conversion or subtraction) on the ADC data stream. It is worth mentioning that for the irradiation campaigns, only the pedestal memories were directly accessible via the slow control interface to perform both read and write operations. For instance, a known 10-bits data pattern could be written and read back for each pedestal memory address, individually.

The pre-trigger sample delay module uses (10×192) bits of DP SRAM IP to facilitate a programmable delay chain for the samples. These programmable delays compensate for any delay from the trigger signal. The Ring-Buffer (RB) is the final element of the data path chain. The RB module accommodates two individual DP SRAM IPs to buffer both the header (10×192) and the data (10×6144) part of the packet. This can eliminate data memory overflow risk in case of higher occupancy events. If the header information was stored with payload in a single SRAM IP, the header information would also be truncated with the data. For keeping track of the packets even without the payload, the header information is stored separately in a header memory. For the daisy-chaining feature, the neighbor RB module accommodates two DP SRAM IPs for buffering both the data (10×2048) and the header (10×256) packets, separately.

3.2.7 Soft error handling in the SAMPA SRAM IPs

Since SRAM IPs occupy more than 60 % of the total digital design area in the SAMPA chip, soft error mitigation techniques are not implemented per address basis for area concerns. Pedestal and pre-trigger SRAM IPs do not have any form of built-in mitigation:

- The pre-trigger module is essentially an extension of the existing data path chain. Hence, soft errors in pre-trigger SRAM IPs are of little concern.
- For detectors that will exploit pedestal memories feature of the BC1 filter, a possible workaround is to periodically refresh (overwrite) stored data-content of the pedestal memories in-between data taking runs. It will eliminate soft errors propagation from these memories.

Since the RB memories stores actual data packets before these packets are serialized and transmitted from detectors, soft error contributions from these memories are of significant concern. The RB module generates a header packet, which contains various critical fields of the associated data packet, presented in Figure 3.4[6]. Figure 3.5 presents the packet format where both the header and payload part is referred to as a single packet. The serial output consists of a fixed-length header and a variable-length data payload.

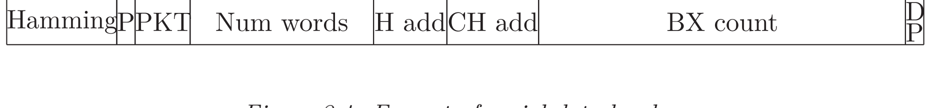


Figure 3.4: Format of serial data header.

0 50

Header | Payload

Figure 3.5: Format of serial data. Length of payload is variable and given in the header information.

The header packet embeds Hamming (50,43) protection bits, with an extra bit is used for the SECDED protection. Hamming bits are interleaved within the existing header packet before the packet is loaded to the RB header memory. During readout, hamming bits are recalculated and compared before the packet is transmitted for serialization. One of the global registers contains a counter. This counter accumulates both single and double (uncorrectable) bit errors from all 32 RB header memories as well as the neighbor RB header memory. The readout packet is discarded upon detecting an uncorrectable error.

Memory pointers of the RB data SRAM IPs are TMR protected. A parity bit is also calculated for the payload part and interleaved in the header packet. It provides a single bit-flip detection mechanism for the payload data.

[6]The header packet contains the respective channel and chip address information, bunch crossing count for event counting, packet type, payload parity information, number of words in the associated payload, hamming code for header error detection and correction, and header parity information.

3.2.8 SAMPA DAS Mode

Direct ADC Serialization (DAS) mode is available for detectors that would not use the data handling capabilities of the SAMPA DSP part. In this mode, raw ADC data is directly sampled, while a clock-gating scheme disables most of the DSP functionality. The data path is susceptible to soft errors in this mode. Therefore, critical signals such as serialization counter and DAS-enable synchronize signals are TMR protected. To avoid glitches from the voter output, the clock division circuit to derive the 5 MHz ADC sampling clock from the 160 MBit/s E-link is not TMR protected. A soft error in the clock division circuit will most likely lead to a phase shift of the ADC sampling clock with respect to other SAMPA chips in the detector. To mitigate this, the spare 11th serial link is used to upstream all ADC sampling clocks together with the data stream on other serial links. As a soft error in one of the clock division circuits may shift the clock phase, monitoring toggling activity from the 11th link can determine this soft error [89].

3.2.9 Clock Manager

The clock manager module divides the incoming 320 MHz serial link clock into multiple clock domains of SAMPA chip[7]. The SAMPA chip operates in four different clock domains:

1. The ADC clock controls data sampling from the analog front-end and acts as the core clock for the data path chain in the DSP core, between pre-trigger and the RB module. The SAR ADC is designed to operate on several clock frequencies of 5, 10, and 20 MHz.

2. The logic between the RB and serial output operates on 160 MHz clock frequency, which is internally generated by the serial link half clock.

3. The serial link data handling circuits operate on the serial link clock of 320 MHz.

4. A bunch crossing counter is implemented, which operates on the LHC bunch crossing clock of 40 MHz. Additionally, the I2C module operates at this frequency.

Since the DSP block operates on multiple clock frequencies, soft error contribution is suspected to be inconsistent between the logic operating on different clock domains. It is mainly due to temporal masking effect reduction, as the logic operating on a faster clock domain is capable of capturing more SET events than their counterparts.

[7] The block diagram of the SAMPA clock generation tree is presented in Figure D.3 in Appendix D on page 170.

3.2.10 Reset manager

The reset manager module is responsible for synchronizing the incoming reset signal to the appropriate clock domains[8]. The reset of the SAMPA chip is divided into hard and soft resets. The hard reset input is an active low differential input, which can be either supplied externally through SLVS receiver or generated by a Power-On Reset (POR) module. A hard reset resets the complete functionality of the SAMPA chip. The embedded SRAM IPs in the DSP block does not have any reset pin. Therefore, a power cycle is required to completely erase the stored data-content in these IPs. The soft reset signal is provided via one of the global registers accessible through the slow control interface. It executes a partial reset of the SAMPA chip by resetting everything besides clock generators and configuration registers.

To avoid synchronization issues between multiple SAMPA chips across a detector, the POR reset signal is brought out to an external pin first, and back into the chip via another external pin[89]. Since the POR reset signal is an optional feature for the ALICE detectors, it was disabled during irradiation campaigns. It would append an additional source to potentially induce SET events on the reset tree, resulting in inefficient beam time. It would also be challenging to identify the real source of triggering hard reset SET events between the SLVS and POR modules.

3.2.11 Slow control registers

The slow control of the SAMPA chip is handled via a master-slave I2C protocol, which follows the I2C standard [92]. A 10-bits addressing scheme is utilized for the read/write operations between 100 kHz and 5 MHz of frequency range. The protocol is presented in Figure D.1 and D.2 with the description in Table D.1 (on page 165).

The SAMPA chip contains two types of registers: global and channel. The global registers are directly accessible through the I2C interface and contain configurations that concern primary operation of the chip as well as the configurations that are common to all channels. The channel registers exist in each channel and contain configurations for each channel individually. The channel registers are only accessible via one of the global registers, as explained in Appendix D.1 (on page 165). A complete list of both global and channel registers of the SAMPA chip is presented in Table D.2 (on page 166) and Table D.11 (on page 173), respectively.

3.2.12 Trigger distributor

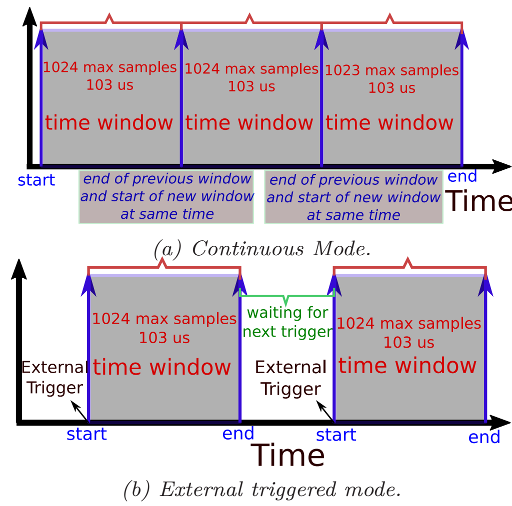
The trigger distributor module is presented in Figure 3.3. It synchronizes external trigger signals and forwards them to the respective modules. A list of SAMPA trigger signals is presented in Table D.3 (on page 167). For example, an event trigger is applied to acquire packets from the SAMPA chip in the triggered

[8] A simplified block diagram of the SAMPA reset generation tree is presented in Figure D.6 in Appendix D on page 178.

readout mode. The event trigger also synchronizes multiple devices running in the continuous readout mode. This event trigger is fed to the event manager module, which further controls the triggering and distribution of the event control signals to all channels.

3.2.13 Event Manager

The event manager module generates a single event packet within a time window[9]. Within this time window, the data stream is sampled from the ADC and forwarded to the DSP. The DSP executes filter and compression operations before the modified data stream is temporary buffered in the RB module. Each time window can configure up to 1024 samples. In other words, every time window is 1024 clock cycles long, where all 32 channels of the SAMPA chip processes the data simultaneously. Each clock cycle is set by the DSP core clock of 10 MHz, providing a maximum time window of $1024 \times \frac{1}{10MHz}$=102.4$\mu$s.



(a) Continuous Mode.

(b) External triggered mode.

Figure 3.6: Different triggered modes of SAMPA chip.

The SAMPA chip supports two readout modes, as illustrated in Figure 3.6: continuous mode and external triggered mode. In continuous mode, a new time window automatically starts upon the end of the preceding time window. In triggered mode, a new time window only starts upon reception of an external trigger signal. At the end of time window, the SAMPA chip goes back to the idle state until the following trigger arrives.

When a time window is ended, a new packet is created with a separate payload and header part. One of the serial output links requests packet acquisition from the RB module in a round-robin arbitration fashion [93]. Some latency can occur from the serial output link request, depending upon the amount of active channels for the respective serial output link. In the SAMPA chip, up to eleven

[9] A time window represents a configurable number of samples within the packet.

serial output links can be enabled, each sharing a maximum of three channels. Table D.9 (on page 171) presents the distribution of channels with respect to the amount of active serial links of the SAMPA chip.

The number of active serial links can affect the soft error contribution from the RB memories. For instance, if only three serial links are active to acquire data from all 32 channels, data acquisition latency per channel will consequently increase as each single link will be shared between 10 channels. It will increase data buffering time in the RB memories, which may lead to higher soft error contribution from the data packets.

3.2.14 Power distribution

The power supply lines of digital circuits often suffer voltage fluctuations during higher switching activities. These fluctuations can couple onto sensitive nodes of the analog circuits and degrade their performance. Both analog and digital blocks of the SAMPA chip are spatially separated to suppress this coupling noise. The SAMPA chip has five power domains, each offering its respective power and ground nets, as presented in Table 3.2.

Power domain	Domain description	SAMPA internal modules
FE1	Front-End 1	CSA, 1st shaper, Gain Arrays, Bias Circuit 1
FE2	Front-end 2	2nd shaper, analog Buffer, Bias Circuit 2, Bandgap
AD	ADC	SAR ADCs
DG	Digital	Digital Core
DR	Driver	I2C and SLVS (TX and RX) drivers

Table 3.2: Various power domains of the SAMPA chip.

All power domains operate on a nominal supply voltage of 1.25 V. The power nets are not merged either inside the chip nor the BGA package but brought outside to individual pins. On the carrier board, a common ground plane is used to connect all internal ground nets. Power nets can either be grouped into [‶FE1+FE2″, ‶AD″, and ‶DG+DR″], or [‶FE1+FE2+AD″and ‶DG+DR″] or a common power plane. During irradiation campaigns, the current consumption was monitored from all power domains individually. It offered possibility to rapidly identify the SEL sensitive power domain within the SAMPA chip.

3.3 An overview of SAMPA prototypes

An overview of various SAMPA prototypes is presented in Table 3.3. It summarizes all memory elements (both SRAM IPs and FFs), which can potentially affect SEE sensitivity of the SAMPA prototypes. Accordingly, soft error mitigation techniques are employed in the consecutive (V2, V3 & V4) SAMPA prototypes. It is worth mentioning that the sensitivity of V3 and V4 prototypes is expected

to be identical for the SEE events. The significant SEE tolerance enhancement between V2 and V3&V4 prototypes is the substitution of SP SRAM IPs with the DP SRAM IPs. More comprehensive details about this improvement are presented in Chapter 6 and 7.

Prototype	**MPW1**	**V2**	**V3 & V4**
Chip size (mm^2)	5×5	9.5×8.9	9.5×8.9
Channels	3	32	32
Memory elements	Only FFs	125K FFs & 2.45MBit SRAM	125K FFs & 2.45MBit SRAM
SRAM IPs	Not present	Both DP and SP	Only DP
Soft error mitigation	Not present	TMR & Hamming	TMR & Hamming

Table 3.3: An overview of various SAMPA prototypes relevant for SEE.

Chapter 4

Test setup for SAMPA irradiation campaigns

Proper test planning is the key for a successful irradiation campaign. It encompasses all aspects in a broader range from selecting an appropriate irradiation facility to test setup development for the campaign. This chapter provides an overview of two independent setups to cover both soft (SET and SEU) and hard (SEL) SEEs during the SAMPA irradiation campaigns.

4.1 SAMPA generic test setup overview

Figure 4.1 illustrates a combined and simplified system overview of the SAMPA test setup for identifying both soft and hard SEEs. Since these campaigns were

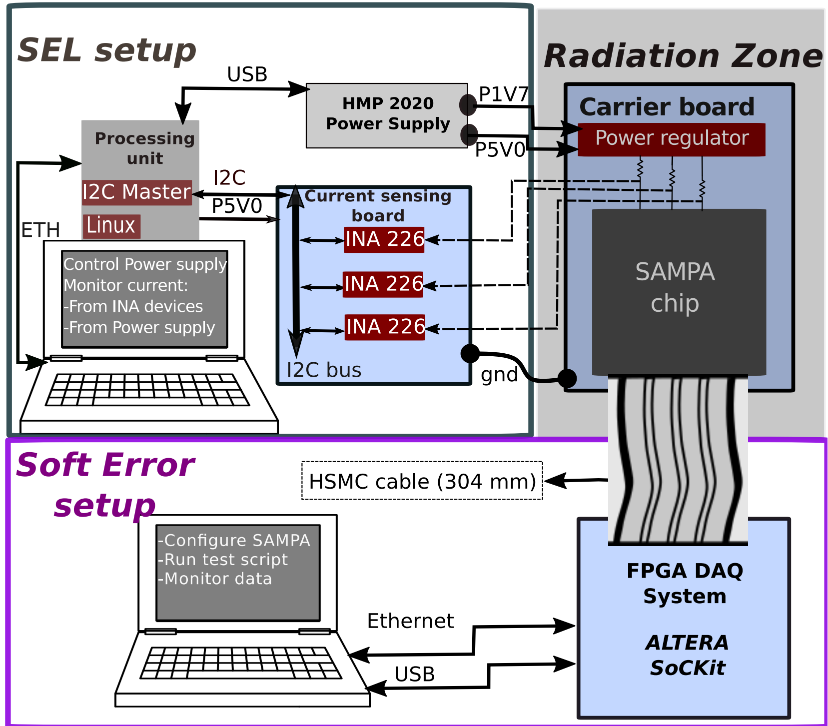


Figure 4.1: A system overview test setup for SAMPA campaigns.

conducted at several facilities with distinct radiation sources (see Table 2.4 on page 36), test setups were appropriately modified to meet requirements at

the respective facilities. Both the SEL setup and the soft error setup modified accordingly as new features were included in the consecutive prototypes.

4.2 Single Event Latch-up test setup

The primary objective of an SEL test setup is to control, monitor, and log supply current consumption data from all power domains of the Device Under Test (DUT) in real-time. In order to distinguish between real (SEL event) and fake (due to wrong DUT configuration) high-current events, the user should acquire extensive knowledge for various nominal standby supply current levels of the DUT expected at different configuration settings.

The typical approach for detecting and removing an SEL event during irradiation campaign is: (i) Employ current sensors at board level to detect excessive current induced by an SEL event, (ii) shut down the power supply if current exceeds a certain threshold level, and (iii) turn on the power after a prespecified amount of time.

Figure 4.1 illustrates a generic SEL test setup of SAMPA campaigns, which mainly consists of a programmable power supply, a processing unit, a current sensing board, a host computer, and the SAMPA carrier board. The carrier boards offered suitable test points for monitoring voltage drops from multiple power rails simultaneously.

4.2.1 Programmable Power supply

During campaigns, a programmable dual-channel HMP2020 DC power supply (from *Rohde & Schwarz* [94]) supplied power to the SAMPA carrier boards. It offered distinct supply voltages for both internal power domains of the SAMPA chip and supportive components on the carrier boards. An USB interface offered both remote access to the power supply and current data monitoring and logging in real-time during the campaigns. The overcurrent protection feature automatically turned off the power supply, in case current exceeded a certain threshold from any of the power rails.

4.2.2 Current sensing board

The current sensing board monitored and transmitted supplied voltage and current consumption from every power domain of the SAMPA chip individually[1]. The current sensing board was designed and fabricated in-house and served as the main interface between the SAMPA carrier boards and the processing unit. The current sensing board hosted multiple INA226 devices [95], where each INA226 device individually monitored supply current consumption for the respective power domain of SAMPA chip. The INA226 is a bi-directional current and power monitoring device with an I2C compatible interface from *Texas Instruments*. Supply current consumption from the DUT was measured

[1] Table 3.2 presents various power domains of the SAMPA chip. The current log from power supply presented a combined supply current consumption from all internal power domains of SAMPA chip.

by sensing shunt voltage drops over the low ohmic (∼100 mΩ) shunt resistors. These shunt resistors were mounted between voltage regulators and internal power pins of the SAMPA carrier boards.

INA226 device integrates a 16-bits ADC, which digitized both the power supply bus voltage[2] and the voltage drop over shunt resistors. The sampled data was transferred to the processing unit, following a master-slave transfer protocol[3]. It allowed a direct computation of power consumption from every single power domain of the SAMPA chip. It is noteworthy that ground planes of both the SAMPA carrier board and the current sensing board were connected to provide a common reference point[4].

4.2.3 Processing Unit

The processing unit is the main communication interface between the user computer, the current sensing board, and the power supply, as presented in Figure 4.1. The essential functionalities of the processing unit are: (i) Provide DC supply voltage between 2.7 V and 5.5 V to the current sensing board, (ii) provide an I2C master device to the address slave devices (INA226) using a master-slave protocol, (iii) provide a Linux platform to control and configure HMP2020 power supply remotely via USB interface, (iv) acquire current log from both INA226 devices and power supply, and (v) transmit data to the host computer over an Ethernet link. During campaigns, the SEL test setup is verified with two different processing units: (i) Smart-Fusion2 (SF2) Starter-Kit [96], (ii) and Raspberry Pi (R.Pi) [97]. Further aspects are presented in Section 4.4.3.

4.2.4 SEL host Computer

A Secure SHell (ssh) connection was established between the processing unit and the SEL host computer, both assigned with dedicated IP addresses. Depending upon requirements of the campaign, either both devices (SEL PC and processing unit) were connected directly via an Ethernet cable or an Ethernet switch was placed in between. The last option could connect several host computers to a single processing unit such that multiple users could simultaneously monitor current log data.

4.3 SAMPA soft error test setup

Unlike the SEL test setup, the soft error test setup is both test and DUT dependent. Figure 4.1 displays a generic soft error test setup for SAMPA campaigns. The setup was mainly composed of the SAMPA carrier board, which was typically resided within the radiation zone, an FPGA based DAQ system, an interface cable, and a host computer to control and monitor the setup.

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[2] Power supply bus voltage refers to the voltage between the voltage regulator and shunt resistor which are mounted on the carrier board.

[3] Processing unit and INA226 device acts as master and slave devices, respectively.

[4] If ground planes were left unconnected, sampled data for bus voltage would differ from expected values. However, it would not affect sampled shunt voltage drop data.

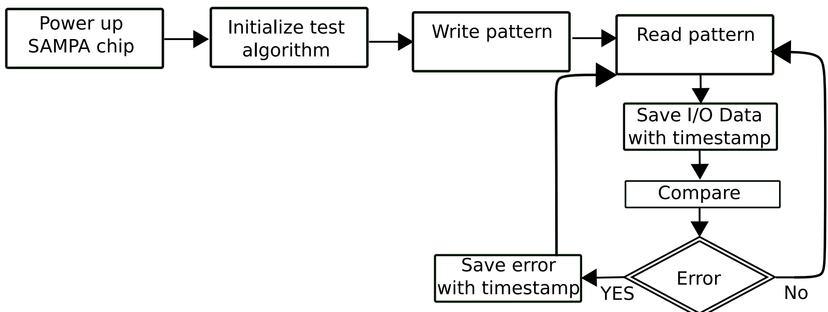


Figure 4.2: Typical flow of SAMPA soft error test setup.

The author developed several test scripts to evaluate soft error sensitivity for various test features of SAMPA prototypes. Figure 4.2 demonstrates a generic flow of these test scripts, which starts with the respective test feature initialization, writing a known pattern, reading and comparing irradiated data, as well as logging both input and output data with appropriate timestamp for future analysis. The script also executed some minor on-site analysis to acquire a soft error rate during the campaign. The outcome of the on-site analysis is important for an efficient campaign, as the user can modify various parameters in the middle of the campaign (i.e., particle beam flux, DUT configurations, or test script).

4.3.1 SAMPA carrier boards

The IPN[5] group developed carrier boards for the SAMPA prototypes. The carrier board interfaced with the DAQ system via a High-Speed Mezzanine Card (HSMC) male connector [98]. All digital input/output and control signals (clocks, triggers, reset) to and from the DUT were granted via a HSMC connector, making it a communication bridge to the outside world. On the carrier boards, a resistor network was placed in-between the HSMC connector and the DUT. The resistor network ensured appropriate voltage levels between the SAMPA SLVS (Scalable Low Voltage Signaling) protocol [99] and the LVDS (Low Voltage Differential Signaling) protocol [100] of the DAQ system.

4.3.2 SAMPA Data AcQuisition (DAQ) System

Arild Velure [89, 101] primarily developed the SAMPA DAQ system, based on an ALTERA System-On-Chip development board called SoCKit. It is centered around a Cyclone-V FPGA [102]. The SocKit hosts an embedded Linux platform with a dual-core ARM Cortex-A9 microprocessor unit. It includes a Hard Processor System (HPS) that connects various peripherals and memory interfaces to the FPGA within a single semiconductor fabric. An overview of the SAMPA DAQ system is presented in Figure 4.3. Several DAQ peripherals

[5]Institut de Physique Nucleaire in Orsay, France.

share a common Avalon Bus using master-slave communication protocol[6], which also establishes communication between the ARM processor and the FPGA.

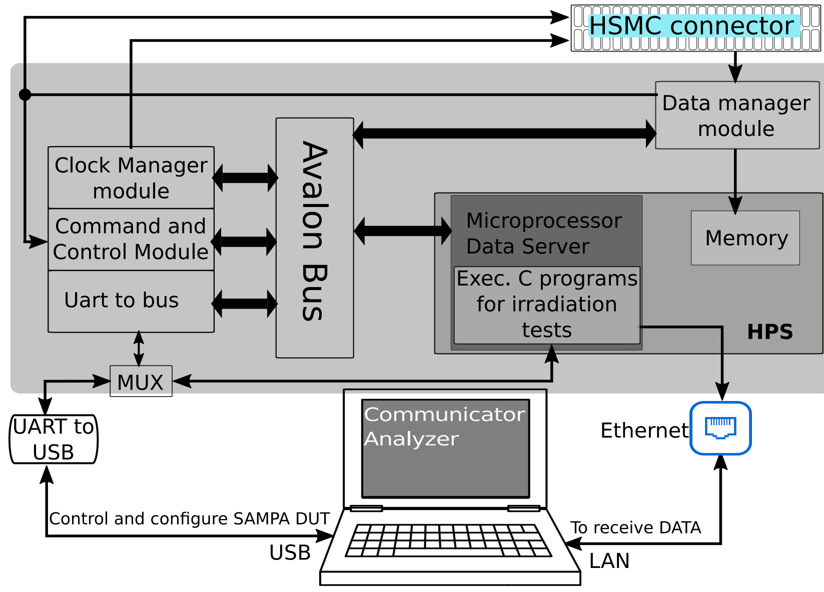


Figure 4.3: Schematic overview of the SAMPA DAQ system.

For general-purpose testing, an USB and a LAN interface established a connection between the host computer and the DAQ system. An Universal Asynchronous Receiver/Transmitter (UART) interface controlled both the internal Avalon bus (control of SAMPA internal registers) and the HPS system via a Multiplexer (MUX). Data packets from the DUT were acquired by the FPGA and transmitted to the host computer via a Gigabit Ethernet interface. The Linux system also offered full access to the incoming data stream from the DUT, as well as the possibility to take control over all the pins of the DUT. More comprehensive details about the various modules of the SAMPA DAQ firmware can be found in Section E.2 (on page 179) and in reference [89, 101].

4.3.3 Host computer

The host computer communicated with the DAQ system via the "SAMPA Communicator" and the "SAMPA Analyzer" software[7]. The SAMPA Communicator software is a graphical user environment written in C# language[8]. It addressed several vital tasks, such as read/write operations of various internal registers (for both DAQ and DUT), clock frequencies to the DUT, appropriate packet acqui-

[6] The HPS operates as a master while the peripherals being the slaves.
[7] Arild Velure [89, 101] developed both software.
[8] SAMPA Communicator offers a plug&play option for non-technical SAMPA users, without requiring in-depth knowledge of the system.

sition mode (trigger or continuous) selection for the DUT, and online status information.

On the host computer, the SAMPA Analyzer program handled serialized data packets from the DUT. The SAMPA Analyzer software was written in C++ language and based on the CERN ROOT framework [103] to provide a common and familiar platform for CERN users. This was automatically configured to acquire data upon successful LAN connection between the host computer and the DAQ board. The acquired data packets could be individually visualized from all 32 channels simultaneously, and automatically saved in root format for further statistical analysis. Figure E.1 (on page 181) and E.2 (on page 182) represent default displays of both SAMPA Communicator and Analyzer software, respectively.

4.4 Practical considerations and setup optimizations for the campaigns

This section summarizes various practical considerations and setup optimizations to conduct efficient irradiation campaigns.

4.4.1 NFS protocol for data transfer

During the accelerator campaigns, the SAMPA carrier boards resided within the radiation zone, where the DUTs were aligned in the center of the beamline. Although both the processing unit and the DAQ board were partially shielded from the beamline, there was a risk of radiation-induced soft errors on these devices. Additionally, if a substantial amount of irradiated data was stored locally in these devices, the internal storage of these devices could also overrun. In both scenarios, there was a potential risk of losing valuable data. Henceforth, separate Network File System (NFS) mount points were set on each of the Linux systems for both devices, which were pointing to separate folders on the host computer(s). It ensured instant data transfer from both devices to the host computer(s) during campaigns.

4.4.2 SAMPA DAQ system optimization

The author performed following modifications in order to optimize the SAMPA DAQ system for irradiation campaigns.

HSMC cable

To isolate the DAQ board from direct beam exposure, a custom HSMC extension cable of 304 mm length (from SAMTEC [104]) was connected between the SAMPA carrier boards and the DAQ board, as presented in Figure 4.1. Prior to campaigns, the author executed measurements to ensure signal integrity and to evaluate the latency due to the HSMC cables.

Practical challenges with Communicator software usage

The SAMPA communicator software granted complete control of both SAMPA and DAQ board registers. Nonetheless, campaigns required a more automatic and efficient way to: (i) Configure these registers, (ii) read register values, (iii) compare outputs with expected values, and (iv) save data with the appropriate timestamp in real-time.

The SAMPA Communicator software supported the UART-to-USB interface. The latency of the serial communication was another limitation for acquiring a substantial amount of data within limited beam time during the campaigns. For instance during the campaign, one test script was dedicated to configure, write, and read all SAMPA registers through slow control interface[9]. This script also executed both writing and reading operations on (10×1024×32) bits of pedestal memory data via channel registers. It is worth mentioning that the pedestal memory was the only SRAM IP accessible for such operations, to fully evaluate soft error sensitivity of embedded SRAM IPs within V2 and consecutive prototypes.

Type	Total registers	Total bits
Global registers	40	243
Channel registers	31 (×32)	350 (×32)
Pedestal SRAM IP	1024 × 10	10240 (×32)
Total		339 Kbit

Table 4.1: Total number of bits which are partially written, read and saved during a single test cycle.

Table 4.1 summarizes the total number of bits encountered in every cycle for performing a write, read, compare, and save operations during script execution. Baud rate of the UART interface was limited to 115,200 for the 8-bits of data. Therefore, only read operation (of all bits) would consume up to ∼30 s during the campaign. All other necessary operations (write, compare, and save) would additionally delay the loop completion time of a single cycle. Due to limited beam time, the author applied a workaround to overcome UART-to-USB interface latency, discussing in the following two sections.

UART to HPS physical address mapping

Most of the SAMPA Communicator tasks can be taken over by the HPS physical addresses mapping. Table C.1 (see Appendix C on page 161) presents direct mapping between UART and HPS physical addresses for internal FPGA modules. Similar to the SAMPA Communicator software, the HPS physical addresses offered full access to the incoming data stream as well as the FPGA modules. Furthermore, the Gigabit Ethernet interface was chosen instead of UART to access internal modules of the FPGA. It significantly enhanced the performance of

[9]Details about the SAMPA slow control registers are previously presented in Section 3.2.11.

previously mentioned test script by completing all operations within a timeframe of 17 s.

Executable C programs

The Linux platform of the DAQ board was based on the YOCTO source package [105], recommended by Altera, where an embedded Linaro-based Linux image was uploaded. By default, Data Server[10] was the only executable C program running on the embedded Linux system of the microprocessor.

To accommodate direct access to the FPGA modules via the HPS physical addresses, the author developed several executable C programs on the Linux platform of the DAQ system. Section C.1 (on page 161) lists typical development steps to generate an executable C program. These executable programs included all essential functionalities required during the campaigns (presented in Figure 4.2), such as DAQ and DUT register configurations, automatized read cycles, online data monitoring and dumping of irradiation test data into a file with appropriate timestamp.

Modification of SAMPA Analyser software

By default, the SAMPA Analyzer software lacked the timing information as well as the timestamp for acquired serialized data packets at the host computer. The author modified the C++ source code of the software to dump both header and payload part of data packets in separate .csv files with μs resolution. The post-campaign analysis was however mainly performed on the ROOT framework due to various built-in statistical functions support. These functions efficiently handled a substantial amount of data from the campaigns. The .csv files were occasionally examined to cross-check results.

Serialized data readout mode

During continuous data acquisition, there was a risk of payload drop due to memory overflow within the DAQ system. There were also uncertainties of data sampling at the changeover point, which could result in invalid data [101]. Since both the beam time and the acquired data from an irradiation campaign is valuable, the data was acquired in triggered readout mode at a reasonable rate, instead of continuous mode to eliminate the risk of data loss or corrupted data.

4.4.3 Some practical considerations regarding SAMPA SEL setup

During the campaigns, the host computer separately monitored and stored current consumption data from both the power supply and the current sensing board. The first SAMPA campaign utilized the Smart-Fusion2 (SF2) Starter-Kit as the processing unit. It was a compact and user-friendly kit with a SF2 FPGA, which is supported by Board Support Packages and Linux packages from

[10] Arild Velure developed the Data Server C code. It was responsible for SAMPA serial link data transmission and TCP/IP connection control with the remote SAMPA Analyzer program running on the host computer in a server/client fashion.

Emcraft. In all consecutive campaigns, the SF2 kit was replaced by Raspberry Pi Model 3 due to its lower cost and higher availability. The Raspberry Pi offered several open-source libraries, which made it easier to utilize General Purpose Input/Output (GPIO) pins for various test objectives. For instance, a 1-wire Digital Thermometer DS18B20 [106] was effortlessly compatible with the Raspberry Pi during campaign No. 4 (see Table 2.4 on page 36). Campaign No. 5 utilized GPIO pins of the Raspberry Pi to generate SEL trigger signals to acquire a SEL sensitivity map.

PYTHON script for the Raspberry Pi

A python script was developed to control the power supply and monitor the current data from the Raspberry Pi[11]. The script offered flexibility to remotely turn off/on power supply during the campaigns. The user could also disable this feature from the script, which helped to evaluate SEL sensitivity for various scenarios: (i) Survival time of the DUT after an event, (ii) whether the following SEL event could further increase current magnitude, and (iii) what kind of acquired data can be affected by the SEL event? During campaign No. 2, the last option was helpful in identifying the source of SEL events.

The current threshold for SEL event could either be set by the acquired current data from the INA226 devices (individual power domain) or by adopting an over-current protection feature of the power supply (combined current consumption from all power domains). Due to the I2C communication protocol, the first option sampled data much faster than the second option, which was supported by the USB protocol.

Current sample from multiple interfaces

A current sample example from both (I2C and USB) communication protocols is presented in Figure 4.4. Current is plotted as a function of exposure time, which is associated with actual SEL events from campaign No. 5. The current log in the upper and lower plot represents the sampled current from HMP2020 power supply and INA226 device, respectively.

The current log curve from the power supply demonstrates that the data sampling capability of the USB protocol is inadequate to consistently capture current jump magnitudes after an SEL event before automatic power cycling of the DUT is initiated. For instance at SEL#1 timestamp, overall current consumption raises with 300 mA of magnitude. The lower plot successfully samples this current jump magnitude, before power cycling of the DUT is executed. However, the upper plot fails to sample this current jump. SEL#3 and subsequent SEL#4 events occur within a relatively shorter timeframe. Contrary to the lower plot, the current log in the upper plot is unable to sample the current magnitude level (0 mA) during the power cycling period.

The plot also demonstrates the advantages of monitoring current consumption from two independent sources in real-time during the campaigns and having

[11] An undergraduate student *Fredrik Winje* initially developed PYTHON script for the Raspberry Pi. Later, the author modified the script concerning the requirements of campaigns.

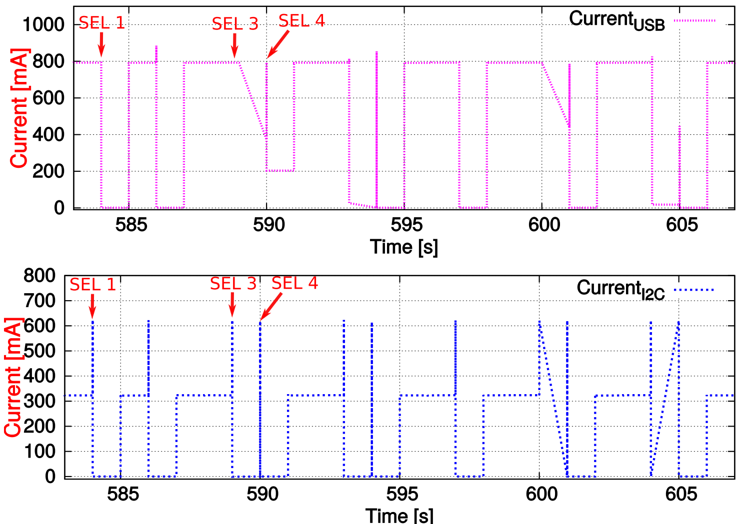


Figure 4.4: Current log sampling comparison between USB and I2C communication interface. The data is taken from campaign No. 5 and presents real SEL events on the digital power domain.

significant test points on the carrier boards to monitor current consumption from multiple power domains simultaneously. For instance, if the current consumption was only monitored from the power supply, it would be time-consuming to identify the SEL sensitive power domain. On the other hand, if the current consumption was monitored only via the INA226 devices, there was a potential risk of data corruption due to radiation-induced errors within the INA226 device[12]. Conclusively, current monitoring from multiple independent sources minimizes the systematic errors, provides additional backup of current log, and confirms the existence of real SEL events.

Selection of low-ohmic shunt resistors

Appropriate shunt resistor values are essential for the accurate operation of the current monitoring setup. According to INA226 datasheet [95], the INA226 device can sense power supply bus voltage within 0-36 V of range. The shunt voltage drop should not exceed $\pm$ 80 mV or + 160 mV for bidirectional and unidirectional currents, respectively. Therefore, the shunt resistor values of a DUT should be selected for its power domain with highest current consumption. Additional margin should also be considered for sampling current jump magnitudes in case of SEL events[13].

Low-ohmic shunt resistors are often tentative due to their thermal and mechanical coefficients alteration. Besides, their total resistance is always higher

[12] Although INA226 devices can be partially isolated from beamline; they should be placed nearby DUT during the campaign.

[13] Digital power domain consumed the highest power in SAMPA prototypes.

due to additional contributions from test points, connectors as well as cables and wires. Overall ohmic resistance contribution should always assess prior to an irradiation campaign in order to accurately determine the current log during the campaigns.

Kelvin or four-terminal technique [107] can be employed to minimize resistance contributions from contacts and wires. The four-terminal technique can improve voltage drop measurements across low-ohmic shunt resistors as compared to the traditional two-terminal measurements. This technique is not tested in the SAMPA SEL test setup as it would increase the complexity of the setup. Also, a highly accurate shunt voltage drop is not required for the SEL detection since a typical SEL event often results in an instant current increase of several orders of magnitude.

Shunt resistors are typically placed in the current conducting path, which can potentially generate a substantial amount of power loss. It is not very important in the SAMPA SEL test setup due to low-ohmic sense resistors. However, this can have an impact for high current applications. During the SAMPA campaigns, the delivered bus supply voltage was always slightly higher than nominal to compensate for any power loss effect due to both the shunt resistors and the long cables.

SELTC current sensing board

The current sensing board presented in this chapter (with INA226 devices) is a rather simple current detecting system, which depends upon the HMP2020 power supply for power cycling the DUT in case of SEL event. A former student (Jonas Birkeland Carlsen) developed an advanced current sensing board (SELTC) during his master project [108]. It offered a power line cut-off of the DUT, independent of the HMP2020 power supply. On the SELTC board, the INA226 devices were upgraded to INA3221 devices [109], which offered shunt voltage drop sampling across multiple shunt resistors (power domains) with a single slave address. Carlsen also assisted the author during the final two SAMPA campaigns (Campaign No. 5 & 6) and verified the functionality of the SELTC board.

Chapter 5

Exploring radiation-induced soft errors in MPW1 and V2 prototype

This chapter presents results from two different proton beam irradiation campaigns, conducted for SAMPA MPW1 and V2 prototypes at The Svedberg Laboratory (TSL) in Uppsala, and the Center of Advanced Radiation Technology (KVI) in Groningen, respectively. The difference between both prototypes is emphasized, concerning various test features accessible in the prototypes. The main objective was to evaluate radiation-induced soft errors (SEU and SET events) performance within both prototypes and to assess TID tolerance of the SAMPA prototypes.

5.1 SAMPA MPW1 prototype

The initial prototype of the SAMPA chip was fabricated in a Multi-Project Wafer (MPW) run and referred to as the MPW1 prototype. Figure 5.1 presents layout of the MPW1 prototype. MPW1 prototype was composed of three mini chips on an area of 5x5 mm^2.

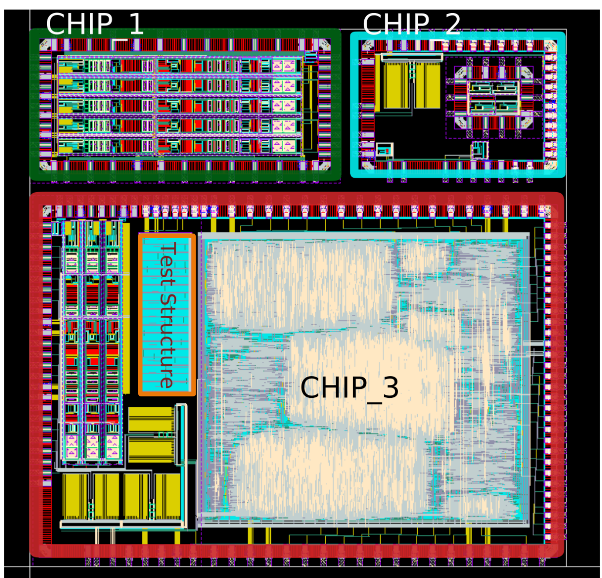


Figure 5.1: Layout of the SAMPA first prototype MPW1.

Chip_1 includes five analog front-end channels of the SAMPA chip, each consisting of a charge sensitive amplifier and a pulse shaper. Chip_2 consists of a 10-bit fully differential SAR ADC, in addition to the custom-made SLVS

drivers. Brief details about Chip_1 and Chip_2 are presented in Appendix E.4 (on page 181), and the performance results are published in reference [110][1]. Due to pure analog blocks of Chip_1 and Chip_2, Chip_3 was more favorable for the irradiation campaigns due to its higher relevance for SEEs.

5.1.1 SAMPA MPW1 Chip_3

The third mini-chip Chip, _3, is presented in the bottom of Figure 5.1, which was composed of 3 complete channels, each including an analog front-end, a ADC, and a simplified DSP block. The total area of the chip was ~3x5mm^2, encapsulated in a CQFP 160 pins package.

The functional specifications of the DSP was immature during the submission of the MPW1 prototype, and a lot of new features were expected in consecutive prototypes. For instance, most of the register-based data storage memory elements of the MPW1 prototype were intended to substitute with the embedded SRAM IPs in consecutive prototypes. Therefore, soft error results of the MPW1 prototype could be insufficient to provide a satisfactory characterization for the final SAMPA versions. Chip_3 was primarily designed to characterize the performance of newly designed analog front-end blocks and the ADC. By keeping the digital part active, digital switching noise can propagate via interconnect and substrate and interfere with analog blocks. It could further degrade overall analog performance [111].

Chip_3 included a dedicated test structure, as presented in Figure 5.1. The test structure consists of a 15,000 long and 1-bit wide shift register (SR) where all FFs are cascaded in a chain. It shifts data by one position at the falling edge of the clock signal. The SR block included the smallest and weakest commercial FFs from the standard digital library for extracting worst-case soft error sensitivity. The SR block is entirely isolated from the rest of the SAMPA blocks, with separate ground and power supply domains. Chip_3 is more beneficial for the SEE campaign as it can evaluate following scenarios:

- It can evaluate SEL tolerance of both analog and digital blocks by monitoring current consumption from multiple power domains during the campaign.
- By irradiating the test structure, the soft error sensitivity of the FFs can be determined, which will help to: (i) Predict the expected failure rate of final SAMPA versions in the ALICE radiation environment, (ii) classify soft errors into various severity levels for the digital core, and (iii) implement appropriate mitigation techniques in consecutive SAMPA prototypes.

[1] The author partially contributed to the layout design phase of chip__1 and chip__2 during his short-stays at CERN in the years 2014 and 2015. At CERN, the author worked closely together with the chief analog designer HUGO Hernandez [84] to accelerate the submission of the initial prototypes. The author has also participated in characterizing analog chip Chip__1 performance, and results are shared with the SAMPA collaboration during weekly meetings. Since these tasks are not directly relevant to the Ph.D. research topic, they are not included here. The presentations are available online at reference [18, 19, 20, 21].

5.2 Irradiation campaign at The Svedberg Laboratory

The Svedberg Laboratory (TSL) [112] is a national research facility, operated by the Uppsala University in Sweden. The Gustaf Werner Cyclotron [113] delivers protons within the range of 20-180 MeV to various irradiation facilities located in the blue hall. The user control room is located at ground level with a distance of ~100 m to the hall. Several interfaces are available between the control room and the blue hall to remotely access the DUT. The SAMPA MPW1 was exposed in proton beamline, which provided a combined effect of both SEE and TID.

5.2.1 Irradiation test setup at TSL

The test setup of MPW1 irradiation campaign is shown in Figure 5.2 and 5.3. A 4 mm thick Ta foil was used to scatter primary proton beam and create a broad uniform proton field. The DUT was located at ~429 cm of distance from the foil, exposed to 159 MeV of average protons energy. Figure 5.2 also presents a square-shaped opening (38×38 mm^2) graphite collimator in the beamline for confining beam spot only at the position of the DUT and shield all supporting electronics of the carrier board.

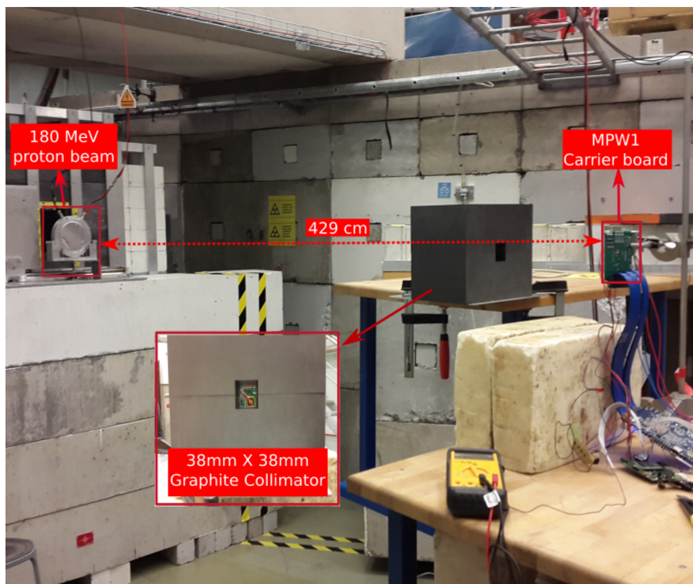


Figure 5.2: SAMPA MPW1 in proton beamline.

Figure 5.3 shows the interface connection for detecting radiation induces soft and hard errors during the campaign. The MPW1 prototype is configured via the FPGA-based DAQ board through the HSMC cable, which provides both the clock and control signals to internal registers of the DUT, and handles the data flow. Additional shielding was applied to the DAQ board, SF2 starter kit as well as the current sensing board. The current is monitored from the power supply

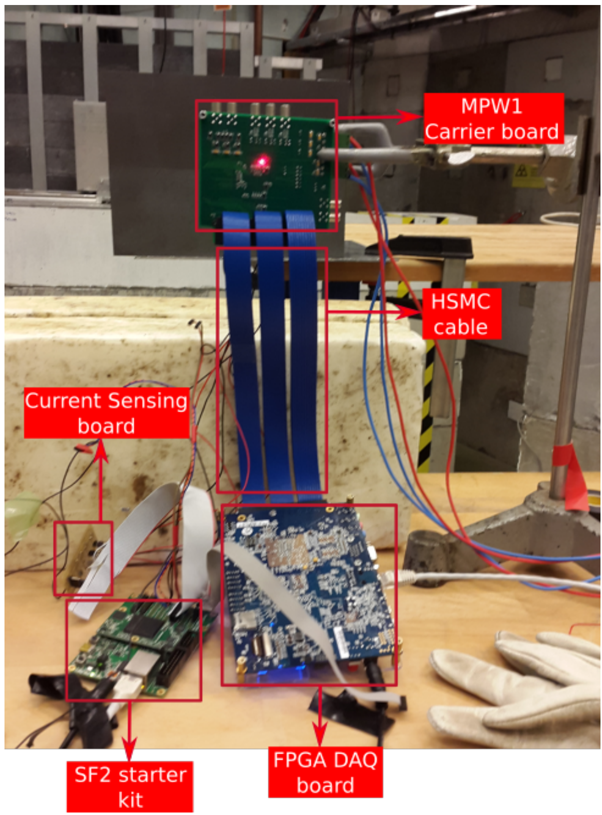


Figure 5.3: MPW1 interfaces for detecting both soft and hard errors during the campaign.

lines via the current sensing board through the SF2 starter kit. A more detailed overview of the irradiation test setup is previously presented in Figure 4.1 (on page 51).

It is worth noting that the HMP2020 power supply, a laptop to control the power supply, and another laptop to access the FPGA DAQ system are not visible in the figures. These devices are located farther away from the beamline within the blue hall. In the control room, one host computer configures the DUT as well as monitors the irradiated data from the SR. Another host computer controls the power supply and monitors current consumption from both power supply and INA226 devices.

5.2.2 Sequence for the shift register test

The SR test program executes the following sequences:

i. The Linux system of the FPGA initiates a dedicated C program, which generates an input pattern from the command line, and an input stimulus is applied to the HSMC pins.

ii. The SAMPA carrier board applies generated input stimuli to the corresponding pins of the SR within the DUT, and corresponding output stimuli are written back to the HSMC pins.

iii. The FPGA reads output stimuli from the SR and stores it into the HPS memory.

iv. The C program reads dedicated register from the HPS memory and dumps both input and output data to the .csv format with an appropriate timestamp.

Different input patterns are initially prepared for the test: (i) Static 0 ("0000"), (ii) static 1 ("1111"), (iii) checkerboard pattern ("010101"), and (iv) random pattern via Linear Feedback Shift Register in the FPGA. During the campaign, only the checkerboard pattern was executed since it could potentially determine soft error sensitivity variations between 0→1 and 1→0 bit-flips. Moreover, it could identify SET events on the clock network tree, which will potentially be masked away by any static input pattern.

The data flow was executed dynamically, where new data was loaded in the SR during each clock cycle, and the run was terminated upon reaching maximum proton fluence. Both input and output data was monitored and logged in 4-Bytes hexadecimal format during each clock cycle.

5.2.3 Bit-flip detection from the shift register

Figure 5.4 illustrates the procedure of detecting abnormal patterns (soft errors) on the SR output data. The serialized output of the SR is alternated every clock cycle, and the output data is displayed in a 32-bits (4-bytes) hexadecimal format. The LSB byte of the hexadecimal format is examined for six consecutive clock cycles in Figure 5.4. A 0→1 bit-flip is considered upon the detection of 0×B instead of 0×A in every even clock cycle. A 1→0 bit-flip is considered upon the detection of 0×4 instead of 0×5 in every odd clock cycle.

Figure 5.4: Soft error detection method in shift register during MPW1 campaign.

5.3 MPW1 campaign test results

The MPW1 was exposed to ∼77 minutes of active beam time, shared between 6 separate runs. Figure 5.5 presents beam dosimetry where flux for each run, together with the total accumulated fluence, is plotted as a function of total irradiated time. The campaign was initiated at a lower proton flux of 6.5×10^6p cm^{-2}s^{-1} for run 1. The beam intensity was increased with a factor of 5 for run 2. The intensity was further increased with a factor of 2 during the last four runs.

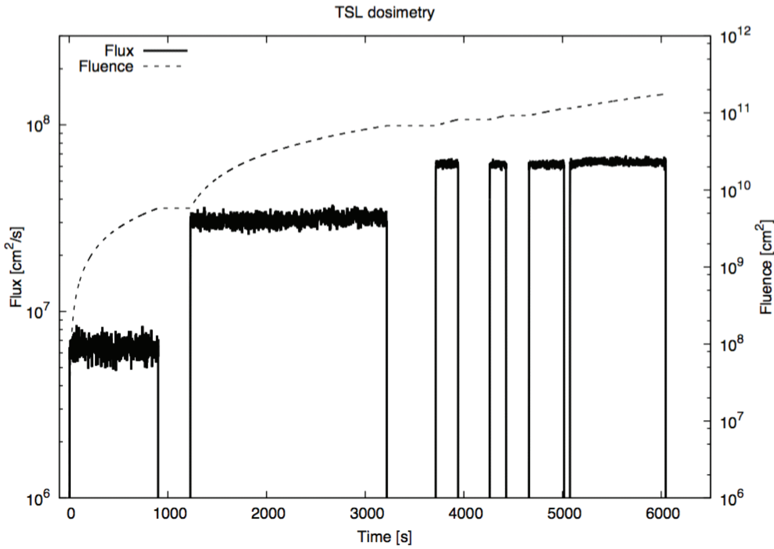


Figure 5.5: Beam dosimetry for SAMPA MPW1 during the TSL proton campaign.

Table 5.1 presents the proton flux, total irradiated time as well as the accumulated fluence from each run. The last column presents the deposited dose in silicon which is calculated by using Equation B.5 (on page 156).

Run No	Time [s]	Flux [p cm^{-2}s^{-1}]	Fluence [p cm^{-2}]	Dose in Silicon [Rad]
1	900	6.5×10^6	5.9×10^9	404
2	2040	3.2×10^7	6.4×10^{10}	4425
3	240	6.2×10^7	1.5×10^{10}	1031
4	120	6.2×10^7	7.4×10^9	512
5	360	6.2×10^7	2.2×10^{10}	1538
6	960	6.4×10^7	6.1×10^{10}	4226
Total	4620	2.9×10^8	1.8×10^{11}	12137

Table 5.1: Beam dosimetry from TSL during MPW1 irradiation campaign.

5.3.1 Soft error results from the shift register

Out of six total runs, only four runs (run 1, 2, 3, and 5) were analyzed for the bit-flips[2]. By using bit-flip detection method from Figure 5.4, soft error cross-section (σ) values of the SR FFs is extracted for all valid runs. It is worth mentioning that run 2 was the longest run, and a few unexpected behaviors were detected during the soft error analysis of this run. This will be discussed in Section 5.3.3. The accumulated soft errors due to these unexpected behaviors are discarded for run 2 and the correlated numbers are summarized in Table 5.2.

Run #	Bit-flip (1→0)	Bit-flip (0→1)	Total bit-flips	Fluence [p cm^{-2}]	σ [cm^2/bit]
1	2	4	6	5.9×10^{9}	$(6.8\pm2.9)\times10^{-14}$
2	22	47	69	6.4×10^{10}	$(7.2\pm1.4)\times10^{-14}$
3	4	9	13	1.5×10^{10}	$(5.7\pm1.8)\times10^{-14}$
5	9	8	17	2.2×10^{10}	$(5.1\pm1.4)\times10^{-14}$
Total	39	68	105	1.0×10^{11}	$(7.0\pm1.2)\times10^{-14}$

Table 5.2: Correlated soft errors for shift register during TSL campaign.

The graph in Figure 5.6 demonstrates a linear correlation between the accumulated number of soft errors and the respective fluence of each run. Although soft errors are aggregated from four separate runs, they fit reasonably with the 1st order polynomial extrapolation, which secures the quality of measured data. The error bars present a confidence interval of 95%.

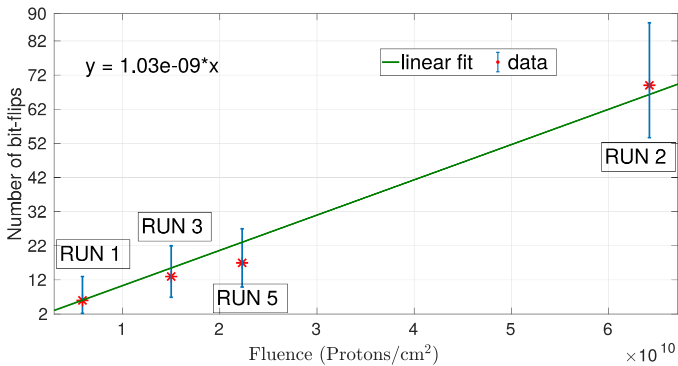


Figure 5.6: Number of soft errors as a function of proton fluence during MPW1 irradiation campaign.

The overall soft error σ value can be determined by extracting the σ value for each run separately, and average the σ values as presented in Table 5.2. Another

[2]A non-nominal setting was applied during run 4. During run 6, the test script was modified to shift 32-bits in a single time window, which made the analysis unnecessary complicated. Hence, run 4 and 6 are discarded from the soft error analysis.

approach is to take the slope coefficient from linear fit equation (presented in Figure 5.6) and normalize the slope coefficient with the number of FFs in the SR, as presented in Equation 5.1.

$$\sigma_{slope_coeff} = \frac{1.03 \times 10^{-9}}{15000} = 6.9 \times 10^{-14} \frac{cm^2}{bit} \tag{5.1}$$

Both methods are accurate, and the results from both Table 5.2 and slope factor do not impose any significant deviations.

5.3.2 Asymmetric bit-flips sensitivity

During the soft error analysis, asymmetry was detected between 0→1 and 1→0 bit-flips. As presented in Table 5.2, the soft error sensitivity for 0→1 bit-flips is 2 times higher than 1→0 bit-flips. References [114, 115] have also previously reported similar sensitivity asymmetry for the standard FFs in 130 nm technology node.

In order to understand this asymmetric bit-flip sensitivity, an architecture overview of the SR structure is presented in Figure 5.7. The schematic in the top presents a typical Master-slave DFF with cross-coupled inverters based latches. Asymmetric bit-flip sensitivity is believed to be due to different critical

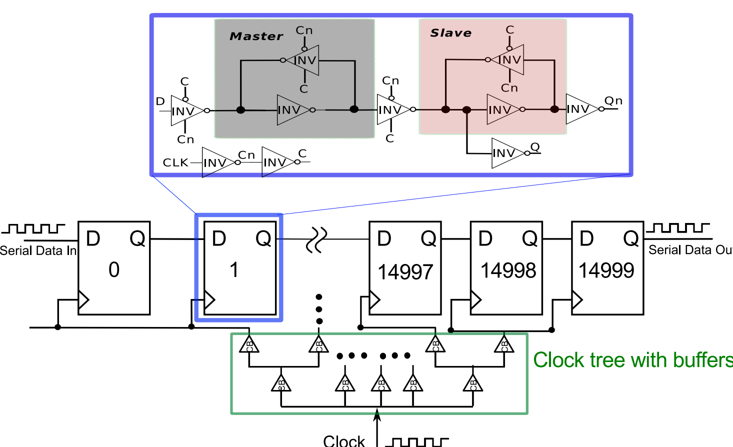


Figure 5.7: Shift register architecture in Chip_3 of MPW1 prototype.

charges Q_{crit} at various sensitive nodes within the master-slave latches of the standard CMOS FFs. This asymmetry has also been reported in reference [40]. In reference [39], SPICE simulations were performed on the identical technology node, where the critical charge required to induce a bit-flip on of the sensitive nodes was 15.6 fC when the latch was holding a high logic value. When holding a low logic value, the critical charge was only 3.2 fC for the identical sensitive

node. Hence, one can expect fewer 1→0 bit-flips than their counterparts when irradiating with particles which deposit similar amount of charge[3].

Conclusively, the observed asymmetry between 0→1 and 1→0 bit-flips from the MPW1 irradiation campaign corresponds reasonably well with simulation results from reference [39]. The physical phenomena behind higher Q_{crit} values while storing logic high state can be related to the physical asymmetrical dimensions of cross-coupled inverters in the CMOS latches.

This bit-flip asymmetry corresponds reasonably well for the first three runs. For the last run (run 5), the bit-flip sensitivity becomes symmetrical, as presented in Table 5.2. This effect can also be seen in Figure 5.8, which demonstrates linear dependence between 1→0 bit-flips and accumulated proton fluence for all runs. However, for 0→1 bit-flips, the accumulated soft errors during run 5 does not lie with the linear curve. This is marked by a black arrow in Figure 5.8.

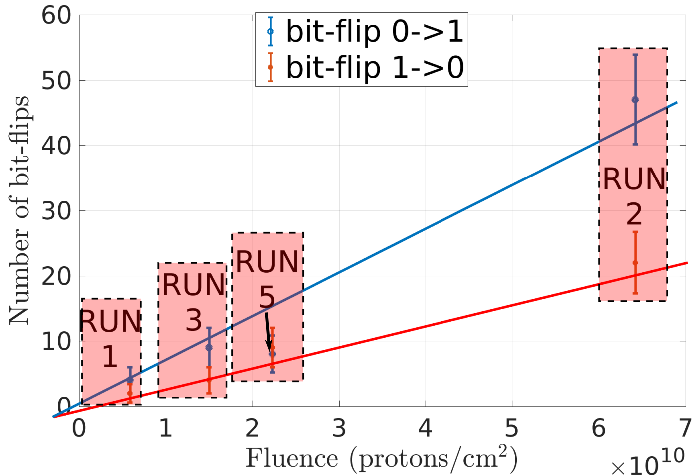


Figure 5.8: 0→1 and 1→0 bit-flip sensitivity as a function of proton fluence during MPW1 campaign.

One possible cause for this behavior can be a sufficient increase in the leakage current of the nMOS transistors at rather low doses for 130 nm TSMC technology, which has been reported in reference [116]. A leakage current increase often imbalances the threshold voltages of the transistors and may impact their soft error sensitivity. Particularly for the nMOS transistors, it may alter the holding capabilities at the sensitive nodes. It then requires additional charge collection (from the incoming particle) to bit-flip the state at the respective nodes. Reference [117] has also reported similar behavior where the soft error σ value of a checker-board pattern increased with accumulated TID. For the checker-board complement pattern, the soft error σ value is reduced after accumulating equivalent amount of TID.

[3]Higher amount of charge should be collected at the sensitive nodes to change the logic high state.

The detected behavior during run 5 may happen as the consequence of ~6.5 kRad TID accumulation up to run 5. As a result, the FFs became more robust against 0→1 bit-flips due to their threshold imbalance. Alternatively, accumulating fewer 0→1 bit-flips during run 5 can also occur due to the statistical nature of radiation-induced SEE events.

5.3.3 Unexpected behaviors from run 2

As stated previously, an unexpected behavior was detected during soft error analysis of run 2, which initially led to a higher (5×) soft error σ value, compared to other runs. The irradiated data was re-examined, and following unexpected signatures were identified:

1. At time 963 s, the output data displayed only 1's (0×FFFFFFFF) for several time windows. This signature persisted for 84 readout cycles before the expected checker-board pattern ("010101") showed again.

2. At time 1426 s, an abnormal behavior was detected on consecutive data pattern after detecting a 1→0 bit-flip. During a typical 1→0 bit-flip, one should expect 0×54 ("01010100") in existing time window and 0×A8 ("10101000") in consecutive time window. During this individual case, the data pattern was changed to 0×A9 ("10101001") in the consecutive time window.

3. At time 1428 s, the output data "stuck" to 0's (0×00000000) and this behavior lasted for another 113 readout cycles.

One of the potential causes for these errors can be that the readout operations interrupted due to soft errors on the output drivers. These drivers are placed in-between the DUT and the HSMC connector on the carrier board, at ~1 cm of distance from the DUT. The FPGA-based DAQ board can be another potential source of these errors since the DAQ board was only partially shielded from beamline.

SET events on the clock source or clock tree buffers can be another source for these errors. Figure 5.7 illustrates a typical clock tree buffer with reduced depth and fan-out. The clock tree network often requires buffers and inverters at multiple levels to distribute the same clock source to all sequential elements in a design. Since these buffers and inverters consist of pure combinational logic gates and do not possess any logical masking effects, a radiation-induced transient with relatively high amplitude and sufficient long duration may propagate to the sinks. It can result in additional clock pulses, which can further lead to the false opening of the sinks, resulting in oversampled data [118].

In the SR test structure of MPW1 prototype, all clock signals were derived from a single source, where no latches or gating techniques were applied on the clock tree network. The clock buffers had a fan-out (strength) between 6 to 12 inverters/buffers. During the campaign, if the elected input data pattern was static 1's or 0's, all SET hits on the clock tree network would be possibly masked away. As the checker-board input pattern was applied, soft error transients from the clock tree network are likely observed on the acquired data[4]. SET events on

the clock tree network seem to be the most valid argument for detected strange behavior during run 2.

Signature#2 represents a scenario where subsequent $k+1$ FF samples logic "0" value twice before the data (logic "1") arrives from the previous k FF in the SR chain. It can occur in case of a SET event on the clock node of $k+1$ FF.

Signature#1 and signature#3 are distinctive as the output displayed only 1's and 0', respectively, for several time windows. The burst of errors in these signatures can depend upon several factors, such as level and node of the clock network tree, which get affected by the SET event [118]. The burst of only 1's and 0's may also appear due to the physical placement of FFs in the SR chain. With the checker-board input pattern scenario, if logic "1" value stores only in even FFs (0,2,4....20), which share clock signal from the same clock buffer instance within the network tree. Then, a SET event on the respective clock buffer can lead to false sampling of the stored value in the subsequent odd FFs (1,3,5,....21) of the chain. Consequently, one can observe 1's at the output node for several readout cycles. References [118, 119, 120] comprehensively presents several common effects and mitigation techniques to eliminate SET events on the clock tree network.

5.4 SAMPA V2 prototype

The second version of the SAMPA chip (SAMPA V2) is a complete replica of the final mass-production SAMPA chip, supporting data processing from 32 channels simultaneously. The performance of the analog front-end and the ADC blocks

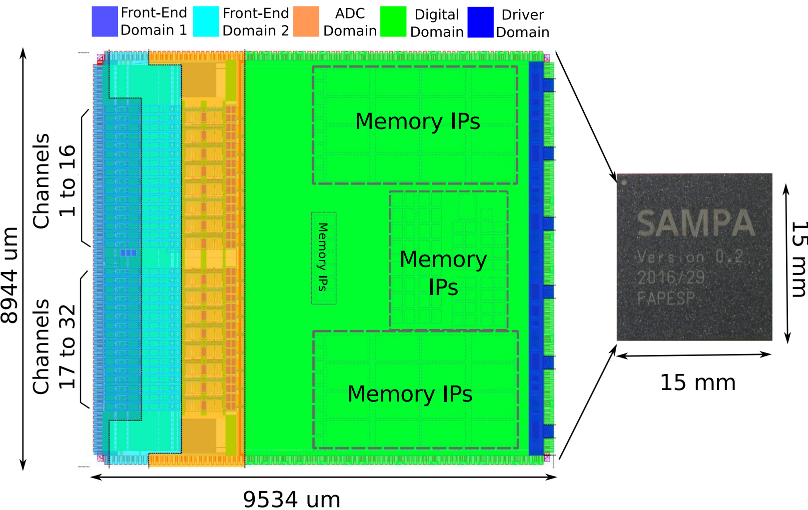


Figure 5.9: SAMPA V2 layout, presenting several internal power domains, with the TFBGA package.

[4] It resulted in a relatively large number of errors in a short period.

of MPW1 prototype were improved in terms of cross-talk, noise as well as the effective number of bits. On the contrary to MPW1, functionality of the digital core was upgraded significantly and included several tests features support.

Figure 5.9 presents layout of the V2 prototype, highlighting all internal power domains. The leftmost partition presents the analog front-end part, which is further splitted into two power domains, followed by 32 ADCs in a separate power domain. The green portion represents the digital power domain, emphasizing physical placement of the SRAM IPs. The blue area represents power domain of the SLVS drivers. The total size of the die is ∼9.6×9 mm^2.

The combination of larger die size together with space restrictions for the final FECs of the ALICE TPC as well as MCH detectors led to design a custom made Thin Fine Ball Grid Array (TFBGA) package. V2 samples were molded inside this package, which will also be employed in the final FECs of the detectors. The package offered an area of 15×15 mm^2 with 1.2 mm of thickness. It offered 372 balls with a pitch of 0.65 mm. Inside the package, a custom-made four layers substrate separated multiple internal power domains of the SAMPA chip.

5.4.1 SAMPA V2 carrier boards

SAMPA V2 carrier boards were designed by the IPN (Institut de Physique Nucleaire d'Orsay) group from Orsay, as a part of the CERN ALICE collaboration. There are two initial versions of the V2 carrier boards: NCCA (Naked Chip

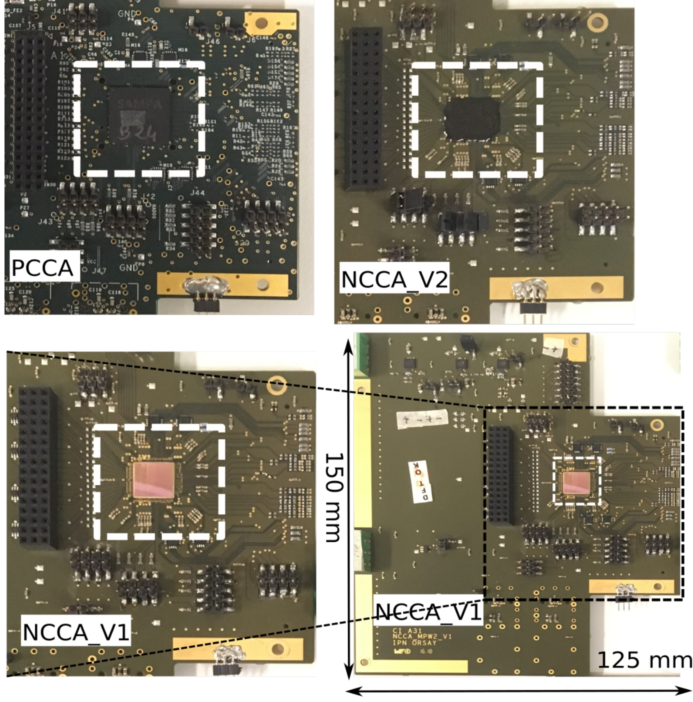


Figure 5.10: Top side of the V2 carrier boards.

Carrier to Altera readout) and PCCA (Packaged Chip Carrier to Altera readout). Figure 5.10 shows various flavors of the V2 prototypes. The top-left presents PCCA (packaged) V2 sample mounted on the PCCA board. The NCCA board utilized chip-on-board technology where naked V2 samples were glued directly on top of the carrier boards, and wires were bonded to the pads. The physical layout of the V2 carrier boards is nearly identical to MPW1, interfacing with the FPGA-based DAQ system via the HSMC connector. The main objective of both NCCA and PCCA carrier boards was to evaluate the impact of package and its substrate on the analog performance of the V2 prototype.

Both PCCA and NCCA carrier boards were reserved for irradiation campaigns. The PCCA carrier boards were preferable for proton campaign since both package and radiation source would be closer to the foreseen operational conditions in the ALICE radiation environment during RUN 3. Another exclusive version (NCCA_V1) was reserved for the heavy-ions campaign. In the NCCA_V1 version, naked V2 samples were left unprotected by any glob-top to ensure that ions could sufficiently penetrate into sensitive regions within the V2 substrate.

5.5 SAMPA V2 campaign at the AGORFIRM facility

At the time of V2 campaign, the TSL facility (previously used during MPW1 campaign) was shut down. Hence, the V2 campaign was conducted at the AGOR Facility for IRradiation of Materials (AGORFIRM) [121], located at the KVI-Center for Advanced Radiation Technology (CART), at the University of Groningen, Netherlands. The AGORFIRM facility utilizes a dedicated beamline from the AGOR superconducting cyclotron [122], which is capable of providing particle beams with protons and ions. The facility can deliver maximum proton energy of 190 MeV with typical fluxes in order of 10^8-10^9 protons cm^{-2}s^{-1}.

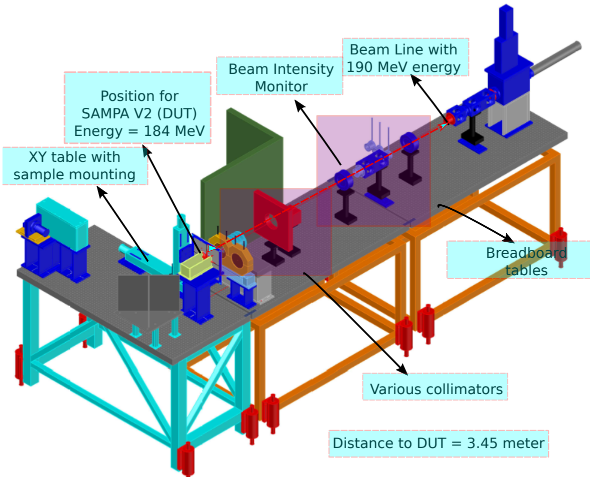


Figure 5.11: The 3D schematic Proton beamline at AGORFIRM with various components in between the existence of the beam source and the DUT [123].

Figure 5.11 displays the layout of the proton beamline, presenting various components located in between the DUT and the beam-exit point. The beamline was located in a dedicated cell of $\sim 10\times 7$ m^2 area. The initial narrow proton beam from the accelerator was broadened as well as flattened using scatter foils, not shown in Figure 5.11. Between the beam-exit point and the collimators, proton flux was monitored via several Beam Intensity Monitors (BIMs). At the DUT position, uniformity of the beam[5] was controlled by a field collimator.

The PCCA carrier board was mounted on an XY table, which allowed 600 mm and 300 mm of DUT's movement both horizontally and vertically, respectively, at 0.01 mm of granularity. After traversing 3.45 m distance in air, the initial 190 MeV of proton energy was degraded to 184 MeV at the location of DUT.

5.5.1 Test setup of the V2 campaign

Figure 5.12 presents the test setup of the V2 campaign, where the PCCA carrier board were mounted on a plate with pre-drilled holes in the left frame. The picture in the right presents partially-shielded supporting components for configuring and controlling various settings of the V2 prototype during the campaign. Additionally, a square-shaped field collimator of 20×20 mm^2 was used to explicitly target packaged V2 sample on the carrier board.

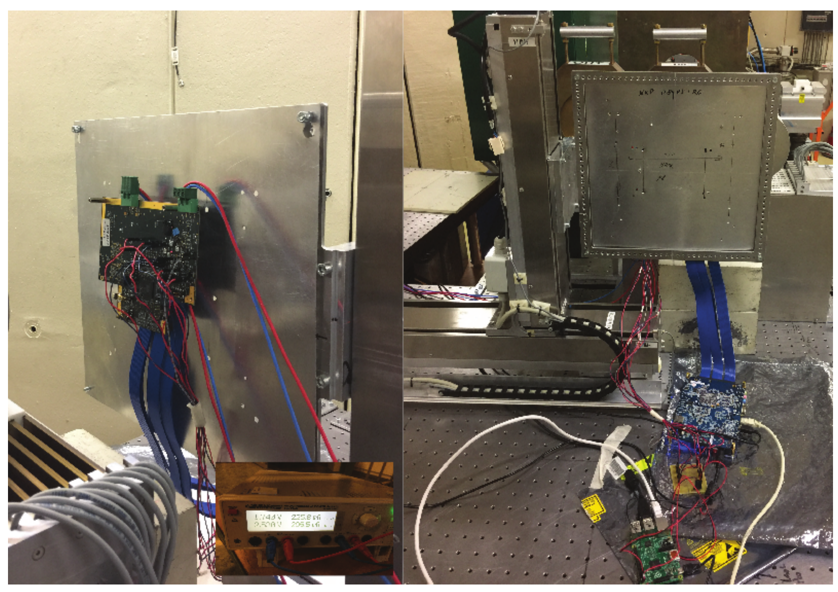


Figure 5.12: The PCCA V2 sample in proton beamline at the AGORFIRM facility.

The system overview of the test setup is previously presented in Figure 4.1 (on page 51). The KVI campaign test setup is relatively comparable to the TSL setup since both facilities offered high energy protons exposure in air. The SF2

[5]The facility offers a wide range of field collimators.

starter kit was replaced by the Raspberry Pi (R.Pi), and the current sensing board was upgraded to host 6 INA devices to monitor current consumption from all power domains of the V2 prototype. Comprehensive details about the test setup are previously discussed in Chapter 4.

5.5.2 SAMPA V2 campaign beam log

In total, 3 PCCA samples were exposed within 10 hours of beam time. Table 5.3 summarizes various test scripts executed on each sample. The samples

DUT ID	RUN No.	Flux [p/cm^2/s]	Fluence [p/cm^2]	Dose [Rad]	Test objective
B_18	1	7.0×10^6	1.0×10^9	62	I^{2}C regs+pedmem
B_18	2	1.8×10^7	2.0×10^{10}	1242	I^{2}C regs+pedmem
B_18	3	1.9×10^7	1.5×10^{10}	900	Scan chain
B_18	4	3.9×10^7	1.5×10^{10}	931	Memory BIST
B_18	5	1.8×10^7	8.9×10^9	558	Pedmem elink readout
B_18	6	1.9×10^7	1.6×10^{10}	986	Baseline elink readout
B_18	7	1.9×10^7	1.5×10^{10}	931	DAS elink readout
B_18	8	2.7×10^8	2.0×10^{11}	12420	I^{2}C regs+pedmem+SEL
B_18	9	3.9×10^8	2.0×10^{11}	12420	I^{2}C regs+pedmem+SEL
Total			4.9×10^{11}	≈30.4K	
B_11	10	3.7×10^7	1.6×10^{10}	975	I^{2}C regs+pedmem
B_11	11	3.7×10^7	2.0×10^{10}	1242	Scan chain
B_11	12	3.7×10^8	2.0×10^{11}	12419	Scan chain+SEL
B_11	13	3.8×10^8	3.1×10^{11}	19431	I^{2}C regs+pedmem+SEL
Total			5.5×10^{11}	≈34K	
B_2	14	4.0×10^7	2.0×10^{10}	1242	I^{2}C regs+pedmem
B_2	15	3.9×10^7	2.0×10^{10}	1242	Scan chain
B_2	16	3.8×10^8	2.0×10^{11}	12171	I^{2}C regs+pedmem+SEL
Total			2.36×10^{11}	≈14.6K	

Table 5.3: The beam log during V2 campaign at KVI.

were irradiated with proton fluxes ranging from 7.0×10^6 to 3.9×10^8 p cm^{-2} s, where high protons flux runs were executed to evaluate SEL and TID effects within a reasonable amount of time. On several occasions during high flux runs, communication between the isolated DAQ system and the user interface was terminated. It could potentially be due to radiation-induced soft errors on the FPGA-based DAQ system or the R.Pi-based current monitoring system[6].

The digital core of the V2 prototype did not offer any intermediate signals for verification. However, Scan Chain (SC) and Built-In-Self-Test (BIST) features were implemented to identify manufacturing defects in the FFs and SRAM IPs,

[6] Both systems should preferably locate far from the beamline, which is difficult due to shorter HSMC extension cable length.

respectively. For the campaign, the author optimized the test setup of these test features to determine soft error σ values from both storage elements.

5.6 Memory BIST

Memory BIST detects internal deficiencies on all internal SRAM IP cores within the digital core. The BIST is initiated by pulling the *sme* pin high (see Table D.14 on page 175). It enables the test by loading a 10-bits checker-board pattern (0×2AA) to all addresses of the SRAM IPs in the first iteration. In the following iteration, it reads and compares the pattern, followed by loading the inverse checker-board pattern (0×155). In the subsequent cycle, it executes read and comparison operations on the inverse checker-board pattern before it reloads the checker-board pattern repeatedly. A more detailed description of the BIST is presented in reference [89].

Upon detecting an unexpected value (soft error) from the SRAM IPs, the BIST alters the status of external pins for one clock cycle. Two status pins are dedicated for error detection, a latched single-ended output *smo* and a pulsed differential output $Serial_Out[0]$ (see Table D.14 on page 175). The pulsed output provides one pulse per address error detection, while the latched output stays high until an error is detected and then goes low until the test is terminated.

5.6.1 Memory BIST procedure and results

During the campaign, an executable C script is developed to support the BIST feature. The script initiates BIST via command line as well as logs toggling activity from $Serial_Out[0]$ pin, which is stored in MEM_ERR register (see Table C.3, address = 0x0E on page 163). During the preparation of test script, it was not feasible to inject any errors in the SRAM IPs manually. Therefore, it was not possible to confirm the correct functionality of the test script beforehand. BIST feature was less favorable for the campaign due to the following practical limitations:

- Multiple bit-flips on identical address counts as a single error.
- BIST executes in parallel on all SRAM IPs, where error outputs are ORed together. If multiple IPs identify soft errors simultaneously, they will mask each other and counts as a single error.
- The typical pulse length of an error is one clock cycle of the memory tester clock domain. If errors occur within two or more consecutive addresses, error pulse from those addresses would be conjoined.
- No real input or output data is available for comparison purposes. The MEM_ERR register has a 10-bit counter for sampling toggling activity from the $Serial_Out[0]$ pin. Upon reaching a maximum count value of 1024, the counter automatically starts back from 0.

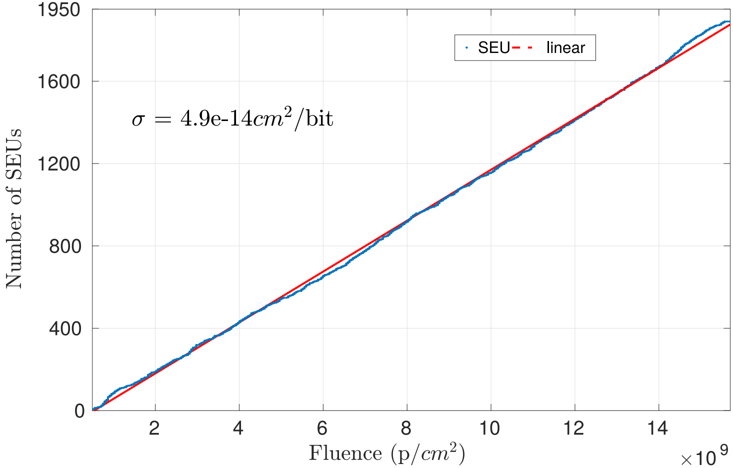


Figure 5.13: Accumulated soft errors from BIST as a function of proton fluence during run 4.

During run 4 from Table 5.3, the accumulated soft errors from BIST are plotted as a function of proton fluence in Figure 5.13. The curve confirms a linear correlation between the accumulated errors and the particle fluence, which is further fitted with a straight line (1st order polynomial). The slope factor is normalized by the total number of bits in the SRAM IPs to extract a soft error σ value of $(4.9\pm0.5)\times10^{-14}$cm^2/bit.

5.7 Scan chain Test

The scan chain (SC) test widely serves as a Design-For-Test (DFT) strategy. It provides observability and controllability of every individual FF within the digital design. The SC feature is primarily dedicated to detect fabrication faults, such as shorts and opens. More details about the architecture of the SC can be found in Appendix E.5 (on page 182). 96% FFs in the digital core of V2 prototype are scannable[7]. These scannable FFs are divided into five SRs, each containing 24259 FFs (24596 FFs in V3 prototype) with separate input (*sdi*), output (*sdo*), and enable (*sen*) pins.

5.7.1 Scan chain test procedure and results

An executable C script was initially developed by the SAMPA design team to test this feature [124]. For the irradiation campaign, the author optimized existing script to generate different input stimuli ("010101", "0000" or "1111") directly from command line. Once initiated, the script continuously monitored and compared toggling activities from all output pins until the run was terminated

[7]The non-scannable FFs are primarily related to the clock divider, reset circuitry and the memory BIST modules.

from command line. Both the toggling data and the accumulated errors were dumped into separate files with appropriate timestamps for further analysis.

The accumulated soft errors from the SC test (run 3 from Table 5.3) are presented in Figure 5.14. The histogram on the left demonstrates a fair soft error contribution in all SRs, where error bars represent a confidence interval of 95%. Coincidentally during this run, accumulated soft errors decrease linearly between SR#0 to SR#4. It likely happened on account of the statistical nature of radiation-induced SEE events. It was further confirmed by performing soft error analysis of the SC test for B_2 sample from run 15, and the results are presented in Figure E.4 (see Appendix E on page 183).

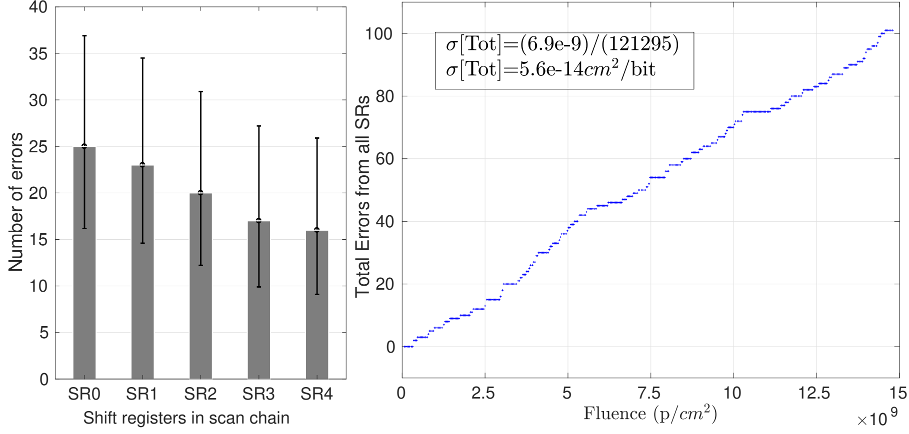


Figure 5.14: Scan chain test results from run 3 (B_18 sample).

The plot on the right hand in Figure 5.14 proves a linear correlation between the aggregated soft errors from all SRs and the particle fluence during this run. The σ_{Tot} value of $(5.6{\pm}0.8){\times}10^{-14}$cm^2/bit is extracted from slope coefficient.

Sample	RUN	Flux [p/cm^2/s]	Eff.Fluence [p/cm^2]	Errors	σ[cm^2/bit]
B_18	3	$1.9{\times}10^7$	$1.5{\times}10^{10}$	101	$(5.6{\pm}0.8){\times}10^{-14}$
B_11	11	$3.7{\times}10^7$	$2.0{\times}10^{10}$	84	$(3.7{\pm}0.6){\times}10^{-14}$
B_11	12	$3.7{\times}10^8$	$1.5{\times}10^{11}$	106	$(5.8{\pm}1.0){\times}10^{-15}$
B_2	15	$3.9{\times}10^7$	$1.9{\times}10^{10}$	115	$(5.0{\pm}0.9){\times}10^{-14}$

Table 5.4: Soft error sensitivity from all irradiated samples during the SC tests.

Table 5.4 summarizes soft error results from all irradiated V2 samples during the campaign. The extracted soft error σ values for run 3, 11, and 15 lie within the Poisson confidence interval. For run 12 with $3.7{\times}10^8$ p cm^{-2}s of high protons flux, the extracted σ value is almost one magnitude lower, compared to other runs. It can potentially occur due to relatively higher number of soft errors during this high protons flux run. For instance, during a readout cycle, the

propagated soft error may have flipped twice internally within the SR, before reaching the output pin. Consequently, the toggling counter at the output pin might fail to capture double error within this single read cycle, which can further lead to a lower σ value for this run.

5.8 Soft error evaluation of the slow control registers

Section 3.2.11 (on page 47) previously stated that the slow control interfaces with two types of SAMPA internal registers: *global* (see Table D.2 on page 166) and *channel* (see Table D.11 on page 173). The channel registers are only accessible via the "channel access" global registers (see Table D.8). Further technical description about the access of channel registers and read/write operations of the pedestal memories (pedmem) is presented in Appendix D.1 (on page 165). This test was frequently executed throughout the campaign as it quantified both the SEE and TID effects within V2 prototypes. Some of the essential aspects were:

I. BC2BSL and BC3BSL (address 0x0E and 0x0F respectively are presented in Table D.11 on page 173) channel registers can be monitored to quantify drift variations in the baseline values due to radiation-induced effects[8]. Any gradual fluctuations in these registers can potentially occur due to TID effects from the analog front-end. Rapid changes may occur due to soft errors in the registers or combinational logic associated with these registers.

II. Soft error evaluation of the TMR protected slow control registers in V2 prototype.

III. The pedestal memory is the only SRAM IP in V2 prototype with direct access for performing both write and read operations on each address individually with known data patterns. It offers a comprehensive soft error analysis of the SAMPA SRAM IPs, compared to the BIST feature. For instance, it can evaluate: (i) single and double bit-flips sensitivity within a single address during the same read cycle, (ii) 0→1 and 1→0 bit-flips sensitivity, and (iii) bit-wise sensitivity of all 10-bits in an entire data word. When shuffling pedestal memory data towards the serial links, it is also possible to deduct soft error contribution from pedestal SRAM IPs by knowing its soft error σ value beforehand. In the end, it can assist in predicting soft error contribution from the ring buffer (RB) and the rest of data path chain in the DSP.

5.8.1 Slow control register test procedure

An executable C script was developed for accessing and monitoring SAMPA slow control registers during the campaign. The script executed both read and

[8] More details about the baseline level calculation are presented in Appendix E.7 on page 183.

write operations either on all or selected slow control registers from command line[9]. Once the script was initiated, it configured various registers and loaded the desired data pattern into the pedestal memories. In consecutive cycles, the script called several functions to: (i) Read pedestal memory data, (ii) acquire baseline values from BC2BSL and BC3BSL registers, (iii) read values from all (global and channel) registers, and (iv) save acquired data in multiple files with appropriate timestamp[10].

As previously stated in Section 4.4.2 (on page 56), the typical duration of a single read cycle was ∼17 s which was dominant by the data acquiring operation of the pedestal memories[11]. The script also executed an online comparison analysis of the acquired data before dumping the results into separate files.

5.8.2 Soft error tolerance of the TMR protected registers

During the campaign, all slow control registers were monitored through the slow control interface. It is noteworthy that few global registers continuously updated stored values due to their dependency on various internal counters. Hence, bit-flip detection was rather complicated from those registers. Besides, most of the static TMR protected registers indicated no signs of bit-flips. Two exceptional registers were:

BC2BCL register

In contrast to promising TID results for baseline levels monitored via BC2BSL registers (presented in Appendix E.9 on page 185), the behavior with respect to soft errors was inadequate. Figure 5.15 plots the sampled values from BC2BSL

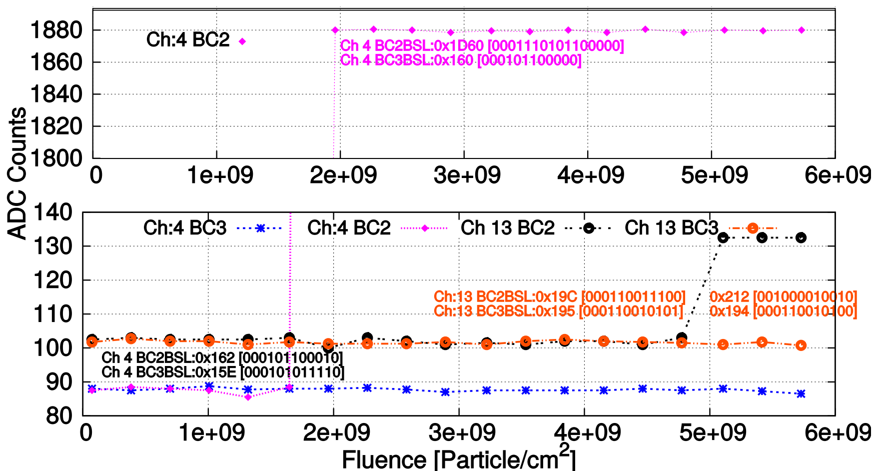


Figure 5.15: Baseline variations between BC3BSL and BC2BSL registers as a function of proton fluence during run 3.

[9]More technical details about the test script is presented in Appendix E.8 on page 184.
[11]It involved 10-bits data word read for all 1024 addresses of 32 channels.

and BC3BSL registers for channel 4 and 13 as a function of proton fluence from run 3.

In the initial phase, both registers sample relatively identical baseline values from both channels. After accumulating a proton fluence of 1.6×10^{9}p cm^{-2}, the sampled value in the BC2BSL register rises unexpectedly from 88 to 1880 ADC counts for channel 4. This new baseline level is persistent until the run is terminated. Similar behavior also occurs for channel 13 after accumulating a proton fluence of 4.8×10^{9}p cm^{-2}, where sampled value in BC2BSL register rapidly changes from 102 to 132. On the other hand, the sampled values in the BC3BSL register are relatively stable for both channels during this time frame.

After a discussion with the SAMPA design team, it was confirmed that the detected behavior on the sampled values of BC2BSL register likely occurred due to radiation-induced soft errors. The potential source of such errors can either be the BC2BSL register itself, which eventually samples the calculated baseline value or the internal FFs of the BC II filter. The former argument is further investigated by analyzing sampled values in hexadecimal format. For instance for channel 4, 0×162 value was changed to 0×1D60 due to a potential soft error. The XOR comparison between these two hexadecimal values results in 0×1C02, indicating four simultaneous bit-flips on various bit positions within BC2BSL register. Although multiple bit-flips can occur, one would have suspected identical multiple bit-flips signatures on other TMR protected registers as well. Throughout the campaign, this multiple bit-flips signature was only detected in the sampled values of the BC2BCL and VPD registers.

BC II is a moving average filter which is based on an expression from Equation D.1 (on page 171). Figure D.5 (on page 177) presents comprehensive circuit details of BC II filter, where several non-TMR protected registers (*sum* and *old_val*) are identified and highlighted. With the effective proton fluence of 2.7×10^{11}p cm^{-2}, 12 soft errors are detected in BC2BSL registers for B_18 sample. It provides a σ_{BC2} value of $(4.4\pm1.4)\times10^{-11}$cm^{2} per SAMPA chip for the BC2BSL register. Equation 5.2 further normalizes the extracted σ_{BC2} value by the number of internal FFs in BC II filter.

$$
\begin{aligned}
\sigma_{FF} &= \frac{\sigma_{BC2}}{(old_value_{FFs} + sum_{FFs}) \times Total_channels} \\
&= \frac{(4.4 \pm 1.4) \times 10^{-11} cm^2}{(14 + 26) \times 32} \\
&= (3.44 \pm 1.1) \times 10^{-14} cm^2/bit
\end{aligned}
\tag{5.2}
$$

The calculated σ_{FF} value is fairly comparable with the previously extracted σ_{FF} values from Table 5.4. It confirms that the detected rapid changes in the sampled BC2BSL register values are potentially due to radiation-induced soft errors within the internal FFs of the BC II filter.

VPD register

Variable PeDestal register (see Table D.11 on page 173, address = 0x0D) is a READ register. It stores baseline values which are calculated by a variable

pedestal filter in the first baseline correction filter (BC1 unit). The variable pedestal filter is calculated by employing an infinite impulse response algorithm to achieve self-calibration of the baseline pedestal values from ADC[12].

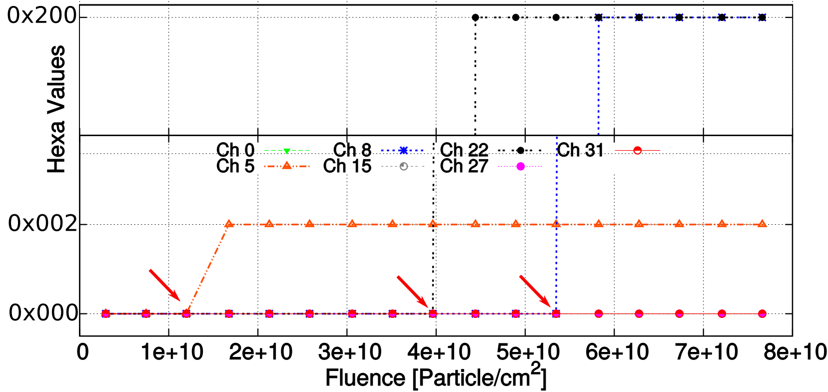


Figure 5.16: Bit-flips in VPD register during run 8.

During the campaign, BC1 unit was disabled and a default value of 0×000 was expected in the VPD register. Figure 5.16 plots sampled hexadecimal values from the VPD registers of some selected channels as a function of proton fluence during run 8. The run starts by sampling the default VPD register values of 0×000 from all channels. After accumulating a proton fluence of 1.2×10^{10}p cm^{-2}, the sampled value in VPD register of channel 5 rapidly changes to 0×002, indicating a 0→1 bit-flip on 2nd LSB. Later at a protons fluence of 4.0×10^{10}p cm^{-2}, the sampled value in VPD register of channel 22 changes to 0×200, indicating a 0→1 bit-flip on 1st MSB. Another bit-flip is occurred on the identical bit position in the VPD register value of channel 8, at the fluence of 5.4×10^{10}p cm^{-2}.

In total, 12 such events are detected in various VPD registers with an effective proton fluence of 2.42×10^{11}p cm^{-2} for the B_18 sample. These events were detected on random channels as well as bit positions and persisted until the end of the respective runs. The extracted σ_{vpd} value of these events is about $4.96\pm1.6\times10^{-11}$cm^2 per SAMPA chip.

A detailed circuit description of the VPD register is presented in Figure D.4 (on page 176), where internal non-TMR protected *sum* register (28 FFs) are identified and highlighted. The σ_{vpd} value is further normalized to 28×32 FFs for extracting σ_{FF} value of $(5.54\pm1.8)\times10^{-14}$cm^2. Similar to BC2BSL register, the normalized σ_{FF} value for VPD register also confirms bit-flips on internal *sum* register within the VPD circuit.

[12] Another relevant filter is FPD (Fixed PeDestal) which is associated with a READ/WRITE FPD register (see Table D.11 on page 173, address = 0x0C). The BC1 unit can be configured to subtract the incoming ADC data stream from the values stored in either FPD or VPD filter. Table D.12 (on page 174) summarizes various operation modes of the BC1 unit.

5.8.3 Slow control register test results for pedestal SRAM IPs

During the initial cycle of the slow control register test, a checker-board pattern (0x155) was loaded to all pedestal memories. During the following cycles, both read as well as comparison operations were executed until the run was terminated. It is worth mentioning that all irradiated samples of V2 prototype experienced current jumps/SEL events during this campaign[13].

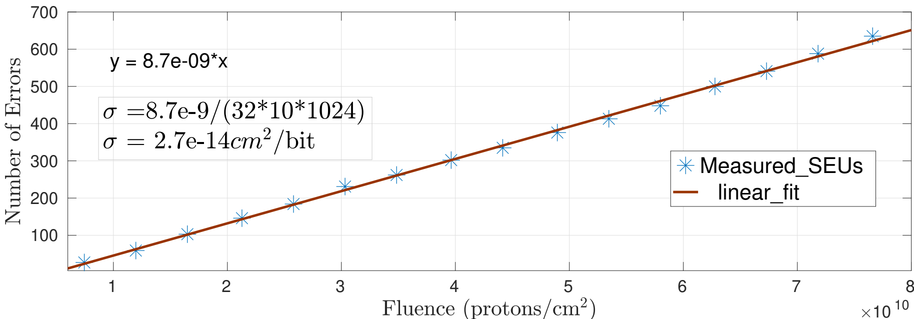


Figure 5.17: Soft errors from pedestal memories as a function of proton fluence during the start of run 8, prior to current jump event.

Figure 5.17 shows accumulated soft errors as a function of proton fluence before the current jump event occurred. The plot demonstrates a linear correlation between the accumulated soft errors from all 32 channels and the proton fluence. The σ value of 2.64×10^{-14}cm^2/bit is extracted from the slope coefficient, which is normalized by the total number of bits in the pedestal memories. As the current jump events directly affected data content of the pedestal memories, acquiring a significant amount of soft errors from a single run was challenging[14].

The upper histogram in Figure 5.18 represents the soft error distribution from each channel during run 8. Although relatively less soft errors are detected between channel 10 and 23, the error bars present a confidence interval of 95%. The histogram also represents 1→0 and 0→1 bit-flips sensitivity results of all channels. The accumulated soft errors may not fully possess 0→1 and 1→0 bit-flips symmetry from individual channels[15]. Nevertheless, aggregated errors from all channels represent a higher degree of bit-flips symmetry.

Another analysis evaluates the bit-wise soft error sensitivity on the acquired data of pedestal memories from same run. The results are presented in the lower histogram of Figure 5.18. It confirms a uniform distribution of accumulated soft errors between all 10-bit positions of the data words. The bit-wise soft error distribution lies within an acceptable range of error bars.

[13] More details about these current jump events will be discussed in Section 6.1.1 on page 97.

[14] Proton fluence in the plot presents only a fraction of total proton fluence accumulated during run 8 (see Table 5.3).

[15] Due to fewer accumulated errors from individual channels and the statistical nature of the soft errors.

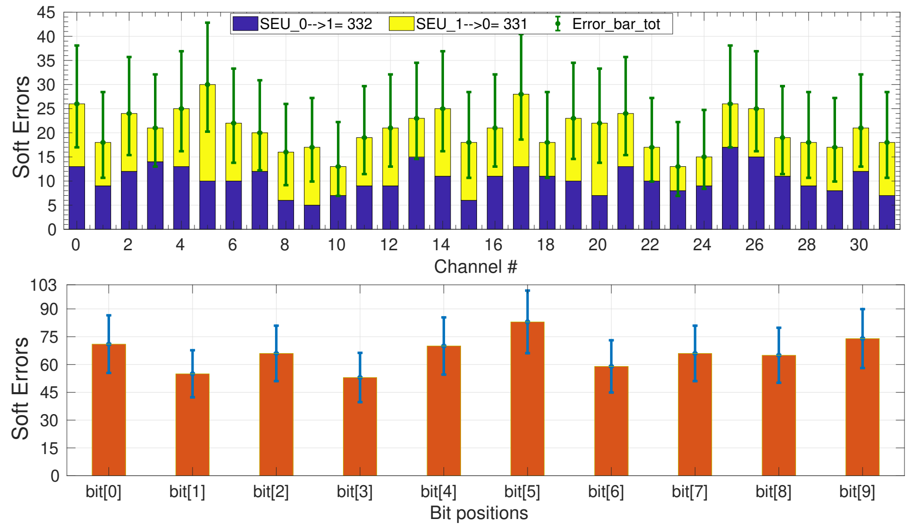


Figure 5.18: Histogram representing soft error distribution of every channel and bit position during run 8.

In order to evaluate chip-to-chip variation in soft error sensitivity of pedestal memories, both the soft errors and the accumulated proton fluence is combined from several short runs prior to the current jump events occurred. The results are summarized in Table 5.5. It demonstrates that the extracted σ values of all irradiated samples lie within an acceptable range of confidence levels. Although the deposited TID differs between each sample, the soft error σ values are relatively identical. Conclusively, this confirms that 11.2 kRad of accumulated TID does not impose any effect on the soft error sensitivity of the pedestal memories.

Sample	**Run #**	**Fluence [p/cm^2]**	**TID [KRad]**	**Soft Errors**	**σ[cm^2/bit]**
B_18	1,2,8,9	1.8×10^{11}	11.2	2077	$(3.5\pm0.5)\times10^{-14}$
B_11	10,13	1.1×10^{11}	6.6	1101	$(3.2\pm0.5)\times10^{-14}$
B_2	14,16	1.0×10^{11}	6.3	1179	$(3.6\pm0.5)\times10^{-14}$

Table 5.5: Chip-to-chip variation evaluation for the pedestal memories soft error sensitivity.

5.9 Serial links stability and soft error sensitivity of the serialized data

The readout stability of the serial links and the soft error sensitivity of the serialized data were assessed in run 5, 6, and 7. During these runs, data packets were acquired through serial links via the FPGA-based DAQ board, which

were further transmitted to the host computer via an Ethernet link. On the host computer, data was handled by the "SAMPA Analyser" software, formerly described in Section 4.3.3 (on page 55). The "SAMPA Communicator" software was used in these runs to synchronize readout communication between the DUT and the DAQ board.

5.9.1 Irradiation test procedure for serial links test

Ideally, serialized data packets should be acquired by injecting charge on the analog inputs, configuring various parameters within the DSP filters, and monitoring serialized data packets accordingly. Due to the limited beam time and access to the DUT during exposure, such detailed characterization was unachievable. As several soft errors could trigger simultaneously during exposure, identifying the exact source of error could also become complicated. For the sake of simplicity, three different cases were tested where no charge was injected on the analog inputs, and most of the DSP functionality was kept to its default. The data packets were acquired in triggered readout mode with 10 Hz of frequency[16]. The worst-case activity was assumed by enabling all eleven serial links, where each serial link was shared among 3 channels[17].

5.9.2 Test results from the pedestal run mode

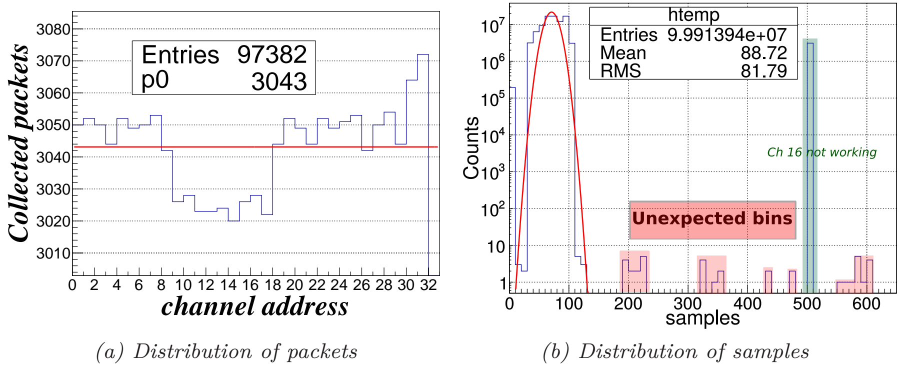
The SAMPA chip supports a "pedestal run" readout mode, which operates without the zero-suppression feature and acquires baseline levels from the analog front-end. This mode generates a significant amount of data packets within a relatively short time, making it ideal for the campaign[18]. All DSP filters are bypassed, and digitized baseline values are pipelined up to the RB module in the data path chain. The RB module creates packets and transmits to the serializer (See Figure 3.3 on page 42 for details). The potential sources of soft errors are the data memories ($6144\times10\times32$), the pipelined FFs (9920), and the output serializer modules.

Figure 5.19a represents the distribution of packets from all channels, each acquiring averagely 3040 packets. The plot demonstrates promising readout stability of all serial links with no functional interrupts up to an accumulated proton fluence of 1.58×10^{10}p cm^{-2}, where 97,382 packets were acquired in total. Unexpectedly, the channels in-between 9 and 18 acquired marginally fewer packets than their counterparts. During post-campaign analysis, the B_18 sample was configured identically in the lab and fairly equivalent amount of packets were acquired. Figure E.6 (on page 186) presents identical behavior and demonstrates that the average number of acquired packets varies between channels. Buffer overflow in the DAQ board or weaker driving strength of the serial links between the DAQ board and the carrier board can lead to such issues.

[16] Section 4.4.2 on page 56 describes the limitations of continuous readout mode for the irradiation campaigns.

[17] See Table D.9 on page 171 as well as Section 3.2.13 on page 48 for details.

[18] During the operation of the SAMPA chip in the ALICE detectors, pedestal runs will be used for calibration purposes to acquire values for the pedestal memories and other relevant parameters of the DSP filters.



(a) Distribution of packets

(b) Distribution of samples

Figure 5.19: Data packets acquired from all channels during run 6.

Channel 30 and 31 acquired more packets than their counterparts since the 11th serial link was only shared between these two channels (see Table D.9 on page 171 for more details).

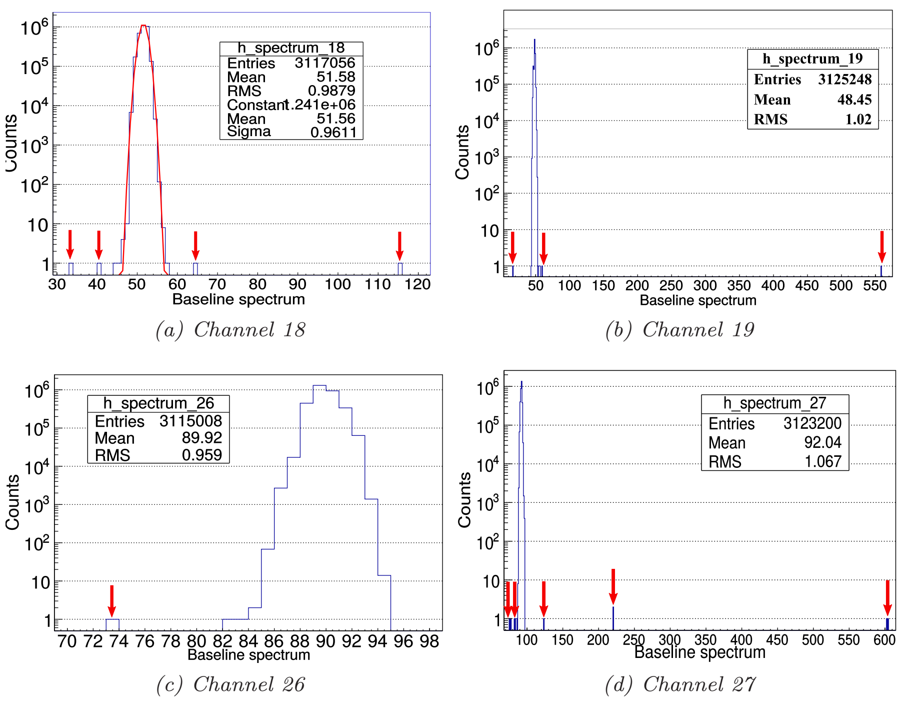
Figure 5.19b presents all 10-bits sample distribution from this run, where the x-axis represents 10-bits ADC values, and the logarithmic y-axis represents bins (counts) of each ADC value. The fitted red curve on the lower spectrum represents the Gaussian distribution of the baseline values for 31 out of 32 channels. It lies within the ADC values range of 25-140 which is expected due to process mismatch between the channels[19]. The higher counts at 500 ADC value represents the baseline level of a partially unresponsive channel (Channel 16) of the B_18 sample. This issue was already spotted during local lab testing prior to the campaign, where no output pulse was generated upon the injection of charge on the analog input of this channel, and the digitized baseline level displayed a constant ADC value of 500. Figure 5.19b also presents several unexpected bins, which randomly distribute within the ADC spectrum range of 200-600. These strange bins arise either as a consequence of some internal noise generation within the DUT or radiation-induced soft errors on the acquired data packets.

The former argument is verified by taking identical measurements on the B_18 sample under similar circumstances locally in the lab. Figure E.7 (on page 186) presents the ADC spectrum of some selected channels with the Gaussian distribution[20] and the extracted mean values. No strange ADC bins are detected outside the expected Gaussian distribution range during local lab testing. It concludes that likely, the detected strange ADC bins during beam exposure occurred due to radiation-induced soft errors on the data packets.

This issue is further investigated by examining the ADC spectrum of each channel individually. Figure 5.20 presents the ADC spectrum distribution from

[19] The data is directly comparable with the baseline values acquired from BC2BSL and BC3BSL slow control registers, presented in Figure E.5 (on page 185) for B_18 sample.

[20] The Gaussian distribution is foreseen in the channels due to systematic effects from the processing chain.



(a) Channel 18 *(b) Channel 19*

(c) Channel 26 *(d) Channel 27*

Figure 5.20: Distribution of baseline spectrum on selected channels during run 6..

four selected channels, where the Gaussian distribution and nominal ADC mean values are identical to the local lab testing results for respective channels. However, several strange ADC bins with fewer counts are perceivable from all channels. These strange ADC bins are distributed randomly between the channels, potentially due to bit-flips on random bit positions of the acquired data samples. For instance, a single entry at 115 ADC bin in Figure 5.20a can potentially occur due to 1→0 bit-flip on the 3rd MSB of the ADC mean value of 51 for channel 18. It is comparatively possible that there are hidden bit-flips on lower significant bits of the mean value, which are confined within ± Gaussian distribution range around the mean value. Thereby, this graphical evaluation may underestimate the actual amount of soft errors.

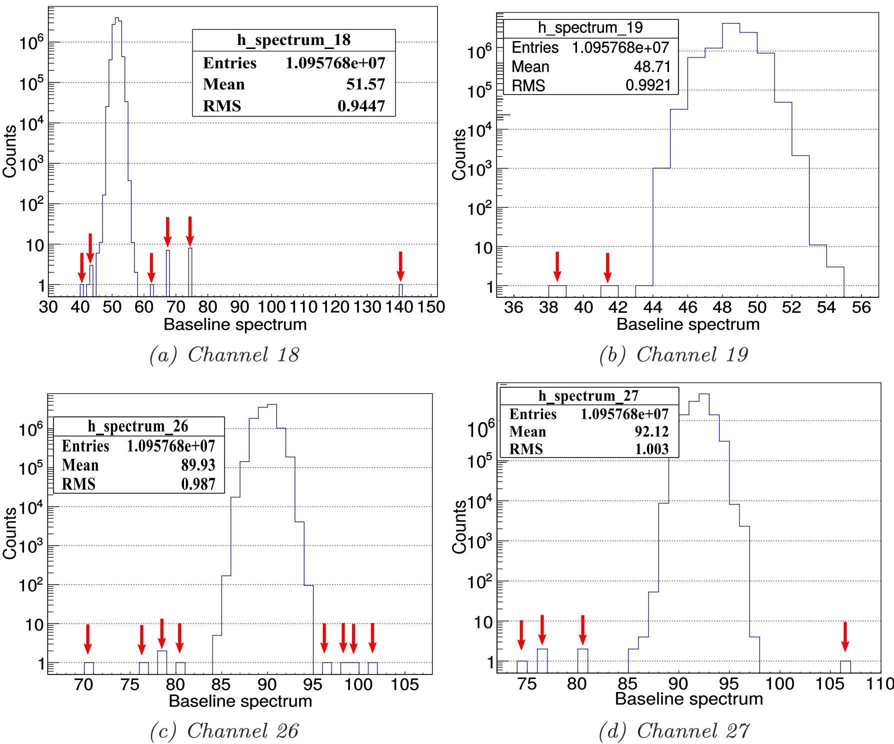
5.9.3 Test results from the DAS mode

In DAS mode, the raw ADC samples are directly serialized and a clock-gating scheme disables most of the DSP functionality. More details about the DAS mode are previously presented in Section 3.2.8 (on page 46). Potential sources of soft errors are: (i) 32×20 FFs in the state machine of SAR ADC , (ii) 42×10 serialization FFs, and (iii) SLVS drivers[21].

[21] Soft error contributions from the SRAM IPs and the pipelined FFs of the DSP block are abolished in DAS mode.

Since the DAS mode only supports continuous data readout mode, a workaround was implemented in the "SAMPA Communicator" software to avoid memory overflow risk in the DAQ system[22]. The maximum amount of samples during each step was limited to 960, which corresponded to 30 samples from each channel. The data throughput was roughly 1.5 kHz per channel during this run, resulting in a total throughput of 45 kHz for all channels. Compared to run 6 with 10 Hz of triggered readout mode, a significantly higher amount of data were acquired during run 7.

First and foremost, run 7 validates persistent data readout up to an accumulated proton fluence of 1.50×10^{10}p cm^{-2}. The combined ADC spectrum in Figure E.8 (on page 187) demonstrates that $\sim3.5\times10^{8}$ samples are acquired from all channels. The ADC spectrum distribution of some selected channels is further



(a) Channel 18 *(b) Channel 19*

(c) Channel 26 *(d) Channel 27*

Figure 5.21: Baseline spectrum distribution of selected channels during run 7.

plotted in Figure 5.21. In comparison with the ADC spectrum from Figure 5.20, plots in Figure 5.21 confirm identical ADC mean values and the Gaussian spread range. However, the strange ADC bins can be seen relatively closer to the Gaussian distribution range of the ADC spectrum in run 7. Although these strange bins can potentially occur due to soft errors in the serializer modules or

[22] By Arild Velure.

the FFs in the state machines of the ADCs, the amount of exposed FFs in the DAS mode is relatively low. Based on the previously extracted σ_{FF} values, the accumulated strange ADC bin counts are significantly higher in run 7.

ASET events on the analog front-end can be another potential source for these strange bins. For instance, these bins are marginally closer to the upper and lower tails of the Gaussian spread in Figure 5.21. This can occur as a consequence of both positive and negative ASET events on the analog baseline level[23]. The typical duration of the SET event is within ps range, while the sampling time of the SAMPA ADC is 12.5 ns. Thereby, most of the ASET events are not captured and sampled by the ADCs. If ASET events occur closer to the sampling window of the ADC, these events can get sampled along with the analog signals. These can further lead to similar ADC bins, which are detected closer to the Gaussian distribution range of the ADC spectrum.

Even if this hypothesis is correct; it may raise concerns regarding the fewer strange bins events detected near the Gaussian distribution range from run 6, previously presented in 5.20. The slow triggered readout mode of 10 Hz justifies this concern. It is even possible that a similar amount of ASET events were actually induced on the analog front-end during run 6. Nonetheless, the trigger signal only enabled an active time window of 103 μs for data readout. Only those ASET events which were sampled by the ADC within this time window appeared on the serialized outputs.

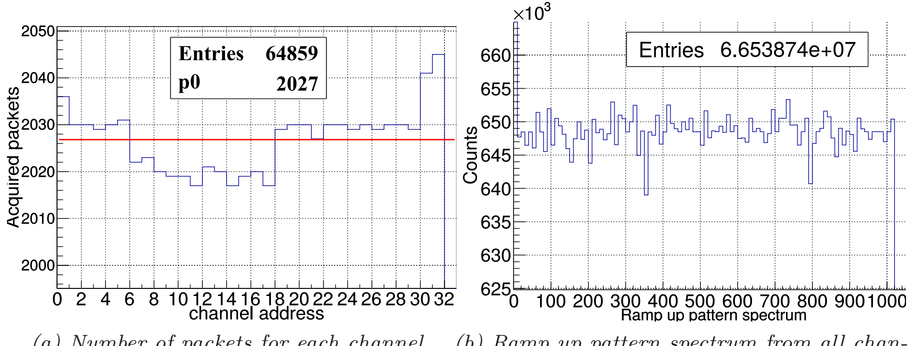
Similar to the pedestal run mode, identical measurements are taken with the DAS mode in local lab. The ADC spectrum plot is presented in Figure E.9 (on page 188) which provides no evidence of strange ADC bins outside the expected Gaussian distribution range.

5.9.4 Test results from pedestal memory run mode

During this mode, a 10-bits data pattern is loaded into the pedestal memories which shuffles through the DSP path, before the data is acquired via serial links. It was an ideal feature during the campaign since one could predict the expected pattern at the serialized outputs. The potential soft error contributors for this scenario are: (i) Pedestal SRAM IPs (1024×10×32), (ii) pipelined FFs (9920), (iii) data SRAM IPs (6144×10×32), and (iv) output serializer modules. Run 5 was initiated by loading a ramp-up pattern into the pedestal memories addresses. The ramp-up pattern was acquired on the serialized outputs with 10 Hz of triggered readout mode (similar to run 6 scenario).

During this run, ~64,859 packets were successfully acquired after accumulating a proton fluence of 8.98×10^{9}p cm^{-2}. The plot in Figure 5.22a demonstrates a uniform packets distribution among all channels, with an average of ~2027 per channel. In Figure 5.22b, the y-axis represents the number of bins, while the x-axis represents the 10-bits ramp-up data stream (0 to 1023) for all 1024 addresses of the pedestal memories. Ideally, one should expect an identical amount of counts/bins for all 1023 data words. However, several discrepancies

[23] 2.1 mV of voltage transient on the nominal baseline level can drift the ADC spectrum with 1 count.



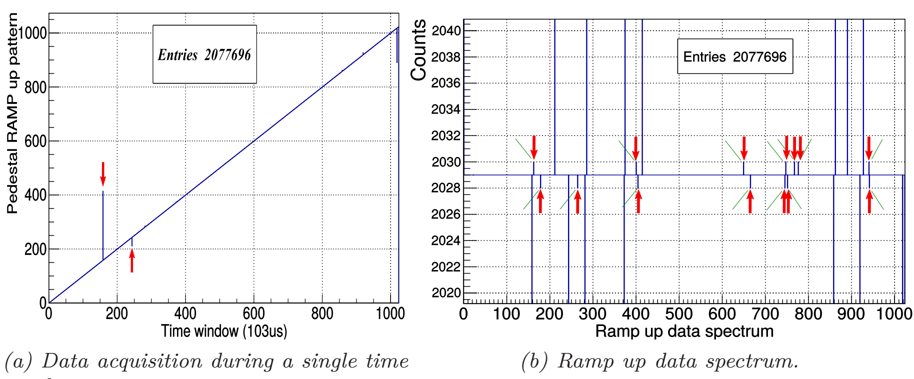
(a) Number of packets for each channel.

(b) Ramp up pattern spectrum from all channels.

Figure 5.22: Samples acquired during run 5.

are detected, which likely occurred as a consequence of soft errors on the acquired data.

This issue is further investigated by visualizing acquired data stream of channel 24 from another perspective, presented in Figure 5.23a. It displays the ramp-up data stream snapshot from the last time window (after final trigger), confirming that the data stream was successfully shuffled through the DSP chain to the serial link outputs. Some spikes are detected on a few 10-bits samples, providing first indication towards soft errors on the acquired payload data.



(a) Data acquisition during a single time window.

(b) Ramp up data spectrum.

Figure 5.23: Acquired samples from channel 24 during run 5.

The spectrum plot from Figure 5.23b can effectively distinguish soft error contribution between the pedestal and the data memories. It demonstrates that each 10-bits sample was averagely acquired 2029 times for channel 24[24]. This

[24] The amount of packets also corresponds to the acquired packets by channel 24 in Figure 5.22a.

spectrum plot also provides both 1→0 and 0→1 bit-flips and bit-wise symmetry statistics.

In Figure 5.23b, several data bins with a single value disparity (from 2029 of mean value) are highlighted with red arrows. These bins are probably associated with bit-flips from data memories as the content of the data memories was refreshed after every read cycle. As the pedestal memories processed the static (unchanged) data content during the entire irradiated time, all bins with more than one value discrepancy are likely due to soft errors contribution from the pedestal memories[25]. The magnitude of the discrepancy depends on the time instant a soft error triggered and corrupted data in the respective pedestal memory address. For instance, if data content corrupted at the beginning of the run, the discrepancy is higher and vice versa.

Decimal value	Binary value	Comment	Acquired bins	Average bins
162	0010100010	Bit-flip on 5th LSB	2030	2029
178	0010110010	in data memory	2028	
211	0011010011	Bit-flip on 6th LSB	4029	2029
243	0011110011	in pedestal memory	29	
281	0100011001	Bit-flip on 3rd LSB	1530	2029
285	0100011101	in pedestal memory	2528	
372	0101110100	Bit-flip on 2nd LSB	13	2029
374	0101110110	in pedestal memory	4045	
400	0110010000	Bit-flip on 3rd LSB	2030	2029
404	0110010100	in data memory	2028	

* All samples for channel 24 which presents discrepancy from mean value are presented in Table E.2 (Section E.11 on page 189).

Table 5.6: Soft error analysis on selected samples of channel 24 during run 5, presenting discrepancy from mean value.

Table 5.6 presents some selected samples of channel 24, which display discrepancies from the mean value of 2029. Interestingly, all samples with lower counts than the mean value have associated samples with an identical magnitude of discrepancy higher than the mean value. For instance, sample "211" and "243" are respectively counted for 4029 and 29 times, indicating a bit-flip on 6th LSB of pedestal memories data content. A bit-flip on 3rd LSB between sample "400" and "404" likely occurred due to soft error within the data memory. Identical bit-flip signatures are also detected on acquired data packets from other channels during run 5. Figure E.10 (on page 190) presents bit-flips on the acquired ramp-up data spectrum for several other channels.

The histogram in Figure 5.24 represents soft error contributions from each channel individually, where soft error contribution from both the pedestal and data memories is determined by performing the spectrum plot analysis. Soft

[25] Data to the pedestal memories was only written at the start of run and never modified afterwards.

error contribution from data memories is also confirmed by comparing the data parity bit received in the header packet with the calculated parity bit of the corresponding data packet.

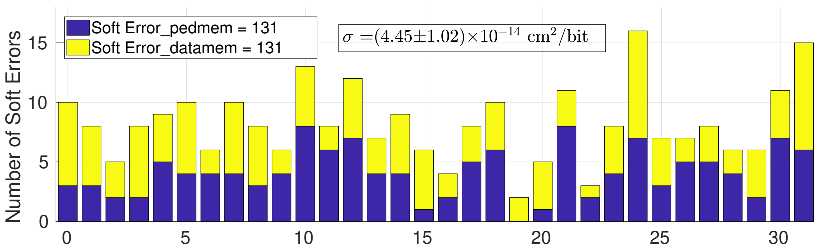


Figure 5.24: Histogram presenting soft error contributions from both data and pedestal memories for each channel during run 5.

Figure 5.24 also presents identical amount of soft errors (131) from both memories, which provides a σ value of $(4.5\pm1.0)\times10^{-14}$ cm^2/bit. This σ value is fairly comparable with previously extracted σ values of the pedestal memories in Table 5.5 (on page 86). Although the above analysis provided identical soft error counts for both memories, it includes some margins of uncertainty:

1. If the bit-flip was occurred within the data content of the pedestal memories during the last readout window, it is counted as the data memories soft error as it exhibits only a single value discrepancy from the mean value.

2. If the bit-flip was induced on identical data samples in both data and pedestal memory, it would be masked out. Nevertheless, the probability of inducing bit-flip on identical bit positions within the same channel is considerably low with protons.

The logical size of the data memory is six times larger than the pedestal memory. Therefore, one may expect higher amount of soft errors from data memories. However, run 5 analysis did not verify this statement. It can potentially be as a consequence of the triggered readout mode where a data stream of 1024 samples was shuffled from the pedestal memories towards the data memories and acquired in the RB modules within a single time window of 103 μs. Therefore, only 1024 addresses of the data memories were sensitive to soft errors in every single time window.

Although the amount of sensitive addresses was identical between the pedestal and data memory, the active data buffering time of the data memory should only be 10% relative to the pedestal memory, as the data stream should only buffer for a time window of 103 μs in the data memory. Consequently, one should only expect 10% of bit-flip errors in the data memory (relative to the pedestal memory bit-flip errors). Run 5 analysis did not provide any such evidence. After a personal communication and discussion with the SAMPA design team, the author acknowledged that there was a design bug in the triggered readout mode of V2 prototype, such that the shuffled DSP data was buffered in the data memory until the reception of the following trigger. Consequently, the effective

data storage time of the data memory was indeed identical to the pedestal memory, resulting in an equivalent amount of soft errors from both memories.

5.9.5 Header and payload parity checks in the header packet

Figure 3.4 (on page 45) presents various fields of the header packet. The header packet embeds parity bits for both the header and payload packet. For every header packet during run 5 and 6, the parity bit was recalculated for the acquired header bits and compared with the corresponding acquired parity bit in the header packet. No disparity was identified between the calculated and acquired parity bit in any header packet. A potential reason that no soft errors in any of the 32×50 bits of the header packets were detected can be related to the accumulated effective proton fluence during these runs. The effective fluence was limited due to both the triggered readout mode error and frequently occurred SEL events in V2 prototype.

For the payload samples from run 5 and 6, the soft errors are also confirmed by comparing the data parity bit in the corresponding header packet with the calculated parity bit of the acquired payload data in the respective packet.

5.10 Summary and Conclusion

During MPW1 campaign, the shift register (SR) test structure was exposed up to a proton fluence of $\sim 1.7\times 10^{11}$p cm^{-2} at the TSL facility. The extracted soft error σ_{FF} value for standard FFs was $7.0\pm 1.2\times 10^{-14}$cm^2/bit. This σ_{FF} value was further applied for predicting the failure rate at the ALICE detectors. The results are presented in Table 8.1 (on page 142) which will be discussed in Section 8.1. Accordingly, registers in the consecutive V2 prototype were classified into various soft error severity levels, and the TMR mitigation technique was employed on all critical registers of the V2 prototype.

During V2 campaign, three PCCA samples were irradiated with 10 hrs of proton beam at the AGORFIRM facility. The V2 prototype included both the SRAM IPs and the TMR protected registers. The soft error sensitivity of the SRAM IPs is evaluated by running the Memory BIST (all SRAM IPs) feature, the slow control register test (only pedestal SRAM IPs) as well as the data packets acquisition from the serial links. No major discrepancy is detected between the extracted σ values of any test. The chip-to-chip variation tests showed no major discrepancy between the extracted σ values of the pedestal SRAM IPs with a mean σ value of $3.5\pm 0.5\times 10^{-14}$cm^2/bit.

The soft error sensitivity of the FFs is evaluated by executing the scan-chain (SC) test and the slow control register test. The SC test showed no significant discrepancy in the mean σ_{FF} value of $5.5\pm 1\times 10^{-14}$cm^2/bit due to chip-to-chip and process variations of the TSMC 130 nm technology. The TMR protected registers were accessible via the slow control interface. Most of the TMR protected registers with static content presented no indication of bit-flips except for the BC2BSL and VPD registers.

During the campaign, three runs were dedicated to evaluate both the readout stability of the serial links and the soft error sensitivity of the serialized data.

During these runs, no radiation-induced fatal errors or transmission halts were discovered, and the acquired packets were evenly distributed among all channels. However, soft errors are detected on the payload part. During the regular operation of the SAMPA chip in the ALICE detector, soft errors are acceptable on the payload part. Most of these soft errors will be filtered out after enabling the zero-suppression feature of the DSP.

The TID qualification is performed by monitoring gradual fluctuations on the baseline levels of the analog front-end blocks. The results confirmed no gradual variations on the baseline levels of the SAMPA channels after accumulating a TID of 30.4 KRad and 34 KRad, for the B_18 and B_11 sample, respectively. The expected accumulated TID is 2.1 kRad for 10 years of SAMPA chip operation period in the ALICE radiation environment [13].

Chapter 6

Exploring Single Event Latch-up effects in SAMPA MPW1 and V2

Single Event Latch-up (SEL) events are a significant concern with high severity level for LHC electronics. It is triggered by a parasitic thyristor structure in the CMOS device (see Figure 2.7a), which establishes a low impedance path between the power rails. If an SEL event is left uncorrected for a more extended period, the high-current path can lead to catastrophic failure due to excessive heating of the active region of the device, metalization, or bond wires. In the worst-case scenario, it may permanently damage the device. This chapter evaluates the SEL tolerance of the MPW1 and V2 prototypes of the SAMPA chip. The SEL results are acquired by conducting high-energy protons, heavy-ions, and pulsed-laser irradiation campaigns at distinct facilities.

6.1 Proton campaigns

As already stated in Chapter 5, MPW1 and V2 prototypes of the SAMPA chip were exposed to high-energy protons at The Svedberg Laboratory (TSL) in Uppsala, and the Center of Advanced Radiation Technology (KVI) in Groningen, respectively. The current monitoring setup of both campaigns is previously presented in Figure 5.3 (on page 66) and 5.12 (on page 76).

The current-time profile from MPW1 campaign is presented in Figure E.11 (Section E.13 on page 191). It does not provide any evidence of real high current (SEL) events. The current jumps during run 4 was resulted from an initial non-nominal operation setting, where the clock frequency parameter was left unoptimized.

6.1.1 SEL in the SAMPA V2 prototype

Following the SEL results from MPW1 campaign, it was predicted that all standard library instances of the TSMC 130 nm technology were technology-robust against SEL effects, at the least for LHC radiation environment. Consequently, no particular design considerations were accounted concerning the SEL effects in the V2 prototype. During the proton campaign, however, V2 prototypes frequently experienced rapid current jumps (SEL events) on one of the five power domains[1].

6.1.2 Current jump events during V2 KVI campaign

Figure 6.1 shows a typical example of a current jump event from run 2 (see Table 5.3 on page 77). The top plot presents overall current consumption of the V2

[1]Different power domains of the V2 prototype are previously presented in Section 3.2.14 on page 49.

prototype, which is directly acquired from the power supply. The bottom plot in Figure 6.1 demonstrates unevenly distributed current consumption between various power domains of the SAMPA chip, where current consumption from the digital core I_{DG} is dominant[2].

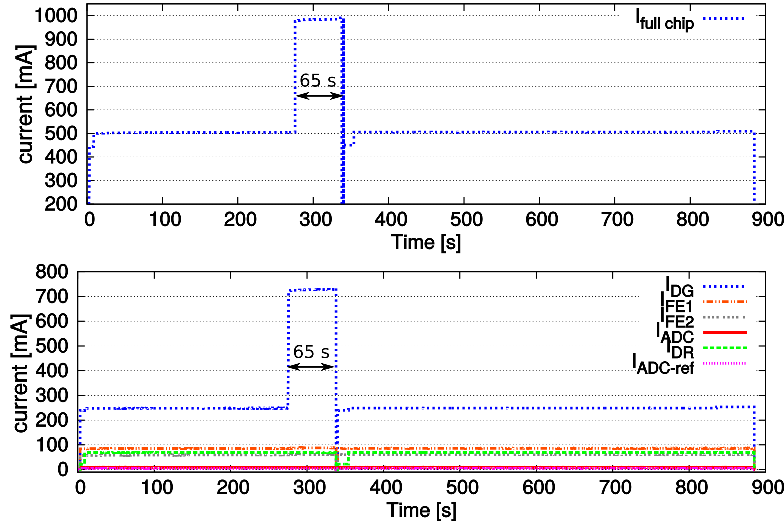


Figure 6.1: Current-time profile of run 2 during V2 proton campaign.

Both plots in Figure 6.1 demonstrate a stable current consumption up to 275 s, follows by a rapid current jump of ∼500 mA of magnitude on the I_{DG} line. Simultaneously, a similar magnitude current jump also occurs on I_{full_chip} in the top waveform. During this event, the current threshold limit was removed to evaluate the magnitude of the current jump event[3]. A remote power cycle was executed after ∼65 s, and the current consumption returned to nominal levels for all power domains. I_{DR} represents the current consumption from the SLVS drivers power domain. A dip on I_{DR} line occurred as a consequence of DUT's power cycling since the number of active serial links changed back to the default value of four. It increased again once the slow control register test script initiated which enabled all eleven serial links of the DUT[4]. After that, the current consumption remained stable until run 2 was terminated.

Similar current jump events (SEL events) were detected on all three irradiated samples during the V2 proton campaign. Figure 6.2 and E.12 (on page 192) presents the current-voltage-time profile for the B_2 and B_11 sample, respec-

[2] The highest current consumption from the digital core is expected as it occupies largest area in the V2 prototype, and is densely populated with the digital circuits.

[3] Leaving the chip in the high current state is generally not recommended as it can damage the DUT. In our case, it was desirable to figure out whether the high current event would arrive automatically back to nominal, and if not, what kind of consequences are expected on the acquired data from the chip?

[4] The details of the slow control register test are previously explained in Section 5.8 on page 81.

tively[5]. For the sake of simplicity, only the delivered supply voltage (VDD_{DG}) and the measured current consumption ($Current_{DG}$) of the SEL sensitive digital power domain is plotted. The nominal supply voltage and current consumption of the digital domain is 1.25 V and 250 mA, respectively. Red arrows in Figure

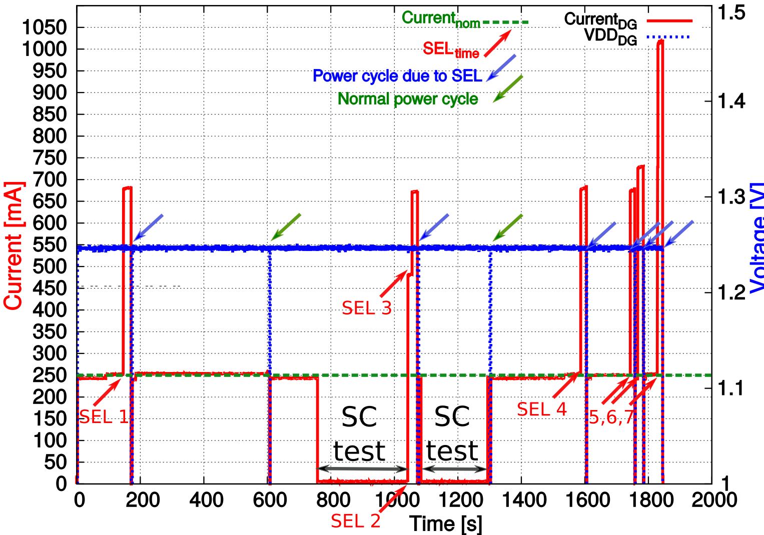


Figure 6.2: Current waveform acquired during the protons exposure of B_2 sample.

6.2 indicate the instant time of current jump events. These events were always followed by power cycling the DUT, indicated by blue arrows. At two additional occasions, a standard power cycle was performed on the DUT, indicated by green arrows. Power cycling always brought back the DUT to the nominal current state, which is a typical signature of a SEL event.

Within a time window of 800-1300 s, the scan chain (SC) test runs resulted in a lower current consumption down to 5 mA. Although most of the digital functionality was disabled during the SC test, the DUT still experienced current jump events. For instance, one can observe a rapid current jump from 5 mA to 470 mA (red arrow #2) at ~1000 s. As the automatic power cycle feature was disabled during this run, another current jump event (red arrow #3) occurred after a couple of seconds. Consequently, the current level magnitude was further increased to 675 mA. A relatively higher number of SEL events occurred toward the end of current waveform plots as the consequence of higher protons flux runs for collecting sufficient statistics of SEL events[6].

6.1.3 Brief high-current transient event analysis

During run 7 (see Table 5.3), the raw ADC data was acquired via serial links in DAS mode. In this mode, more than 80% logic in the digital domain was disabled

[5]The plotted time presents only the active time when current/voltage data is acquired from the samples, and not the actual beam time.
[6]Beam log for the V2 campaign is presented in Table 5.3 (on page 77).

by employing the clock-gating scheme. The digital power domain encountered a high-current event as presented in Figure 6.3. This event was left uncorrected and the data packets were successfully acquired from the serial links for a total irradiated time of 798 s.

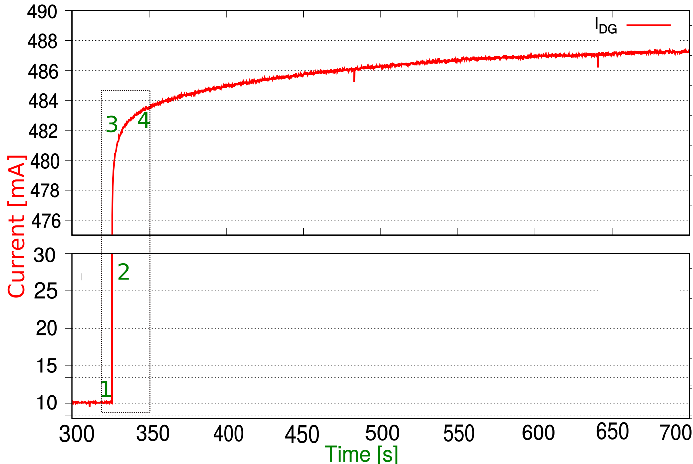


Figure 6.3: Rise time shape of the high current transient event during run 7.

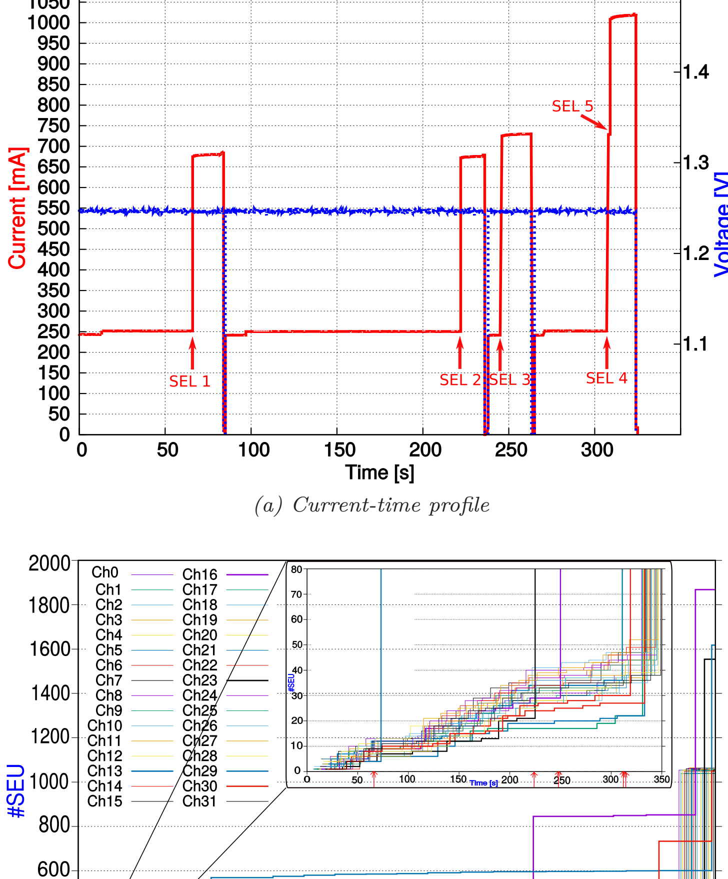
The current waveform in Figure 6.3 offers a closer inspection for the rise time shape of the acquired current transient. It is comparable to the transient latch-up current modeled by simulating a 0.18μm CMOS inverter in reference [125]. It eventually confirms that the encountered high-current events of the V2 prototype are caused by the latch-up triggering in the CMOS npnp thyristor (see Figure 2.7a on page 23). According to reference [125], the SEL current involves four transient steps in a typical npnp thyristor, highlighted in Figure 6.3:

1. The transient current increases the voltage, which triggers the vertical pnp transistor, and the pnp transistor starts operating in the linear region.
2. This further triggers the lateral npn transistor, which also starts drifting in the linear region.
3. The lateral npn transistor turns into the saturation region.
4. The vertical pnp transistor also turns into the saturation region, and the total current gradually increases towards the maximum current level.

6.1.4 SEL events correlation with bursts of soft errors from Pedestal SRAM IPs

During the V2 proton campaign, the highest amount of SEL events were detected during the slow control register tests[7]. Among several other features, the pedestal

[7] It is worth reminding that the slow control register test was conducted frequently, as presented in Table 5.3 (on page 77).



(a) Current-time profile

(b) Bursts of soft errors on individual channels

Figure 6.4: Correlation between SEL and burst of soft errors in the pedestal memories during run 16.

memories were directly accessed for performing both write and read operations on all addresses of the individual channels.

During run 16 (see Table 5.3), the test script was initiated that accumulated soft errors from the pedestal memories. Figure 6.4a presents the current-time profile of run 16, together with the accumulated soft errors of every channel in Figure 6.4b. The subplot in Figure 6.4b represents the zoomed y-axis, which proves a linear dependence between the accumulated soft errors from all channels

and the irradiated time at the beginning of the run. At ~65 s, 1st SEL event was triggered as presented in Figure 6.4a. Before that, only four single bit-flips were accumulated at distinct addresses in the pedestal memory of channel 29. During the subsequent read cycle (after 1st SEL event), a burst of both single and multiple bit-flips were counted on more than half of the pedestal memory addresses for this respective channel.

Another SEL event was triggered at 220 s, correspondingly showing burst of soft errors from the pedestal memory of channel 23. In total, 5 SEL events occurred at different times during this run, marked by red arrows in Figure 6.4b. As a consequence, either the data-content of the pedestal memories was corrupted for five random channels, or the read interface of the respective pedestal memories was disrupted. Similar signatures were also detected on other irradiated V2 samples during the slow control register tests.

6.1.5 Proton SEL cross-section of the V2 prototype

All irradiated V2 samples experienced frequent SEL events during the proton campaign. The distribution of current jump magnitudes relative to the nominal current level is presented in Figure 6.5. It concludes that most of the SEL events have an amplitude within the range of 400-500 mA.

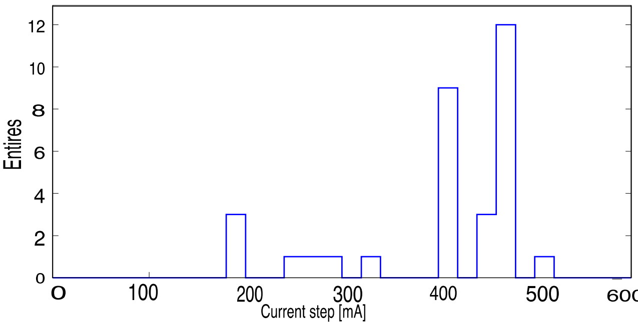


Figure 6.5: Distribution of current jump events during V2 proton campaign.

The effective proton fluence, number of SEL events, and the extracted σ_{SEL} values of all irradiated samples are summarized in Table 6.1. It demonstrates that the measured σ_{SEL} values are fairly comparable among all irradiated samples.

Device	**Fluence [p/cm^2]**	**# of SEL**	σ_{SEL}**[cm^2/device]**
B_18	3.8×10^{11}	16	$(4.2\pm1.2)\times10^{-11}$
B_11	3.7×10^{11}	12	$(3.3\pm1.1)\times10^{-11}$
B_2	1.6×10^{11}	7	$(4.5\pm1.8)\times10^{-11}$

Table 6.1: SEL σ values of all irradiated V2 samples during proton campaign.

6.2 SEL cross-section curve with heavy-ions

In May 2017, another irradiation campaign was conducted on the V2 prototypes at the Universitè Catholique de Louvain (UCL) Heavy-Ion irradiation Facility (HIF) in Belgium [126, 127]. The facility uses a CYCLONE accelerator which is a multi-particle, variable energy cyclotron, capable of delivering both protons (up to 85 MeV), alpha particles and the heavy-ions. Reference [126] provides additional information about the relevant ion species at the HIF. The two main objectives of this campaign were:

I. To fully characterize the SEL sensitivity of the V2 prototypes by determining the energy and ions dependency of the SEL events. Since heavy-ions interact with silicon through direct ionization, a significantly higher amount of SEL events can be collected, compared to a proton or neutron campaign.

II. To localize the source of SEL events in the V2 prototypes.

6.2.1 Test setup at the heavy-ions facility

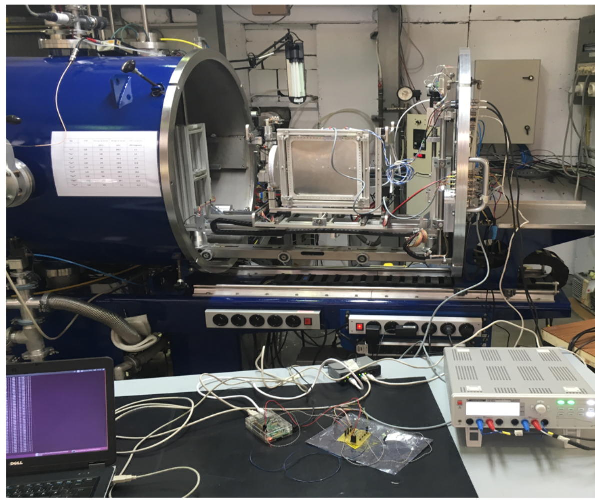
During a HIF campaign, the DUT is typically exposed within a vacuum chamber for preventing energy loss or absorption of charged particles in air. The physical dimensions of the NCCA_V1 carrier board were identical to the PCCA carrier boards (used during proton campaign). However, a dedicated PCB frame and several cables were prepared for supporting feed-through connectors available at the HIF facility[8]. For proper configuration of the DUT, the HSMC connection was required between the carrier board and the DAQ board. Since the HSMC connector feed-through was not available at the HIF, both devices were mechanically mounted on a 24.2×24.2 cm^2 board frame inside the chamber, as presented in Figure 6.6.

Figure 6.7 illustrates an overview of the V2 HI campaign test setup. Most of the setup is identical to the previously conducted proton campaigns. However, the power supply was delivered to both the DUT and the DAQ board via a BNC connector interface, and the current was also monitored from various power domains of the DUT via identical interface. The USB and Ethernet transition connectors were utilized to communicate with the DAQ board. Compared to the proton campaigns, the HI campaign provided quicker access to the DUT during the exposure. The current monitoring system and the power supply were placed outside the radiation zone, which reduced any radiation-induced malfunction risk on the current monitoring system.

Compared to PCCA boards[9], the NCCA _V1 board offered only three current monitoring test points, each placed at the output of the voltage regulator. One voltage regulator provided power supply to the analog (FE1, FE2, and AD) power domains, another to the digital (DG and DR) power domains. The last

[8]The list of cables and connectors developed for the heavy-ions campaign is presented in Appendix F (on page 195).

[9]The PCCA boards offered six current monitoring test points for every power domain individually.



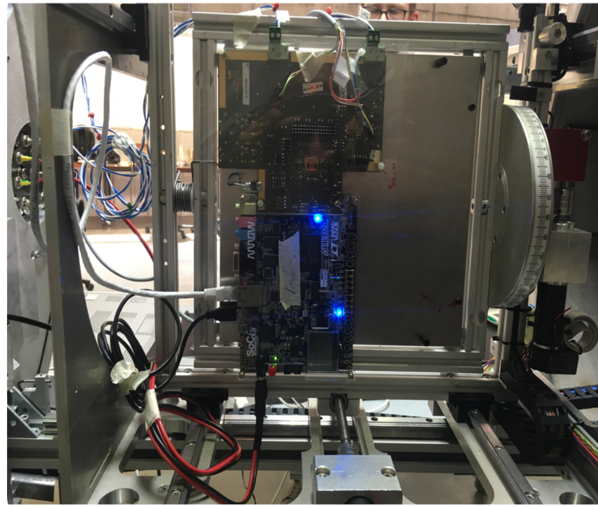


Figure 6.6: SAMPA V2 campaign setup at the HIF facility.

regulator provided reference voltage to the internal ADCs of the V2 prototype. If no proton campaign was performed on the V2 prototypes beforehand, it would be difficult to distinguish whether the source of SEL events is related to the DG or DR power domain of the SAMPA chip during the HI campaign.

6.2.2 SEL test procedure

During an HI campaign, it is normal to acquire the cross-section points at various LET values to be able to extract a σ_{SEE} curve. The σ_{SEE} curve is frequently used to determine the sensitive volume of a DUT with respect to a SEE failure. For the V2 prototype, a test plan was developed with a typical SEL test flow, presented in Figure 6.8. Since the maximum expected LET generated by the

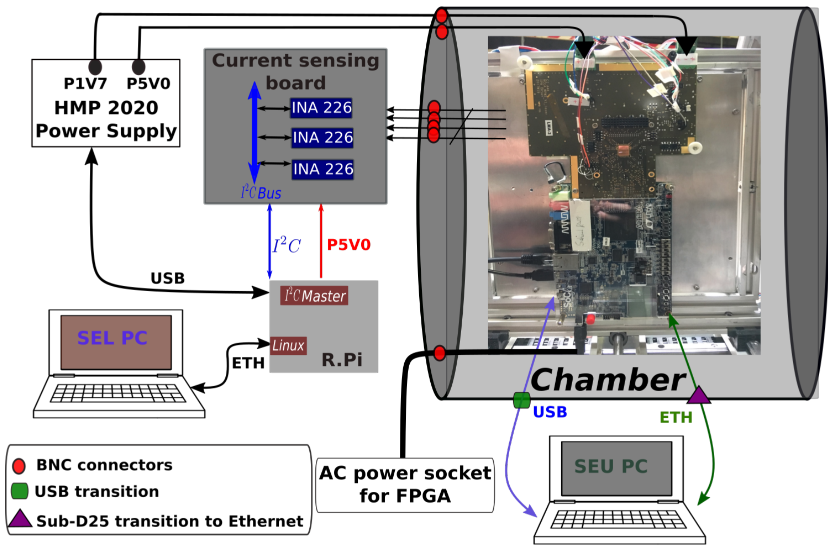


Figure 6.7: Block diagram overview of the SAMPA test setup during HI campaign.

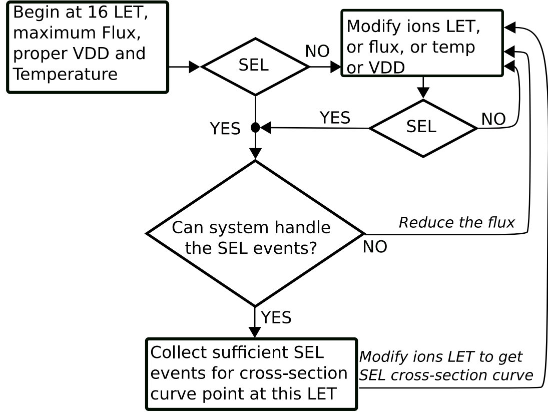


Figure 6.8: Test flow for SAMPA SEL tests during HI campaign.

nuclear interactions of hadrons with silicon is less than 16 MeV cm^{2}mg^{-1}, the campaign was initiated by exposing with ion of LET value of 16 MeVcm^{2}mg^{-1} at the maximum ion flux. The V2 σ_{SEL} curve was primarily acquired at room temperature with nominal supply voltage of 1.25 V.

6.2.3 V2 SEL cross-section results

The V2 prototype was exposed to various ion beams with a broad range of Linear Energy Transfer (LET) from 3.3 to 32.4 MeVcm^{2}mg^{-1} presented in Table 6.2. In order to accumulate a reasonable amount of SEL events that could easily be handled by the current monitoring system, the flux was varied between

5×10^1-1.5×10^4 ions cm^{-2} s^{-1}, depending on the LET values of the ions.

ION	LET[MeV cm^2/mg]	Energy [MeV]	Range [μm Si]	Flux [i cm^{-2} s^{-1}]	Eff.Fluence [i cm^{-2}]	SEL events	σ [cm^2]
^{34}Kr	32.4	769	94.2	5.3×10^1	4.8×10^4	247	$(5.2\pm0.6)\times10^{-3}$
^{53}Cr	16.0	513	107.6	1.4×10^2	1.1×10^5	335	$(3.2\pm0.3)\times10^{-3}$
^{40}Ar	10.0	379	120.5	5.1×10^1	8.1×10^4	145	$(1.8\pm0.3)\times10^{-3}$
^{27}Al	5.7	350	131.2	1.55×10^4	3.7×10^7	29	$(7.8\pm2.5)\times10^{-7}$
^{22}Ne	3.3	238	202	1.53×10^4	3.3×10^7	23	$(7.0\pm2.5)\times10^{-7}$

Table 6.2: SEL results of the V2 prototype acquired from HI campaign.

The number of SEL events were counted for each LET value and the effective fluence was calculated by subtracting the dead-time between all SEL events[10]. The σ_{SEL} values are further extracted by dividing accumulated SEL events with the effective fluence of the respective ions. The standard deviation is associated with a confidence interval of 95% from the Poisson distribution.

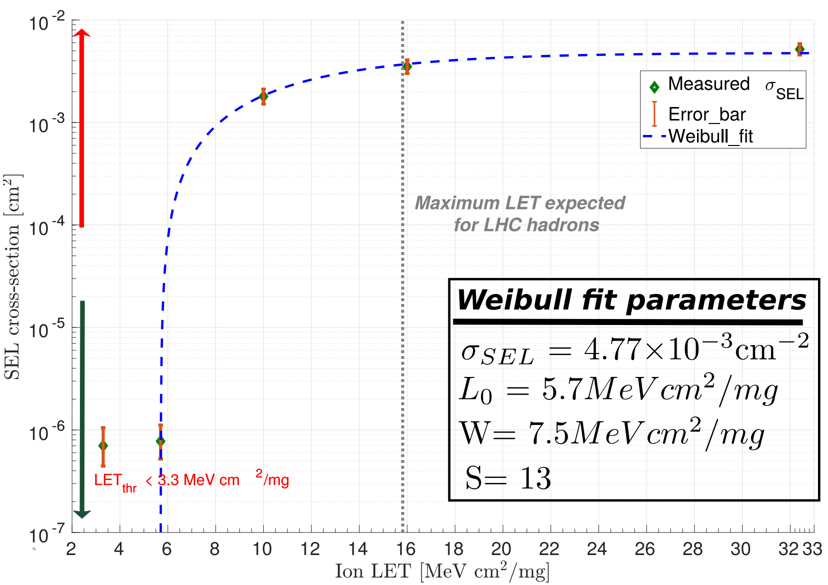


Figure 6.9: SAMPA V2 SEL cross-section as a function of LET spectrum.

In order to derive σ_{SEL} curve, the extracted σ_{SEL} values are logarithmically plotted as a function of the LET spectrum in Figure 6.9. Following the JEDEC standard [128], the extracted σ_{SEL} points are further fitted by a smooth curve. The curve is derived from the four-parameter Weibull function [129], presented

[10] The dead-time is the period from a SEL event triggers in the DUT until the DUT arrives back to nominal operation after power cycling. Since the DUT is not operational during this period, all such intervals should be discarded from the total exposed time.

in Equation B.2 (on page 155). The fit parameters are provided in Figure 6.9. The plot demonstrates that the extracted σ_{SEL} points fits very well with the Weibull curve, and the σ_{SEL} points lie precisely on the curve between the LET range of 5.7–32.4 MeV cm^{2}mg^{-1}. The σ_{SEL} curve saturates at 4.77×10^{-3}cm^2 in between the LET range of 16–32.4 MeV cm^{2}mg^{-1}. This saturated region represents the entire SEL sensitive region within the V2 prototype. At an LET value of 10 MeV cm^{2}mg^{-1}, the σ_{SEL} is reduced by 37%, which rapidly falls off with several orders of magnitude between 5.7–10 MeV cm^{2}mg^{-1}.

The extracted σ_{SEL} point at an LET value of 3.3 MeV cm^{2}mg^{-1} shows a tail that does not correspond to the expected Weibull fall-off curve. Reference [130] has previously reported similar σ tails, where several commercial ICs were exposed to the heavy-ions beams. The plausible justification for this σ_{SEL} point is that these SEL events are likely triggered with a different interaction mechanism at lower LET values in the V2 prototypes. For instance, during ions exposure with LET values of 5.7 MeV cm^{2}mg^{-1} and above, SEL events were dominated by direct interaction mechanism. At lower LET values, the nuclear (indirect) interaction mechanism dominated and caused the SEL events. This behavior is also referred to as the sub–LET threshold region in reference [131].

6.2.4 Impact of supply voltage on the SEL sensitivity

The reduction of supply voltage (V_{DD}) can significantly enhance the latch-up tolerance of a CMOS device[48][11]. It was desirable to identify V_{DD} threshold, where the V2 prototype was completely robust against severe latch-up events. During the ions exposure with LET values of 5.7, 10, and 32 MeV cm^{2}mg^{-1}, V_{DD} of the DUT was reduced stepwise and the σ_{SEL} values were accordingly extracted.

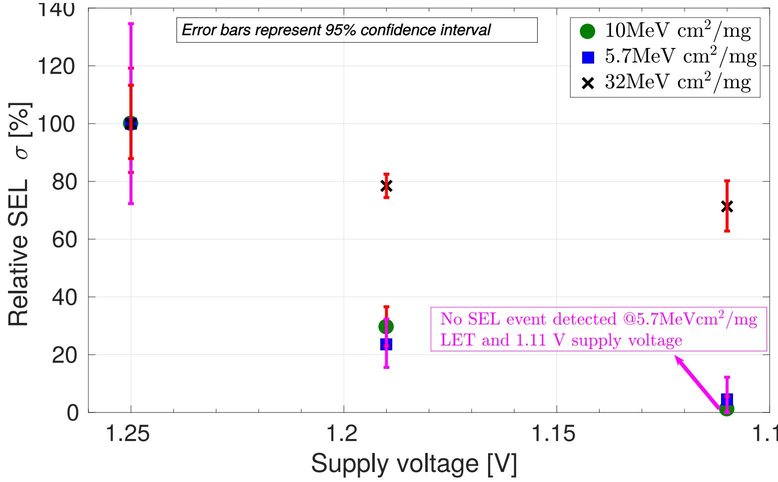


Figure 6.10: Impact of supply voltage on SEL sensitivity at various LET values.

[11] As previously stated in Section 2.4.3 (on page 23). $V_{DD} < V_h$ ensures that the maximum power supply on the chip is below the voltage required to sustain latchup.

Figure 6.10 plots the relative σ_{SEL} values for the supply voltage of 1.25 V, 1.19 V, and 1.11 V. For all LET values, the σ_{SEL} values decrease with the reduction of supply voltage, and the relative decrease is higher for the lower LET values. At the V_{DD} of 1.11 V and for an LET value of 32 MeV cm^2mg^{-1}, the σ_{SEL} value is reduced by 29% when compared to a V_{DD} of 1.25 V. For an LET of 10 MeV cm^2mg^{-1}, the σ_{SEL} is reduced by ~99%. For the lowest LET of 5.7 MeV cm^2mg^{-1}, no SEL event was detected at the lowest supply voltage.

6.2.5 SEL σ comparison between heavy-ions and protons

According to reference [132], Equation 6.1 can provide proton σ_{SEE} value estimation from the σ_{SEE} data points of a HI campaign.

$$A_b = L_{0.1} + 15 \tag{6.1}$$

A_b is the *Bendel A* parameter and $L_{0.1}$ is the LET value at which the cross-section is 10% of its limiting (saturating) level. Reference [132] provides more comprehensive details about the Bendel A parameter and explains the fundamentals behind expression in Equation 6.1. This method has been attempted to confirm the extracted σ_{SEL} results from both the proton and HI campaigns of the V2 prototype.

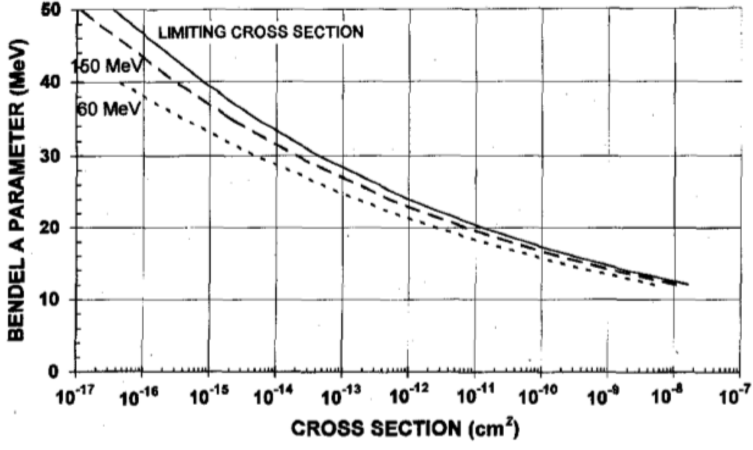


Figure 6.11: Relation between A_b parameters and the cross-section (cm^2) with protons. ©1996 IEEE. Reprinted, with permission, from [132].

$L_{0.1}$ value of ~5.7 MeV cm^2mg^{-1} is identified from the σ_{SEL} curve of Figure 6.9, which is further employed in Equation 6.1 to extract A_b value of 20.7 MeV. The relation between A_b parameters and σ_{SEE} values at various proton energies is presented in Figure 6.11. This demonstrates that A_b value of 20.7 MeV corresponds to the proton σ value of $\sim10^{-11}cm^2$. This assumption corresponds fairly well with the mean σ_{SEL} value of $4.0\pm1.4\times10^{-11}cm^2$ (presented in Table 6.1) for the V2 prototype during 185 MeV protons exposure.

6.3 Experimental methods to localize the origin of SEL events in V2 prototype

Commercial SRAM IPs were implemented in the V2 prototypes[12]. The consistency of SEL events with the burst of soft errors in the SRAM IPs provided initial indication towards the potential source of SEL events in the V2 prototypes. Further campaigns were conducted to confirm and localize the origin of SEL events in the V2 prototypes.

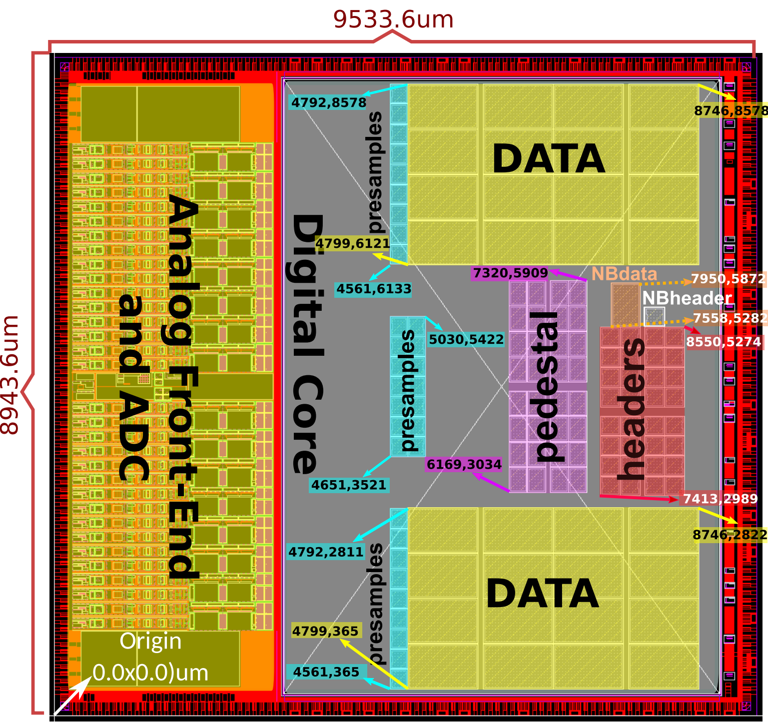


Figure 6.12: The placement of SRAM IPs within the V2 prototype layout. All units are given in µm.

The design file (gds file) of the V2 prototype was inspected using the KLayout tool [133], to identify physical coordinates of the SRAM IPs within the digital core. Figure 6.12 shows the layout of the V2 prototype where the analog front-end and the ADCs of all 32 channels reside on the left side (highlighted with yellow color), and a single digital core is placed on the right side (highlighted by gray color). Inside the digital core, the physical regions of various SRAM IPs are highlighted with different colors[13]. The bottom left corner reflects the origin of the chip, and the physical coordinates with several islands of the SRAM regions

[12] More details about the SRAM IPs are presented previously in Section 3.2.6 on page 44.

are identified and measured.

Table 6.3 summarizes the logical array size, the physical footprint size as well as the total mapped area of the SRAM IPs in the V2 prototype. The right-most column represents the total area occupied by the SRAM IPs. It indicates that more than 50% of the total digital core area is populated with the SRAM IPs. Both the single-port (SP) and dual-port (DP) based SRAM IPs were embedded in the digital core, where the SP SRAM IPs were only utilized for the pedestal memories. Since both SRAM IPs were generated by distinct memory compilers from ARM [90][14], different physical layout rules could be expected between these SRAM IPs, each providing different susceptibility to SEL events. Therefore, the SRAM IPs regions are further categorized into the DP and SP regions.

SRAM IP	**SRAM type**	**Array size(bit)**	**Footprint (μm)^2**	**Mapped Region(m^2)**	**Area(%)**
Data	Dual-port	32×(6144×10)	945×609	1.94×10^{-5}	38.5
Pedestal	Single-port	32×(1024×10)	246×339	3.05×10^{-6}	6.05
Header	Dual-port	32×(256×10)	266×266	2.56×10^{-6}	5.15
Presample	Dual-port	32×(192×10)	231×266	2.02×10^{-6}	4.01
Data^*_{NB}	Dual-port	1×(2048×10)	591×392	2.31×10^{-7}	0.46
Header^*_{NB}	Dual-port	1×(256×10)	266×266	7.08×10^{-8}	0.14
Total	Single-port	3.28×10^{5}		3.05×10^{-6}	6.05
Total	Dual-port	2.13×10^{6}		2.43×10^{-5}	48.2
Total		2.46×10^{6}		2.74×10^{-5}	54.3

* NB: Neighbour for daisy chaining.

Table 6.3: Details of SRAM IPs in V2 prototype.

6.4 Heavy-ions tests with collimators

Figure 6.13 shows two aluminum collimators, which were designed and produced in-house for the HI campaign. The DP collimator offered two identical rectangular openings of ∼4192μm×1900μm for irradiating ∼65% of the DP IP regions. The SP collimator had a single opening of ∼1000μm×2181μm to irradiate ∼68% of the SP IP regions. At the UCL facility, Carbon ions ($^{13}C^{4+}$) with an energy of 131 MeV and an LET of 1.3 MeV cm^{2}mg^{-1} offered the most extended penetration depth in silicon. Simulations with SRIM software [135] showed that the projected range of $^{13}C^{4+}$ is 236 μm in aluminum. Hence, the aluminum collimators were designed with 2 mm of thickness, including a safety factor of ∼10. The drawings of the collimators and their openings can be found in Appendix F (on page 195).

[13] The physical visualization indicates that all SRAM IPs (Data, pedestal, header, Neighbor) are isolated from each other with reasonable distance.

[14] Memory compilers automatically generate the physical layout and behavioral level models, which provides silicon verification. It only allows the designers to verify front-end simulations of the memory. Back-end features such as layout are directly delivered to the fab [134].

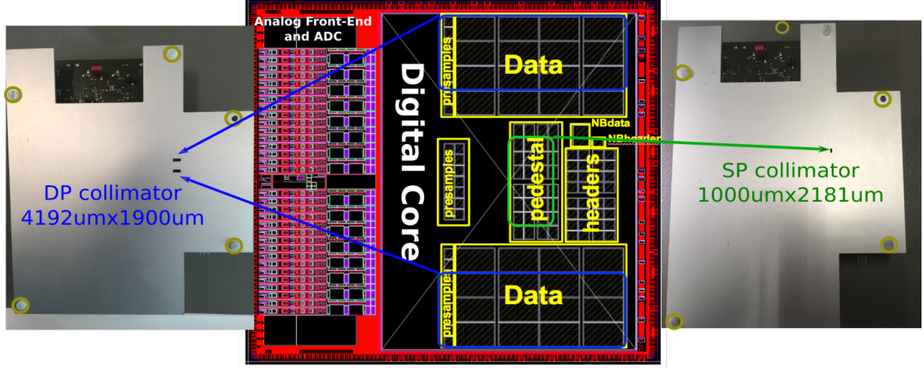
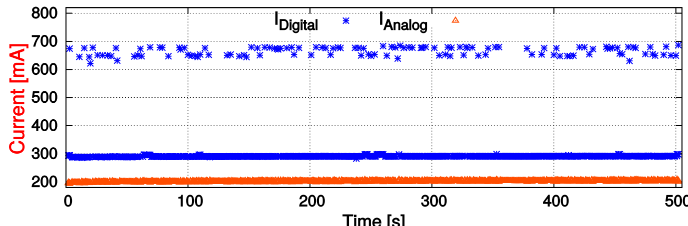


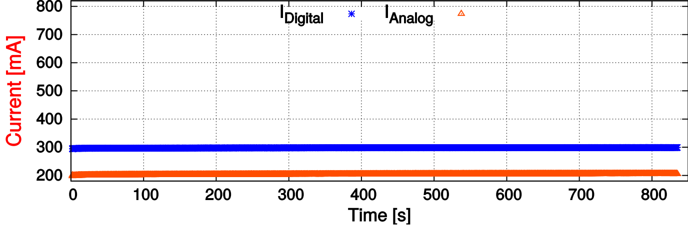
Figure 6.13: Accessible SRAM IP regions with the collimators during the HI campaign.

6.4.1 Collimator test setup and results

During the campaign, the collimators were mounted directly on top of the carrier boards, where a smaller region was left open for easier access to the DUT's current monitoring test points. Figure F.1 (see Appendix F on page 199) shows a picture from the campaign where the DP collimator is mounted on top of the DUT and fastened by the PCB holding frame within the vacuum chamber. Besides that, the test setup was identical to the previously presented HI campaign setup in Figure 6.6 and 6.7.



(a) SP collimator with accumulated fluence of 2.22×10^5 ions/cm^2.



(b) DP collimator with accumulated fluence of 1.25×10^7 ions/cm^2.

Figure 6.14: Impact of collimators on SEL events during the exposure of $^{40}Ar^{12+}$ ion with LET value of 10 MeV cm^{2}mg^{-1}.

The V2 prototype was exposed to ions with various LET values, and

both collimators evaluated the SEL sensitivity of the DUT. Figure 6.14 represents the current-time profile during $^{40}Ar^{12+}$ ion exposure with LET value of 10 MeV cm^2mg^{-1}. The plot in Figure 6.14a demonstrates that a significant amount of SEL events were detected in the V2 prototype during ion exposure with the SP collimator. By using the DP collimator, the current waveform in Figure 6.14b demonstrates stable current levels for all power domains. The accumulated fluence during the DP collimator run was 1.25×10^7ions cm^{-2}, which was almost two orders of magnitude higher than the run with the SP collimator. It concludes that the SP SRAM IPs are the potential source of SEL events in the V2 prototypes.

6.4.2 Confirming results with DP collimator

The current waveform plot from Figure 6.14b demonstrates no signs of SEL events with the DP collimator run at an LET value of 10 MeV cm^2mg^{-1}. To entirely ensure the robustness of DP SRAM IPs against SEL events, the DUT with DP collimator was exposed with ions of different LET values. The results are summarized in Table 6.4.

LET[MeV cm^2mg^{-1}]	Flux [i $cm^{-2}s$]	Fluence [i cm^{-2}]	SEL events	σ [cm^2]
5.7	1.5×10^4	1.4×10^7	0	$< 2.7\times10^{-7}$
16	5.2×10^3	5.4×10^6	0	$< 7.1\times10^{-7}$
10	1.5×10^4	7.5×10^6	1	$1.3(+7.5,-0.03)\times10^{-7}$
10	1.5×10^4	2.1×10^7	0	$< 1.8\times10^{-7}$

Table 6.4: Exposure of DUT with DP collimator at various LET values.

In the beginning, no SEL events were detected during the ion exposure with LET values of 16 and 5.7 MeV cm^2mg^{-1}. However, during the ion exposure with LET value of 10 MeV cm^2mg^{-1}, one SEL event encountered after accumulating a fluence of 7.48×10^6 i cm^{-2}. Subsequently, another run was conducted with the identical ion to acquire sufficient statistics. After reaching a fluence of 2.06×10^7 i cm^{-2}, no additional SEL events were detected.

Since the accumulated SEL events with the DP collimator runs were significantly lower than the runs without collimator as well as with the SP collimator, it raised concerns about the appropriate alignment of the DP collimator on the targeted DP SRAM IP regions. In worst case, the openings of the DP collimator could be completely unaligned, and the ions did not strike any of the SRAM IP regions within the digital core at all. The alignment of DP collimator was confirmed by executing the Memory BIST[15] test during the ion exposure with LET value of 10 MeV cm^2mg^{-1} as well as the maximum flux of 1.5×10^4 i cm^{-2} s^{-1}. This run successfully accumulated soft errors, confirming the alignment of the DP collimator with the SRAM IP regions. The results are presented in Figure F.3 (in Appendix F on page 201).

[15]Memory BIST feature is previously described in Section 5.6 on page 78.

6.4.3 Evaluating the efficiency of collimators

The results with collimator runs from Figure 6.14 strongly indicates that the SP SRAM IPs are the primary source for triggering SEL events in the V2 prototypes. If we believe that the entire SEL sensitive region lies only within the SP SRAM IPs regions, the corresponding σ_{SEL} value should be $\sim$1.8±0.3×10^{-3}cm^2 (from Table 6.2) with ion exposure of 10 MeV cm^{2}mg^{-1} LET value. The SP collimator was initially designed to expose about 65% of the SP SRAM IP regions. However during the SP collimator run, the extracted σ_{SEL} value[16] is (5.6±0.9)×10^{-4}, which is only (32±10)% relative to the σ_{SEL} value of the entire chip. It indicates that the designed collimators were not entirely aligned at the target regions.

Configuration	Eff.Fluence [i cm^{-2}]	SEL events	σ [cm^2]	Factor (%)
No collimator	8.1×10^4	145	(1.8±0.3)×10^{-3}	100
SP collimator	2.2×10^5	124	(5.6±0.9)×10^{-4}	32 ±10
DP collimator	1.3×10^7	0	$< 2.9\times10^{-7}$	< 0.02

Table 6.5: Evaluating impact of collimators on σ_{SEL} at LET of 10 MeV cm^{2}mg^{-1}.

Alignment offset between the collimators and the carrier boards was somehow expected due to significant narrower openings. For instance with SP collimator usage, only 1 mm offset in the horizontal direction could lead to complete "miss" of the target (SP SRAM IP) regions within the V2 prototype. The usage of collimators also offered several factors of uncertainties, such as their mechanical construction, their mounting mechanism on the carrier boards as well as minor DUT offsets between various carrier boards.

A single SEL event detected with the DP collimator run can occur due to: (i) Extremely low SEL sensitivity of the DP SRAM IPs, or (ii) misalignment of the collimator opening regions, or (iii) scattering of ions due to strike on the collimators corners, which further diverged ions angle towards the SEL sensitive regions within the SP SRAM IPs.

6.5 Pulsed-laser backside irradiation

One SEL event detection during the DP collimator run as well as the misalignment risk of the collimators led to conduct a pulsed-laser (PL) campaign at the IES (Institute of Electronics and Systems) in Montpellier. The PL SEE campaign is previously described in Section 2.9.3 (on page 34), which often uses as a diagnostic tool for identifying SEE sensitive regions with the resolution of μm.

The previous results indicated that only 18% of the total SP SRAM region was sensitive to SEL events[17]. The main objectives of the PL campaign were to gain in-depth knowledge about the SEL sensitive regions within the SP SRAM

[16] σ_{SEL} value is taken from Table 6.5 at 10 MeV cm^{2}mg^{-1} LET value.

[17] $\frac{\sigma_{SEL_sat}}{SP_area} = \frac{4.77\times10^{-7}\ m^2}{2.67\times10^{-6}\ m^2} = 18\%$

region as well as confirming that the DP SRAM IPs were insensitive to SEL effects.

6.5.1 Sample preparation

Due to several metal layers shadowing on the top side of the DUT, dedicated carrier boards were developed with a rear opening to allow a convenient laser source penetration into the substrate of SEL sensitive region within V2 prototype. Figure 6.15 presents the carrier board of the PL campaign.

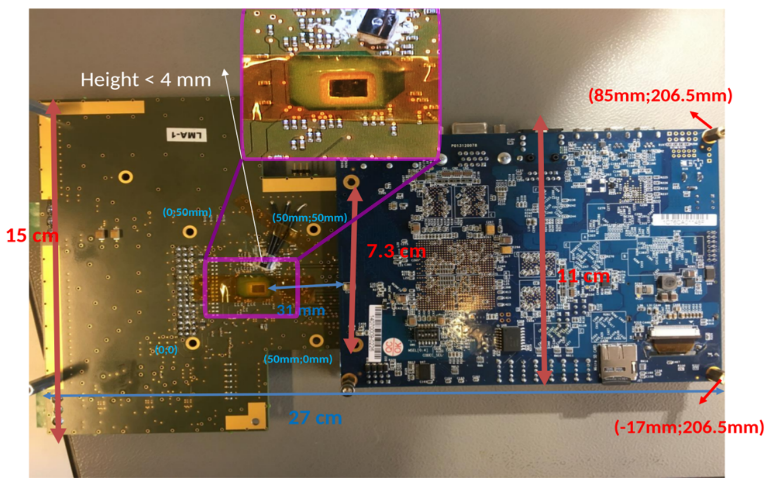


Figure 6.15: Dedicated V2 carrier board (with DAQ board) for PL campaign.

In order to allow precise focusing of the lens onto the DUT, no jumpers or header pins over a height of 9.5 mm could be placed closer to the DUT within an "exclusion zone" of 37 mm^2. Additional screw holes were drilled around this zone to directly mount the carrier boards on the sample holder at the facility. The backside surface quality of the V2 samples was evaluated via an microscopic inspection, prior to the PL campaign. The pictures are presented in Figure G.1 (on page 216). More details about the sample preparation and the mechanical requirements of the PL campaign can be found in Appendix G.1 (on page 207).

6.5.2 SAMPA setup during the pulsed-laser campaign

The PL campaign was performed with the PULSYS-RAD system from PULSCAN [136]. Figure G.2 (on page 216) presents an overview of the PULSYS-RAD system which mainly consists of the following subsystems:

1. PULSYS Main Frame:
   It consists of an infrared camera to visualize the internal structures of the DUT, a PC display for monitoring these internal structures by the camera, a laser with magnification levels of ×5, ×20 and ×100, and a sample holder for the DUT. Laser pulses were deposited to the DUT in this frame.

2. PULSBOX-PICO:
   PULSBOX-PICO is a smart laser source, which is optimized for single-photon absorption in silicon [75]. It offers complete laser pulse control for the SEE characterization of the semiconductor devices. It controls the laser energy, the pulse frequency as well as provides the user communication interfaces. It delivers ultra-short pulsed laser with a duration of 30 ps and a wavelength of 1064 nm[18]. Other relevant parameters, such as the repetition rate (up to 20 MHz) and the energy (up to 50 nJ), are adjustable, depending upon the system performance of the user interface.

3. Multi-Channel Oscilloscope:
   The facility provides a 4 GHz bandwidth multi-channel oscilloscope from the Agilent technologies [137]. It acts as a primary interface between the user system and the facility system to superimpose SEE sensitive map of the DUT after the campaign.

4. GUI-based PULSCAN software:
   PULSCAN software controls various parameters for performing both the manual and automatized laser scan tests on the DUT. This software can also visualize internal structures of the DUT.

5. Laser control:
   This controls various parameters of the laser source. It can also be utilized for manual injection and movement of laser pulses at different locations within the DUT.

Figure 6.16: SAMPA test setup connected to the PULSYS-RAD system during the pulsed-laser campaign.

[18]Laser wavelength of 1064 nm can penetrate ∼600 μm of distance in silicon (see Figure B.2 on page 157).

Figure 6.16 shows test setup pictures of the V2 prototype during the PL campaign, where the SAMPA test setup is connected to the PULSYS-RAD system at the IES facility. The system overview of the SAMPA test setup was almost identical with the previous performed HI irradiation campaign on the V2 prototype, presented in Figure 6.7. No unique connector interfaces were required to communicate with the DUT during this campaign. The current sensing board was replaced with SELTC board, developed by Jonas Birkeland Carlsen during his master project [108].

6.5.3 Accessible SAMPA regions during the PL campaign

Figure 6.17 presents the chip orientation, as seen by the IR camera[19]. The IR camera determined a substrate thickness of 175 μm for the DUT. This thickness was expected as the V2 samples were thinned down at the wafer level for BGA packaging purpose. The physical locations of both SP and DP SRAM IPs

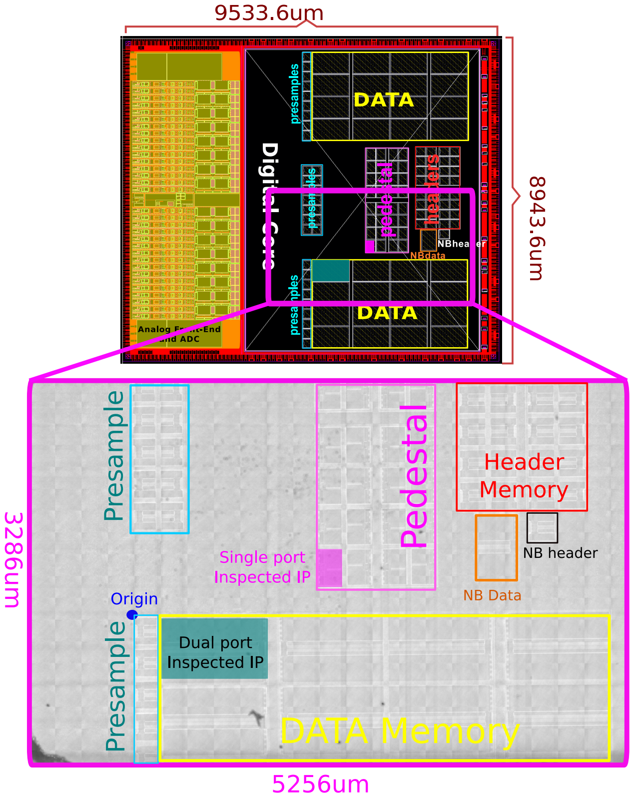


Figure 6.17: IR camera visualization through the silicon substrate, showing accessible regions of the V2 prototype.

[19]From above, while standing in front of the microscope. The quality of the image mainly depends upon the backside surface quality and the substrate doping level of the DUT.

were visible by the IR camera. Due to unpolished backside surface, thorough transistors level structures were invisible. Since there were 32 identical SP and DP SRAM IPs, it was sufficient to inspect only a single SRAM IP of each type. Figure 6.17 highlights the inspected IPs during the campaign.

6.5.4 PL campaign methodology

For a high-resolution scan of 1 μm on the entire SP IP region of $(246\times339)\mu\text{m}^2$ presented in Table 6.3), the laser should pulse at least once at each position in both horizontal and vertical directions. The total number of pulses was determined beforehand by using an expression from Equation 6.2:

$$Total\ number\ of\ Pulses = \frac{246 \times 339}{1} = 83394 \tag{6.2}$$

The expected scan time was further calculated by dividing the number of pulses by the repetition (pulse) rate. A repetition rate of 10 HZ was adopted after taking into account both the SEL handling time of the SAMPA current monitoring system and the power cycling period.

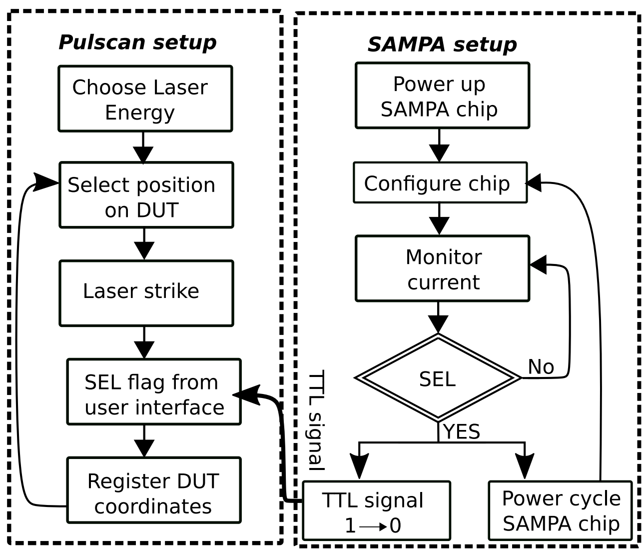


Figure 6.18: Automatic laser scan setup to acquire SEL sensitive regions

Figure 6.18 illustrates the test setup flow chart of an automatic laser scan. During the automatized scan, the laser was pulsed with a frequency of 10 Hz and an x-y step-size of 0.5–1 μm was set. At each grid position, the Raspberry Pi monitored the current consumption of the DUT in real-time. Upon the detection of SEL events, the Raspberry Pi informed both the facility's oscilloscope and the HMP2020 power supply by sending trigger signals. The laser system further acquired a waveform from the oscilloscope in order to evaluate whether an SEL event occurred. In case of SEL event detection, the PULSCAN system stored

the coordinates of the event, while the DUT was power cycled. At the end of scan, the laser system built a sensitivity map (x-y coordinates of the SEL events) and superimposed this map on the actual layout of the chip.

6.5.5 SEL sensitive region confirmation in V2 prototype

Following the procedure and limitations provided in Section 6.5.4, the expected time to scan entire SP IP region was ∼2.31 hr. Since the campaign time was limited to 8 hr, it was impractical to perform an automatized laser scan on the entire SP IP region. Hence, the campaign was initiated by performing manual scans to identify relatively smaller SEL sensitive region within the SP SRAM IP.

Figure 6.19: SEL region within the SP IP region during manual laser scanning

Figure 6.19 presents the manual scan region within the SP IP region where the SEL sensitive area (highlighted in red color) were initially spotted at a laser energy of 276 pJ. This region is believed to exist within the memory array of the SP IP. The laser pulses were gradually injected around this region to spot the most SEL sensitive regions for the automatized scan run. The determined SEL threshold energy was within 117–124 pJ.

Two highlighted regions with green color in Figure 6.19 are believed to be the peripheral circuits of the SP SRAM IP[20]. By increasing the laser energy up to 276 pJ, the manual scan demonstrated that the peripheral circuits were not sensitive to SEL events. A quick manual scan was also performed in the middle of the DP SRAM IP region to evaluate its SEL sensitivity. No SEL events were detected up to a laser energy of 690 pJ.

6.5.6 Power supply voltage effect on the SEL sensitivity

The plot in Figure 6.20 shows the relationship between the SEL threshold laser energy and the supply voltage (V_{DD}) of the V2 prototype. At nominal V_{DD} of 1.25 V, the laser energy threshold for SEL events was 131 pJ. By lowering V_{DD} to 1.23 V, no SEL events were detected at 131 pJ energy threshold. The laser energy was gradually increased until SEL events triggered again at 144 pJ.

The supply voltage was further reduced stepwise, which resulted in an increase of laser energy threshold for SEL events. For instance, at V_{DD} of 1.11 V, no SEL

[20]The peripheral circuits consist of several sub-blocks such as Bit PreCharge, Row and Column decoder, Sense Amplifiers, Control logic, and DATA I/O [138].

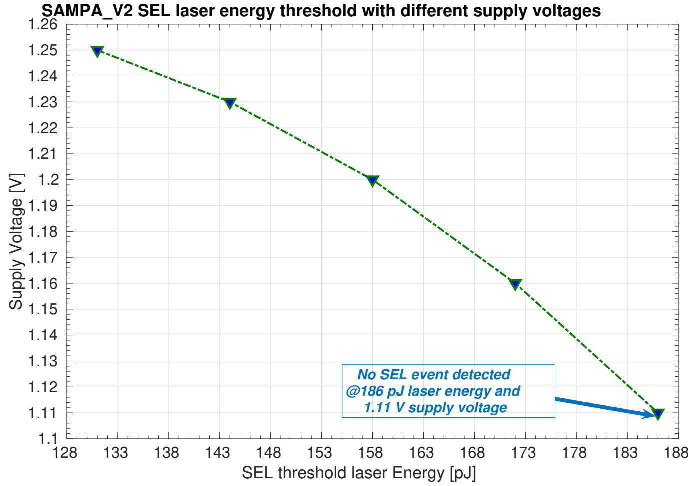


Figure 6.20: Supply voltage as a function of the SEL threshold of laser energy

events was detected at a laser energy of 186 pJ. This is relatively compatible with the HI results (presented in Figure 6.10), where no SEL events were detected at an LET value of 5.7 MeV cm^{2}mg^{-1}. It provides the first indication that the laser energies within the range of 131–182 pJ corresponds to an ion equivalent LET value between 5.7–10 MeV cm^{2}mg^{-1}.

6.5.7 Automatized laser scan results

In total, three automatized laser scan runs were performed on the V2 prototype during the campaign. Figure 6.21 presents the scanned regions within both the SP and DP SRAM IPs[21]. Table 6.6 summarizes various relevant parameters

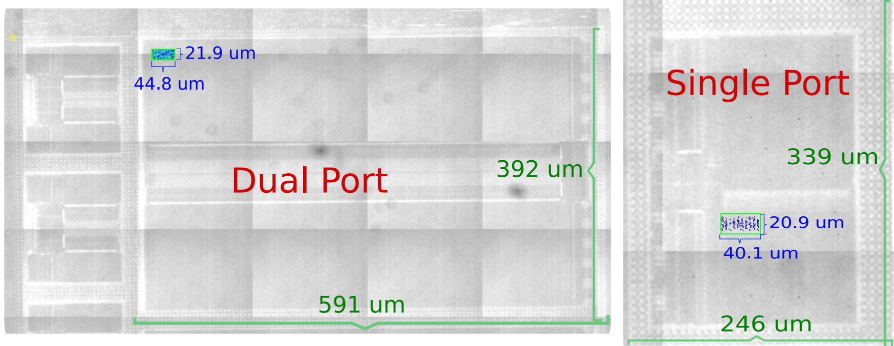


Figure 6.21: Automatized laser scanned regions within both the SP and DP SRAM IPs.

from these runs, where the number of pulses are calculated by dividing the scanned area with the respective step size, as presented in Equation 6.2.

[21] Manual scanning identified these SEL sensitive regions.

Memory	Laser Energy	Scanned Area [μm^2]	Δx$\times\Delta$y	Repetition Rate	# of pulses	Time [s]
SP	131 [pJ]	40.1×20.9	1μm×1μm	10 Hz	~840	~1000
SP	131 [pJ]	40.1×20.9	0.5μm×0.5μm	10 Hz	~3352	~3400
DP	690 [pJ]	44.8×21.9	1μm×1μm	10 Hz	~982	~1015

Table 6.6: An overview of various parameters during automatized laser scan runs.

Figure 6.22 presents the acquired SEL sensitive map of SP IP with a laser scan resolution of 0.5μm, where XY-axes represent coordinates inside the IP, and the color represents the SEL trigger level. By default, the trigger signal was high (red points), and in case of SEL detection, the trigger signal was changed from high to low (blue points). The blue points indicate the entire SEL sensitive regions, located within the scanned area of SP IP at a laser incident energy of 131 pJ.

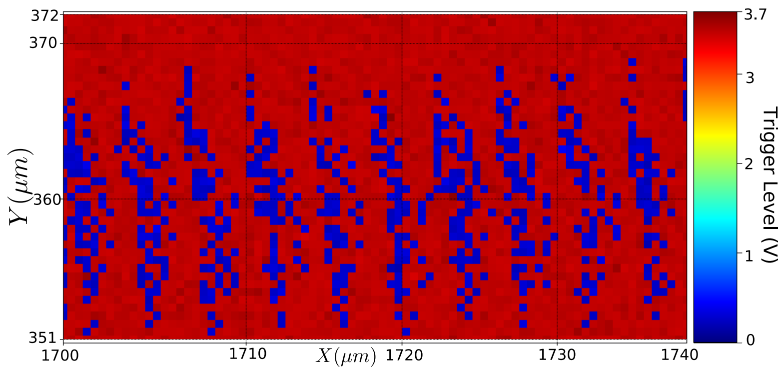


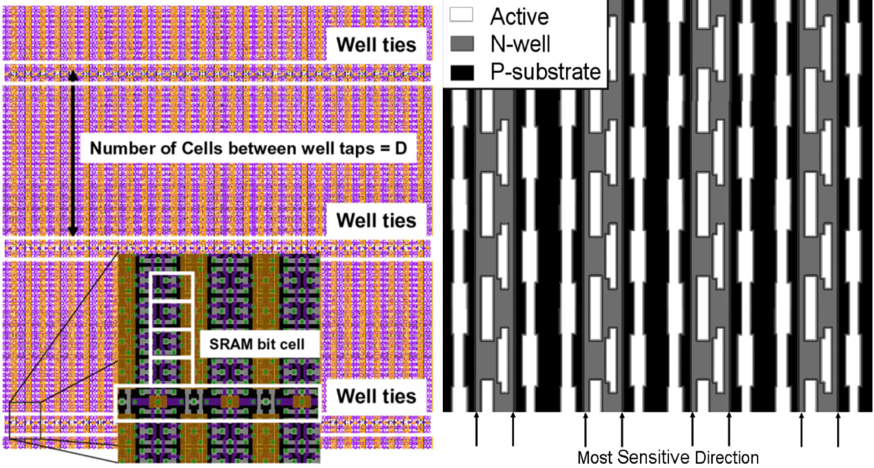
Figure 6.22: SP SRAM IP SEL sensitive map from 0.5μm resolution automatized laser scan

During the automatic laser scan of the DP SRAM IP region, the SEL trigger signal was constantly high up to the laser incident energy of 690 pJ. It ensured that the DP SRAM IPs in the V2 prototype are not sensitive to SEL events. The sensitive map for the DP IP is presented in Figure G.3b in Appendix G.3 (on page 217).

6.5.8 Analysis of the SEL sensitive map

The SEL sensitive map in Figure 6.22 presents a repetitive pattern toward both the horizontal and vertical directions. It is probably due to the matrix architecture of the memory array, which shares common power planes[22]. In a memory array, every individual transistor is not connected to a well (V_{SS} for NMOS source terminal and V_{DD} for PMOS source terminal) [139]. These contacts are typically repeated every 2,4,8,16 or more cells to achieve higher array density. Figure 6.23a presents an example of the SRAM array layout,

where the well-tie rows are distributed between every 32 SRAM cells.



(a) Layout of the SRAM cell array showing the periodical distribution of the well tie rows every 32 cells

(b) The N-wells arranged in long columns present a likely most sensitive lateral directionality for SEL events in an SRAM array

Figure 6.23: ©2007 IEEE. Reprinted, with permission, from [141] and [142] respectively.

When a particle strikes within the memory cell and the distance between the memory cell location and its respective well contact is significant, some of the created charges can result in higher voltage drop and trigger the latch-up condition. The voltage drop is typically proportional to the distance between the source terminal and the respective well contact. According to reference [142], N-well is the most SEL sensitive region in a typical CMOS SRAM layout structure. Figure 6.23b represents an SEL sensitive repetitive pattern that is compatible with the SEL sensitive pattern presented in Figure 6.22. Thereby, the triggered SEL events in the SP SRAM IPs of the V2 prototype have likely occurred due to a significantly larger distance between the n-well and substrate contacts to the P+ and N+ implants of the memory cells.

6.5.9 SEL σ comparison between PL and HI campaign

Reference [143] presents a theoretical expression for σ_{SEE} conversion between the PL energy and ion equivalent LET, which requires certain optical parameters (reflection and absorption coefficients) and device parameters (sensitive depth and substrate doping coefficients). Nevertheless, a simpler expression to

[22] The memory cells within a memory array are physically mirrored and overlapped with each other to share common nets, such as word-line, bit-line, supply voltage V_{DD}, and ground plane V_{SS}[140]. It effectively reduces the layout area of the memory array.

extract the experimental PL σ_L is provided in Equation 6.3 [143]:

$$\sigma_L = \frac{S}{\frac{M}{step\ size} \times \frac{N}{step\ size}} \times N_E \tag{6.3}$$

where S is the scanned laser area, M and N are the elementary pixels in both horizontal and vertical directions, respectively, and N_E is the total number of detected events. Additionally, the division of M and N parameters with the respective step sizes is required.

During the automatized laser scan runs of SP IP region with a step size of 1 and 0.5 μm as well as the laser energy of 131 pJ, the accumulated number of SEL events were 233 and 963, respectively (see Table 6.6). By using the expression from Equation 6.3, the extracted σ_{SEL} value lies within the range of (2.3±0.3)–(2.4±0.2)×10^{-6}cm^2. The comparison between the extracted σ_{SEL} values of PL campaign and the σ_{SEL} values of the HI campaign[23] indicates that the σ_{SEL} value of ~2.4×10^{-6}cm^2 lies within the LET value range of 5.7 and 10 MeV cm^{2}mg^{-1}.

Another theoretical expression to determine ion equivalent LET value from the absorbed laser energy is presented in Equation 6.4 [144].

$$LET = 0.0527J\ (MeV\ cm^2\ mg^{-1}) \tag{6.4}$$

where J represents the laser energy in pJ. Reference [144] presents comprehensive details of this expression. The expression from Equation 6.4 provides an ion equivalent LET value of 6.9 MeV cm^{2}mg^{-1} for a laser energy of 131 pJ. It eventually also confirms the results from the previous approach.

During the DP SRAM IP automatized scan, no SEL event was detected up to the laser energy of 690 pJ. Hence, the ion equivalent LET value threshold is higher than 36 MeV cm^{2}mg^{-1} for the DP SRAM IP. These results are also compatible with the HI results where no SEL event was detected up to an LET value of 32 MeV cm^{2}mg^{-1} with the DP collimator run.

6.6 Summary and conclusion

No SEL events were detected up to the fluence of 1.76×10^{11}protons cm^{-2} during the MPW1 campaign. The upper-bound σ_{SEL} value is calculated by using the confidence interval of 95%. The extracted σ_{SEL} value is lower than 1.7×10^{-11}cm^2 per MPW1 prototype. For the V2 prototype, all protons irradiated samples encountered frequent SEL events. A σ_{SEL} value of (4.0±1.4)×10^{-11}cm^2 per V2 prototype is extracted by taking the mean σ_{SEL} values of all irradiated V2 samples previously presented in Table 6.1 (on page 102).

Table 6.7 presents the SEL event failure rate of the V2 prototype for both the TPC and MCH detectors in the ALICE experiment. The values are extracted by considering the maximum flux locations , previously presented in Table 2.2

[23] Presented in Table 6.2 and Figure 6.9 on page 106. The derived σ_{SEL} for LET values of 5.7 and 10 MeV cm^{2}mg^{-1} is (7.7±2.5)×10^{-7}cm^2 and (1.8±0.3)×10^{-3}cm^2, respectively.

(on page 31). It demonstrates that in the ALICE radiation environment, the expected mean time between SEL is ~7.8±2.2 minutes and 3.76±1 minutes for the TPC and MCH detector, respectively.

Prototype	# of chips	TPC	MCH
	1	×16,380	×34,000
SEE/s			
V2	$(1.3\pm0.3)\times10^{-7}$	$(2.1\pm0.5)\times10^{-3}$	$(4.4\pm1)\cdot10^{-3}$
MTBF			
V2	$(2.1\pm0.6)\cdot10^{3}$ hr	(7.8±2.2) min	(3.76±1) min

Table 6.7: Expected failure rate for SEL events in the ALICE experiment. The results are based on the outcomes of V2 proton campaigns.

Due to the higher SEL failure rate of the V2 prototypes, subsequent HI and PL campaigns were conducted to determine both the threshold and SEL sensitive regions within the V2 prototype. The HI campaign concluded that the LET_{thr} for the SEL events was below 3.3 MeV cm^2mg^{-1}. The reduction of supply voltage also confirmed correlation with the SEL sensitivity. The supply voltage reduction can improve the expected SEL failure rate for both ALICE detectors. However, it may require new power domain integration in the digital core, where the SP SRAM IPs operate at the supply voltage of 1.11 V.

The automatized laser scan runs on the SP IP region presented a repetitive pattern within the memory cells. It is believed to be due to a significantly longer distance between the n-well and substrate contacts to the P+ and N+ implants between the memory cells. Since the physical layout of the SRAM IPs were not accessible to the design team, IMEC[145] was requested to perform design rule checks to evaluate well taps distance between the SRAM IPs. IMEC verified that the SP and DP IPs were designed with well-taps distance of 46μm and 2μm, respectively. The well-taps distance of 46μm likely produced higher enough voltage drops to forward-bias the p-n junctions of the CMOS thyristor within the memory arrays of the SP SRAM IPs. Similar behavior has also been previously reported in reference [146] by performing 3D TCAD simulations on the SRAM memory cells of an identical technology node. The results confirm that the SEL tolerance increases significantly by reducing the well-taps distance from 34μm to 8.5μm. One of the SEL layout mitigation techniques suggested in reference [146] is to increase the frequency of N and P well-taping contacts to V_{DD} and V_{SS}, respectively. It minimizes the average resistance between the location of the particle strike and the charge collection node.

All SEL campaigns confirmed that the detected SEL events in the V2 prototype were not immediately destructive since power cycling always brought back the DUT to its nominal operation. On fewer occasions during the proton campaign, successive step increases were detected on the nominal current level (see Figure 6.2 and E.12). These current jump events are likely associated with multiple SEL events at distinct locations within the SP SRAM IP regions. In references [147, 148, 139], such SEL sensitive regions are referred to as the

"micro latch-up" regions in the memory array, where only a limited array of the memory cells is sensitive to SEL events. If the heat build-up from the subsequent SEL events exceeds the heat dissipation capacity of the package or the internal structures, it can lead to thermal damage. Hence, successive non-destructive events can eventually lead to the DUT failure. No post-latch-up life test were performed on the irradiated V2 samples to evaluate the latent damage effects. Reference [149] reports that the latent damage due to non-destructive SEL events can cause cracking of the insulator material or voiding of the interconnect metal within the CMOS devices, which can lead to reliability issues within the devices.

Chapter 7

The final SAMPA campaign

This chapter presents results from the final heavy-ions irradiation campaign conducted on the final versions (V3 & V4) of the SAMPA chip. The main objective of the campaign was to qualify the chips and ensure that the SEL sensitivity of the final versions was significantly reduced at least up to the LET threshold of 16 MeV $cm^2 mg^{-1}$ (maximum expected LET for the LHC hadron environment).

7.1 SEL mitigation in SAMPA V3 and V4

From a radiation sensitivity perspective, the functionality of the V3 and V4 prototypes was equivalent because of the common digital core[1]. In order to enhance SEL susceptibility of the digital core, the following suggestions were addressed among the SAMPA collaboration:

Removal of the Pedestal (single port) SRAM IPs

This option works fine for the ALICE TPC detector since the TPC detector will use the SAMPA chip in Direct ADC Serialization (DAS) mode, where the digital functionality will be disabled. However, it is inconvenient for the ALICE MCH detector which relies on the pedestal memories feature to correctly process data from the detector.

New power domain for the Pedestal SRAM IPs

The main objective of this option is to turn off the power supply of the pedestal SRAM IPs when they operate in idle state (not in use). During the normal read or write operation, the pedestal IPs will operate at a lower supply voltage of 1.11 V[2]. From a design perspective, it requires modifications in the chip floorplan to handle power stripes of the new domain. It also requires level shifters and switches for reliable performance. On the Front End Cards side, significant modifications are required by the ALICE detector groups. Lastly, it demands the redesign of the BGA package substrate to support the new power domain in the final versions.

Register-based pedestal memory

A standard register-based multiport memory uses flip-flops as a primary storage unit instead of an SRAM cell. Register-based memories were already implemented

[1] The analog blocks differ slightly to meet specific specification requirements.

[2] Previous SEL campaigns demonstrated a significant reduction in SEL sensitivity at 1.1 V of the supply voltage.

in the MPW1 prototype, and the irradiation campaign confirmed that the register-based memories were robust against SEL events. The design team performed a rough area estimation for this approach, which concluded that a register-based pedestal memory (446224 μm^2) would require five times larger area than a SRAM IP (83394 μm^2). It was undesirable due to strict area limitations.

Supply voltage reduction of the entire digital core

Supply voltage reduction of the entire digital core is another alternative that could reduce SEL sensitivity. However, it can lead to adverse effects on the soft errors (SEU and SET events) sensitivity. Additionally, new high energy proton or neutron campaigns will require to re-qualify the final SAMPA versions against soft errors. Speed performance reduction in the digital core is another major drawback, which can lead to timing and synchronization issues between various interfaces, such as the ADC, the SLVS, and the slow control interface.

Leave the SEL events untreated

Both the pulsed-laser and the ion beam campaigns confirmed that the SEL sensitive regions were confined within the SRAM cells of the SP IPs. If it is optimistically assumed that these micro-SEL events only affect the stored data-content within the pedestal memories and that the SAMPA chip always survives after such events, these SEL events can be left untreated on chip level. However, it requires dedicated latch-up protection, detection as well as removal mechanism on the system level. This option involves certain risk factors and requires additional features for the FECs. For instance, if multiple SAMPA chips share a common power supply control mechanism on the FECs, a SEL event in a single SAMPA chip may require power cycling of several SAMPA chips simultaneously[3].

Leaving the SEL events untreated may also result in long-term reliability issues for the SAMPA chips due to the latent damage effects, as previously mentioned in Section 6.6. It will then be imperative to conduct post-latch-up tests to carefully evaluate the latent damage effects, and estimate the lifetime reliability of the SAMPA chips accordingly.

Generate SRAM IPs by CERN radiation-hard compiler

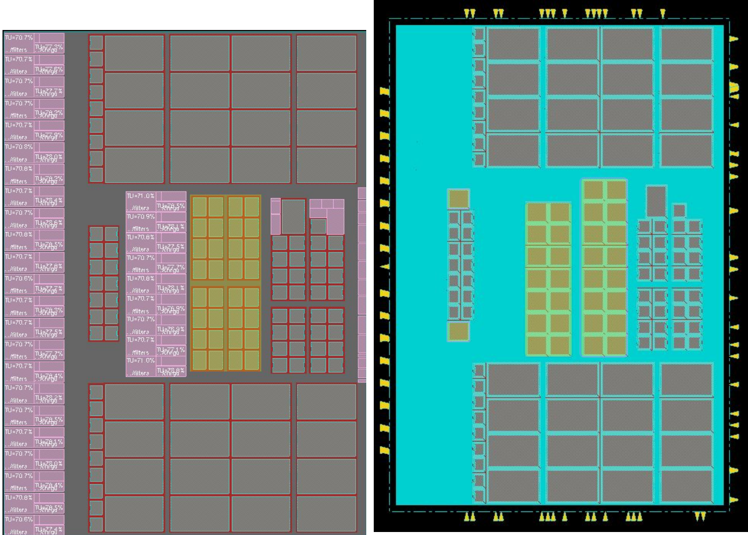
Memory compiler from CERN could be an ideal solution since the memory compiler is Radiation-Hard-By-Design [150]. However, it only supported 8-bits wide data words, which would require significant design modifications in the digital core of the SAMPA chip.

Implement pedestal memories with Dual-Port IPs

Both the ion beam (with collimators) and the pulsed-laser campaigns verified that the DP SRAM IPs are robust against SEL effects. Hence, the replacement of the SP SRAM IPs with the DP SRAM IPs is another alternative. The depth

[3]Each FEC contains 5 and 2 SAMPA chips for the TPC and MCH detector, respectively.

and width configurations of the pedestal memories will remain unchanged with this option. This option was employed in the final versions of SAMPA chip as it required a minimal amount of effort by the design team, and no changes were required in the FECs.



(a) SP pedestal IPs in V2 prototype. *(b) DP pedestal IPs in V3&V4 prototypes.*

Figure 7.1: Physical placement of the pedestal memories in the digital core layout of various SAMPA prototypes are highlighted in yellow.

Due to a slightly larger area of the DP IPs, some back-end challenges were faced for achieving timing enclosure requirements. These issues were resolved by placing two of the pedestal DP IPs physically apart from the initial pedestal IPs region of the V2 prototype. Figure 7.1 highlights the physical placement of the pedestal SRAM IPs within the layout of the V2 and V3 & V4 versions. The functionality of the pedestal memories was preserved by disabling the extra port of the DP SRAM IPs.

7.2 Irradiation campaign of the final versions

Usually, irradiation campaigns with high energy protons or neutrons are favored for the qualification of the LHC electronics. For the V2 prototype, the SEL Weibull curve (see Figure 6.9 on page 106) was previously extracted from a HI campaign at the UCL facility, where the LET_{thr} of the SEL events was below 3.3 MeV $\text{cm}^2\text{mg}^{-1}$. Thereby, it was preferred to evaluate the SEL LET_{thr} of the final SAMPA versions by conducting a similar HI campaign at the identical facility.

7.2.1 Test setup of the final campaign

Most of the test setup of SAMPA V3 & V4 campaign is identical to the V2 HI campaign, presented in Figure 6.7 (on page 105). However, the current sensing board with the INA226 devices was replaced by the SELTC board developed by Jonas Birkeland Carlsen during his master project [108]. The ambient temperature monitoring of the DUT [128] was another planned feature of the final campaign.

Temperature effect on SEL sensitivity

An elevated temperature may trigger latch-up due to the following phenomena: (i) Higher substrate and well resistivity, (ii) amplification of the parasitic bipolar transistor's gain, and (iii) reduction in the potential that turns on the emitter/base junctions of the parasitic bipolar transistors [151]. Reference [46, 151] reports that both the threshold LET and the saturation σ region of the SEL events can be increased at the elevated temperatures. The devices which do not trigger latch-up at the room temperature may latch at the elevated temperature. Hence, only the room temperature testing can be insufficient for an exhaustive SEL qualification.

Temperature requirements for the SAMPA chip

For the ALICE TPC detector, the cooling system for the Front-End Electronics (FEEs) is under-pressure leak-less water-cooled system [152]. Therefore, the ambient temperature is not expected to exceed 30°C for the TPC FECs. For the MCH detector, the FEEs will be air-cooled. Therefore, the ambient temperature of the FECs is likely to be above 40°C for most of the time. In a worst-case scenario, the SAMPA chips can suffer ambient temperatures up to 60°C.

Temperature monitoring setup

During both the proton and HI campaigns of the V2 prototype, no temperature monitor feature was implemented due to a relatively short timeframe between the campaigns. It is worth reminding that both the FPGA-based DAQ board and the SAMPA carrier board were placed inside the vacuum chamber during the V2 HI campaign. As both devices dissipate heat inside the chamber, an ambient temperature monitoring feature seemed to be imperative in the following SEL qualification campaign at the UCL facility. Under vacuum, the heat dissipation is much slower than normal air circumstances. Therefore, higher σ_{SEL} values from the V2 campaign could occur due to higher ambient temperatures within the chamber than what expected at the ALICE detectors.

The final campaign included both the temperature monitoring and elevation features, as presented in Figure 7.2[4]. Temperature monitoring setup was implemented by using 1-wire digital thermometer "DS18B20" from *Maxim Integrated* [106]. DS18B20 is a 9 to 12-bits temperature sensor, which can sense

[4]For clarity, Figure 7.2 only presents the temperature monitoring system. The additional setup required for current monitoring and communication with the DAQ system previously presented in Figure 6.7 on page 105.

temperatures within the ranges of -55°C and +125°C and an accuracy of ±0.5^{o}C. It was compatible with the processing unit (Raspberry Pi). A PWR221T-30 series power resistor from *BOURNS* [153] was used for power elevation purpose[5].

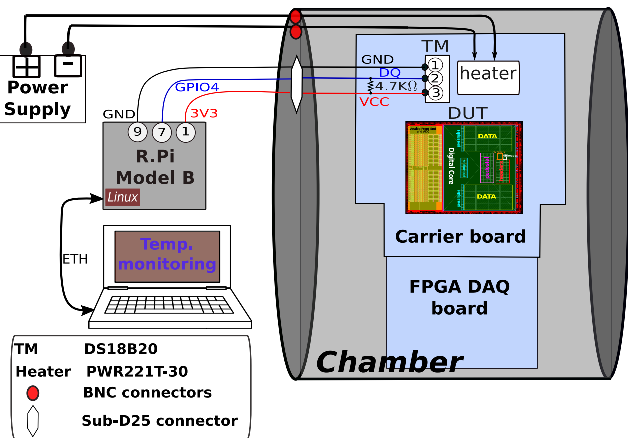


Figure 7.2: Temperature monitoring setup overview for SAMPA V3 & V4 HI campaign.

Figure F.4 (on page 203) presents the placement of both components on the rear of the carrier board. Both components were placed close to the DUT. The thermometer device was glued on every carrier board. Python scripts were developed to acquire temperature logs from these sensors via processing unit. Similar to the current and voltage data, the temperature was also monitored both in real-time and saved in separate files for future analysis.

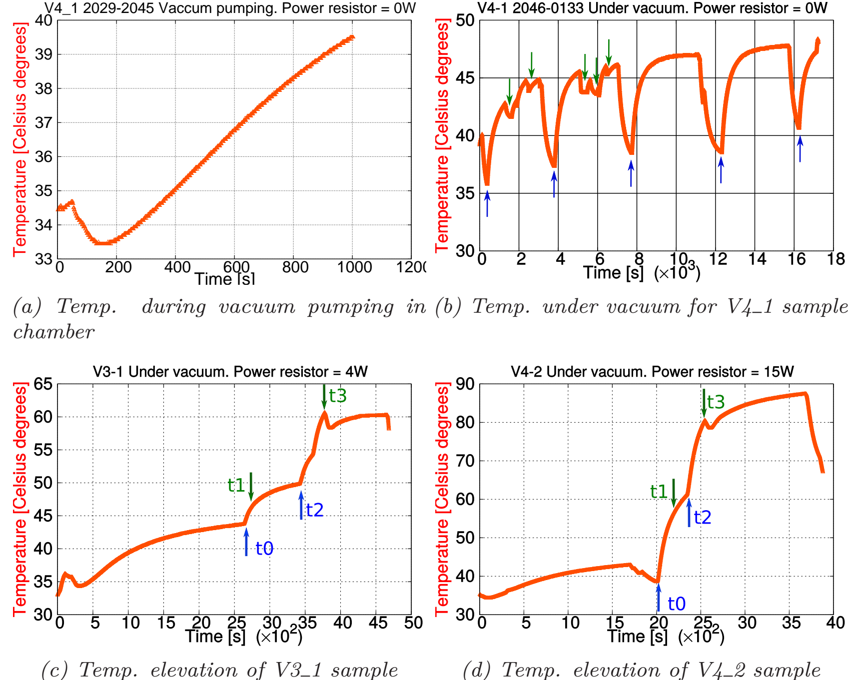
7.2.2 Temperature monitoring results

Two V4 (V4_1 and V4_2) and one V3 (V3_1) samples were irradiated with heavy-ions during the campaign. The plots in Figure 7.3 represent the temperature logs acquired from the thermometers during the campaign. Figure 7.3a represents the temperature log as a function of time. It shows the time period for reaching the near-vacuum pressure level inside the chamber at the UCL facility. The ambient temperature inside the chamber was ~33°C before vacuum pumping down process initiated. It took ~1000 s to reach the near-vacuum pressure and the ambient temperature was linearly increased up to ~40°C. Both the carrier board and the DAQ board were powered on during this period.

Figure 7.3b represents the temperature log during the HI exposure of "V4_1" sample. Within the total irradiation time of 4.78 hr, the relative ambient temperature was gradually increased from 39°C to 48°C[6]. Several dips can be observed

[5]Reference [154] presents extensive details about the use of DS218B20 with the R.Pi. The power resistor has a resistor value of 25Ω, which is capable of delivering maximum effect up to 30 Watt. It requires an additional power supply for delivering sufficient current.

[6]The power resistor was turned off for the V4_1 sample since the ambient temperature inside the chamber was already within the expected range of the ALICE detectors.



(a) Temp. during vacuum pumping in chamber *(b) Temp. under vacuum for V4_1 sample*

(c) Temp. elevation of V3_1 sample *(d) Temp. elevation of V4_2 sample*

Figure 7.3: Temperature data monitored within the vacuum chamber during the campaign.

in the temperature magnitude, where the smaller magnitude dips (marked by green arrows) correspond to the power cycling of DUT. The power cycling was performed between the execution of various test scripts. The larger dips marked with blue arrows were associated with changing the ion type, where the vacuum pressure was slightly dropped while chamber door remained closed.

The plots in Figure 7.3c and 7.3d represents the temperature log from the V3_1 and V4_2 carrier boards, respectively. Due to the vacuum pumping process, both plots show a gradual increase in temperature at the beginning. In order to evaluate the effect of temperature elevation on the SEL sensitivity, the power resistor was turned on. The delivered effect was 4 W and 15 W on V3_1 and V4_2 carrier boards, respectively. The rapid temperature increase at the $t0$ and the $t2$ time instant (marked by blue arrows) represents the moments when the power resistor was turned on. The gradual temperature increase at the $t1$ time instant, and the dip followed by the gradual temperature increase at the $t3$ time instant (marked by green arrows) occurred when the power resistor was turned off. The plots conclude that both the temperature monitoring and elevation setup was successfully executed during the campaign, and the thermometers efficiently sensed a rapid temperature elevation up to 88°C.

7.2.3 SEL results of the final SAMPA prototypes

V4_1 sample was irradiated with ions having different LET values up to maximum LET of 125 MeV cm^{2}mg^{-1}. The maximum LET value was accomplished by tilting the DUT (carrier board) to an angle of 60° for the incoming ^{124}Xe^{35+} ions[7]. The ambient temperature of the DUT was within a range of 40°C and 48°C. The V3_1 sample was exposed to ^{124}Xe^{35+} ions both at normal and 60° incident angle while the ambient temperature was elevated to 60°C by turning on the power resistor. Another V4 sample "V4_2" was irradiated with the same ions up to the maximum effective LET value while the ambient temperature was further increased to 88°C.

Table 7.1 presents a brief summary of the SEL results from V3 & V4 SAMPA prototypes, and the results are compared with the V2 prototype[8]. An exhaustive summary of the SEL results can be found in Table F.1 (on page 203).

Sample	Eff.LET [MeVcm^2/mg]	Eff.Fluence [i/cm^2]	Temp [^{o}C]	SEL events	σ_{SEL}[cm^2]
V4_1	Up to 125	1.0×10^7 *	45	0	$< 3.9\times10^{-7}$
V3_1	125	1.5×10^7	60	0	$< 2.5\times10^{-7}$
V4_2	125	1.0×10^7	85	0	$< 3.7\times10^{-7}$
V2**	32.4	4.8×10^4	-	247	$(5.2\pm0.6)\times10^{-3}$
V2**	16.0	1.1×10^5	-	335	$(3.2\pm0.3)\times10^{-3}$

* V_1 sample irradiated with ions of various LET values. 1.0×10^7 of fluence achieved at an effective LET value of 125 MeV cm^2 mg^{-1} .

* V2 campaign did not support temperature monitoring feature.

Table 7.1: SAMPA V3 & V4 HI SEL results summary.

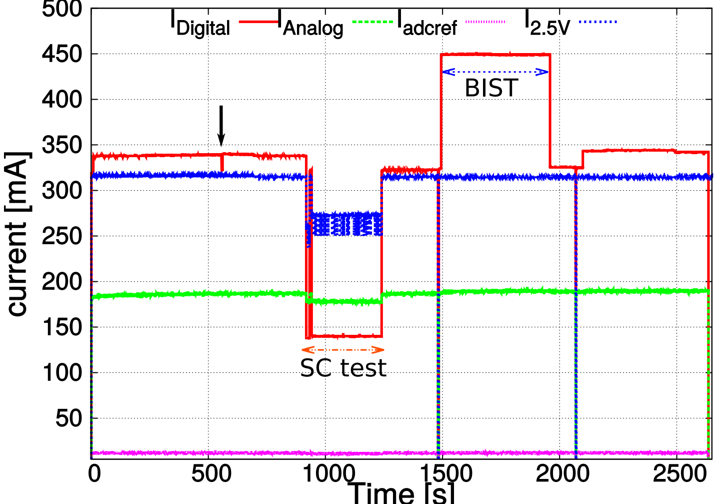
During the campaign. the current was monitored from all internal power domains of the DUT. Figure 7.4 presents the current profile during ion exposure with LET values of 16 and 32.4 MeV cm^{2}mg^{-1}. Both current waveforms indicate no signatures of high current jump (SEL) events on the V4_1 sample. Various runs were executed on the DUT during the ions exposure[9]. As the current consumption of the scan chain and BIST tests differ from the nominal level, the respective time-frames are highlighted in both plots. Some unexpected current drop events with 15-20 mA of magnitude reduction are detected which will be discussed in Section 7.3.

Since no SEL events were detected in the V4_1 sample, the upper boundary limit for SEL events was extracted by following JEDEC recommendations from [128]. The upper boundary limit of 3.67 SEL events was determined by using chi-squared (χ^2) distribution expression from Equation B.8 (on page 158) to achieve

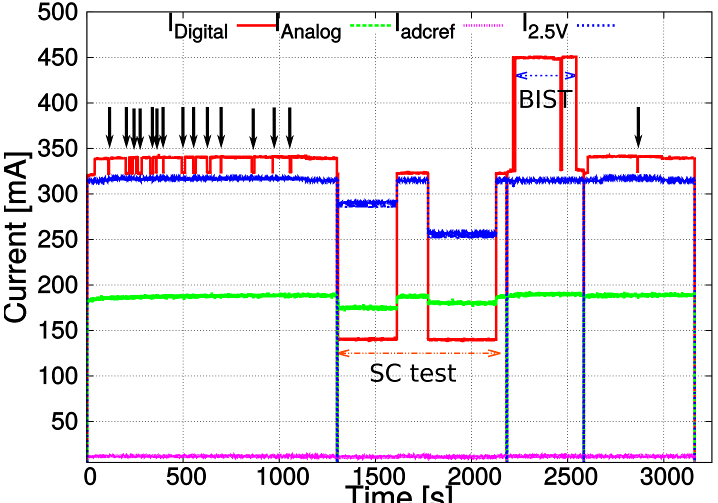
[7] ^{124}Xe^{35+} was the heaviest available ion at UCL facility with the normal LET value of 62.5 MeV cm^{2}mg^{-1}.

[8] The V2 HI SEL results are previously presented in Table 6.2 on page 106.

[9] Scan chain, Built-In-Self-Test and slow control registers read and write tests were executed during the campaign.



(a) Ion exposure with LET value of 16 MeV cm^{2}mg^{-1}, reaching 1.46×10^7 i cm^{-2} of fluence.



(b) Ion exposure with LET value of 32.4 MeV cm^{2}mg^{-1}, reaching 2.10×10^7 i cm^{-2} of fluence.

Figure 7.4: Current time waveform for V4_1 sample for the maximum expected LET at ALICE detectors.

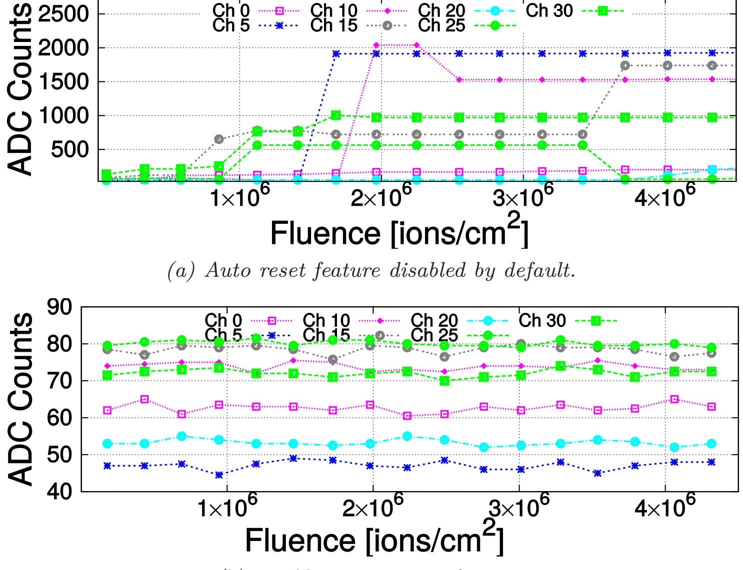
a confidence level of 95% for the Poisson distributed errors. The upper limit σ_{SEL} value was further extracted from the accumulated fluence of respective ions. In comparison to the σ_{SEL} values of V2 prototype with identical ions of LET values of 16 and 32.4 MeV cm^{2}mg^{-1}, the SEL sensitivity of the final versions is reduced with several orders of magnitude. For instance for V4 prototype, the relative σ_{SEL} value is lower than 0.003% and 0.008% for the identical ions,

respectively. Even at the elevated temperature of 88°C and the maximum LET of 125 MeV cm^{2}mg^{-1}, the final SAMPA prototypes are tolerant against SEL events.

The SEL tolerance of V4 prototype was also verified during the pulsed-laser campaign, where an automated scan was performed on the same pedestal memory region within the V4 prototype. No SEL events was detected up to the incident laser energy of 1025 pJ, which is almost 10× higher than the SEL threshold energy for the V2 prototype.

7.2.4 Auto-reset feature verification for the BC2 filter

During the proton campaign of V2 prototype, rapid fluctuations were detected in the sampled values of the BC2BSL registers, whereas the sampled values in the BC3BSL registers were stable[10]. These fluctuations happened due to soft errors on the internal non-TMR protected FFs of the second baseline filter, highlighted in Figure D.5 (on page 177). To mitigate these soft errors, the design team suggested a manual workaround to enable the *Auto Reset* configuration of the BC2 filter[11]. During the final campaign, this workaround was verified during the ion exposure with an LET value of 16 MeV cm^{2}mg^{-1}. Figure 7.5 plots the sampled values from the BC2BSL register of some selected channels as a function of ion fluence.



(a) Auto reset feature disabled by default.

(b) Enabling auto reset feature.

Figure 7.5: Verification of auto reset functionality of BC2 filter during ion exposure with an LET value of 16 MeV cm^{2}mg^{-1}.

[10] Figure 5.15 previously presented results on page 82.

[11] BC2 auto-reset enables by setting bit[10] high in BC2CFG register (see Table D.11 on page 173, address = 0x15).

Figure 7.5a presents the accumulated soft errors from the sampled values of some selected channels where the auto-reset feature was disabled. Due to the dominant direct interaction mechanism of heavy ions with silicon, the soft error rate is significantly higher than for the proton campaign at KVI. After enabling auto-reset feature, no rapid fluctuations (soft errors) were encountered on any channel after accumulating equivalent ion fluence, as presented in Figure 7.5b. Thereby, the auto-reset enabling feature can significantly suppress the soft error contribution from the BC2BSL registers.

7.3 Investigation of current drop events

To understand the phenomena behind the current drop events detected in Figure 7.4, it is essential to confirm that these events are related to real soft errors instead of any unknown setup configuration. The current waveform from Figure 7.4a demonstrates that only one single current drop event was triggered at an LET value of 16 MeV cm^2mg^{-1}. However, these current drop events frequently occur with ions of LET values of 32.4 MeV cm^2mg^{-1} or higher. The current drop events with identical ion exposure are combined from all irradiated samples, and the σ values of these events are extracted with the effective fluence of the respective ions. The effective fluence is calculated by discarding the time period of every current drop event.

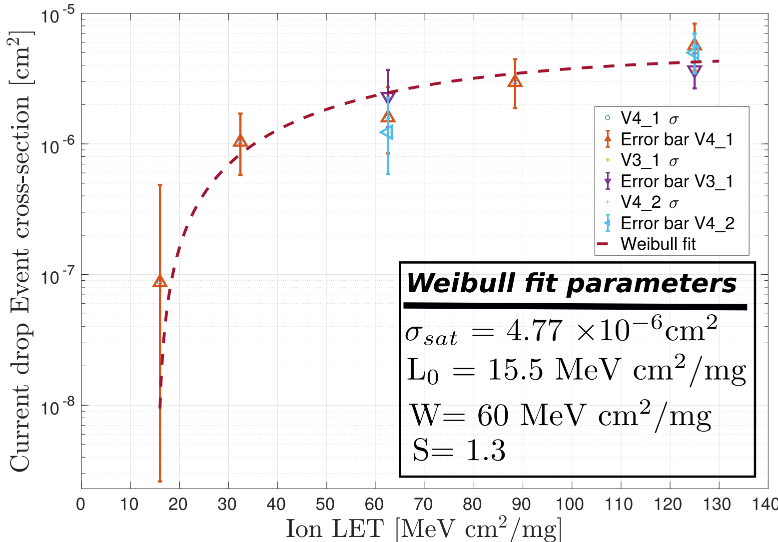


Figure 7.6: SAMPA V3 & V4 current drop events σ as a function of LET spectrum.

Figure 7.6 plots the σ values of the current drop events as a function of the LET spectrum, where the error bars present a confidence interval of 95% with the Poisson distribution. The σ values are further extrapolated with the four-parameter Weibull fit [129] and the fit parameters are shown in the plot.

The Weibull curve demonstrates a rapid fall-off between the LET value of 16 and 32.4 MeV cm^{2}mg^{-1}, and a gradual saturation within the range of 32.4 and 125 MeV cm^{2}mg^{-1}. The alignment between the σ points and the Weibull curve justifies the association of these events with real soft errors. The source of these events is further identified by evaluating the following signatures: (i) Consistent current drop magnitude of 15-20 mA, (ii) typical duration of these events, and (iii) impact of these events on the acquired data.

The waveform in Figure 7.7 presents the first 300 seconds of the run which is previously presented in Figure 7.4b. By default, only four serial links were enabled in the DUT (see Table D.2 on page 166, addr = 0x12, SOCFG). At ~40 s, the slow control register test script was executed[12]. It enabled all eleven serial links of the DUT and the current consumption was increased with 18 mA. The test script initiated an infinite loop for executing various read and write operations on the slow control registers where every cycle was completed in ~18 s.

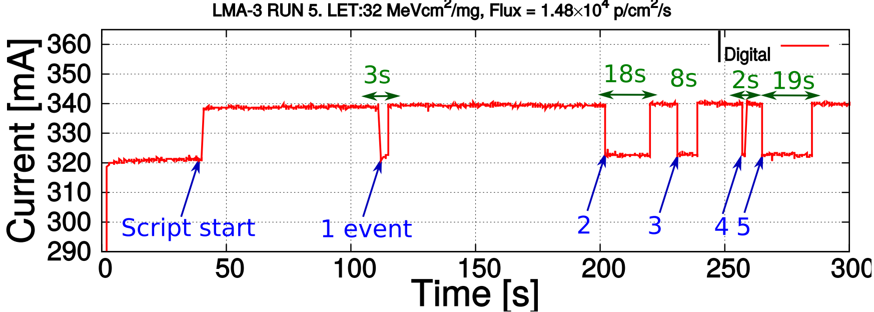


Figure 7.7: Zoomed waveform during ions exposure with 32.4MeV cm^{2}mg^{-1} LET.

Ideally, the current consumption level should be persistent once the script was initiated as the number of serial links should remain constant. It is worth noting that the current drop magnitude of all events is equivalent to the nominal current level at the beginning of the time window. It provides first indication that the current drop event may occur due to an unexpected change in the amount of active serial links back to the default value of four. This would only be possible either by reconfiguring the *SOCFG* register or by resetting the SAMPA chip. The plot further demonstrates that the current level increased again after some amount of time. It is believed to happen due to the automatic enabling of all eleven serial links at the start of each cycle in test script. The variable period of the current drop event is dependent on when the soft error occurred within the cycle. For instance, if the soft error occurred near the end of cycle, the duration of the current drop event would be shorter. If it occurred at the start of cycle, the duration was longer.

The online data monitoring and soft error comparison of the pedestal memories data-content was the most time-consuming operations of the 18 s loop cycle.

[12]The details of the slow control register test are previously explained in Section 5.8 on page 81.

If these current drop events are associated with real reset events, these events should not impact the stored data-content within the pedestal SRAM IPs as these IPs did not have any reset pin. The data-content of the memories could only be modified either after power cycling the DUT or writing the modified data to the memories.

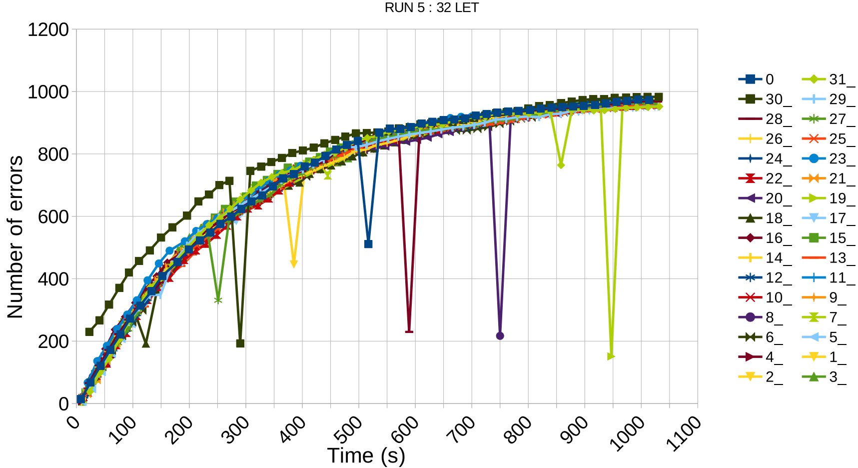


Figure 7.8: Errors accumulated from the pedestal memories IPs during ion exposure with LET value of 32.4 MeV $cm^2 mg^{-1}$.

The graph in Figure 7.8 represents the accumulated soft errors from all 32 pedestal memories as a function of ions exposure time. For every channel, the soft error curve is linearly increased at the start of run, and is gradually saturated after that. This saturation occurs since multiple soft errors are accumulated on the individual 10-bits addresses of the pedestal memories. There was a bug in the analysis script which counted these multiple soft errors as a single error[13]. Occasionally, the soft error curves present several dips in the soft error counts for some random channels. When accumulating soft errors in the following read cycle, the curve arrives back to the expected trend for the corresponding channel. It is noteworthy that the fall-off time of these curves corresponds reasonably well with the time instant of the current drop events, presented in Figure 7.4b. It confirms that the data-content of the pedestal memories did not corrupt due to the current drop events, but rather the readout communication was halted for a time fraction. It points towards a reset event triggering within the DUT that halted the slow control interface (I2C) communication for some fraction of time, upon receiving a reset transient and returned to its normal operation afterward.

[13]The analyses script was not optimized to support soft error counting from a hostile radiation environment where soft errors generation primary dominated by direct ionization mechanism.

7.3.1 SAMPA reset manager

The reset manager module of the SAMPA chip is briefly explained in Section 3.2.10 (on page 47) and comprehensively in reference [89]. The SAMPA chip supports both the hard and soft reset, where only the hard reset is capable of resetting SAMPA configuration registers such as *SOCFG*. The hard reset is an active low differential input which can either be supplied externally through the SLVS receiver (RX) module or generated by the Power-On-Reset (POR) module.

Figure D.6 (on page 178) presents a simplified diagram of the SAMPA reset tree where the reset signals from both the POR and the SLVS RX modules are combined together to provide a common reset assertion signal. Since the POR feature was disabled during the irradiation campaigns, the SLVS RX module can potentially be the source of triggering hard reset pulses within the DUT. The SLVS module internally converts the low voltage differential signal (SLVS) to a single-ended high voltage signal, which further goes to the hard reset pin of the SAMPA chip.

7.3.2 SET simulations on the SLVS RX module

Hugo Hernandez designed both the SLVS RX and TX modules of the SAMPA chip [155]. Hugo Hernandez was requested to perform SET simulations on the SLVS RX module, by injecting current at different sensitive nodes within the circuit[14]. Appendix H (on page 231) presents the sensitive nodes and the simulation results.

The generated current pulse by a particle strike typically has a faster drift and slower diffusion process time (see Figure 2.3b on page 17). During the simulation, the injected current presented a rise and fall time of 50 ps and 150 ps, respectively, with a period of 10 ns. The current magnitude was varied within the range of 2 mA to 7 mA, with a step size of 1.25 mA, and the current was injected at four distinct sensitive nodes within the internal structures of the SLVS RX module. At the same time, the voltage was monitored at the output node. The simulation results demonstrated that the current threshold for generating a pulse at the output node lies within the range of 2 mA and 3.25 mA, for three out of four sensitive nodes[15]. It corresponds to the deposited charge threshold between the range of 0.4 pC and 0.65 pC.

The Weibull curve of the current drop events from Figure 7.6 demonstrates that the LET threshold lies in the range of 16 to 32 MeV cm^2mg^{-1}. Table B.1 (on page 156) presents the conversion of the deposited charge and energy with respect to different LET values in silicon. For LET value of 16 and 32 MeV cm^2mg^{-1}, the deposited charge is 0.16 pC/μm and 0.33 pC/μm, respectively. Considering a typical charge collection sensitive depth of 2μm, the SET threshold of the SLVS RX module from the simulation results corresponds reasonably well with the σ and threshold values acquired during the HI campaign.

The SLVS RX module has an area of $116.4\times10^{-6}cm^2$, whereas the σ curve confirms a gradual saturation at $\sim4.77\times10^{-6}cm^2$. This indicates that $\sim4.1\%$

[14]CERN micro-electronics group (EP-ESE-ME) [83] provided SET current injection model.
[15]The most sensitive nodes even generated output voltage at the current magnitude of 2 mA.

of the area within the SLVS RX module is potentially sensitive to trigger reset pulses.

7.3.3 Consequences of SET events from the SLVS RX modules

The hard reset signal is among one of the several signals which arrive into the SAMPA chip through several SLVS RX modules. In total, the SAMPA chip has nine identical SLVS RX modules:

- Three SLVS RX modules for various trigger signals (Bx_sync_trg, hb_trg, Event_trg).
- Three SLVS RX modules for various clock inputs (clk_bx,clk_ADC_in,clk_SO).
- One SLVS RX module for the hard reset.
- One SLVS RX module for the NB flowstop_in.
- One SLVS RX module for Neighbor data from daisy-chaining.

Since the trigger and neighboring signals are synchronous to the clock, the SET events should occur close to the active clock edge to impose any effect. Furthermore, a SET event on one of the clock lines could potentially result in an additional clock pulse. Nevertheless, this effect may also be suppressed due to the typically short duration (250 ps) of the SET events. In the reset manager module, the FFs are employed with asynchronous reset in the first synchronizers, as presented in Figure D.6 (on page 178). A FF with an asynchronous reset has a reset control input that changes the FF state the moment reset goes active, regardless of the clock. Once a reset signal is asserted in the SAMPA chip, it typically lasts for the maximum period of 206.25 ns (2×ADC clock cycles + 2×serial clock cycles). Although the SET triggering probability is relatively low for most of the signals arriving from the SLVS RX modules, it can be more apparent for the hard reset signal. This is further confirmed by evaluating *TRCNTL* and *TRCNTH* register values (see Table D.2 on page 166, address 0x01 and 0x02) from the campaign. These registers counted the number of event triggers accumulated by the trigger module. Due to SET pulses from the respective SLVS RX module, the *TRCNTL* register accumulated false trigger counts. However, the frequency of trigger events was much lower than the current drop/reset events.

Figure 7.9 plots the extracted σ values from both the reset and trigger events as a function of ions LET values. It demonstrates that the SET σ values of the trigger events are almost one magnitude lower than the current drop events. It is expected since only those SET events, which occur close to the active clock edge, were sampled and accumulated in the *TRCNTL* register.

7.4 Summary and conclusion

The results from the final HI campaign assured that the SEL tolerance of the final SAMPA prototypes was significantly improved. The measured σ_{SEL}

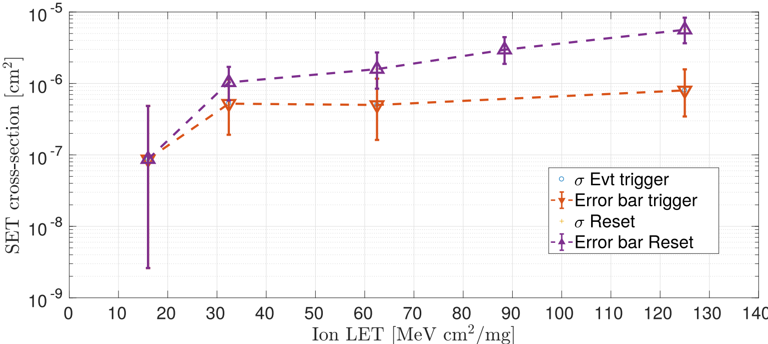


Figure 7.9: SET σ comparison between the reset and event trigger signals of the SAMPA chip.

values demonstrated that the SEL sensitivity is reduced with several orders of magnitude, as compared to the results of V2 prototype. The relative σ_{SEL} values of the V4 prototype is lower than 0.003% and 0.008%, compared to the V2 prototype, for ion exposure with LET values of 32.4 and 16.0 MeV cm^{2}mg^{-1}, respectively. No SEL events were encountered on any of the irradiated prototypes up to an ambient temperature of 88°C during the ion exposure with an effective LET value of 125 MeV cm^{2}mg^{-1}. Both the ambient temperature and the ion LET value are far above the expected values of the ALICE environment.

Furthermore, the enabling of the auto-reset feature in the BC2 filter is verified. The results confirmed that enabling this feature can significantly reduce or altogether remove the soft error contribution from the BC2 filter for the ALICE radiation environment.

Besides accomplishing satisfactory results during the final HI campaign, frequent current drop events were detected on all power domains of the final prototypes. The σ values were used to extrapolate the Weibull curve, which confirmed that the current drop events were potentially associated to a soft error. Further investigations and analysis were performed on the acquired data, which showed the propagation of hard reset pulses internally within the SAMPA chip. Since the hard reset signal arrives from the SLVS RX module, the SET simulation was performed on this module, which confirmed contingency for triggering transient pulses. The consequences of transient pulses were further evaluated on various signals coming from the identical SLVS RX modules. Among them, the hard reset signal seemed to be most sensitive to the SET events due to the asynchronous reset path in the reset manager module.

Although SET events on the hard reset signal is a severe SEE, it is indeed encouraging that only one current drop event was detected at an LET value of 16 MeV cm^{2}mg^{-1}, which is just above the maximum LET of recoils generated by hadrons interaction with silicon. Hence, this event may never trigger in the real LHC radiation environment, or at least very rarely.

Chapter 8

Summary and conclusion

This research work investigated the single event effect tolerance of the SAMPA chip. The SAMPA chip will be used in the upgraded front-end cards of the Time Projection Chamber (TPC) and the Muon CHamber (MCH) detectors in the ALICE experiment after the second Long Shutdown period. The radiation environment at the LHC mainly consists of high-energy hadrons (HEH), which induces failures due to single event effects in the readout electronics of the detectors. In the context of the presented results from previous chapters, Section 8.1 evaluates the expected failure rates for various kinds of single event effects in the ALICE radiation environment. Section 8.2 presents some limitations of this research work. Section 8.3 provides some improvement suggestions for the future, following a concluding section.

8.1 Prediction of soft error rate in the ALICE experiment

The SAMPA chip should withstand a flux of 3.4 kHz cm^{-2} of HEH (with a safety margin of 2) to operate safely in the worst-case locations for both the TPC and the MCH detectors [13]. The sensitivity of a circuit to a SEE error is typically characterized by its cross-section (σ) value. This σ_{SEE} value predicts the probability of the SEE event to happen in the actual radiation environment. The SEE failure rate ($\frac{SEE}{s}$) is determined by multiplying the extracted σ_{SEE} value by the expected, maximum particles flux in the respective radiation environment.

$$\frac{SEE}{s} = \sigma_{SEE} \times flux \times N_B \tag{8.1}$$

The result of Equation 8.1 provides the soft error rate or the number of soft errors per unit time. N_B is the number of SEE sensitive devices in the respective system. The Mean Time Between Failure (MTBF) is further extracted by taking the inverse of the failure rate.

8.1.1 Soft error evaluation of the registers in the SAMPA chip

Since register-based sequential elements are the essential building blocks of the SAMPA digital core, the soft error sensitivity of the FFs was evaluated during the MPW1 prototype campaign. The derived σ_{FFs} of $(7.0\pm1.2)\times10^{-14}cm^2$ was employed for predicting the expected SEE failure rate in the ALICE experiment, as presented in Table 8.1. For the V2 prototype, ~55 kFFs were approximately required to implement the entire functionality of the digital core.

The data from Table 8.1 demonstrates that the expected failure rate of the registers in the SAMPA chip is about 4 seconds and 2 seconds for the MCH and TPC detector, respectively. These failure rates are extracted before the Triple

Register type	# of regs	1 chip	TPC (×16,380)	MCH (×34,000)
Before TMR protection				
			SEE/s	
All registers	55k	1.49×10^{-5}	0.24	0.5
Configuration registers	34.3k	9.3×10^{-6}	0.15	0.32
			MTBF	
All registers	55k	18 hr	4 s	2 s
Configuration registers	34.3k	30 hr	6.6 s	3.1 s
After TMR protection				
			SEE/s	
Configuration registers	103k	2.8×10^{-5}	0.45	0.95
Data-path (no TMR)	17.7k	4.8×10^{-6}	0.08	0.16
			MTBF	
Configuration registers	103k	10 hr	2 s	1 s
Data-path (no TMR)	17.7k	58 hr	12 s	6 s

Table 8.1: The effect of implementing TMR protection in the SAMPA registers and their respective failure rates in the ALICE detectors.

Modular Redundancy (TMR) mitigation technique was implemented in the SAMPA registers. To enhance the soft error susceptibility, the SAMPA registers were classified in various severity levels, as previously discussed in Section 3.2.5 (on page 43).

There were ∼17.7k pipeline FFs in the data path of the SAMPA chip. Since soft error contribution from this part is acceptable, no TMR mitigation is employed. Thereby, one can expect bit-flips every 6 second in one of the 1 million readout channels for the MCH detector. In the V2 and final versions of the SAMPA chip, the control and configuration registers were initially composed of ∼34.3 kFFs. Therefore, a soft error was expected every ∼3 second in one of the control registers for the MCH detector. It could potentially malfunction the readout of the ALICE detectors. The MTBF for the configuration registers was suppressed by employing the TMR protection technique in the V2 and final versions of the SAMPA chip. Consequently, the total FF counts were increased to 103 K. It will lead to soft error mitigation every 1 second and 2 second for the TPC and MCH detector, respectively.

As previously mentioned in Section 3.2.8 (on page 46), for the TPC detector in the DAS mode, the clock division circuit to derive the 5 MHz ADC sampling clock is not TMR protected. The clock division circuit is composed of 9 FFs. Considering the worst-case scenario for the TPC detector with 16,380 SAMPA chips, the measured σ_{FF} value is used to extract the expected MTBF of 5.5 hours. Since all sampling clocks of the SAMPA chip are monitored via the 11th serial link in the DAS mode, the soft error will be detected in the Common Readout Unit (CRU) and resolved by resetting and re-configuring the respective SAMPA

chip.

During the proton campaign of the V2 prototype, the efficiency of employing TMR protection on the configuration registers is evaluated. It demonstrated high robustness against individual bit-flips, except for the VPD[1]and BC2BSL[1] channel registers. Although both these registers are TMR-protected, the internal FFs in the computational logic blocks are not TMR-protected. Hence, the soft errors from these blocks were further sampled into the TMR-protected registers. Table 8.2 summarizes the measured σ values of both registers and their expected failure rates in the ALICE detectors.

Register	**Address**	σ**[cm^2/chip]**	**MTBF (MCH)**	**MTBF (TPC)**
BC2BSL	0x0E	$(4.4\pm1.4)\times10^{-11}$	196±63 s	408±129 s
VPD	0x0D	$(5.0\pm1.6)\times10^{-11}$	174±56 s	362±116 s

Table 8.2: Prediction of soft error failure rate for the BC2BSL and VPD register in the ALICE detectors.

Considering the worst-case scenario for the MCH detector with 34,000 SAMPA chips, the expected MTBF of the BC2BSL and VPD register is 196±63 s and 174±56 s, respectively. Since these errors were spotted after the submission of the final SAMPA versions, no design improvements are implemented. A potential fix for the BC2BSL register error would be to TMR protect the output *sum* register of the moving average filter. Another manual workaround is to enable the auto-reset feature of the BC2 filter by setting bit[10] of the BC2CFG[1] register high. It will reset the calculated baseline value of the BC2BSL register if the signal stays outside the configured threshold due to bit-flips for longer than a predetermined time. During HI campaign # 4, this workaround has been tested and verified.

Each channel has an ADC baseline level, which can be subtracted by a programmable set of values from the VPD registers such that the baseline level becomes zero. Since the MCH detector requires to perform subtraction operation on the incoming ADC baseline level in the BC1 unit, it is recommended to utilize the FPD[1] filter (Fixed PeDestal register) as an alternative for the VPD register. However, it does not support the self-calibration feature, offered by the VPD register. The auto-reset feature is another manual workaround for the BC1 unit, which can be enabled via the BC1RSTCNT[1] register. The threshold limit can be configured beforehand, and if the values are sampled outside these thresholds due to bit-flips, it will reset the sampled values inside the VPD register. This workaround has not been verified in the final campaign.

[1]see Table D.11 on page 173, VPD address=0x0D, BC2BSL address=0x0E, BC2CFG address=0x15, FPD address=0x0C, BC1RSTCNT address=0x1C

8.1.2 Soft error evaluation of the SRAM IPs in the SAMPA chip

For intermediate data storage in the V2 and final versions, several commercial SRAM IPs are embedded in the digital core of the SAMPA chip. During the proton campaign of the V2 prototype, a detailed chip-to-chip variation analysis of the soft errors sensitivity is performed on the pedestal SRAM IPs. No major discrepancy is observed between the extracted σ values of the SRAM IPs among various irradiated samples, providing a mean σ value of $3.5 \pm 0.54 \times 10^{-14}$cm^2/bit.

Prediction of pedestal memory soft errors in the ALICE detectors

For the ALICE detectors, one realistic scenario of the pedestal memory usage is the configuration of the time-dependent subtraction mode, which removes any systemic effects of the incoming ADC data stream. The content in the pedestal memories can be programmed beforehand with the shape of the systematic perturbation, and then a subtraction operation can be executed between the programmed values and the incoming ADC baseline values.

Detectors that intend to use this operation mode of the BC1 unit should expect soft error contribution on the data content of the pedestal memories. Based on the measured σ values from the pedestal memories and considering the worst-case scenario of the MCH detector, a soft error is expected every 0.75 ± 0.15 second in the pedestal memories. Since the soft error contribution from the pedestal memories is considered low priority, no soft error mitigation are implemented. It is, therefore, recommended to periodically refresh the data-content of the pedestal memories between the data taking runs or when an opportunity is available.

One of the mitigation techniques are addressed in reference [89]. It recommends to hamming protect the pedestal memory data by reducing the width of the data-word to 6 bits for each address and use the remaining 4 as the parity bits (SECDED (10,6)). This technique is not implemented in the final SAMPA versions due to lower priority.

Prediction of data memory soft errors in the ALICE experiment

The irradiation results verified that the soft error sensitivity of both the data and pedestal SRAM IPs was identical. The soft error contribution from the data memory depends upon several factors: The occupancy of the channel, readout frequency of the serial links, and the number of active serial links. For instance, the probability of accumulating bit-flips in the data memories is higher with the readout frequency of 80 MB/s than with 320 MB/s. It is due to a slower data readout rate at 80 MB/s, where the data buffers in the data memories for a longer time.

With a channel occupancy of 30% for the innermost pad row of the TPC detector [8], the average buffer usage is 1000 words$\times$10-bits$\times$30% = 3 kbit. Based on the measured σ values of $(4.45 \pm 1.02) \times 10^{-14}$cm^2/bit , the soft error rate per SAMPA chip is $(1.45 \pm 0.33) \times 10^{-5}$ per second for the TPC detector.

For the full TPC detector, a soft error is expected every 4 second in the data memories.

The average channel occupancy of the MCH detector is 9%. During one single time window of 102.4μs, the average length of the packet is 90-bits. This is composed of 50-bits of the header data, 20-bits of the charge sum information, 10-bits of the cluster timestamp, and 10-bits of the cluster length [13]. The header bits will be buffered in the header memories and the remaining 40-bits will be buffered in the data memories. Considering the worst-case scenario, the expected soft error failure rate in the data memories is ~151 seconds for the MCH detector.

8.1.3 Prediction of hard error rate in the ALICE experiment

The V2 prototypes of the SAMPA chip were sensitive to proton-induced SEL events. Considering the maximum HEH flux locations in the ALICE radiation environment for the V2 prototypes, the expected mean time between SEL events was ~7.8±2.2 minutes and 3.76±1 minutes for the TPC and MCH detector, respectively. Due to a higher SEL failure rate of the V2 prototypes, subsequent heavy-ions (HI) collimator and pulsed-laser (PL) campaigns were conducted to localize the SEL sensitive regions within the V2 prototype. Accordingly, the SEL sensitive SP SRAM IPs were substituted with the DP SRAM IPs in the final versions of the SAMPA chip. The final HI campaign confirmed that the final versions of the SAMPA chip were completely robust against SEL events.

8.2 Discussion and limitation of this work

Frequent current drop events were detected in the digital domain after resolving SEL issues in the final SAMPA versions. The signatures of these events pointed towards triggering of the hard reset transients from the SLVS RX module. Since no design modifications were implemented in the SLVS RX module between the V2 and final SAMPA versions, it is firmly believed that the SLVS RX module was sensitive to these hard reset transients in the V2 prototype as well. However, the frequently appearing SEL events of the V2 prototypes buried these hard reset events. During the PL campaign, fast manual scans were performed to reproduce these events, where the laser source was injected as close as possible to the physical placement of the SLVS RX modules. However, no hard reset events were detected as the physical placement of the SLVS RX module was located outside the accessible region from the rear of the carrier boards.

It is worth reminding that these hard reset events were triggered in a hostile radiation environment of heavy-ions, whereas the LHC radiation environment mainly consists of the HEH. It is indeed encouraging that only one hard reset event was triggered at the LET value of 16 MeV cm^{2}mg^{-1}, which is just above the maximum LET of recoils generated by the hadrons interaction within the silicon. Hence, this event may never trigger in the ALICE detectors, or at least very rarely.

The σ_{SEL} curve of the V2 prototype was previously presented in Figure 6.9 (on page 106). The σ_{SEL} curve demonstrated a rapid fall-off between the LET

value of 5.7 and 10 MeV cm^{2}mg^{-1}. During the final HI campaign, the V2 carrier board was tilted with 40° to accomplish a σ_{SEL} point at the effective LET value of 7.44 MeV cm^{2}mg^{-1}. Unexpectedly, no SEL event was detected up to the ion fluence of 1.66$\times$10^6 i cm^{-2}. It raises concerns about the SEL qualification of a device by utilizing DUT tilting methodology to achieve the desired effective LET values [142, 156, 157].

The effectiveness of the LET method relies upon the assumption that the total energy deposited in the sensitive volume of the device is proportional to the ion path length, which obeys an inverse-cosine law. The commonly proposed explanation for this phenomenon is that the depth-to-width aspect ratio of the device's sensitive volume is not small enough to apply the inverse cosine law [158]. In other words, the Rectangular ParallelePiped (RPP) is box-shaped rather than the typical slab-shaped. The effective LET methodology was also utilized for accumulating hard reset transients, which demonstrated no contingency between the extracted σ points at various effective LET values.

The pulsed laser has proved to be a powerful diagnostic tool to localize the sensitive regions for various kinds of SEEs. However, photon interactions with silicon do not involve any nuclear reaction mechanisms, which has also been reported in reference [75]. For the V2 prototype, the derived σ_{SEL} value from the PL campaign provides no indications of SEL events detected under the sub–LET threshold region during the HI campaign. Nevertheless, one can convert the ion equivalent LET value from the incident laser energy first, and later use models to predict the nuclear reactions σ_{SEE} values from the extracted LET values. The determined σ_{SEL} value from the PL campaign was converted to the ion equivalent LET value by using models from reference [159, 144], and the ion equivalent LET values were compatible with the HI results. In the context of the LHC electronics, no direct correlation can be performed between the σ values from the HEH and the energy threshold from the laser source.

The SEL events in the V2 prototypes were detected at a very critical phase of the project when the SAMPA team was intended to deliver the final versions of the SAMPA chip for fabrication. The shutdown of the TSL facility and the limited availability of the KVI facility delayed the initial V2 proton campaign. After detecting the SEL events in the V2 prototypes, subsequent irradiation campaigns were urgently conducted to localize and identify the source of SEL events. However, the author did not accomplish to detect other hidden errors (soft errors in the BC2BSL and VPD register and the packets readout bug in the triggered readout mode). If sufficient time would have been available between the subsequent campaigns, the author could have potentially modified test plans to further investigate these hidden errors, and accordingly recommend design modifications before the submission of the final SAMPA versions.

The online analysis script for monitoring soft errors from the pedestal memories was not fully optimized to handle a higher amount of soft errors from the direct interaction mechanism of the heavy-ions exposure. It is noteworthy that the commercial SRAM IPs of the SAMPA chip did not include any form of built-in soft error mitigation techniques. Hence, several multiple bit errors were accumulated on a single 10-bits address, which were counted as the single errors

by the analysis script. The soft errors from these IPs were irrelevant during the final HI campaigns, as the prototypes were exposed to a more hostile irradiation environment than expected at the LHC.

8.3 Suggestions for future work

During the final HI campaign, unresolved and unexpected current drop events were frequently detected during the ions exposure with LET values of 32.4 MeV cm^2mg^{-1} and higher, while only one such event was detected at 16 MeV cm^2mg^{-1}. Unfortunately, no data was taken for LET values between 8 and 16 MeV cm^2mg^{-1}. If another HI campaign is conducted on these prototypes, it will be interesting to confirm that no current drop event is detected in this range. One possible workaround is the triplication of the SLVS RX module which delivers the hard reset signal to the SAMPA chip. The output signals of the triplicated SLVS RX modules can be fed to a voter logic. This solution is not implemented as it requires re-spin of the final SAMPA versions.

It is also preferable to perform high energy neutron or proton campaign on the final versions. This can justify the occurrence of reset events in the real hadrons environment and may provide a failure rate prediction of such events in the ALICE detectors. Additionally, one can also verify the readout stability of the serial links by irradiating up to higher particle fluences. It was inadequate during the V2 proton campaign due to frequently triggered SEL events.

The effect of device tilting on the SEL sensitivity of a device can also be further investigated on the V2 prototypes with ions exposure of various strike angles and LET values. Reference [157] reports that grazing angle strikes either perpendicular or parallel along the N-well regions can provide distinct SEL sensitivity of the DUT.

It is also recommended to conduct a final SEE qualification campaign on the entire readout system of the ALICE detectors. The campaign can be conducted at the CHARM (CERN High energy Accelerator Mixed-field) facility [160], which replicates the actual radiation environment of the ALICE experiment.

For the HEP or other radiation environment applications, the ASIC designs should follow the physical design rules for the latch-up protection, as recommended by the foundry. If design IPs are required from an external vendor, the vendor should be requested to perform dedicated design rule checks which can potentially identify the risk of SEL events at an early stage.

The memory BIST feature is included in the final versions of the SAMPA chip. The ALICE detectors can utilize this feature to measure the soft error failure rate within the ALICE radiation environment. However, the SAMPA chip can not perform any data taking operations during the execution of this feature.

The soft error test setup is often application dependent. One should carefully optimize the test setup with respect to the available species at the selected radiation facility. For instance, a soft error test setup developed for a hadrons radiation environment may not be entirely appropriate for a heavy-ions radiation environment.

In a SEL test setup, the supply current monitoring is the core feature for any DUT. The SEL setup of the SAMPA campaigns was based on the Raspberry Pi based processing unit. Although the setup was compact and portable, it was heavily dependent on the HMP2020 power supply. This dependency was resolved with the SELTC board in the final campaigns[2]. A GUI-based current waveform visualizer is another potential feature of the SEL test setup. It should offer current monitoring feature from the DUT in real-time during the campaigns, without increasing the complexity of the setup. Due to the limited time between subsequent SEL dedicated campaigns, the author did not prioritize to implement this feature.

In the final HI campaign, a temperature monitoring feature was included which lacked the direct regulation between the power resistor and the temperature sensor. The temperature was increased cautiously by turning on the power resistor. Since heat dissipation in the vacuum is much slower than in normal air, it could lead to equipment melting inside the vacuum chamber. One possible improvement is to develop a temperature monitoring system which is based on the PID (Proportional-Integral-Derivative) control scheme. It can provide an automatic temperature regulation by sustaining the desired temperature values [161].

8.4 Conclusion

This research work provides SEE qualification of the SAMPA chip with respect to the HEH radiation environment foreseen for the ALICE detectors during RUN 3. During this research, a significant amount of work is dedicated to prepare and execute irradiation campaigns at various external facilities (high energy protons, heavy-ions, and pulsed-laser). To ensure successful campaigns, the author has independently organized all campaign-related activities, such as: (i) Preparation and execution of test plans during the campaigns, (ii) test setup modification to acquire the utmost amount of data from all relevant sources within the DUT, which in turn helps in capturing all kinds of SEEs, (iii) the preparation and verification of the equipment (carrier boards, interface cables, and connectors) for the campaigns, and (iv) safe transportation of the equipment between the facilities.

Several mitigation techniques are implemented within the SAMPA prototypes to enhance the susceptibility against various kinds of SEEs. Furthermore, the effect of design improvements is evaluated in the consecutive prototypes. The outcomes of the campaigns successfully qualify the final versions of the SAMPA chip to withstand the expected irradiation levels foreseen at both ALICE detectors during RUN 3 and ensure stable data acquisition from both detectors.

At the time of writing, the mass production of the final SAMPA versions was already executed. About 91,000 SAMPA chips underwent functional testing with the help of a semiautomatic robot setup at the University of Lund in Sweden, and their final production yield was 79.6%. For the MCH detector, the FECs

[2]Jonas Birkeland Carlsen [108] designed SELTC board during his Master thesis.

are produced and the performance of more than 90% of the FECS has been verified with the SAMPA chips. Both the FECs as well as the upgraded support electronics is installed on Station 3 and Station 4 of the MCH detector, and Station 3 is already commissioned in the ALICE experiment.

For the TPC detector, the FECs are produced and tested with the SAMPA chips with the help of an automated test station. The test station provided automated control of voltages and monitored the output signals to execute basic functionality testing (noise, baseline, gain, crosstalk) for all 160 channels per FEC. The overall final FEC production yield for 3646 FECs was 99.7%. During the pre-qualification phase, the overall stability test with a single upgraded readout chamber (ROC) of the TPC detector is performed at the LHC in the ALICE cavern, a few meters from the interaction point. This demonstrated outstanding performance of the upgraded FECs during the irradiation period of several hours at the highest luminosity. Recently, all the ROCs of the upgraded TPC readout system have successfully passed the final irradiation campaigns at the LHC, and have been accepted for installation. Currently, the commissioning and validation of the entire upgraded readout system of the TPC detector is on-going at the ALICE experiment, which foresees to complete in 2020.

Appendices

Appendix A

List of Publications

A.1 As primary author

- First irradiation test results of the ALICE SAMPA ASIC.
  Mahmood, S.M. et al. for the ALICE Collaboration
  Proceedings Of Science, Vol. 313 - Topical Workshop on Electronics for Particle Physics (TWEPP-17)
  https://doi.org/10.22323/1.313.0093
- Investigation of Single Event Latch-up effects in the ALICE SAMPA ASIC.
  Mahmood, S.M. et al. for the ALICE Collaboration
  Proceedings Of Science, Vol. 343 - Topical Workshop on Electronics for Particle Physics (TWEPP-18)
  https://doi.org/10.22323/1.343.0023

A.2 As SAMPA collaborator

- SAMPA chip: a new ASIC for the ALICE TPC and MCH upgrades.
  Barboza, S.H.I. et al.
  Journal of Instrumentation, Vol. 11, No. 2, C02088, 2016.
  https://doi.org/10.1088/1748-0221/11/02/C02088
- SAMPA Chip: the New 32 Channels ASIC for the ALICE TPC and MCH Upgrades.
  Adolfsson, J et al.
  Journal of Instrumentation, Vol. 12, No. 4, C04008, 2017,
  https://doi.org/10.1088/1748-0221/12/04/C04008

In addition, 223 publications are listed from April 2014 to present as an ALICE collaboration member co-author (based on search from SPIRES-HEP).

Appendix B

Technical terms and calculations for irradiation campaigns

An overview of several technical terms which are frequently employed during this thesis:

- **Flux**: is the rate at which the particles strike upon a unit surface area. It is normally defined as number of particles per cm^2 per second and its unit is $particles/cm^2/s$. The time integral of flux is fluence.
- **Fluence:** It is the total number of particles that strike upon a unit surface area. Its unit is particles/cm^2 .
- **SEE cross sections** σ: It is used for the SEE-sensitive cross-sectional area of a microelectronic device/circuit. This cross-section value indicates the sensitivity area of the device for SEEs, and the derived cross-sections are typically used to predict failure rates for a given radiation environment. They are normally derived from experimental measurements, by dividing the number of events (SEU, SEL, etc.) by the particle fluence. This is generally expressed in units of cm^2, or sometimes in cm^2/bit in case of memory elements.
- **Linear Energy Transfer (LET):** LET describes the energy loss per unit path length of a material as it passes through a material. It is a function of particle's mass and energy, and the density of the target material. It has a unit of MeV/mg/cm^2.
- **Effective LET:** The LET value of an ion can be increased by tilting the DUT so that the ion beam is no longer normal (perpendicular) to the die surface. The effective LET of the tilted DUT is calculated by

$$LET_{eff} = \frac{LET}{cos\theta} \tag{B.1}$$

  where LET$_{eff}$ is the effect LET for an ion incident at the angle of θ from the normal incidence, and LET is the ion's normal incidence LET.
- **Weibull fit parameters:** The formula for the weibull fit is presented in Equation B.2.

$$\sigma(L) = \begin{cases} \sigma_{sat} \times [1 - exp(-(\frac{LET-LET_0}{W})^S)] & \text{for } LET > LET_0 \\ 0 & \text{for } LET < LET_0 \end{cases} \tag{B.2}$$

  where, (i) σ_{sat} is the saturation cross-section, that is the total SEE sensitive area of the DUT, (ii) LET$_0$ is the threshold under which the DUT should

not be sensitive to SEE errors, (iii) W is the width of the rising portion of the curve, and (iv) S is the parameter that determines the shape of the curve.

To use units more convenient for the electronic designers, the LET can be converted to charge per unit length (pC/μm or fC/μm). This conversion is performed by first deriving conversion factor between charge and energy. The amount of energy w_{ehp} required to create an electron-hole (e-h) pair is material dependent. Silicon requires an energy of 3.6 eV to create a single e-h pair, so the conversion factor for the silicon will be :

$$\frac{w_{ehp}}{q} = \frac{3.6 \times 10^{-6}\ \text{MeV/(e-h pair)}}{1.6 \times 10^{-7}\ \text{pC/(e-h pair)}} = 22.5\ \frac{\text{MeV}}{\text{pC}} \tag{B.3}$$

The next step is to determine the equivalent charge transfer rate per unit length when an ionized particle transverse through the material. Equation B.4 presents the formula to calculate this charge transfer rate. Besides other parameters, it also depends upon the material density ρ. The density ρ of silicon is 2.32 g/cm^3. For a given LET of 1 MeV/mg/cm^2, the equivalent charge transfer rate will be :

$$\begin{aligned} \frac{LET \times \rho}{w_{ehp}/q} &= \frac{(1\, MeV \cdot cm^2/mg) \times (2330\, mg/cm^3)}{(22.5\, MeV/pC) \times (10,000\, \mu m/cm)} \\ &= 0.0103\ \frac{pC}{\mu m} = 10.3\ \frac{fC}{\mu m} \end{aligned} \tag{B.4}$$

Typically in silicon, an ionizing particle with an LET of 97 MeV/mg/cm^2 is capable of inducing a charge of 1pC/μm.

LET[MeV cm^2/mg]	**Range[μm Si]**	**Q$_{dep}$[pC]**	**E$_{dep}$[MeV]**	**Q$_{dep}$[pC/μm]**	**E$_{dep}$[MeV/μm]**
3.3	202	6.86	154.6	0.034	0.765
5.7	131.2	7.69	173.5	0.057	1.32
10.0	120.5	12.4	279.5	0.103	2.32
16.0	107.6	17.7	399	0.164	3.71
32.4	94.2	31.4	707.3	0.33	7.51

Table B.1: Deposited charge and energy with respect to silicon depth and LET values.

The high LET particles are generally less penetrating in silicon. This is due to the fact that the faster the particles lose energy in silicon, the sooner they come to rest. Penetration depth in silicon is specifically important during SEL qualification, because SEL mechanism involves current flows along conduction paths relatively deep in substrate. Therefore, sufficiently ion range is necessary to activate these conduction paths [162].

B.1 Calculations of Dose in Silicon

The formula for calculating the deposited dose in silicon is given by :

$$Dose(Silicon) = \frac{\delta E}{\delta x} \cdot \frac{\phi \times t}{C} \tag{B.5}$$

where $\frac{\delta E}{\delta x}$ stopping power of a single proton at the irradiated energy in silicon, $\phi \times t$ is the accumulated fluence, and C is $0.624{\cdot}10^8$ which is a conversion factor between Gray and Rad (1 Gray = 100 Rad) . The value of stopping power is calculated from the graph in plot B.1.

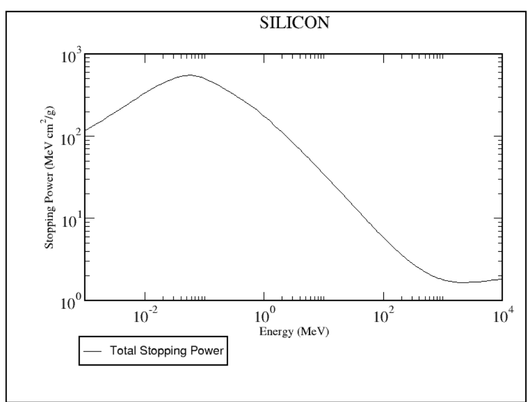


Figure B.1: Stopping power of proton in silicon as a function of proton energy [163].

B.2 Absorption coefficient and penetration depth of photons in silicon

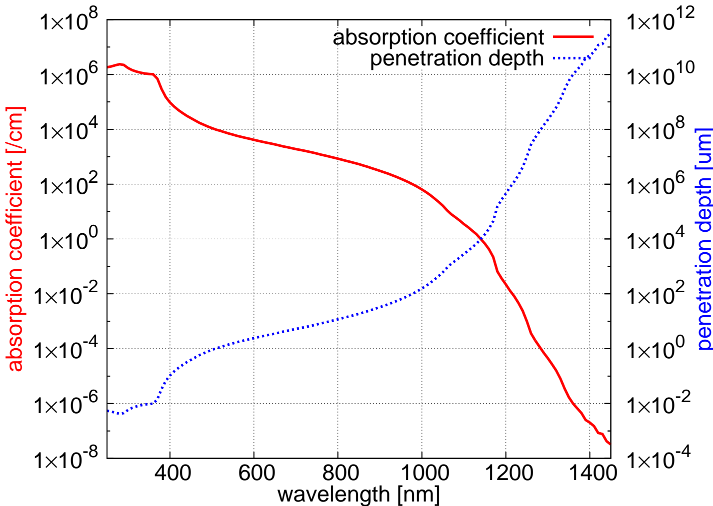


Figure B.2: Absorption coefficient and penetration depth of photons in silicon, as a function of λ. The data is taken from [164]

B.3 Single Event Cross-section calculation

The SEE cross-section σ is given by:

$$SEE(\sigma) = \frac{N_{errors}}{F} \tag{B.6}$$

where N_{errors} is the number of events observed at a accumulated fluence of F. The uncertainty on the cross-section is given by :

$$\frac{\delta\sigma}{\sigma} = \sqrt{\left(\frac{\delta N_{errors}}{N_{errors}}\right)^2 + \left(\frac{\delta F}{F}\right)^2} \tag{B.7}$$

The second term $\frac{\delta F}{F}$ is the uncertainty on the measured fluence (± 15% from TSL, and ± 10% from KVI). The first term $\frac{\delta N_{errors}}{N_{errors}}$ is the standard deviation on the measured number of SEE errors.

Since SEEs are stochastic in nature, they can occur at completely random intervals of time in the irradiated environment. The number of errors observed in a given time follows the Poisson distribution in the start, and, as the number of errors become large, it becomes a Gaussian distibution [165].

According to [165], a general rule of thumb is if $N_{errors} < 21$, Poisson distibution should be followed. Otherwise, follow the Gaussian distribution.

Following the Gaussia distribution, the standard deviation of N events is $\sqrt{N}$. The fractional standard deviation is $\frac{\sqrt{N}}{N} = \frac{1}{\sqrt{N}}$.

Since Poisson distributed variables have a probability distribution function that is a gamma function, a special case is recommended by JEDEC standard [128] of the gamma function, the chi-squared (χ^2) distribution to determine the variance μ in the mean. Using the (χ^2) distribution, the two-sided upper and lower 100(1-α) % confidence intervals for the errors can be expressed as:

$$\frac{\chi^2((\alpha)/2; 2 \cdot n)}{2} \leq \mu \leq \frac{\chi^2((1-\alpha)/2; 2 \cdot (n+1))}{2} \tag{B.8}$$

For example, if the accumulated errors n is 6 with 95% confidence interval, $2.20 \leq \mu \leq 13.1$. This represents that the lower limit for the error bar will be 2.20, while the upper limit will be 13.1. There are cases of interest where small numbers of events are observed (including the case where no events occur) when a large number of particles are incident on the device. The cross-section can be bounded for such cases using the upper and lower counting events. Values are given for 1% and 5% confidence limits. In using this table, the first column is the actual number of events observed in the experiment. The upper and lower limits show how high (or low) the number of events could actually be if the experiment were continued for much longer time periods. The probability that the number of counts exceeds the upper limit is 1% for the 99% confidence limit and 5% for the 95% confidence limit.

Gaussian Distribution		Poisson Distribution			
N	$\frac{\delta N}{N}$ (%)	N	$\frac{\delta N}{N}$ (%)	N	$\frac{\delta N}{N}$ (%)
25	20.0	0	89.9	10	28.6
50	14.1	1	66.7	12	26.3
75	11.5	2	53.7	14	24.4
100	10.0	3	46.5	16	22.7
250	6.3	4	41.7	18	21.7
500	4.5	5	38.0	20	20.8
1000	3.2	6	35.2		
2500	2.0	7	33.3		
5000	1.4	8	31.25		
10000	1.0	9	29.4		

Table B.2: Standard deviation for SEE errors following Poisson and Gaussian distibution.

Appendix C

SAMPA DAQ registers

FPGA modules	UART address	HPS address
Command and control	0x0000	0xFF200000
Data Manager	0x0040	0xFF201000
PLL	0x0080	0xFF202000
I2C	0x00B0	0xFF203000

Table C.1: FPGA modules base addresses for the SAMPA DAQ board.

C.1 Procedure to develop executable C program on SAMPA DAQ linux platform

1. A header file is created which contained the physical addresses for all FPGA modules.

2. The header file is included in the main C program in order to call *dev/mem* device file and execute *mmap* and *munmap* kernel functions.

3. *dev/mem* is the file that represents the physical memory of the Linux system. An access into this file at some offset is equivalent to accessing physical memory at the offset address.

4. By using *mmap* to map the *dev/mem* file into a virtual memory, one can map physical addresses to the virtual addresses, allowing C program to access physical addresses.

5. At the end of the operation, *munmap* is used to close the previously opened virtual address mapping.

C.2 Command and control

The registers for the command and control module, located at address 0x0000 from the UART or 0xFF200000 from the HPS, is listed in Table C.2.

Value	Description
0x1	Reset FPGA and SAMPA
0x2	Reset SAMPA
0x3	Send event trigger
0x4	Send heartbeat trigger
0x5	Send sync signal
0x6	Send trigger to external pulse generator
0x9	Reset HPS

Table C.2: Commands for command and control unit.

C.3 Data manager registers

The registers for the data manager module, located at address 0x0040 from the UART or 0xFF201000 from the HPS, is listed in Table C.4.

Register name		Address	Type	Default	Description	
CMD	[31:0]	0x03	RW	0x00	[15:0]	Commands, see Tabel C.2
			RW	0x00	[30:16]	Loop count for commands
			RW	0x00	[31]	Continuous running for commands
PULSE	[18:0]	0x04	RW	0x00	[12:0]	External pulse generator control
			RW	0x00	[11:0]	Spacing between pulses
			RW	0x00	[16:12]	Shift pulse in reference to ADC
			RW	0x00	[18:17]	Reserved
EVT_CFG	[31:0]	0x07	RW	0x00	[1:0]	Test signal output
			RW	0x00	[2]	Reserved
			RW	0x00	[3]	Enable built in memory testing
			RW	0x00	[31:3]	Reserved
SMP_STS1	[31:0]	0x0A	R			Status of signals to and from SAMPA (updated every clock cycle)
			R		[0]	sme
			R		[1]	TME
			R		[2]	sclk
			R		[7:3]	sen
			R		[12:8]	sdi
			R		[13]	NBflowstop_in
			R		[14]	dinN
			R		[15]	scl
			R		[16]	sda
			R		[17]	hb_trg
			R		[18]	trg
			R		[19]	bx_sync_trg
			R		[20]	hrstb
			R		[24:21]	hadd
			R		[31:25]	clk_config
SMP_STS2	[17:0]	0x0B	R			Status of signals to and from SAMPA cont.
			R		[0]	TDO
			R		[1]	smo
			R		[6:2]	sdo
			R		[11:7]	serialOut
			R		[12]	NBflostop_out
			R		[13]	TRST
			R		[14]	TCLK
			R		[15]	TMS
			R		[16]	TDI
			R		[17]	sda
SMP_CFG	[28:0]	0x0C	RW			Control of signals to SAMPA
			RW	0x37	[6:0]	clk_config (only for internal)
			RW	0x00	[10:7]	hadd (only for internal)
			RW	0x00	[11]	TDI
			RW	0x00	[12]	TMS
			RW	0x00	[13]	TCLK
			RW	0x00	[14]	TRST
			RW	0x00	[15]	dinN
			RW	0x00	[16]	NBflowstop_in
			RW	0x00	[17]	sme
			RW	0x00	[18]	hb_trg
			RW	0x00	[19]	bx_sync_trg
			RW	0x00	[20]	trg
			RW	0x00	[21]	clk_BX for DFT
			RW	0x00	[22]	clk_SO for DFT
			RW	0x00	[23]	clk_ADC for DFT
			RW	0x01	[24]	scl for DFT
			RW	0x01	[25]	hrstb
			RW	0x00	[26]	TME
			RW	0x00	[27]	Enable override for DFT signals
			RW	0x01	[28]	sda for DFT
MEM_ERR	[10:0]	0x0E	R			Errors detected in built in memory test
			R	0x00	[9:0]	Number of errors
			R	0x00	[10]	Error detected
VER	[31:0]	0x0F	R			SVN version build was based on in dec
SMP_CFG1	[10:0]	0x10	RW			Control of signals to SAMPA continued
			RW	0x00	[4:0]	sdi
			RW	0x00	[5]	sclk
			RW	0x00	[10:6]	sen

Table C.3: Command and control registers

Register name		Address	Type	Default	Description	
CNTRL	[31:0]	0x00	RW	0x00		Control register
			RW	0x00	[10:0]	Enable acquisition serial link 10-0
			RW	0x00	[11]	Enable acquisition DAS
			RW	0x00	[12]	Acquire data (one shot)
			RW	0x00	[13]	Clear fifo full flag
			RW	0x00	[15:14]	Reserved
			RW	0x00	[31:16]	Number of packets to acquire
PKT0	[31:0]	0x01	R	0x00	[31:0]	Packets written to memory from link 0
PKT1	[31:0]	0x02	R	0x00	[31:0]	Packets written to memory from link 1
PKT2	[31:0]	0x03	R	0x00	[31:0]	Packets written to memory from link 2
PKT3	[31:0]	0x04	R	0x00	[31:0]	Packets written to memory from link 3
PKT4	[31:0]	0x05	R	0x00	[31:0]	Packets written to memory from link 4
PKT5	[31:0]	0x06	R	0x00	[31:0]	Packets written to memory from link 5
PKT6	[31:0]	0x07	R	0x00	[31:0]	Packets written to memory from link 6
PKT7	[31:0]	0x08	R	0x00	[31:0]	Packets written to memory from link 7
PKT8	[31:0]	0x09	R	0x00	[31:0]	Packets written to memory from link 8
PKT9	[31:0]	0x0A	R	0x00	[31:0]	Packets written to memory from link 9
PKT10	[31:0]	0x0B	R	0x00	[31:0]	Packets written to memory from link 10
PKTDAS	[31:0]	0x0C	R	0x00	[31:0]	Packets written to memory from DAS
FIFO0	[8:0]	0x0D	R	0x00	[7:0]	Number of 64 bit words in FIFO 0
FIFO1	[8:0]	0x0E	R	0x00	[7:0]	Number of 64 bit words in FIFO 1
FIFO2	[8:0]	0x0F	R	0x00	[7:0]	Number of 64 bit words in FIFO 2
FIFO3	[8:0]	0x10	R	0x00	[7:0]	Number of 64 bit words in FIFO 3
FIFO4	[8:0]	0x11	R	0x00	[7:0]	Number of 64 bit words in FIFO 4
FIFO5	[8:0]	0x12	R	0x00	[7:0]	Number of 64 bit words in FIFO 5
FIFO6	[8:0]	0x13	R	0x00	[7:0]	Number of 64 bit words in FIFO 6
FIFO7	[8:0]	0x14	R	0x00	[7:0]	Number of 64 bit words in FIFO 7
FIFO8	[8:0]	0x15	R	0x00	[7:0]	Number of 64 bit words in FIFO 8
FIFO9	[8:0]	0x16	R	0x00	[7:0]	Number of 64 bit words in FIFO 9
FIFO10	[8:0]	0x17	R	0x00	[7:0]	Number of 64 bit words in FIFO 10
FIFO11	[8:0]	0x18	R	0x00	[7:0]	Number of 64 bit words in FIFO 11
HPS	[31:0]	0x19	R			Control register for sampa_server
			R	0x00	[0]	Client connected (acquisition can start)
			R	0x00	[7:1]	Reserved
			R		[31:8]	Version of sampa_server program
STATUS	[16:0]	0x1A	R			Status of ADC signals
			R		[10:0]	Serial link 10-0 is synced
			R	0x00	[11]	DAS is synced
			R		[23:12]	Fifo 11-0 went full
SYNC0	[31:0]	0x1B	R	0x00	[31:0]	Number of times sync was lost from link 0
SYNC1	[31:0]	0x1C	R	0x00	[31:0]	Number of times sync was lost from link 1
SYNC2	[31:0]	0x1D	R	0x00	[31:0]	Number of times sync was lost from link 2
SYNC3	[31:0]	0x1E	R	0x00	[31:0]	Number of times sync was lost from link 3
SYNC4	[31:0]	0x1F	R	0x00	[31:0]	Number of times sync was lost from link 4
SYNC5	[31:0]	0x20	R	0x00	[31:0]	Number of times sync was lost from link 5
SYNC6	[31:0]	0x21	R	0x00	[31:0]	Number of times sync was lost from link 6
SYNC7	[31:0]	0x22	R	0x00	[31:0]	Number of times sync was lost from link 7
SYNC8	[31:0]	0x23	R	0x00	[31:0]	Number of times sync was lost from link 8
SYNC9	[31:0]	0x24	R	0x00	[31:0]	Number of times sync was lost from link 9
SYNC10	[31:0]	0x25	R	0x00	[31:0]	Number of times sync was lost from link 10
EDGE_SEL	[22:0]	0x26	R	0x00		Link edge selection
			R		[10:0]	Serial link 10-0 is captured on rising edge = 1 fallinge edge = 0
			R		[21:11]	Delay serial link 10-0 with one cycle
			R		[22]	Invert serial link clock for PCCA
DROP0	[31:0]	0x27	R	0x00	[31:0]	Number of packets dropped from fifo 0
DROP1	[31:0]	0x28	R	0x00	[31:0]	Number of packets dropped from fifo 1
DROP2	[31:0]	0x29	R	0x00	[31:0]	Number of packets dropped from fifo 2
DROP3	[31:0]	0x2A	R	0x00	[31:0]	Number of packets dropped from fifo 3
DROP4	[31:0]	0x2B	R	0x00	[31:0]	Number of packets dropped from fifo 4
DROP5	[31:0]	0x2C	R	0x00	[31:0]	Number of packets dropped from fifo 5
DROP6	[31:0]	0x2D	R	0x00	[31:0]	Number of packets dropped from fifo 6
DROP7	[31:0]	0x2E	R	0x00	[31:0]	Number of packets dropped from fifo 7
DROP8	[31:0]	0x2F	R	0x00	[31:0]	Number of packets dropped from fifo 8
DROP9	[31:0]	0x30	R	0x00	[31:0]	Number of packets dropped from fifo 9
DROP10	[31:0]	0x31	R	0x00	[31:0]	Number of packets dropped from fifo 10
DROP11	[31:0]	0x32	R	0x00	[31:0]	Number of packets dropped from fifo 11
TRUNC0	[31:0]	0x33	R	0x00	[31:0]	Number of packets truncated from fifo 0
TRUNC1	[31:0]	0x34	R	0x00	[31:0]	Number of packets truncated from fifo 1
TRUNC2	[31:0]	0x35	R	0x00	[31:0]	Number of packets truncated from fifo 2
TRUNC3	[31:0]	0x36	R	0x00	[31:0]	Number of packets truncated from fifo 3
TRUNC4	[31:0]	0x37	R	0x00	[31:0]	Number of packets truncated from fifo 4
TRUNC5	[31:0]	0x38	R	0x00	[31:0]	Number of packets truncated from fifo 5
TRUNC6	[31:0]	0x39	R	0x00	[31:0]	Number of packets truncated from fifo 6
TRUNC7	[31:0]	0x3A	R	0x00	[31:0]	Number of packets truncated from fifo 7
TRUNC8	[31:0]	0x3B	R	0x00	[31:0]	Number of packets truncated from fifo 8
TRUNC9	[31:0]	0x3C	R	0x00	[31:0]	Number of packets truncated from fifo 9
TRUNC10	[31:0]	0x3D	R	0x00	[31:0]	Number of packets truncated from fifo 10
TRUNC11	[31:0]	0x3E	R	0x00	[31:0]	Number of packets truncated from fifo 11

Table C.4: Data manager registers.

Appendix D

SAMPA registers

0	1–5	6–7	8	9	10–11	12–17	18	19–26	27	28–35	36	37
S	11110	Chip addH	0	A	Chip addL	Add	A	Data@Add	A	Data@Add +1	A	P

Figure D.1: Format for writing to the SAMPA. Boxes marked in gray are bits sent by the SAMPA.

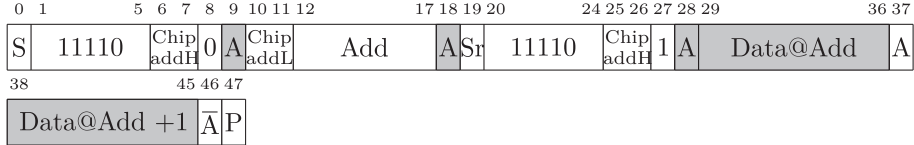


Figure D.2: Format for reading from to the SAMPA. Boxes marked in gray are bits sent by the SAMPA.

Name	Bits	Description
S	1	I2C start
Sr	1	I2C start repeat
A	1	I2C acknowledge
$\overline{\text{A}}$	1	I2C not acknowledge
P	1	I2C stop
11110	5	Fixed preamble address for 10 bit addressing
Chip addH	2	Chip address [3:2]
Chip addL	2	Chip address [1:0]
Add	6	Register address
Data	8	Register data to be read/written

Table D.1: Protocol bit field descriptions of I2C.

D.1 Channel register access

The register layout has been designed to minimize the amount of writes needed to update the channel registers and pedestal memories of each channel. By using the I2C automatic address increment feature, it is possible to complete all writes needed to update one channel or pedestal address in one continuous

Register name	Address	Type	Default		Description
HWADD	0x00	R	0x00	[3:0]	Chip address (hardware address)
TRCNTL	0x01	R	0x00	[7:0]	Trigger count, lower byte
TRCNTH	0x02	R	0x00	[7:0]	Trigger count, upper byte
BXCNTLL	0x03	R	0x00	[7:0]	Bunch crossing count, lower byte
BXCNTLH	0x04	R	0x00	[7:0]	Bunch crossing count, mid byte
BXCNTHL	0x05	R	0x00	[3:0]	Bunch crossing count, upper byte
PRETRG	0x06	RW	0x00	[7:0]	Number of pre-samples (Pre-trigger delay), max 192
TWLENL	0x07	RW	0xE7	[7:0]	Number of cycles for time window +1, lower byte
TWLENH	0x08	RW	0x03	[1:0]	Number of cycles for time window +1, upper byte
ACQSTARTL	0x09	RW	0x00	[7:0]	Number of cycles to wait before acquisition starts, lower byte
ACQSTARTH	0x0A	RW	0x00	[1:0]	Number of cycles to wait before acquisition starts, upper byte
ACQENDL	0x0B	RW	0xFF	[7:0]	Number of cycles elapsed from trigger to acquisition end +1, lower byte
ACQENDH	0x0C	RW	0x03	[1:0]	Number of cycles elapsed from trigger to acquisition end +1, upper byte
VACFG	0x0D	RW	0x31		Various configuration settings
		RW	0x01	[0]	Continuous mode enabled
		RW	0x00	[1]	Raw data enable
		RW	0x00	[2]	Cluster sum enable
		RW	0x00	[3]	Huffman enable
		RW	0x01	[4]	Enable header generation for empty channels
		RW	0x01	[5]	Power save enable
		RW	0x00	[6]	Enable automatic clock gating on I2C block
		RW	0x00	[7]	Enable clock gating on neighbour block when number of neighbour is 0
CMD	0x0E	RW	0x00	[2:0]	Commands, see D.4
NBCFG	0x0F	RW	0x40		Neighbor configuration settings
		RW	0x00	[5:0]	Neighbor input delay, ca. 0.2 ns per bit for a total of ca. 12.5ns
		RW	0x01	[7:6]	Number of neighbors
ADCDEL	0x10	RW	0x00		ADC sampling clock delay
		RW	0x00	[5:0]	ADC sampling clock delay, ca. 1.5ns per bit for a total of ca.94.5ns
		RW	0x00	[6]	Invert ADC sampling clock
ADCTRIM	0x11	RW	0x04	[2:0]	Voltage reference trimming
SOCFG	0x12	RW	0x14	[4:0]	Serial link configuration
SODRVST	0x13	RW	0x55		Serial link drive strength configuration, see D.5
		RW	0x01	[1:0]	Drive strength of serial out 4-0
		RW	0x01	[3:2]	Drive strength of neighbor flow stop out/serial out 5
		RW	0x01	[5:4]	Drive strength of serial out 6,8,10
		RW	0x01	[7:6]	Drive strength of serial out 7,9
ERRORS	0x14	R	0x00		Errors accumulated
		R	0x00	[4:0]	Correctable header hamming errors
		R	0x00	[7:5]	Uncorrectable header hamming errors
PMADDL	0x15	RW	0x00	[7:0]	Pedestal memory address, lower byte
PMADDH	0x16	RW	0x00	[1:0]	Pedestal memory address, upper byte
CHRGADD	0x17	RW	0x00	[4:0]	Channel register address
CHRGWDATL	0x18	RW	0x00	[7:0]	Channel register write data, lower byte
CHRGWDATH	0x19	RW	0x00	[4:0]	Channel register write data, upper byte
CHRGCTL	0x1A	RW	0x00		Channel register control
		RW	0x00	[4:0]	Channel number
		RW	0x00	[5]	Broadcast to all channels (channel number ignored)
		RW	0x00	[6]	Write, not read from register address (returns to read after write)
		RW	0x00	[7]	Increment PMADD (returns automatically to zero)
CHRGRDATL	0x1B	R	0x00	[7:0]	Channel register read data, lower byte
CHRGRDATH	0x1C	R	0x00	[4:0]	Channel register read data, upper byte
CHORDAT	0x1D	RW	0x00	[4:0]	Channel readout order data
CHORDCTL	0x1E	RW	0x00		Channel readout order control
		RW	0x00	[4:0]	Position in order
		RW	0x00	[5]	Write enable
BYPASS	0x1F	RW	0x00	[3:0]	Bypass inputs to serial 0, see D.6
SERCHSEL	0x20	RW	0x00	[4:0]	Channel select for ADC test serializer mode in bypass
RINGCNT	0x21	R	0x00	[7:0]	Ring oscillator counter difference from reference ADC clock
CLKCONF	0x22	R	0x00	[6:0]	Clock configuration pin status
BOUNDARY	0x23	R	0x00		Status of differential input pins
		R	0x00	[0]	NBflowstop_in
		R	0x00	[1]	DinN
		R	0x00	[2]	hb_trg
		R	0x00	[3]	trg
		R	0x00	[4]	bx_sync_trg
CHEN0	0x24	RW	0xFF	[7:0]	Channel enable 7-0
CHEN1	0x25	RW	0xFF	[7:0]	Channel enable 15-8
CHEN2	0x26	RW	0xFF	[7:0]	Channel enable 23-16
CHEN3	0x27	RW	0xFF	[7:0]	Channel enable 31-24

Table D.2: Global registers. Usable gated indicates which registers have any useful function in the Direct ADC Serialization mode.

Name	Dir	Type	Description
hb_trg+	I	SLVS	Heartbeat trigger p
hb_trg-	I	SLVS	Heartbeat trigger n
trg+	I	SLVS	Event trigger p
trg-	I	SLVS	Event trigger n
bx_sync_trg+	I	SLVS	Bunch crossing sync p
bx_sync_trg-	I	SLVS	Bunch crossing sync n

Table D.3: BX sync, event- and heartbeat trigger pins

Command name	CMD[2:0]	Description
NOP	0x0	No operation
SWTRG	0x1	Software trigger
TRCLR	0x2	Clear trigger counter
ERCLR	0x3	Clear errors
BXCLR	0x4	Clear bunch crossing counter
SOFTRST	0x5	Software reset
LNKSYNC	0x6	Generates sync packet on serial links
RINGOSCTST	0x7	Run ring oscillator test

Table D.4: Command register, register returns to 0 after command is executed

Drive strength [1:0]	Iout mean (mA)	Vdiff (mV)	Description
00	1.95	438	Normal mode
01	1.61	348	Low power mode
10	2.87	610	High drive strength mode

Table D.5: Serial link drive strength configuration

I2C command. An additional broadcast bit can be set to write the same data to all channels so that individual access is not needed. When filling the pedestal memory it is possible to set the pedestal memory to increment on each write avoiding the need to update the two registers each time. Table D.8 lists the register needed to access the channel registers.

Write

1. Set CHRGADD (CHannel ReGister ADDress) to the address of the channel register that you wish to write to.
2. Set the data to write at CHRGWDATH:CHRGWDATL (CHannel ReGister Write DATa).
3. Set CHRGCTL[6] (CHannel ReGister ConTroL) high for write, set CHRGCTL[5] high if you wish to write the same value to all channels

BYPASS[3:0]	Description
0x0	Serializer 0
0x1	Feed-through from bx_sync input
0x2	Feed-through from trg input
0x3	Feed-through from hb_trg input
0x4	Feed-through from neighbour input (dinN)
0x5	Feed-through from delayed neighbour input (dinN_del)
0x6	Output of 31 bits lfsr generator
0x7	Output of ADC test serializer
0x8	Internal ADC clock for digital part 10/20MHz
0x9	Internal serial out clock divided by 2
0xA	Internal bunch crossing clock 40MHz
0xB	Internal ADC clock for analog part 10/20MHz
0xC	Internal SAR ADC statemachine clock for analog part 80/160MHz
0xD	Clock from ring oscillator (only when triggered to run) 100-220 MHz

Table D.6: Bypass signals for serial out 0 output

Register name		Address	Type	Default	Description
TRCNTL	[7:0]	0x01	R	0x00	Trigger count, lower byte
TRCNTH	[7:0]	0x02	R	0x00	Trigger count, upper byte
BXCNTLL	[7:0]	0x03	R	0x00	Bunch crossing count, lower byte
BXCNTLH	[7:0]	0x04	R	0x00	Bunch crossing count, mid byte
BXCNTHL	[3:0]	0x05	R	0x00	Bunch crossing count, upper byte
PRETRG	[7:0]	0x06	RW	0x00	No. of pre-samples (Pre-trigger delay), max 192
TWLENL	[7:0]	0x07	RW	0xE7	No. of cycles for time window +1, lower byte
TWLENH	[1:0]	0x08	RW	0x03	No. of cycles for time window +1, upper byte
ACQSTARTL	[7:0]	0x09	RW	0x00	No. of cycles to wait before acquisition starts, lower byte
ACQSTARTH	[1:0]	0x0A	RW	0x00	No. of cycles to wait before acquisition starts, upper byte
ACQENDL	[7:0]	0x0B	RW	0xFF	No. of cycles elapsed from trigger to acquisition end +1, lower byte
ACQENDH	[1:0]	0x0C	RW	0x03	No. of cycles elapsed from trigger to acquisition end +1, upper byte
VACFG	[7:0]	0x0D	RW	0x31	Various configuration settings
			RW	0x01	Continuous mode enabled
CMD	[2:0]	0x0E	RW	0x00	Commands, see D.4
CHEN0	[7:0]	0x24	RW	0xFF	Channel enable 7-0
CHEN1	[7:0]	0x25	RW	0xFF	Channel enable 15-8
CHEN2	[7:0]	0x26	RW	0xFF	Channel enable 23-16
CHEN3	[7:0]	0x27	RW	0xFF	Channel enable 31-24

Table D.7: Event management registers

(broadcasting), set CHRGCTL[4:0] to the channel number that you wish to write the data to. When broadcasting the channel number is ignored.

Read

1. Set CHRGADD to the address of the channel register that you wish to read from.
2. Set CHRGCTL[6] low for read, set CHRGCTL[4:0] to the channel number that you wish to read from. Broadcast (CHRGCTL[5]) is ignored for reads.
3. The data will appear at CHRGRDATH:CHRGRDATL (CHannel ReGister Read DATa).

Pedestal memory write

1. Make sure the data path configuration for the channel to be written to (DPCFG, see Table D.12) is not using a lookup function f(), as the lookup function utilizes the pedestal memory and will cause corrupted writes.
2. Set PMADDH:PMADDL (Pedestal Memory ADDress) to the address in the pedestal memory that you wish to write to.
3. Set CHRGADD to 0x10 which is the address for PMDATA (Pedestal Memory DATA) in the channel register.
4. Set the data to write at CHRGWDATH:CHRGWDATL.
5. Set CHRGCTL[7] high to automatically increment the currently set pedestal memory address (increment before write), set CHRGCTL[6] high for write, set CHRGCTL[5] high if you wish to write the same value to all channels (broadcasting), set CHRGCTL[4:0] to the channel number that you wish to write to. When broadcasting the channel number is ignored.

Pedestal memory read

1. Make sure the data path configuration for the channel to be read from (DPCFG, see Table D.12) is not using a lookup function f(), as the lookup function utilizes the pedestal memory and will cause corrupted reads.
2. Set the address in the pedestal memory that you wish to read from at PMADDH:PMADDL.
3. Put the register address for the channel register PMDATA (0x10) at CHRGADD.
4. Set CHRGCTL[7] high to automatically increment the currently set pedestal memory address (increment before read), set CHRGCTL[6] low for read, set CHRGCTL[4:0] to the channel that you wish to read from. Broadcast (CHRGCTL[5]) is ignored for reads.

5. The data will appear at CHRGRDATH:CHRGRDATL.

Register name	Address	Type	Default		Description
PMADDL	0x15	RW	0x00	[7:0]	Pedestal memory address, lower byte
PMADDH	0x16	RW	0x00	[1:0]	Pedestal memory address, upper byte
CHRGADD	0x17	RW	0x00	[4:0]	Channel register address
CHRGWDATL	0x18	RW	0x00	[7:0]	Channel register write data, lower byte
CHRGWDATH	0x19	RW	0x00	[4:0]	Channel register write data, upper byte
CHRGCTL	0x1A	RW	0x00		Channel register control
		RW	0x00	[4:0]	Channel number
		RW	0x00	[5]	Broadcast to all channels
		RW	0x00	[6]	Write, not read from register address (returns to read after write)
		RW	0x00	[7]	Increment PMADD (returns automatically to zero)
CHRGRDATL	0x1B	R	0x00	[7:0]	Channel register read data, lower byte
CHRGRDATH	0x1C	R	0x00	[4:0]	Channel register read data, upper byte

Table D.8: Channel access registers

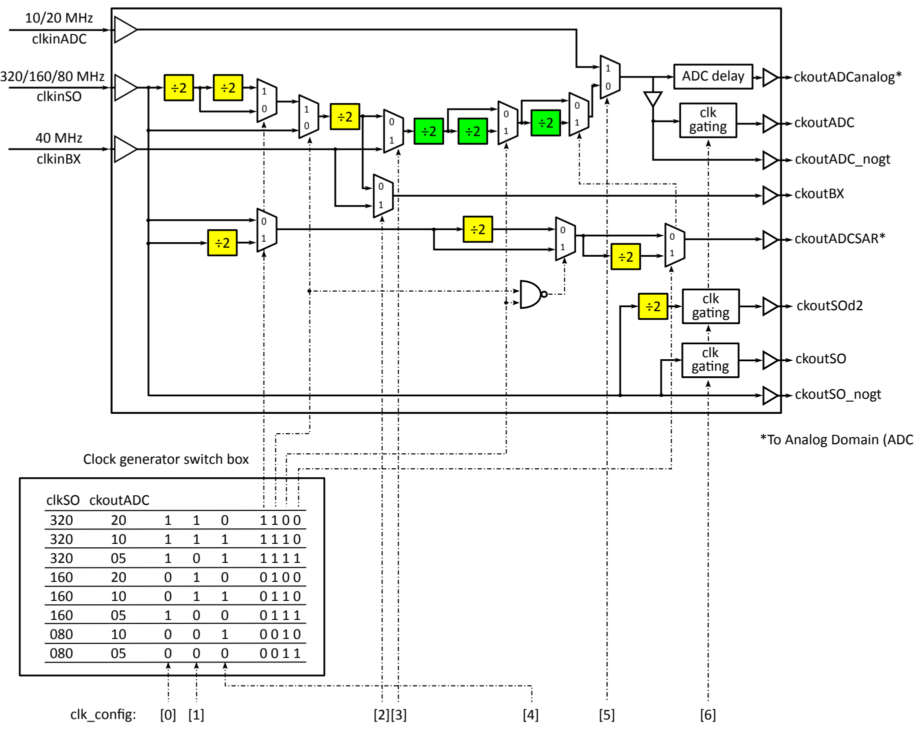


Figure D.3: Block diagram of the clock generation tree.

Channel	Number of links enabled										
	1	2	3	4	5	6	7	8	9	10	11
0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	0
2	0	0	0	0	0	0	0	0	0	0	0
3	0	0	0	0	0	0	0	0	0	0	1
4	0	0	0	0	0	0	0	1	1	1	1
5	0	0	0	0	0	0	1	1	1	1	1
6	0	0	0	0	0	1	1	1	1	1	2
7	0	0	0	0	1	1	1	1	1	1	2
8	0	0	0	1	1	1	1	2	2	2	2
9	0	0	0	1	1	1	1	2	2	2	3
10	0	0	0	1	1	1	2	2	2	2	3
11	0	0	1	1	1	1	2	2	2	3	3
12	0	0	1	1	1	2	2	3	3	3	4
13	0	0	1	1	1	2	2	3	3	3	4
14	0	0	1	1	2	2	2	3	3	4	4
15	0	0	1	1	2	2	3	3	3	4	5
16	0	1	1	2	2	2	3	4	4	4	5
17	0	1	1	2	2	3	3	4	4	5	5
18	0	1	1	2	2	3	3	4	4	5	6
19	0	1	1	2	2	3	3	4	4	5	6
20	0	1	1	2	3	3	4	5	5	6	6
21	0	1	1	2	3	3	4	5	5	6	7
22	0	1	2	2	3	4	4	5	5	6	7
23	0	1	2	2	3	4	4	5	6	7	7
24	0	1	2	3	3	4	5	6	6	7	8
25	0	1	2	3	3	4	5	6	6	7	8
26	0	1	2	3	4	4	5	6	7	8	8
27	0	1	2	3	4	5	5	6	7	8	9
28	0	1	2	3	4	5	6	7	7	8	9
29	0	1	2	3	4	5	6	7	8	9	9
30	0	1	2	3	4	5	6	7	8	9	10
31	0	1	2	3	4	5	6	7	8	9	10

Table D.9: This table lists which channel is connected to which serial link when the specified number of links is selected. In case the channel ordering is in use, then the list position can be substituted for the channel.

$$baseline = \frac{sum - old_val + new_val}{filterlength} \tag{D.1}$$

Register name	Address	Type	Default		Description
NBCFG	0x0F	RW	0x40	[7:0]	Neighbor configuration settings
		RW	0x00	[5:0]	Neighbor input delay, ~0.2ns/bit for a total of ~12.5ns
		RW	0x01	[7:6]	Number of neighbors
SOCFG(V2)	0x12	RW	0x14		Serial link configuration
SOCFG(V3)	0x12	RW	0x34		Serial link configuration
		RW	0x04	[3:0]	Number of serial out, 0-11
		RW	0x01	[4]	Disable internal termination of input differential links
		RW	0x01	[5]	Enable NBflowstop_in pin
SODRVST	0x13	RW	0x55		Serial link drive strength configuration, see Table D.5
		RW	0x01	[1:0]	Drive strength of serial out 4-0
		RW	0x01	[3:2]	Drive strength of neighbor flow stop out/serial out 5
		RW	0x01	[5:4]	Drive strength of serial out 6,8,10
		RW	0x01	[7:6]	Drive strength of serial out 7,9

Table D.10: Serial link driver and receiver registers

Register name	Address	Type	Default	Description	
K1	0x00	RW	0x000	[12:0]	First pole of the TCFU
K2	0x01	RW	0x000	[12:0]	Second pole of the TCFU
K3	0x02	RW	0x000	[12:0]	Third pole of the TCFU
K4	0x03	RW	0x000	[12:0]	Fourth pole of the TCFU
L1	0x04	RW	0x000	[12:0]	First zero of the TCFU
L2	0x05	RW	0x000	[12:0]	Second zero of the TCFU
L3	0x06	RW	0x000	[12:0]	Third zero of the TCFU
L4	0x07	RW	0x000	[12:0]	Fourth zero of the TCFU
L30	0x08	RW	0x000	[12:0]	TCFU IIR SOS first zero(L3) gain
ZSTHR	0x09	RW	0x000	[11:0]	Zero suppression threshold
ZSOFF	0x0A	RW	0x000	[12:0]	Offset added before truncation
ZSCFG	0x0B	RW	0x000		Zero suppression configuration
		RW	0x000	[1:0]	Glitch filter, min. accepted pulse, all, >1, >2, >2
		RW	0x000	[4:2]	Post-samples
		RW	0x000	[6:5]	Pre-samples
		RW	0x000	[7]	Change position of BC3 in pipeline (BC3 after BC2)
		RW	0x000	[8]	Enable Raw data output of ZSU
FPD	0x0C	RW	0x000	[12:0]	BC1 Fixed pedestal (offset subtracted)
VPD	0x0D	R	0x000	[12:0]	BC1 variable pedestal, 2's compliment
BC2BSL	0x0E	R	0x000	[12:0]	BC2 Computed Baseline, 2's compliment
BC3BSL	0x0F	R	0x000	[12:0]	BC3 Computed Baseline, 2's compliment
PMDATA	0x10	RW	0x000	[9:0]	Data to be stored or read from the pedestal memory
BC2LTHRREL	0x11	RW	0x003	[9:0]	BC2 lower relative threshold
BC2HTHRREL	0x12	RW	0x003	[9:0]	BC2 higher relative threshold
BC2LTHRBSL	0x13	RW	0x400	[10:0]	BC2 lower saturation level for baseline
BC2HTHRBSL	0x14	RW	0x3FF	[10:0]	BC2 higher saturation level for baseline
BC2CFG	0x15	RW	0x000		BC2 configuration
		RW	0x000	[1:0]	No. of taps in moving average filter
		RW	0x000	[3:2]	BC2 pre-samples
		RW	0x000	[7:4]	BC2 post-samples
		RW	0x000	[8]	BC2 glitch removal
		RW	0x000	[10:9]	Auto reset configuration
BC2RSTVAL	0x16	RW	0x032	[7:0]	Reset value for maf baseline when auto reset is enabled
BC2RSTCNT	0x17	RW	0x0FF	[7:0]	No. of samples outside of thresholds before resetting maf filter (divided by 4)
DPCFG	0x18	RW	0x000		Data path configuration
		RW	0x000	[3:0]	BC1 mode, see D.12
		RW	0x000	[4]	BC1 data input polarity
		RW	0x000	[5]	BC1 pedestal memory polarity
		RW	0x000	[6]	BC1 pedestal memory record from input
		RW	0x000	[7]	TCFU enabled
		RW	0x000	[8]	BC2 maf enable
		RW	0x000	[9]	BC3 filter enable
		RW	0x000	[10]	TCFU SOS Architecture enable
		RW	0x000	[11]	TCFU signed Pole/Zero enable
BC1THRL	0x19	RW	0x7FD	[10:0]	Lower threshold of variable pedestal filter
BC1THRH	0x1A	RW	0x003	[10:0]	Higher threshold of variable pedestal filter
BC1CFG	0x1B	RW	0x114		BC1 configuration
		RW	0x004	[3:0]	No. of taps in variable pedestal filter
		RW	0x001	[4]	Define open threshold time of 31(high)/15(low) samples after (auto)reset
		RW	0x000	[5]	Force enable IIR also inside time window
		RW	0x000	[6]	High if BC1THR should be considered absolute
		RW	0x002	[8:7]	Shift output data of pedestal memory
		RW	0x000	[9]	BC1 negative clipping enabled
BC1RSTCNT	0x1C	RW	0x000	[7:0]	No. of samples outside of thresholds before resetting vpd filter (divided by 4)
		RW	0x000		0 disables the auto reset
BC3SLD	0x1D	RW	0x020	[7:0]	Rate of the BC3 baseline down counter
BC3SLU	0x1E	RW	0x010	[7:0]	Rate of the BC3 baseline up counter

Table D.11: Channel specific registers

DPCFG[3:0]	Effect
0x0	din - FPD
0x1	din - f(t)
0x2	din - f(din)
0x3	din - f(din - VPD)
0x4	din - VPD - FPD
0x5	din - VPD - f(t)
0x6	din - VPD - f(din)
0x7	din - VPD - f(din - VPD)
0x8	f(din) - FPD
0x9	f(din - VPD) - FPD
0xA	f(t) - FPD
0xB	f(t) - f(t)
0xC	f(din) - f(din)
0xD	f(din - VPD) - f(din - VPD)
0xE	din - FPD
0xF	din - FPD

Table D.12: Operating modes of the first Baseline Correction. The lookup function f() is the pedestal memory with the argument as the address.

Pin	Name	Dir	Type	Function
B15	TME	I	LVCMOS (1.2 V)	Test mode enable (active high)
A17	sen[0]	I	LVCMOS (1.2 V)	Scan chain enable for chain 0 (active high)
AA14	sen[1]	I	LVCMOS (1.2 V)	Scan chain enable for chain 1 (active high)
A16	sen[2]	I	LVCMOS (1.2 V)	Scan chain enable for chain 2 (active high)
AB12	sen[3]	I	LVCMOS (1.2 V)	Scan chain enable for chain 3 (active high)
A14	sen[4]	I	LVCMOS (1.2 V)	Scan chain enable for chain 4 (active high)
B18	sdi[0]	I	LVCMOS (1.2 V)	Scan chain data in for chain 0
AB13	sdi[1]	I	LVCMOS (1.2 V)	Scan chain data in for chain 1
B17	sdi[2]	I	LVCMOS (1.2 V)	Scan chain data in for chain 2
AA13	sdi[3]	I	LVCMOS (1.2 V)	Scan chain data in for chain 3
B16	sdi[4]	I	LVCMOS (1.2 V)	Scan chain data in for chain 4
C22	sdo+[0]	O	SLVS	Scan chain data output for chain 0 p
C21	sdo-[0]	O	SLVS	Scan chain data output for chain 0 n
Y22	sdo+[1]	O	SLVS	Scan chain data output for chain 1 p
Y21	sdo-[1]	O	SLVS	Scan chain data output for chain 1 n
B22	sdo+[2]	O	SLVS	Scan chain data output for chain 2 p
B21	sdo-[2]	O	SLVS	Scan chain data output for chain 2 n
AB20	sdo+[3]	O	SLVS	Scan chain data output for chain 3 p
AA20	sdo-[3]	O	SLVS	Scan chain data output for chain 3 n
B20	sdo+[4]	O	SLVS	Scan chain data output for chain 4 p
A20	sdo-[4]	O	SLVS	Scan chain data output for chain 4 n

Table D.13: Scan chain test interface pins.

Pin	Name	Dir	Type	Function
AA12	sme	I	LVCMOS (1.2 V)	Memory test enable (active high)
AA15	smo	O	LVCMOS (1.2 V)	Latched memory test failure output (active low)
L19	serialOut+[0]	O	SLVS	Pulsed memory test failure output p (active high)
L18	serialOut-[0]	O	SLVS	Pulsed memory test failure output n (active high)

Table D.14: Memory Built In Self Tester interfaces pins.

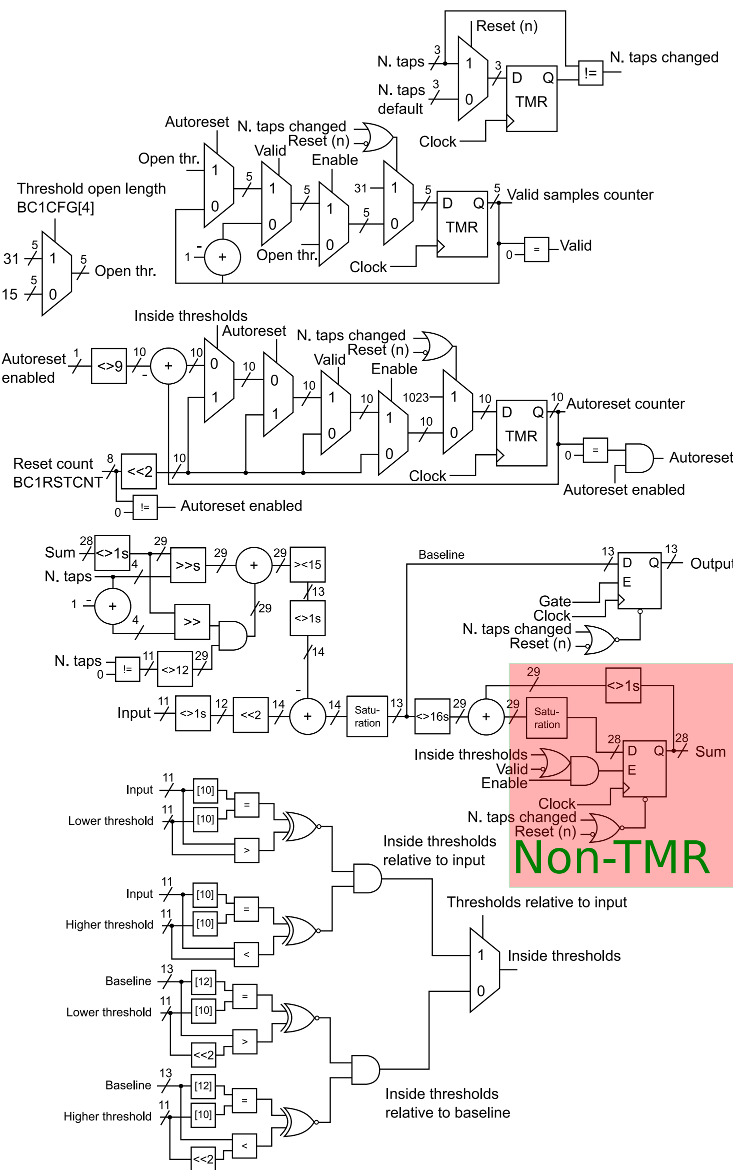


Figure D.4: Description of Variable pedestal IIR circuit.

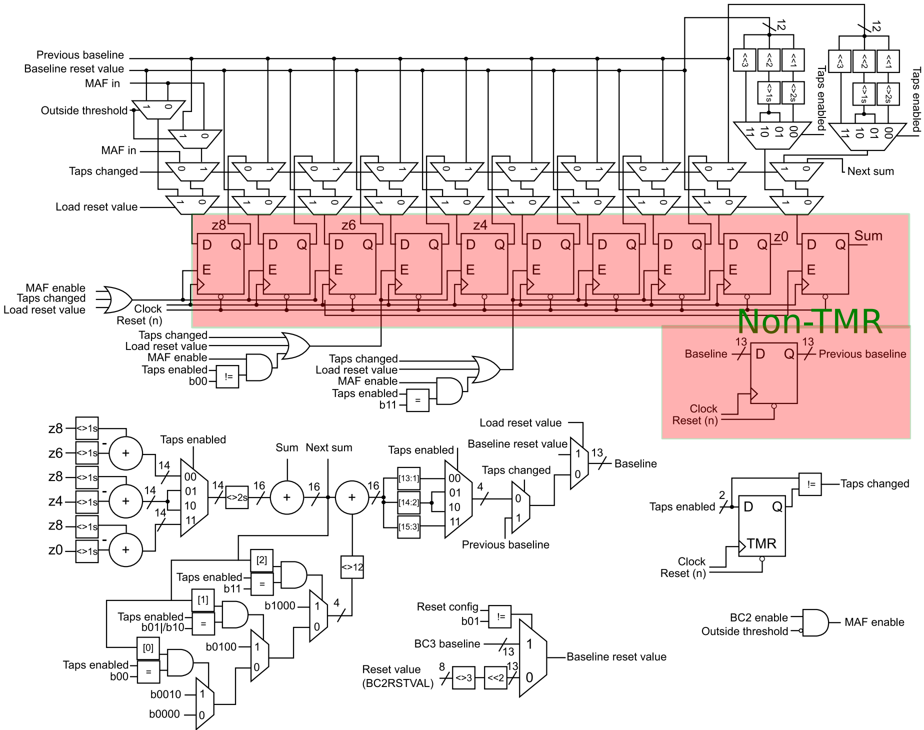


Figure D.5: Circuit description of Moving average BC II filter.

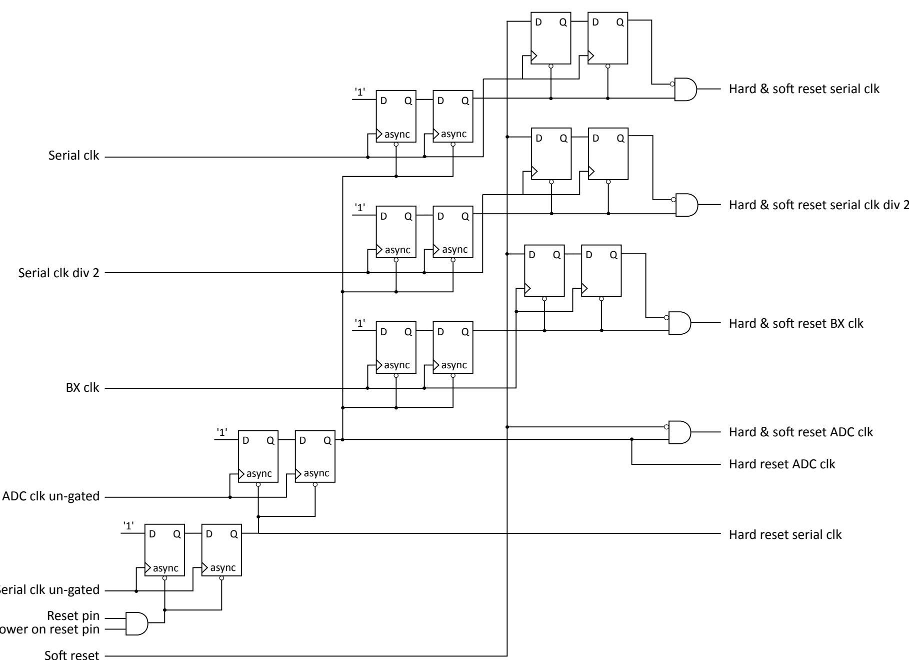


Figure D.6: Simplified block diagram of the SAMPA reset tree.

Appendix E

SAMPA setup and proton irradiation results

E.1 TPC components during RUN 3

Components	Total numbers
Readout pads	524160
SAMPA chips	16380
Output rate per SAMPA	1.6 Gbit/s
Front-End Cards	3276
Output rate per FEC	8 Gbit/s
GBTx chips	6552
GBT-SCA chips	3276
VTTx/VTRx	6552
Total number of optical fibers	14112
Common-Readout Units	360
FECs per CRU	10
Input rate per CRU	89.6 Gbit/s
Total input rate for CRUs	$\sim$ 30 Tbit/s

* The numbers are updated from the Technical Design Report [8].

Table E.1: Components and their bandwidths requirements for the TPC readout electronics during RUN 3 [8].

E.2 SAMPA DAQ firmware description

The DAQ firmware is divided into the following main parts [89, 101]:

1. Command and Control Module:
   The command and control unit enabled the slow control handling and the pin control for the SAMPA prototypes and was the main bridge between the user computer and the DUT. It also acted as control unit for other surrounding modules, which included a module for handling the slow control communication with the SAMPA for reading and writing the SAMPA I^2C registers, in addition to the modules for reset generation and event trigger handling. In the later prototypes, this module also supported specialized test features such as built-in memory tester for all the SRAM IPs and the

scan-chain for all the registers. These test features have been immensely useful during the irradiation campaigns.

2. Data Manager Module:
   The data manager synchronized and deserialized the data from each link into 10-bit words, verified the header parity and determined the total length of the followed payload. The deserialized packets were further segmented into 64-bit words to make the processing to 32/64 bit system more efficient. Furthermore, the packets were aggregated from all eleven de-serializers into four memory-writer modules via individual buffers where each memory-writer module was connected to a separate 64-bit 100 MHz bus that interfaces to a 400 MHz Double Data Rate (DDR) memory shared with the microprocessor.

   During continuous data acquisition, there was risk of payload drop due to memory overflow. In addition, there was also the possibility that the data would be sampled at the changeover point, resulting in invalid data [101]. Since both the beam time and the acquired data during the irradiation campaign are precious, the data was acquired with the triggered readout mode at a reasonable rate than the continuous mode to eliminate the risk of data loss or corrupt data.

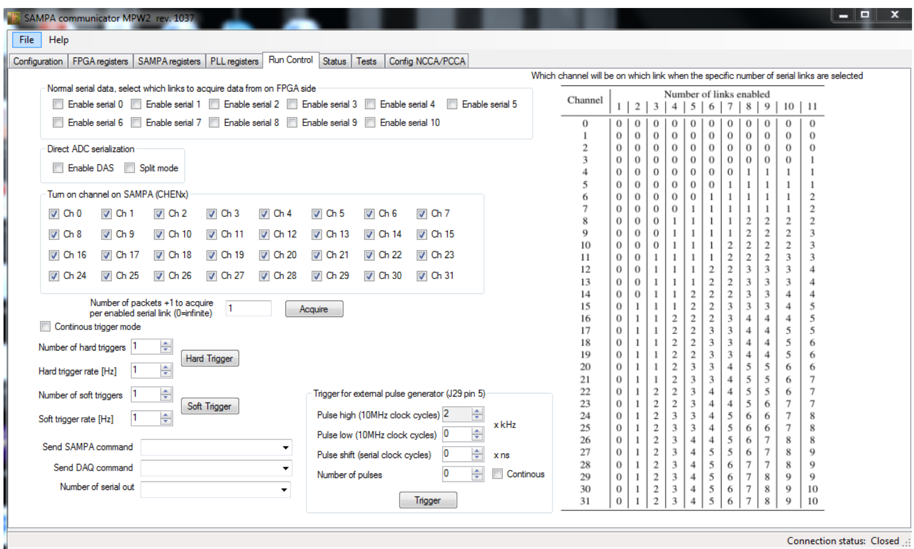
3. Clock Manager Module:
   The SAMPA chip required several clock domains. The user could configure either to provide all clock frequencies externally or derive the slower clock frequencies from a single fast clock source. The SoCKit board supported both options with the help of the clock manager unit, which contained a reconfigurable fractional Phase Locked Loop (PLL) on the SoCkit board, provided a system clock of 50 MHz. The PLL configured the sampling clock of the SoCKit board as well as provided the main clock to the SAMPA digital part, once the connection between the SoCKit board and the SAMPA carrier board was established.

   During the irradiation campaigns, the first option was considered since the final FECs for the SAMPA chips will derive all internal clock frequencies of the SAMPA chip from a single clock source. It is also worth mentioning that even though Campaign # 3 and 5 (see Table 2.4) were dedicated for SEL characterization of the SAMPA prototypes, the connection between the DAQ system and the SAMPA carrier boards was necessary to provide the appropriate clock and register configurations to the SAMPA chips. This was challenging during the Heavy-Ion campaigns since additional efforts were required to mount the DAQ board together with the SAMPA carrier boards and provide the appropriate communication interface to the DAQ board with the available feed-through connectors at the facility.

4. Data Server:
   By default, Data Server was the only executable C program running on the embedded Linux system of the microprocessor. It was responsible for

SAMPA serial link data transmission and TCP/IP (Transmission Control Protocol/Internet Protocol) connection control with the remote SAMPA Analyzer program running on the host computer in a server/client fashion. Since the data from the serial links was packet based with a payload and a header portion, it could be transmitted directly to the host computer using the TCP protocol with a maximum speed of 670 Mbps.

E.3 SAMPA commuicator and Analyzer



Channel	Number of links enabled 1	2	3	4	5	6	7	8	9	10	11
0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	0
2	0	0	0	0	0	0	0	0	0	0	0
3	0	0	0	0	0	0	0	0	0	0	1
4	0	0	0	0	0	0	0	1	1	1	1
5	0	0	0	0	0	0	1	1	1	1	1
6	0	0	0	0	0	1	1	1	1	1	2
7	0	0	0	0	1	1	1	1	1	1	2
8	0	0	0	1	1	1	1	2	2	2	2
9	0	0	0	1	1	1	1	2	2	2	3
10	0	0	0	1	1	1	2	2	2	2	3
11	0	0	1	1	1	1	2	2	2	3	3
12	0	0	1	1	1	2	2	3	3	3	4
13	0	0	1	1	1	2	2	3	3	3	4
14	0	0	1	1	2	2	2	3	3	4	4
15	0	1	1	1	2	2	3	3	3	4	5
16	0	1	1	2	2	2	3	4	4	4	5
17	0	1	1	2	2	3	3	4	4	5	5
18	0	1	1	2	2	3	3	4	4	5	6
19	0	1	1	2	2	3	3	4	4	5	6
20	0	1	1	2	3	3	4	5	5	6	6
21	0	1	1	2	3	3	4	5	5	6	7
22	0	1	2	2	3	4	4	5	5	6	7
23	0	1	2	2	3	4	4	5	6	7	7
24	0	1	2	3	3	4	5	6	6	7	8
25	0	1	2	3	3	4	5	6	6	7	8
26	0	1	2	3	4	4	5	6	7	8	8
27	0	1	2	3	4	5	5	6	7	8	9
28	0	1	2	3	4	5	6	7	7	8	9
29	0	1	2	3	4	5	6	7	8	9	9
30	0	1	2	3	4	5	6	7	8	9	10
31	0	1	2	3	4	5	6	7	8	9	10

Figure E.1: SAMPA communicator GUI showing the functions in Run Control tab.

E.4 SAMP MPW1: Chip_1 and Chip_2

Chip_1

Chip_1 is the top left mini chip presented in Figure 5.1 with an approximate area of 2x3 mm^2, encapsulated in a CQFP64 package. It was an analog chip containing five channels of the front-end block including charge sensitive amplifier and two stages shapers. The main objective of this chip was to characterize the performance of the analog front-end block, such as the sensitivity, linearity, noise and cross-talk. The normal testing of the chip was executed by injecting a charge on the input with a pulse generator, and measure the differential output voltages with an oscilloscope.

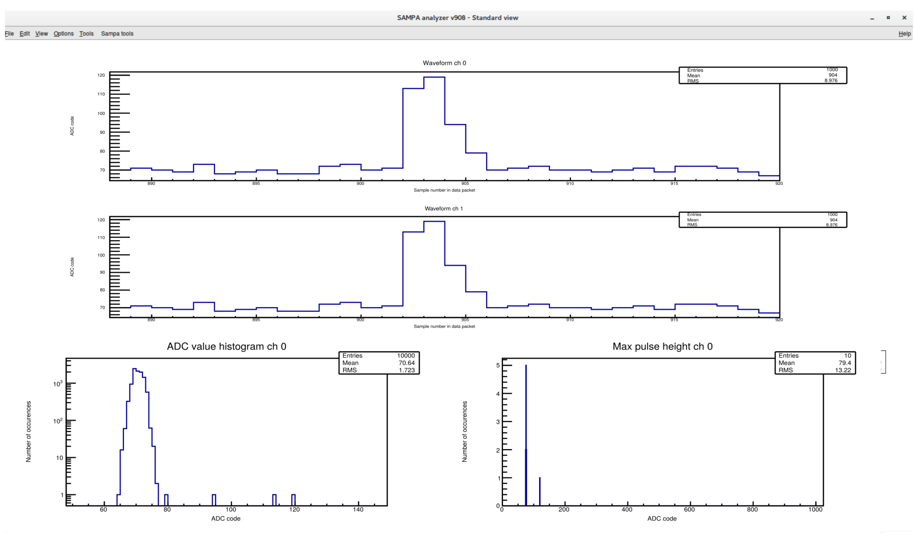


Figure E.2: The main screen of the SAMPA Analyzer program.

Chip_2

The second mini-chip Chip_2 is presented in the top right side i Figure 5.1. It occupied an area of ≈ 2x2 mm^2 and was binded in a JLCC 44p package. It consists of a 10-bit fully differential SAR ADC. In addition, a custom made SLVS driver (Scalable Low Voltage Signaling) was implemented on the same chip. The SLVS driver consists of both the transmitter and a receiver block. The purpose for implementing a stand-alone ADC was to characterize both the static (Differential and Integral Non-Linearity (DNL,INL)) and dynamic (Effective Number Of Bits (ENOB), Signal to Noise Ratio (SNR) and Spurious-Free Dynamic Range (SFDR)) performance of the chip without the impact of any external source of error.

E.5 Scan chain feature in digital design

A typical architecture of the scan chain is illustrated in Figure E.3 where standard flip-flops are typically substituted by the SC flip-flops, and an additional multiplexer is inserted at the input of every flip-flop. One input of the multiplexer acts as a functional input D, while other being scan chain data sdi. The selection between D and sdi is controlled by scan chain enable signal sen. Scan chain flip-flops usually operate in two modes. In normal mode, the flip-flops behave as expected where the output Q is connected to combinatorial logic. By enabling the sen signal, all the flip-flops are cascaded in a chain, forming a long shift register spanning over entire chip.

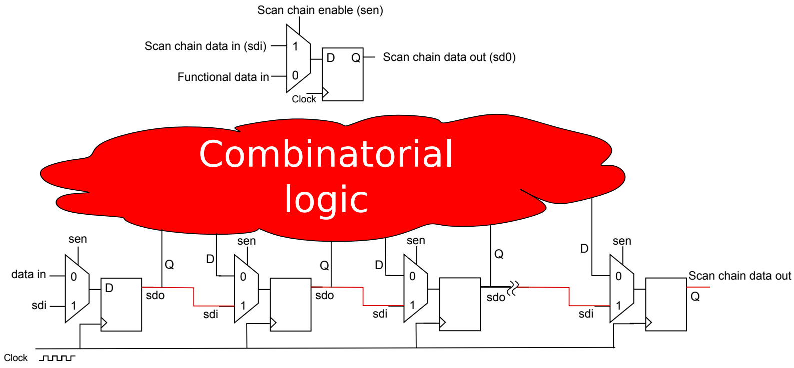


Figure E.3: A typical scan chain flow.

E.6 Shift register scan chain test results from B_2 sample

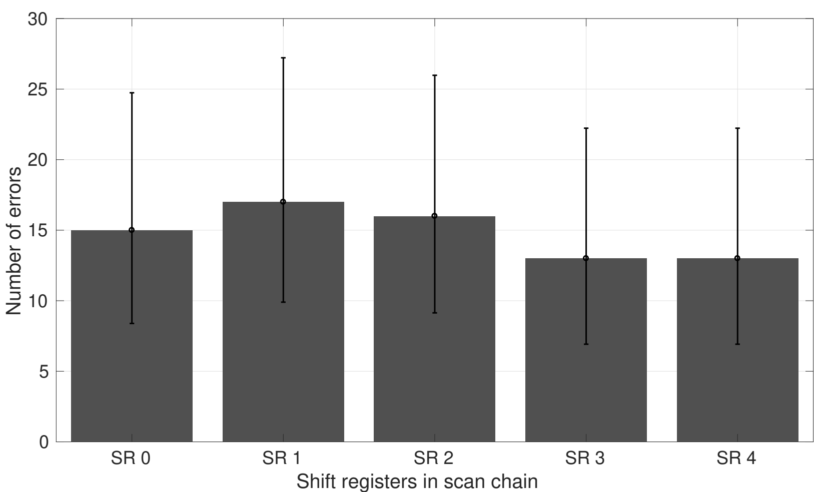


Figure E.4: Scan chain test results from run 15 (B_2 sample).

E.7 SAMPA baseline level calculation

In the absence of front-end input signals, the analog front-end block generates DC (baseline) level at the output of every channel, which further samples into digital core after digitization. From post-layout simulation results, the typical baseline level lies around 100 mV which corresponds to 47 ADC counts, calculated

by formula in Equation E.1.

$$voltage = \frac{2 \times ADC_{ref} \times ADC\ value}{2^n} \tag{E.1}$$

ADC_{ref} is 1.1 V reference voltage of the ADC. It is multiplied by 2 since the ADC is differential, and n are number of bits in ADC which is 10bits for SAMPA SAR ADC. 1 ADC count (Least Significant Bit) corresponds to 2.14 mV. The baseline values differ between the channels due to analog front-end offset, ADC offset, mismatch and process variations.

E.8 Test script for SAMPA slow control interface

Two different test scripts using the C executable programs were developed to monitor slow control registers (./ mon_on_all_reg) and (./single_run) where the later script was used to select one of the single tests from the command line. For example, only reading baseline values from BC2 and BC3 registers, monitoring the frequency of the shift registers, writing and reading pedestal memory from a specific channel. All the outputs was saved in different files with time stamp.

The first script called several functions sequentially from the main program. In the start of the program, the user needed to provide the parameters for the pedestal memory data through the command line where the broadcast option was to select all channels. If broadcast was 0, then the user needed to the second *channel* parameter to specify the channel to which the data pattern should be written to pedestal memory.

```
"Please give the PEDMEM pattern : broadcast channel write pattern : "
```

Further if the *write* is 0, then the pedestal data will only be read back. The last parameter is *pattern* for the pedestal memories. There were in total seven pattern options from the command line.

1. PATTERN_IN: a ramp up pattern (0,1,2,....,1023) to fill all addresses between 0 to 1023.
2. PATTERN_DEC: a ramp down pattern (1023,1022,1021,.....1,0) to fill all addresses between 0 to 1023.
3. PATTERN_155 : a checker board pattern (0,1,0,1........0,1) on all addresses.
4. PATTERN_2AA : an inverse checker board pattern (1,0,1,0,........,1,0) on all addresses.
5. PATTERN_00 : only static "0s" on all addresses.
6. PATTERN_0F0 : an alternating pattern of "0s" and "1s" on all addresses.
7. PATTERN_FFF : only static "1s" on all addresses.
8. PATTERN_F0F : an alternating pattern of "1s" and "0s" on all addresses.

A screenshot of the log output from the terminal window is presented below where both single and multiple bit-flips for each channel and address are captured and printed by the test script.

3/29 5:6:35;129; Single bit flip on channel;6;addr;448;Read;325;Expected;341;XOR;16

3/29 5:16:15;245; Multiple bit flip on channel;18;on addr;837;Read;61680;Expected;341;XOR;61861

E.9 TID results from BC2BSL and BC3BSL registers

The results from the BC2BSL and BC3BSL slow control registers can be distinguished with respect to both TID and soft error effects. The baseline values which are acquired through both registers are presented in Figure E.5 for each channel individually . The baseline level for each channel is plotted and compared before and after accumulating TID of 30.4 KRad and 34 KRad, for B_18 and B_11 sample respectively.

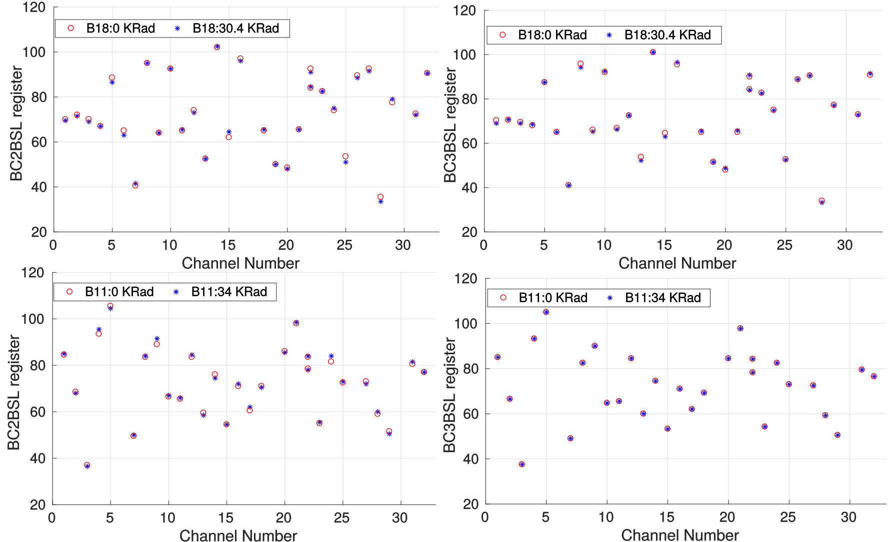


Figure E.5: Baseline variations for B_18 and B_11 sample due to deposited proton dose.

Between the channels, the baseline variations were expected due to the process and mismatch which can be also be observed from the plot. However, no fluctuations are observered between the baseline values for the corresponding channels after the dose deposited by the protons. This concludes that the analog front-end is robust against the TID effects upto several KRads without degrading the performance.

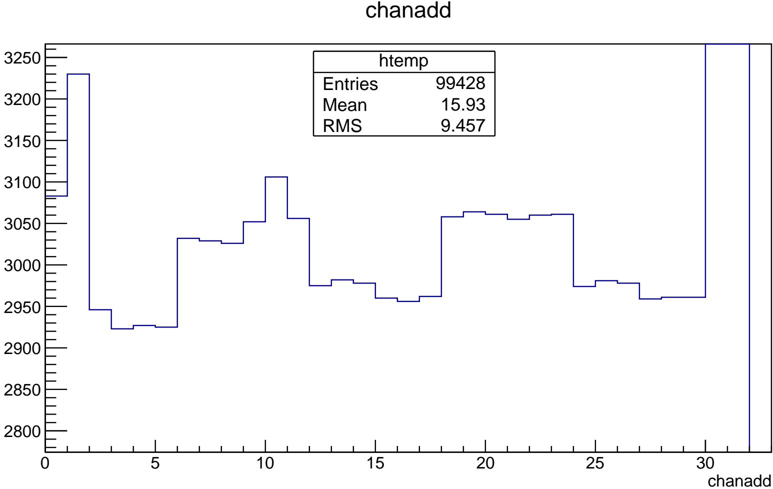
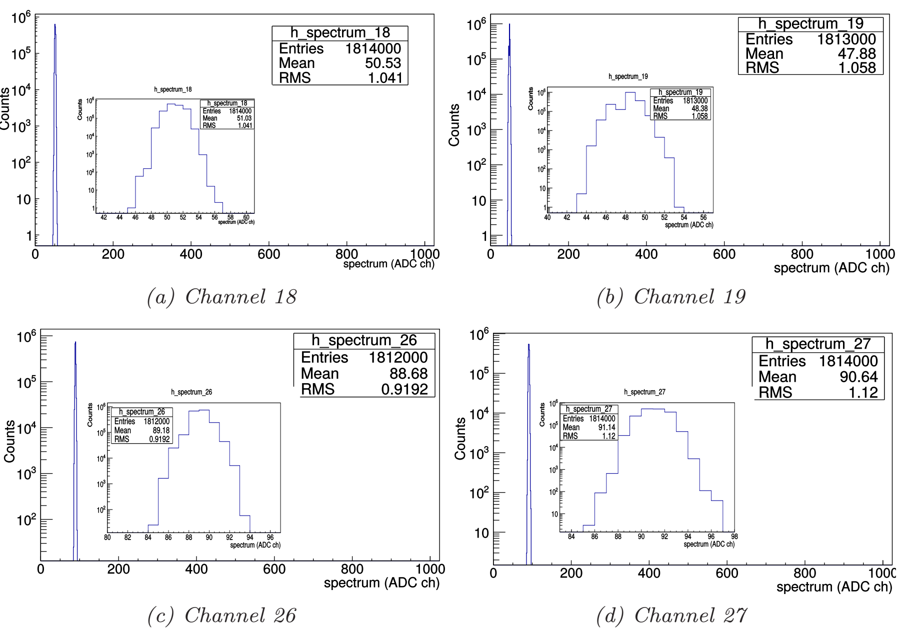


Figure E.6: Distribution of packets per channel during normal lab testing.



(a) Channel 18

(b) Channel 19

(c) Channel 26

(d) Channel 27

Figure E.7: Distribution of baseline spectrum on selective channels without beam in normal mode.

E.10 Results from SAMPA serial link data without beam

SAMPA Direct ADC Serialization (DAS) mode operates with a serialization speed of 32 × the ADC sampling speed where the output bits from 32 ADCs are transmitted. For example, the 10-bit data for channel 0 will be put on the serial link 9-0 in the first cycle, and in the consecutive cycle, the data from channel 1 will be transferred via serial links, and so on.

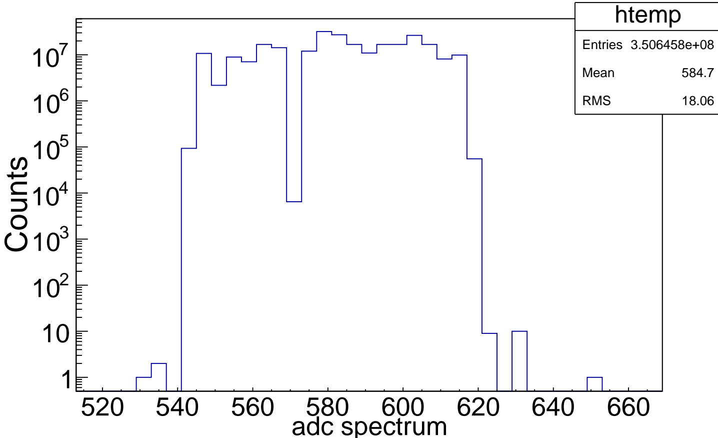


Figure E.8: Distribution of samples acquired from all SAMPA channels during run 7 KVI campaign.

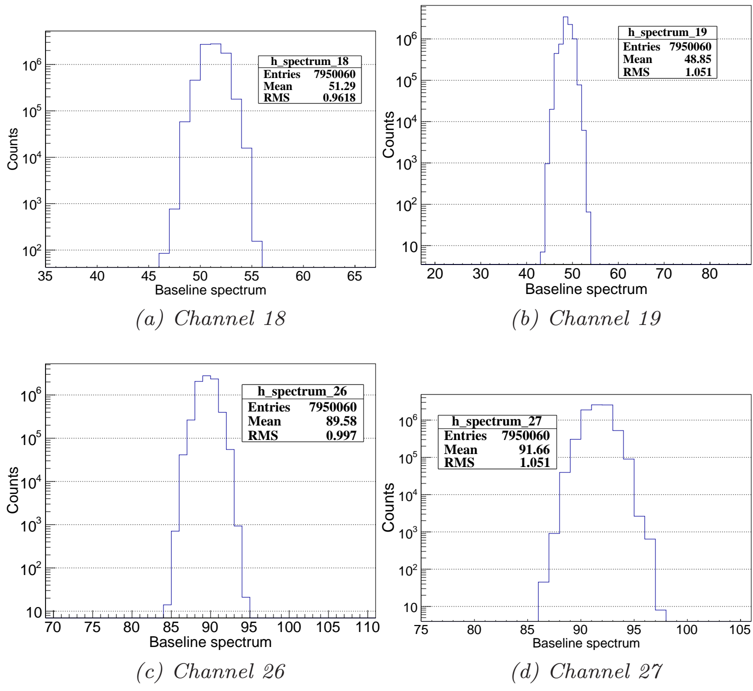
The samples in Figure E.8 shows a wider spectrum of adc values as expected due to process variations in the baseline values for each channel. Additionally, the adc values are within a spectrum range between 540 and 630 due to the fact that MSB of the SAMPA ADC in V2 prototype was inverted.

The SAMPA analyzer did not decode the data on the receiving end and dumped the incoming data packets as they arrive (ch0, sample 0, ch1 sample 0,.....ch31 sample 0, ch1 sample 1, ch2 sample 1, and so on). In order to examine the behavior from each channel individually, decoding is performed on the acquired root file where the samples were rearranged with respective channels.

E.11 Additional soft error results for Pedestal memories data from serial links

E.12 Shunt resistor values for SAMPA SEL setup

Table E.3 represented the expected voltage drop with respect to different shunt resistor values for the typical current consumption level of the SAMPA digital power domain. The table concludes that using a shunt resistor of 1Ω value is undesirable for the SAMPA SEL setup since the voltage drop exceeds the



(a) Channel 18 *(b) Channel 19*

(c) Channel 26 *(d) Channel 27*

Figure E.9: Distribution of baseline spectrum on selective channels without beam in TPC DAS mode.

INA226 device specifications of 160 mV. Depending upon the expected current consumption of the SAMPA power domains, the values of the shunt resistors were within the range of 50 mΩ to 100 mΩ.

E.13 MPW1 Single Event Latch-up results

During MPW1 campaign, current was continuously monitored and logged during the irradiated time. The current-time profile is presented in Figure E.11, where the log from all six runs is plotted together. Both plots provide identical information. The current and voltage data plotted in Figure E.11a is directly taken from HMP2020 power supply. In contrast, the data in Figure E.11b presents the buss voltages and current consumptions from each of the SAMPA MPW1 power domains, measured through the INA226 devices mounted on the current sensing board.

Both plots in Figure E.11 presents stable current and voltage data, demonstrating no signs of high current (SEL) events in five of the six runs. The current jumps during run 4 were due to an initial non-nominal operation setting, where adjustment of clock frequency parameter was forgotten.

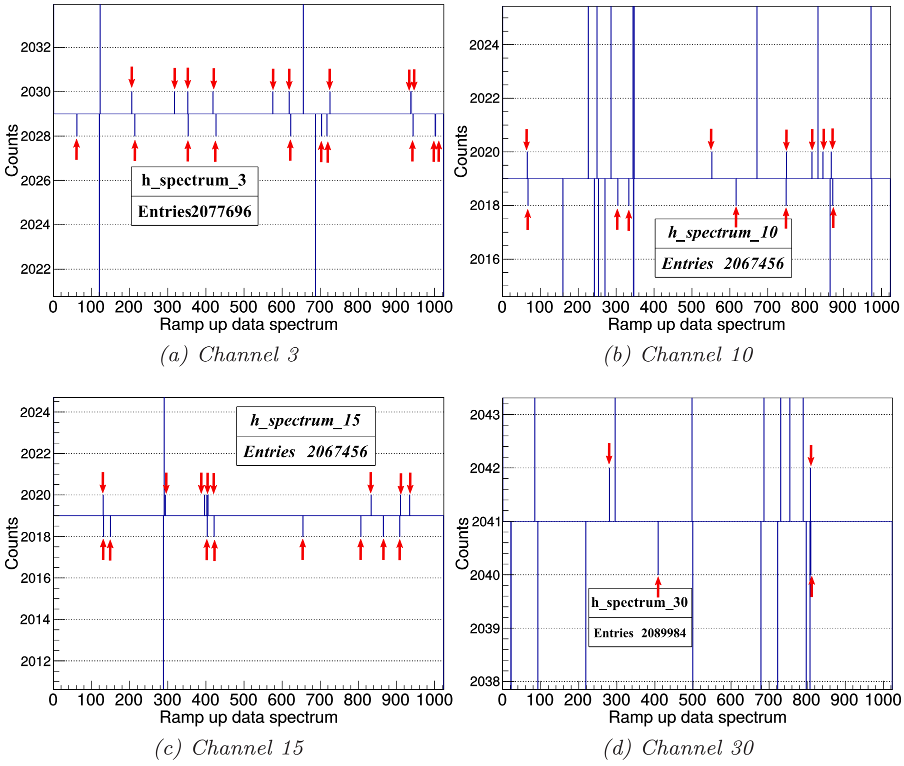
Decimal value	**Binary value**	**Comment**	**Acquired bins**	**Average bins**
162	0010100010	bit-flip on 5th LSB	2030	2029
178	0010110010	data memory	2028	
211	0011010011	bit-flip on 6th LSB	4029	2029
243	0011110011	pedestal memory	29	
281	0100011001	bit-flip on 3rd LSB	1530	2029
285	0100011101	pedestal memory	2528	
372	0101110100	bit-flip on 2nd LSB	13	2029
374	0101110110	pedestal memory	4045	
400	0110010000	bit-flip on 3rd LSB	2030	2029
404	0110010100	data memory	2028	
414	0110011110	bit-flip on 9th LSB	4058	2029
158	0010011110	pedestal memory	0	
649	1010001001	bit-flip on 5th LSB	2030	2029
665	1010011001	data memory	2028	
745	1011101001	bit-flip on 2nd LSB	2028	2029
747	1011101011	data memory	2030	
751	1011101111	bit-flip on 5th LSB	2028	2029
767	1011111111	data memory	2030	
776	1100001000	bit-flip on 10th LSB	2030	2029
264	0100001000	data memory	2028	
858	1101011010	bit-flip on 3rd LSB	30	2029
862	1101011110	pedestal memory	4028	
919	1110010111	bit-flip on 4th LSB	6	2029
927	1110011111	pedestal memory	4052	
940	1110101100	bit-flip on 1st LSB	2030	2029
941	1110101101	data memory	2028	
1018	1111111010	bit-flip on 8th LSB	1937	2029
890	1101111010	pedestal memory	2121	

Table E.2: Detailed analysis of soft errors on channel 24 during run 5.

Expected current (mA)	shunt resistor (mΩ)	Voltage drop (mV)
350	1000	350
350	100	35
350	50	17.5

Table E.3: Determining shunt resistor value for SAMPA digital Power domain.

Due to 1.2 V of identical supply voltage for both analog and digital power domains in MPW1 prototype, $V_{digital}$ and V_{analog} data points are ovelapping in Figure E.11b. The plots also indicate no significant performance degradation on the power supply lines with respect to TID effect of 12 kRad.



(a) Channel 3

(b) Channel 10

(c) Channel 15

(d) Channel 30

Figure E.10: Ramp up data spectrum for selective channels during run 5.

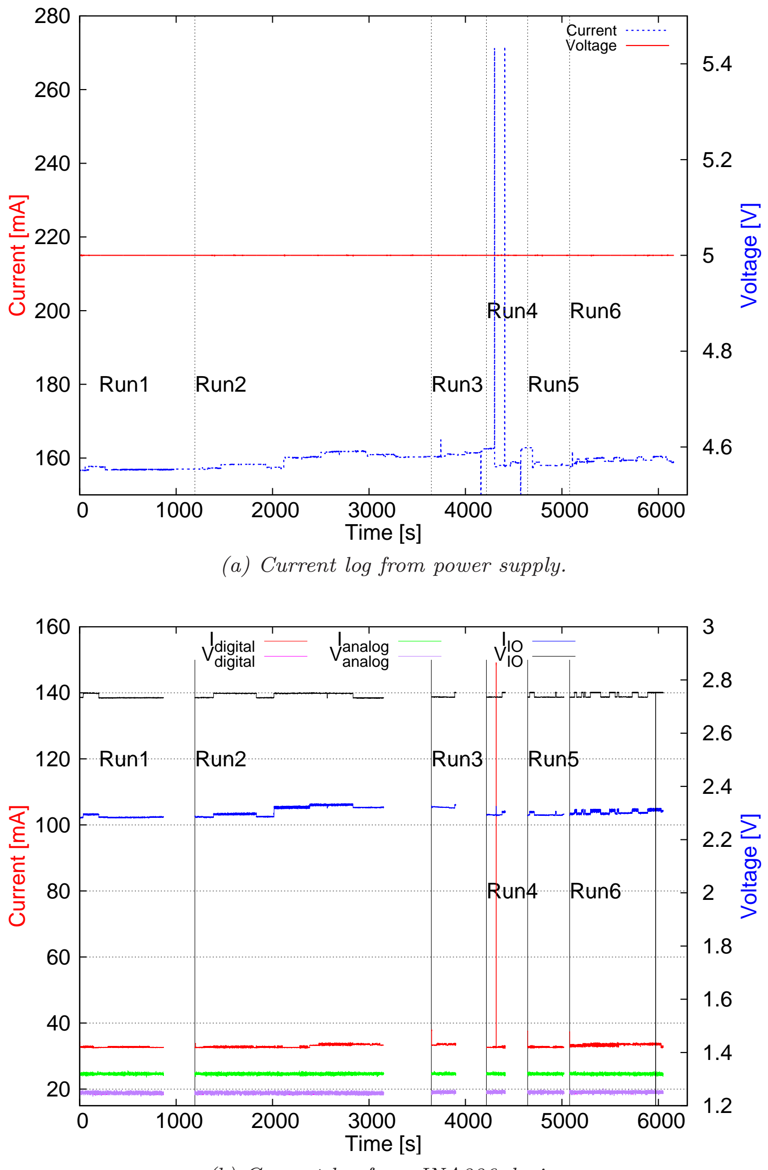
E.14 Proton induced SEL events in V2 prototype

Figure E.12 presents the accumulated SEL events from one of the irradiated samples of V2 prototype.

An example is presented is Figure E.13 where the scan chain test was initiated to determine σ_{SEU} for flip-flops.

The subplots on the left present the current profile and the accumulated soft errors from each shift register during the test. Three current jump events were observed during the irradiated time of 800 s. Although first current jump event appeared around 100 s and the amplitude of the current was rapidly increased to 500 mA, it was decided to continue the test without power cycling the SAMPA chip in order to evaluate the impact of SEL event on the collected errors. The current remained stable for 600 s in the high current state, until a new current jump event appeared and the current raised up to 760 mA. Finally, a new current jump event occurred at 780 s which raises the current up to 960 mA. At this stage, the initiated test was stopped and the device was power cycled.

The top-left plot presents the acquired soft errors from individual shift registers which demonstrates a linear dependence between the irradiated time,



(a) *Current log from power supply.*

(b) *Current log from INA226 devices.*

Figure E.11: Current waveform during SAMPA MPW1 irradiation campaign at TSL. The current jumps during run 4 is due to an initial non-nominal operation setting, where the clock frequency parameter is not optimized.

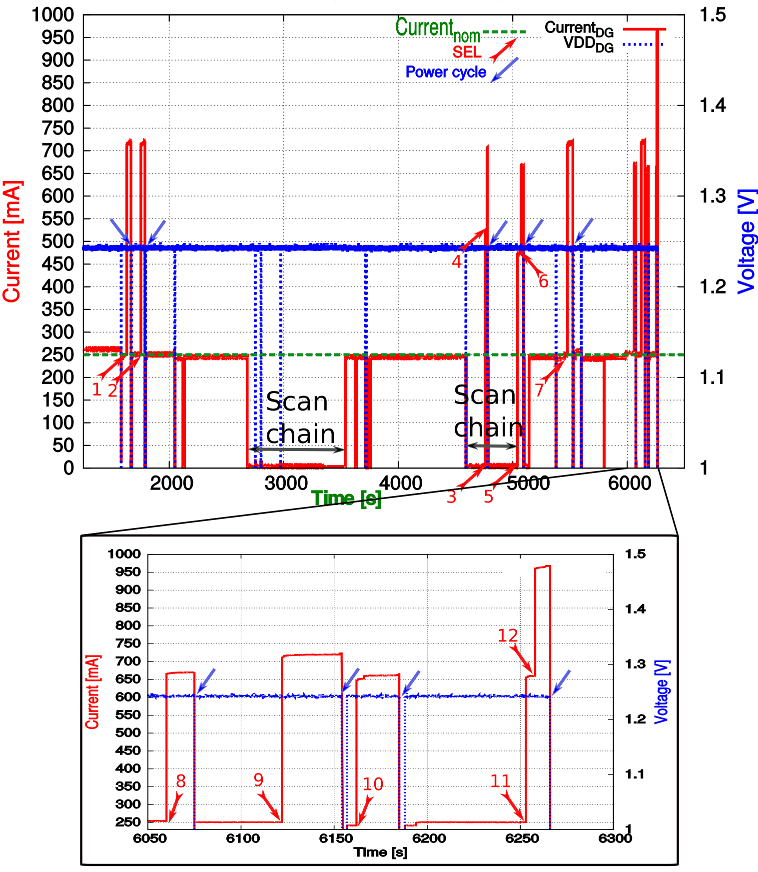


Figure E.12: Current waveform acquired during proton irradiation of B_11 sample (V2 prototype).

and the number of errors collected from the shift registers.

This provided the first indication, that SEL events potentially effect specific region inside the digital domain, without having any impact on the soft error rate for the flip flops. Since the DUT was fully operational after power cycling, this also indicated that the observed SEL events can be left uncorrected for some fraction of time (around 700 s in this example), without any severe destructive consequences on the chip.

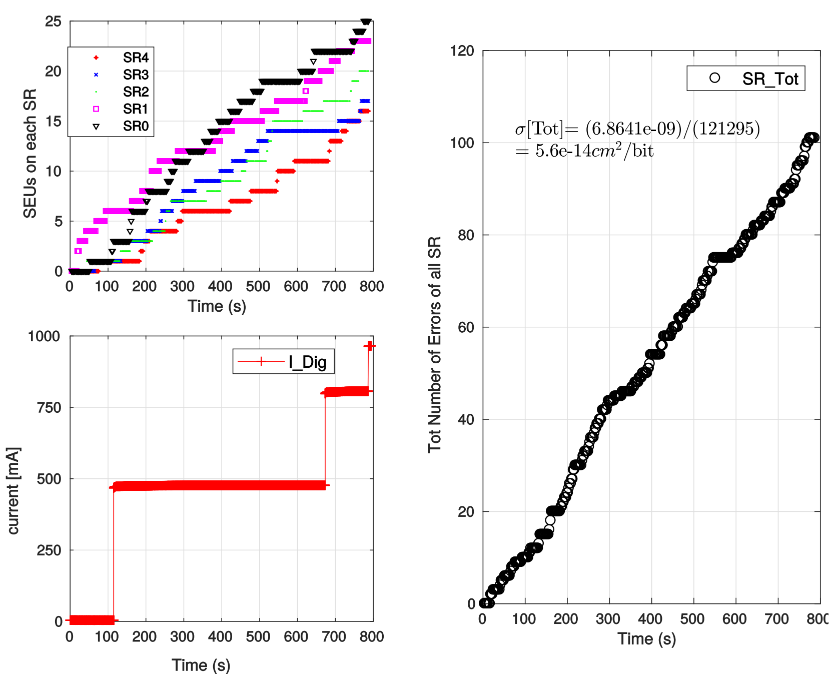


Figure E.13: SEL event during scan chain test in run 3.

Appendix F

SAMPA setup and results for Heavy-Ion campaign

F.1 Connectors available at UCL facility

HIF Feed through Connectors

Here is below the list of the flanges available with their feed through connectors. The irradiation chamber can support 2 large flanges and 5 small flanges according to the users' requirements.

Large Flange:

- 10x BNC (F/F)
- 10x BNC (Ground isolated) (F/F)
- 10x SMA (Ground isolated) (F/F)
- 6x Sub D 25 (Cannot be dismounted) (M outside/F inside)

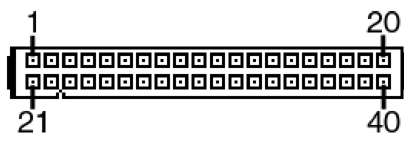
Small Flange:

- 8x BNC + 2x SHV (F/F)
- 9x BNC (F/F)
- 7x BNC (Ground isolated) (F/F)
- 2x USB (M/M)
- 10x SMA (F/F)
- 2x Sub D 25 (M/F)
- 2x HE 10 40 pin (M/M)
- 2x H80A2CO 40 (M/M)**
- Water cooling 4-6mm hose with rack connectors input/output + Thermocouple connector

Transition available on special request:

- Sub-D25 transition to Ethernet (M/Eth, F/Eth)
- USB transition Type A to Type A (F/F)
- USB transition Type A to Type B (F/F)

** Warning the connection pin to pin is inverted on the flange



IDC40
(on Cable)

First connector (upwards on the flange)

OUTSIDE	INSIDE
1	20
2	19
3	18
4	17
5	16
,,,	,,,
20	1

OUTSIDE	INSIDE
21	40
22	39
23	38
24	37
25	36
,,,	,,,
40	21

Second connector (downwards on the flange)

OUTSIDE	INSIDE
1	21
2	22
3	23
4	24
5	25
,,,	,,,
20	40

OUTSIDE	INSIDE
21	1
22	2
23	3
24	4
25	5
,,,	,,,
40	20

Cables for HI SAMPA – UCL 230517

- Internal vacuum chamber barrel dimension: Height 71 cm, width 54 cm, depth 76 cm
- Cable lengths inside chamber : 1m
- Cable lengths outside chamber : 2 m
- 2 power supples to SAMPA : 1.7V and 5 V

  Isolated bnc : 2 bnc connections for 4 wires :

  2 PCB power connector -> 2 bnc connector isolated. 1m
  2 bnc connector (isolated) -> 4 banana cables for power supply. 2 m

  Non-isolated bnc : 4 bnc connections for 4 wires inside chamber:

  PCB power connector -> 4 bnc connector 1m
  4 bnc connector -> 4 banana cables for power supply. 2 m
- Shunt voltage monitoring
  - 3 senses resistors -> 6 cables + 1 gnd
  - Isolated bnc : 3 bnc connections for 6 wires + 1 connection for gnd
    - 3 (+1) Current sensing pin (7 wires) -> 3 (+1) bnc connector isolated. 1m
    - 3 (+1) bnc connector (isolated) -> 6 (+1) wires to ina card. 2m
  - Non-isolated bnc : 7 bnc connections for 7 wires
    - 3 (+1) Current sensing pin (7 wires) -> 7 bnc connector . 1m
    - 7 bnc connector (isolated) -> 7 wires to ina card. 2m
  - 7 wires on Sub D-25 connector
    - 7 wires to D-25 . 1m
    - D-25 to INA card. 2m
- USB cable
  - 2 usb cable (FPGA(Communicator) + PI (Power supply))
    - 1 chamber to FPGA, 1 chamber to Pi . 1m
    - 2 chamber to PC (normal usb). 2m
- Ethernet cable
  - 2 ethernet cable (FPGA + PI)
    - 2 Sub-D25 transition to ethernet. 1 chamber to FPGA, 1 chamber to Pi . 1m
    - 2 ethernet cable chamber to PC . 2m
- Power supply for FPGA
  - 1
    - 12 V DC to bnc. 1m
    - Bnc to powersocket. 2m

F.2 Preparation of the collimators

The dimensions and coordinates for the openings of the collimators were designed after careful and detailed inspection of the physical layout for both the SAMPA V2 prototype and the carrier board, where the bottom left side of the carrier board was considered as the origin of the coordinates. Then the bottom left coordinates were measured where the naked V2 prototype was mounted on the carrier board, as presented in Figure 6.13. From those coordinates, the positions for the actual openings were determined.

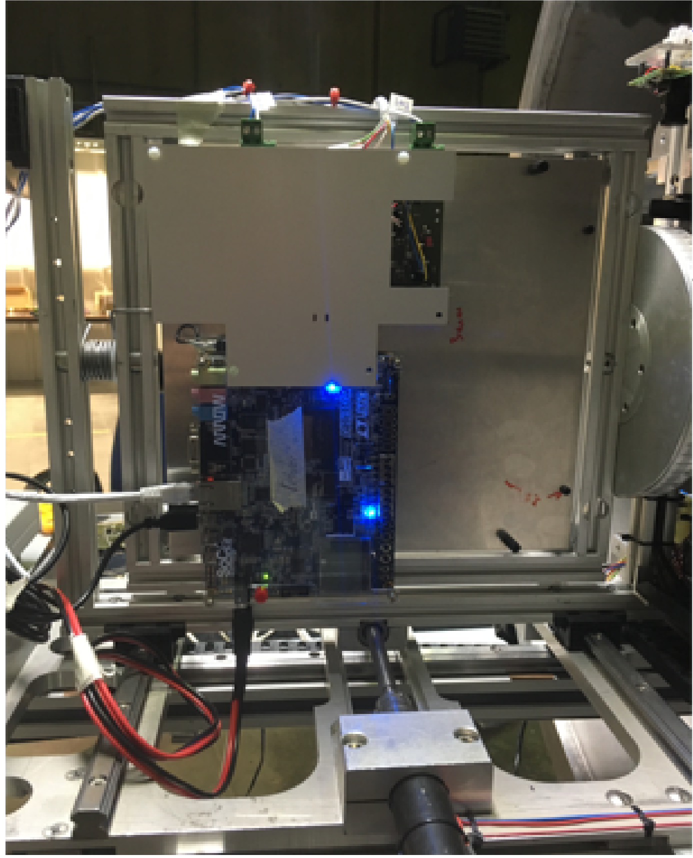
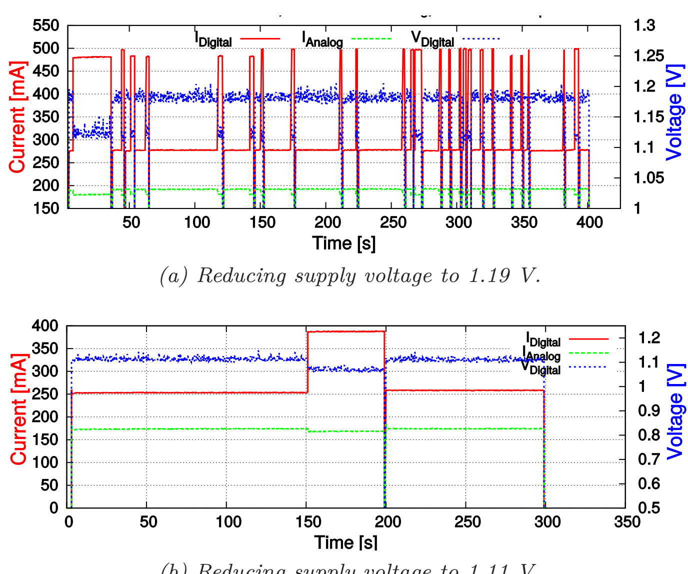


Figure F.1: Dual port collimator mounted on top of the SAMPA V2 carrier board during Heavy-Ion campaign.

As observed in Figure 6.13, there was space for composing wider openings in the collimators, to cover most of the area regions within different SRAM IPs. However, in order to ensure that the ions strike either dual or single port SRAM IPs at a single time, distance margins were considered.

F.3 Impact of supply voltage on SEL events

The current waveform plots presented in Figure 6.14 demonstrated that the SEL events were detected on the single port memory regions in the SAMPA V2 prototype by using the single collimator. Further, the sensitivity of the SEL events was evaluated with the reduction of supply voltage V_{DD}, by irradiating the SAMPA V2 prototype with single collimator, with the ion of LET 10 MeV cm^2/mg. The current consumption was monitored , and the the current time profile is plotted in Figure F.2.



(a) Reducing supply voltage to 1.19 V.

(b) Reducing supply voltage to 1.11 V.

Figure F.2: SEL sensitivity with the reduction of supply voltage at LET value of 10 MeV cm^2/mg, with single collimator.

By comparing the current waveform plots in Figure 6.14a, F.2a and F.2b, a significant reduction has been observed in the occurrence of SEL events by lowering the supply voltages, from 1.25 V, down to 1.19 V and 1.11 V. In fact, at supply voltage of 1.11 V, only one single SEL event was detected, with the exposure time of 300 s.

F.4 Confirming the alignment of Dual Port collimator

The results from Memory BIST are presented in Figure F.3, where the horizontal axis presents the time with ms resolution, and the vertical axis represents the number of accumulated soft errors from the error counter. Since the error counter was only 10-bits, the error counted started from 0 every time the counter reached the maximum value of 1023. The errors accumulated in this run verified that the dual collimator was aligned with the memory regions on the device.

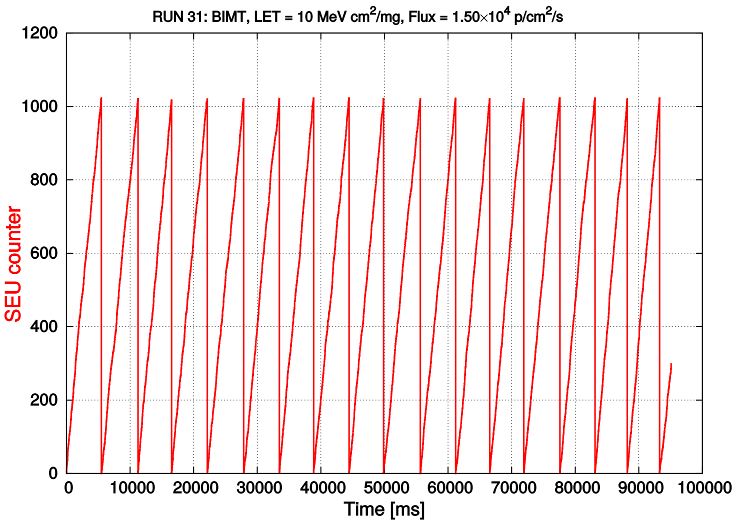


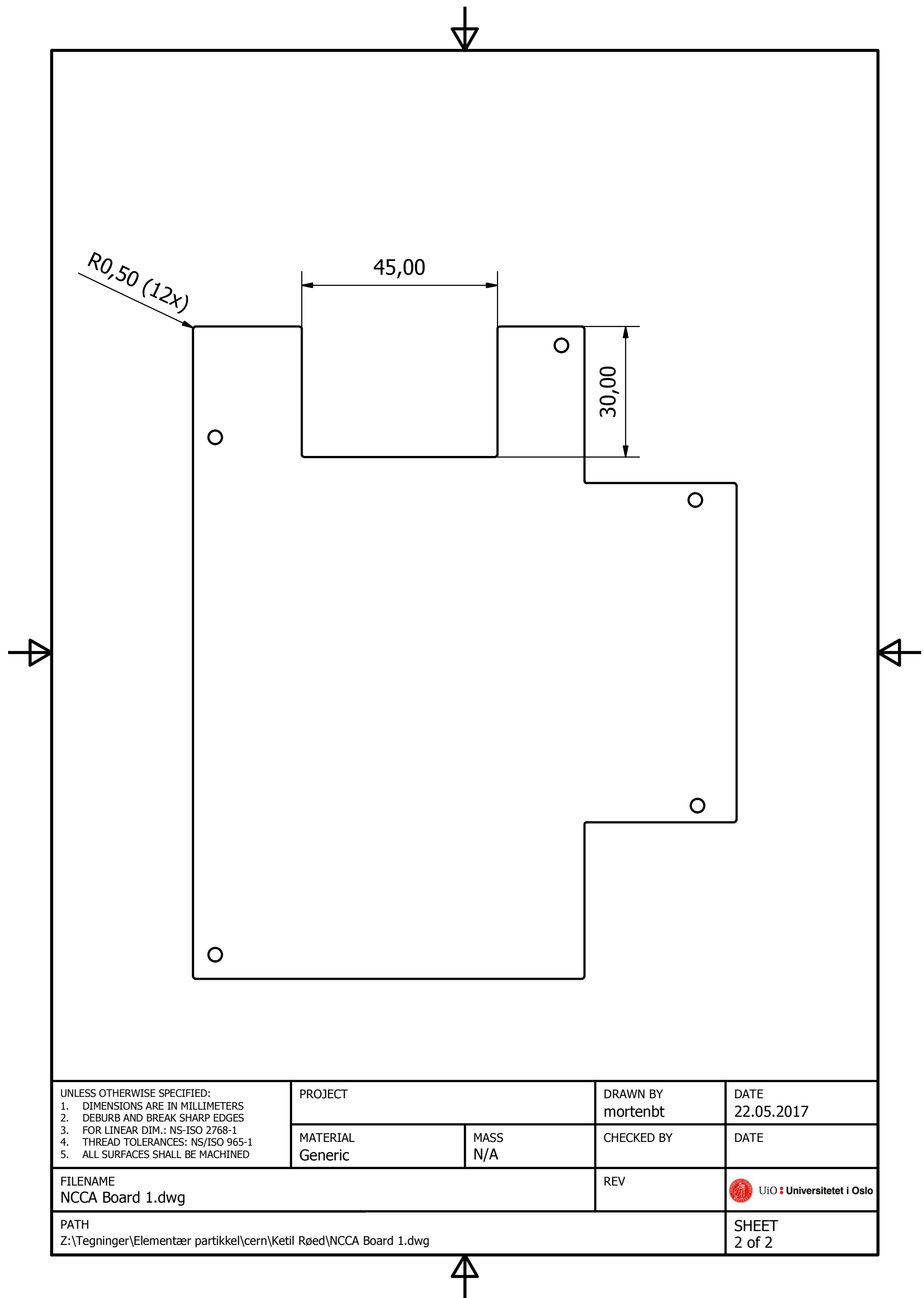
Figure F.3: Verifying the ions strike on memory region by running Memory BIST.

F.5 Digital core layout for SAMPA V2 and V3&V4

Thermometers are glued on every carrier board using an industrial thermal conductive adhesive, called *LOCTITE 384* [166]. Due to limited number of power resistors, these are not glued directly on all carrier boards, but rather attached on an ultra soft thermal conductive pad, known as TG-2030 from *T-Global Technology* [167]. In this way, one can easily shift power resistor from one carrier board to another. It is preferable to place these components right underneath the DUT. It was not possible however, due to hole on rear of the carrier boards for PL campaign.

F.6 SEL qualification results for SAMPA V3 & V4

F.7 Mechnical drawings for the prepared collimators


R0,50 (12x)
45,00
30,00
UNLESS OTHERWISE SPECIFIED:
1. DIMENSIONS ARE IN MILLIMETERS
2. DEBURB AND BREAK SHARP EDGES
3. FOR LINEAR DIM.: NS-ISO 2768-1
4. THREAD TOLERANCES: NS/ISO 965-1
5. ALL SURFACES SHALL BE MACHINED
PROJECT
DRAWN BY
mortenbt
DATE
22.05.2017
MATERIAL
Generic
MASS
N/A
CHECKED BY
DATE
FILENAME
NCCA Board 1.dwg
REV
UiO : Universitetet i Oslo
PATH
Z:\Tegninger\Elementær partikkel\cern\Ketil Røed\NCCA Board 1.dwg
SHEET
2 of 2

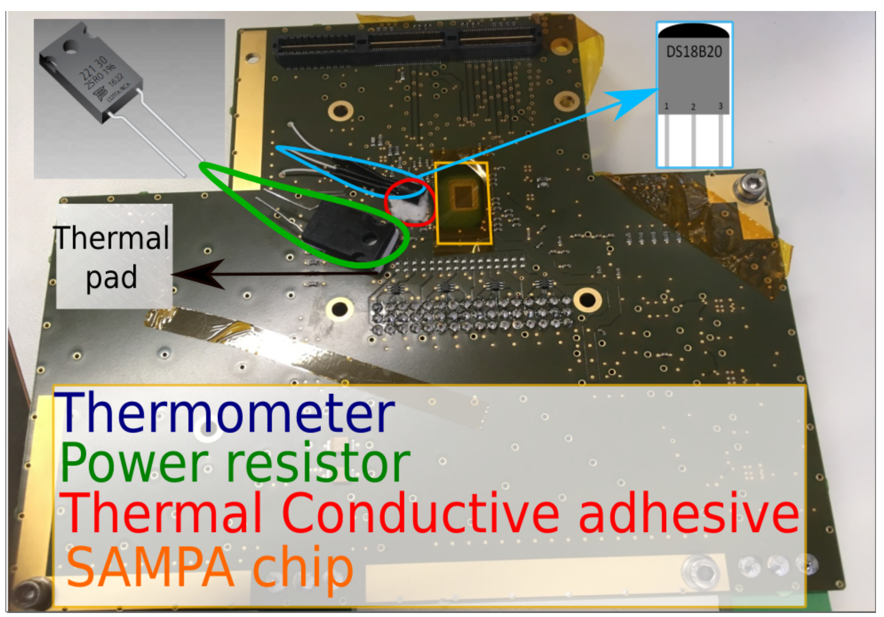
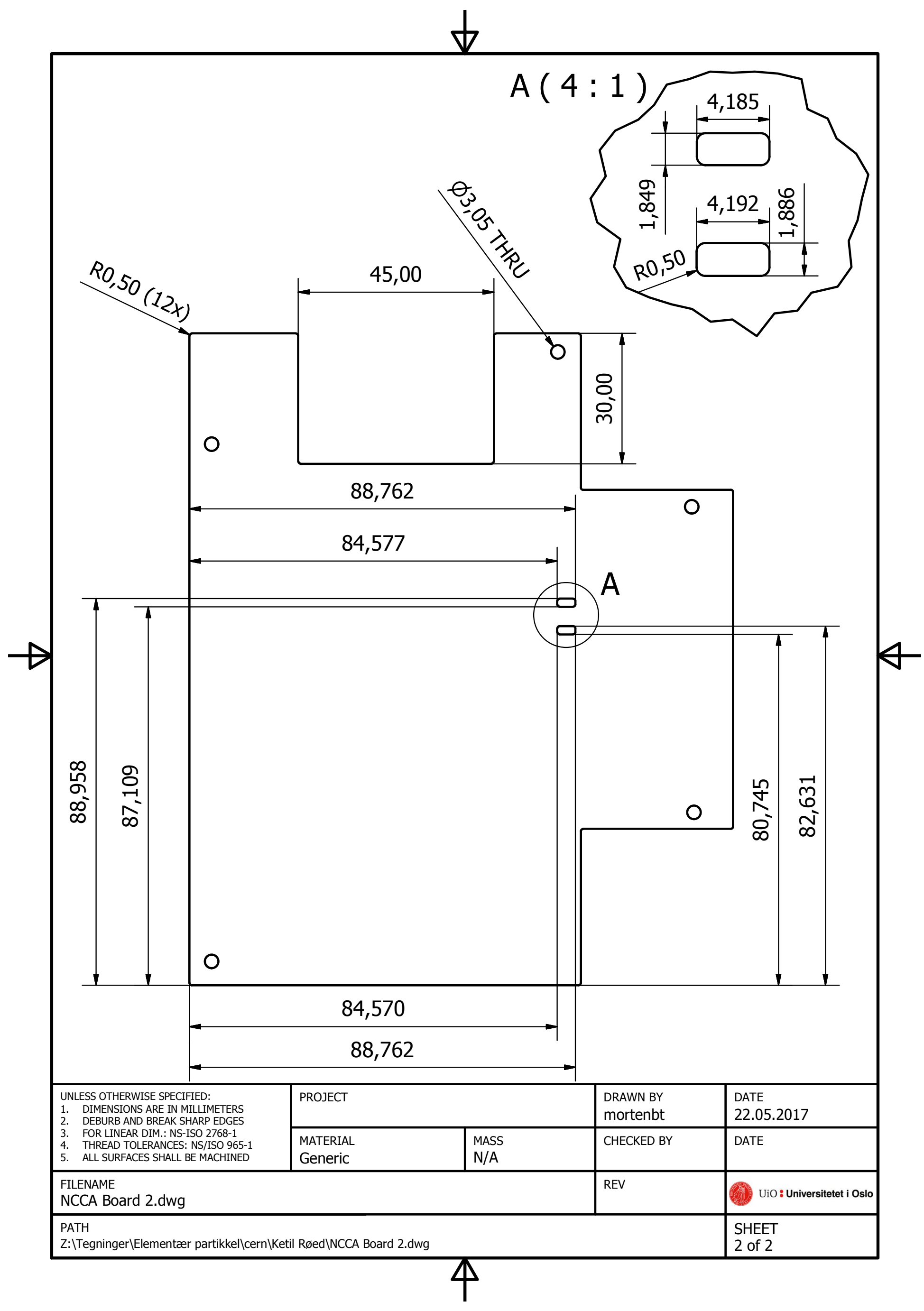
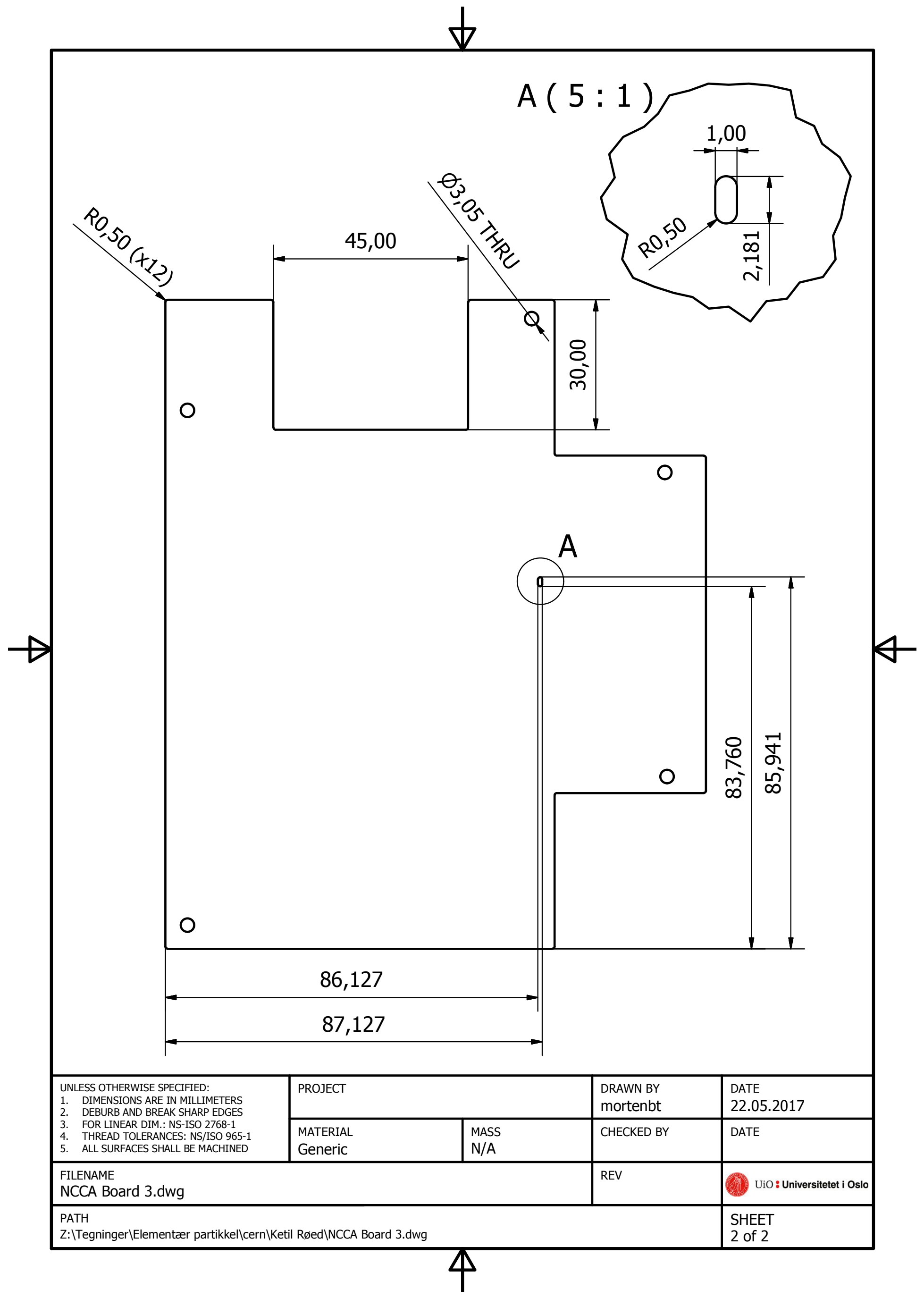


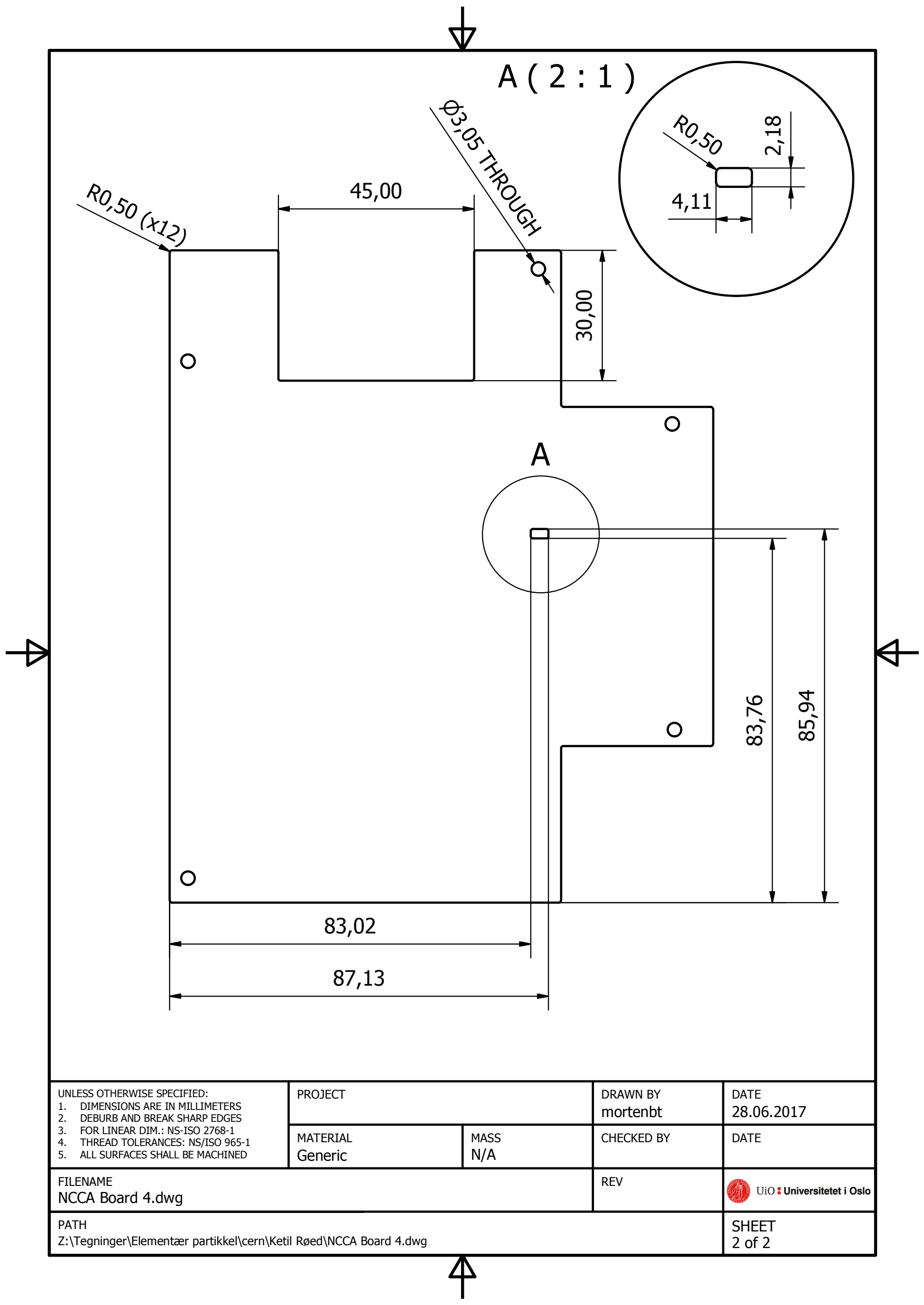
Figure F.4: Physical location of the temperature monitoring components on SAMPA carrier board.

DUT	ION	Angle [^{o}]	Eff.LET [MeV cm^2/mg]	Eff.Fluence [i/cm^2]	Temp [^{o}C]	# of SEL events	σ_{SEL}[cm^2]
V4_1	^{13}C^{4+}	0	1.30	1.00×10^6	45	0	$< 3.67\times10^{-6}$
V4_1	^{13}C^{4+}	45	1.84	1.00×10^6	45	0	$< 3.67\times10^{-6}$
V4_1	^{27}Al^{8+}	0	5.70	8.35×10^6	45	0	$< 4.42\times10^{-7}$
V4_1	^{27}Al^{8+}	45	8.06	1.00×10^6	45	0	$< 3.67\times10^{-6}$
V4_1	^{53}Cr^{16+}	0	16.0	1.46×10^7	45	0	$< 2.53\times10^{-7}$
V4_1	^{84}Kr^{25+}	0	32.40	2.10×10^7	45	0	$< 1.75\times10^{-7}$
V4_1	^{124}Xe^{35+}	0	62.50	1.00×10^7	45	0	$< 3.68\times10^{-7}$
V4_1	^{124}Xe^{35+}	45	88.39	1.00×10^7	45	0	$< 3.68\times10^{-7}$
V4_1	^{124}Xe^{35+}	60	125	1.00×10^7	45	0	$< 3.68\times10^{-7}$
V3_1	^{124}Xe^{35+}	0	62.5	1.00×10^7	45	0	$< 3.68\times10^{-7}$
V3_1	^{124}Xe^{35+}	60	125	1.50×10^7	60	0	$< 2.45\times10^{-7}$
V4_2	^{124}Xe^{35+}	0	62.5	1.01×10^7	45	0	$< 3.64\times10^{-7}$
V4_2	^{124}Xe^{35+}	60	125	1.00×10^7	85	0	$< 3.68\times10^{-7}$

Table F.1: SAMPA V4/V3 heavy-ion SEL results summary.


A (4 : 1)
4,185
1,849
4,192
1,886
R0,50
Ø3,05 THRU
R0,50 (12x)
45,00
30,00
88,762
84,577
A
88,958
87,109
80,745
82,631
84,570
88,762
UNLESS OTHERWISE SPECIFIED:
1. DIMENSIONS ARE IN MILLIMETERS
2. DEBURB AND BREAK SHARP EDGES
3. FOR LINEAR DIM.: NS-ISO 2768-1
4. THREAD TOLERANCES: NS/ISO 965-1
5. ALL SURFACES SHALL BE MACHINED
PROJECT
DRAWN BY
mortenbt
DATE
22.05.2017
MATERIAL
Generic
MASS
N/A
CHECKED BY
DATE
FILENAME
NCCA Board 2.dwg
REV
UiO : Universitetet i Oslo
PATH
Z:\Tegninger\Elementær partikkel\cern\Ketil Røed\NCCA Board 2.dwg
SHEET
2 of 2


A (5 : 1)
1,00
R0,50
2,181
R0,50 (x12)
45,00
Ø3,05 THRU
30,00
A
83,760
85,941
86,127
87,127
UNLESS OTHERWISE SPECIFIED:
1. DIMENSIONS ARE IN MILLIMETERS
2. DEBURB AND BREAK SHARP EDGES
3. FOR LINEAR DIM.: NS-ISO 2768-1
4. THREAD TOLERANCES: NS/ISO 965-1
5. ALL SURFACES SHALL BE MACHINED
PROJECT
DRAWN BY
mortenbt
DATE
22.05.2017
MATERIAL
Generic
MASS
N/A
CHECKED BY
DATE
FILENAME
NCCA Board 3.dwg
REV
UiO : Universitetet i Oslo
PATH
Z:\Tegninger\Elementær partikkel\cern\Ketil Røed\NCCA Board 3.dwg
SHEET
2 of 2


A (2 : 1)
R0,50
2,18
4,11
Ø3,05 THROUGH
45,00
R0,50 (x12)
30,00
A
83,76
85,94
83,02
87,13
UNLESS OTHERWISE SPECIFIED:
1. DIMENSIONS ARE IN MILLIMETERS
2. DEBURB AND BREAK SHARP EDGES
3. FOR LINEAR DIM.: NS-ISO 2768-1
4. THREAD TOLERANCES: NS/ISO 965-1
5. ALL SURFACES SHALL BE MACHINED
PROJECT
DRAWN BY
mortenbt
DATE
28.06.2017
MATERIAL
Generic
MASS
N/A
CHECKED BY
DATE
FILENAME
NCCA Board 4.dwg
REV
UiO : Universitetet i Oslo
PATH
Z:\Tegninger\Elementær partikkel\cern\Ketil Røed\NCCA Board 4.dwg
SHEET
2 of 2

Appendix G

SAMPA Pulsed-Laser campaign setup and report

G.1 Sample Preperation and Test board requirements

PULSYS

APPLICATION NOTE

SAMPLE PREPARATION AND TEST BOARD REQUIREMENTS

Version 1.0 – February 2011

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2. Test board requirement 4
   a. Objective lenses restrictions 4
   b. Test board fastening on PULSYS 5
   c. Test board volume restrictions 6
   d. I/O positioning 7

1. Sample preparation

Laser light can't go through the chip package; therefore, the chip has to be specially prepared for laser testing.

In most cases, the package is chemically or mechanically opened, either from front-side or from back-side, although only the back-side opening will allow a direct access to all the sensitive structures. If opened on front side, the metallization will mask a part of the sensitive structures. Front-side laser testing may be possible if metallization layers do not exceed 2 or 3 levels depending on the specific layout of the circuit.

In the case of back-side opening, laser light goes through the silicon bulk. The infrared laser beam delivered by the PULBOX Pico laser source allows to go through up to 600µm of silicon (however it is recommended to thin-down the silicon bulk to 400µm if possible).

The most important step in the backside preparation is to polish very carefully the silicon backside surface. A bad condition of the surface with scratches or dirt may results with laser scattering or absorbing and then high power losses. Furthermore, the infrared light used for internal structure imaging is also scattered and leads to poor image quality. On Figure 1-1, the structures have been visualized before and after backside polishing with different magnification, demonstrating the need for a polished surface..

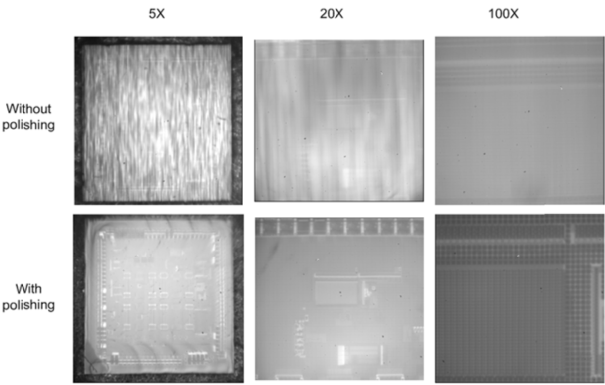


Figure 1-1 backside imaging of the same chip before and after polishing.

2. Test board requirements

a. Objective lenses restrictions

When designing the test board, it is important to respect the exclusion zone in which no components higher than the working distance of the objective should be placed. The working distance of the 100X magnification lenses is the more demanding (10mm). The exclusion zone depends on the chip die size and is equal to the 100X lens diameter (37mm) plus the width or height of the die as shown on Figure 2-1.

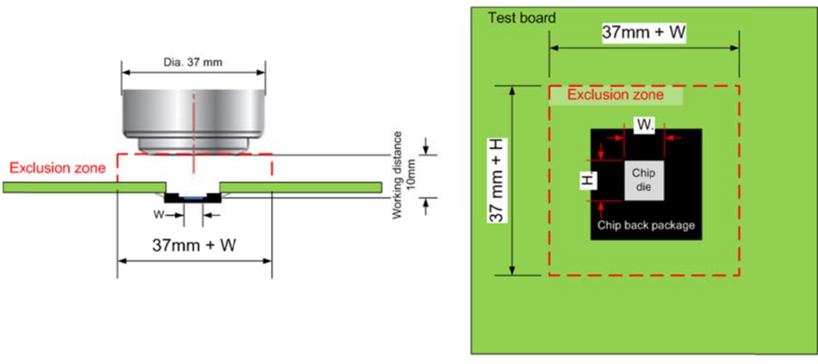


Figure 2-1 Exclusion zone *Left* : in Z direction *Right* : In X/Y direction

For instance, avoid placing jumpers, header pins or screws close to the chip. Most CMS components can be placed within the exclusion zone, as long as their height doesn't exceed 9.5mm. On Figure 2-2, the jumper was soldered too close to the chip precluding the correct focus of the lens on the chip.

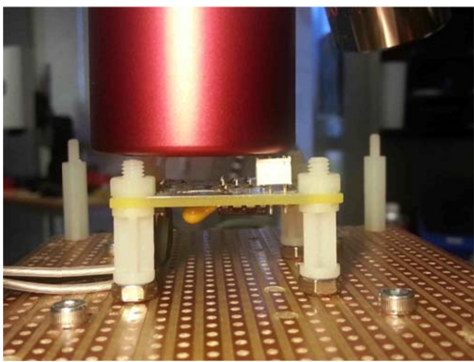


Figure 2-2 Jumper too close to the chip precluding the correct focusing of the lens on the chip

Moreover, due to the high numerical aperture of the 100X objective lens, the IR light cone angle is close to 45°, so it is important that the test board or package edge do not cut a

part of the light beam leading to high laser power losses and very dark image when you scan the edge of the die as shown on Figure 2-3.

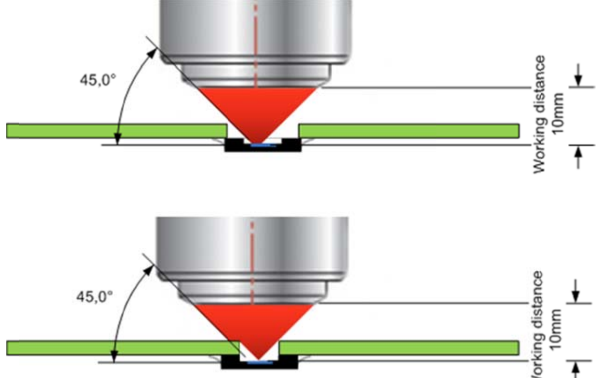


Figure 2-3 TOP: Correct test board opening, BOTTOM: opening too small resulting in the cut of the incoming light beam

b. Test board fastening on PULSYS

Eight M3 threaded holes are available in order to fasten the test board on the PULSYS sample holder (the hole pattern is shown on Figure 2-4, there are two sets of 4 holes at 100mm or 50mm spacing). Use at least four M3 screws to attach the board. Due to the course of X/Y stages, the chip should be approximately centered on the sample holder, at least within the 50mm square as shown on Figure 2-4.

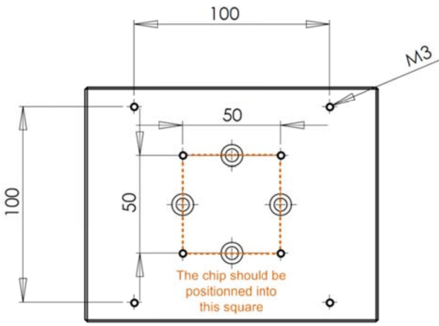


Figure 2-4 Top view of the PULSYS sample holder. 8 metric threaded holes are available for fixing the test board.

If the test board doesn't meet the hole pattern and chip positioning of fig 2-4, , a simple interface made of an aluminum plate or a PCB can be used to accommodate with different hole patterns and to center the chip within the stages range as shown on Figure 2-5.

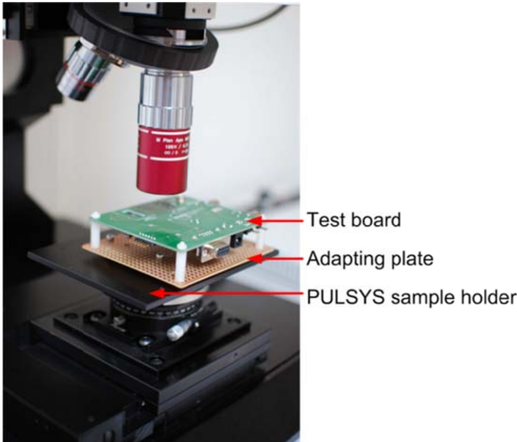
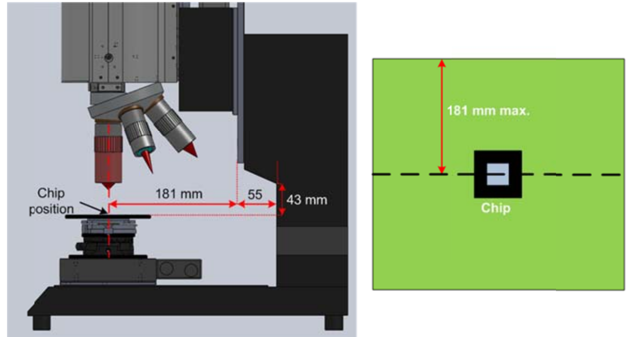


Figure 2-5 Board under microscope fixed on an adapting plate which is fixed on the PULSYS sample holder.

c. Test board volume restrictions

The distance between the center of the chip and the closest edge of the board should not exceed 181mm, with 55mm extra margin if the distance between the sample holder and the top of the test board is not higher than 43 mm, as shown on Figure 2-6. There is no other mechanical restrictions on the distances from the chip to the 3 other edges.



PULSYS profile view   Test board top view

Figure 2-6 *Left* : PULSYS profile view; *Right* : Test board top view. The distance between the chip and the closest-edge of the board should not exceed 181 mm.

Furthermore, in the standard configuration of the PULSYS microscope, the distance between the top surface of the sample holder and the chip surface should not exceed 50mm as shown on Figure 2-7. This range is extended to 200mm with the Z long-range option as shown in fig 2-8.

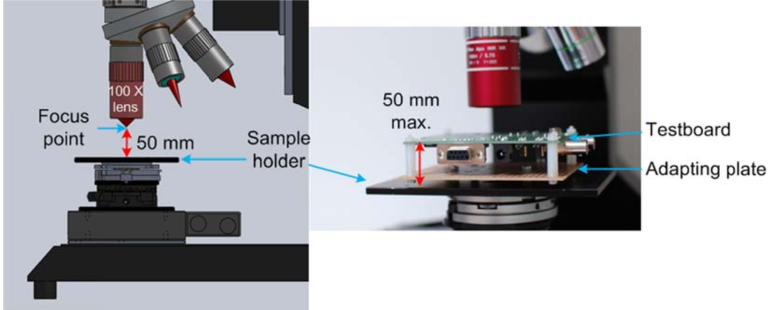


Figure 2-7 *Left* : PULSYS profile view; *Right* : photo of a test board with an adapting plate under microscope. The distance between the top face of the sample holder and the chip surface should not exceed 50 mm to focus the laser beam on the chip.

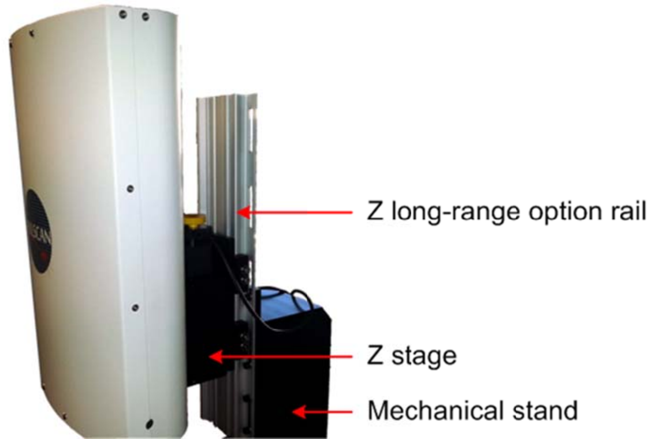


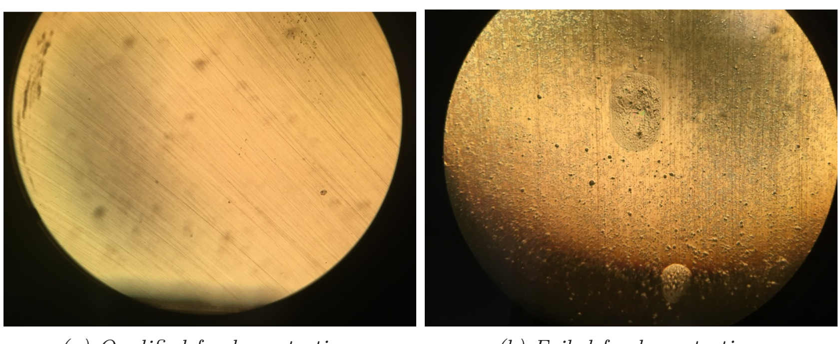
Figure 2-8 Z long-range option rail, giving 200mm extra range on the Z axis.

d. I/O positioning

Finally, it is preferable to use horizontal I/O connectors when possible, as on Figure 2-9, in order to clear the area above the test board. This makes easier the board installation and the lenses rotation. Cable should be fixed in a way that there is no strong mechanical constraint on the board during scanning.

Figure 2-9 A test board with all horizontal I/O connectors.

G.2 SAMPA test setup for pulsed-laser campaign



(a) Qualified for laser testing. *(b) Failed for laser testing.*

Figure G.1: Microscopic inspection for backside surface quality of SAMPA V2 samples.

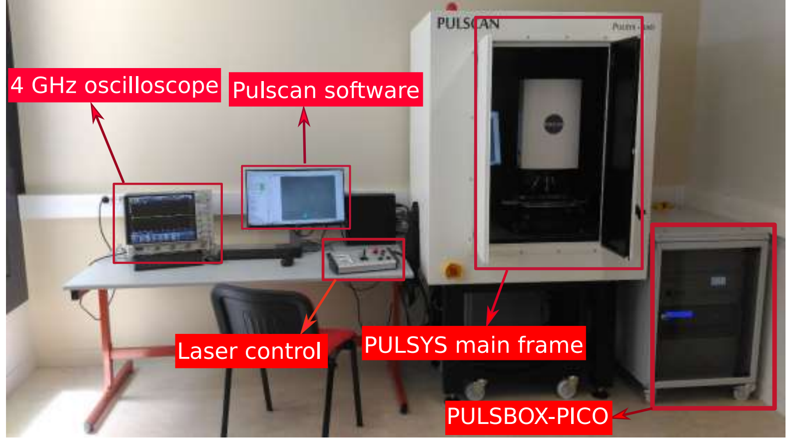
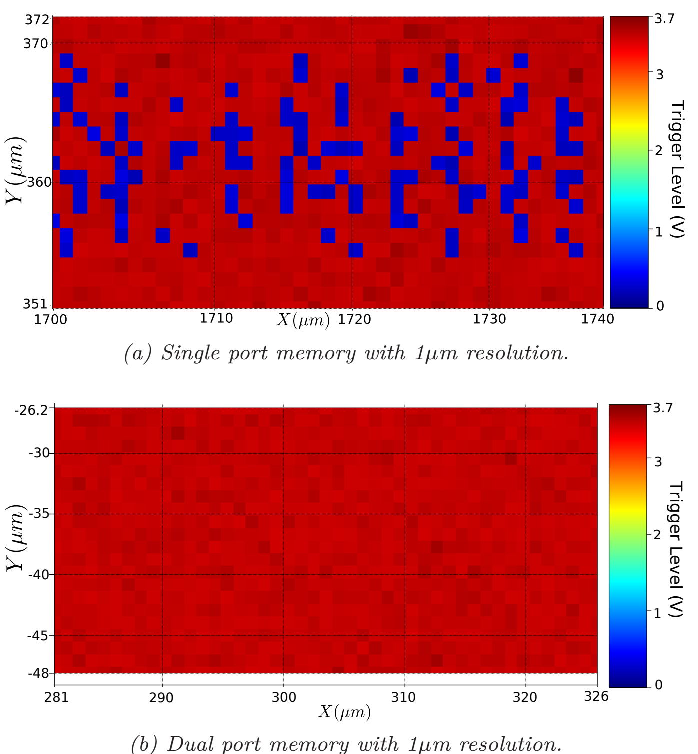


Figure G.2: An overview of PULSYS-RAD system from PULSCAN.

G.3 Results from automatized laser scan runs



(a) Single port memory with 1μm resolution.

(b) Dual port memory with 1μm resolution.

Figure G.3: SEL sensitive map from automatized scanned regions in both single and dual port sram memories.

G.4 SAMPA Pulsed-Laser campaign Test Report

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N° SIRET : 50778566500039
N° TVA : FR40507785665

Tél : 05 56 49 12 71
Web : www.pulscan.com
e-mail : contact@pulscan.com

Laser Test Report
18011501

Devices	SAMPA
Campaign dates	January, 15 2018
Facility	1P laser system from IES laboratory, Montpellier
Report date	18/01/2017
Revision	1
Author	Sébastien Jonathas

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1 General test description

1.1 Device

Information on the devices under test is detained by the University of Oslo. The measurements are performed on the following devices:

Device	*Function*	*Size*	*Substrate thickness*	*Technology*
SAMPA “V2” (SEL sensitive)	ASIC	9mm x 9mm	175µm	130nm
SAMPA “V4” (new design)	ASIC	9mm x 9mm	175µm	130nm

1.2 Facility

The test is performed at IES Single-Photon laser facility. The system is composed of a PULSYS microscope and a PULSBOX PICO laser source from PULSCAN. This system is dedicated to laser radiation testing.

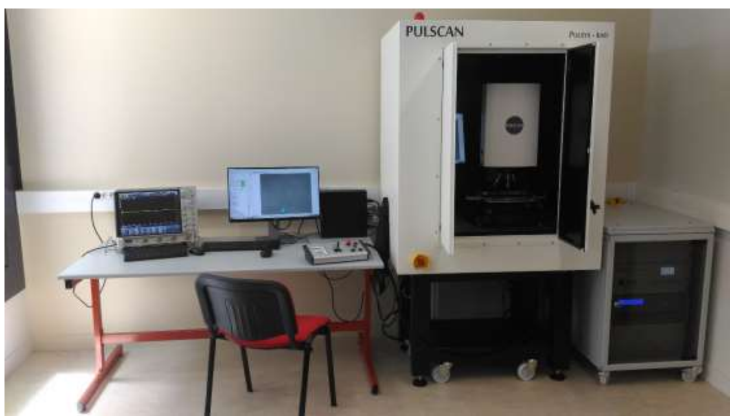


Figure 1-1 PULSYS-RAD system

The PULSYS-RAD system is optimized both for backside imaging and ultra-short pulsed laser injection in the near-infrared (i.e. the best wavelengths for testing silicon technologies).
PULSBOX-PICO is a compact system optimized for single-photon absorption in silicon. It is a smart laser source offering complete laser pulse control for semiconductor testing and analysis.

1.3 Team

The test is conducted by:

- Sohail Musa Mahmood, University of Oslo
- Jonas Carlsen
- Sébastien Jonathas, Pulscan

1.4 Objectives of the campaign

Recent radiation tests have shown that the SAMPA prototype “V2” is sensitive to Single Event Latchup (SEL). A new SAMPA prototype “V4” has been designed. During a new radiation test, no SEL was detected on this new prototype.

The main objective of the campaign is to reproduce and find where the SELs are happening on SAMPA “V2” and confirm that the new design of SAMPA “V4” is not sensitive to SEL.

In parallel, SEU sensitivity threshold will be measure on SRAM memories for different configurations.

2 Test conditions

2.1 DUT settings

DUT specific settings are detained by the University of Oslo.

The test board checks continuously if an error has occurred (SEL or SEU). If SEL occurs, the test board sends out an electrical pulse to the oscilloscope of the PULSYS laser system. For SEU, the error log is not interfaced with the laser system.

During a scan, the laser is injected continuously (repetition rate between 2Hz and 100Hz). Without data acquisition by the laser system, only the test board records if errors have occurred or not. The XY position of the errors cannot be known.

During a scan with data acquisition by the laser system, at each DUT position, the laser system acquires the waveform of the oscilloscope in order to know if an error has occurred (low level signal from the test board) or not (High level signal from the test board). At the end of a laser scan on a specific zone, the laser system built the sensitive map (XY position of the errors) and superimposes this error map on the device picture from the IR camera or on the layout picture of the device.

2.2 Laser Settings

Parameter	Value	Comment
Pulse duration	30ps	Standard duration for Single-Photon SEE laser testing
Wavelength	1064 nm	Standard wavelength compatible with Single-Photon absorption in the silicon
Repetition rate	[2Hz to 100Hz]	The laser pulses are continuously delivered at this rate.
Spot size	1.2µm ± 0.2µm (100X lens)	Close to diffraction limited beam
Pulse energy	32pJ – 1.035nJ	Incident energy on the device used for this campaign

2.3 Microscope Settings

2.3.1 Test board mounting

The test board is attached to the translation stages by means of an adaptation plate. The laser beam is focused on the backside of the device.

Figure 2-1 Test board attached to the PULSYS laser system

2.3.2 Visualization, orientation and coordinates

An Infrared (IR) camera is used to visualize the internal structures through the silicon substrate. The image quality of these structures is very dependent on the backside surface quality and the substrate doping level.

The field of view is clear but the presence of scratches on the backside can induce laser scattering. The energy of the laser pulse in the active area cannot be known with accuracy.

The chips orientation, as seen by the camera (i.e. from above while standing in front of the microscope), is presented in Figure 2-2. The origin of the coordinates is taken on specific point on the DUT:

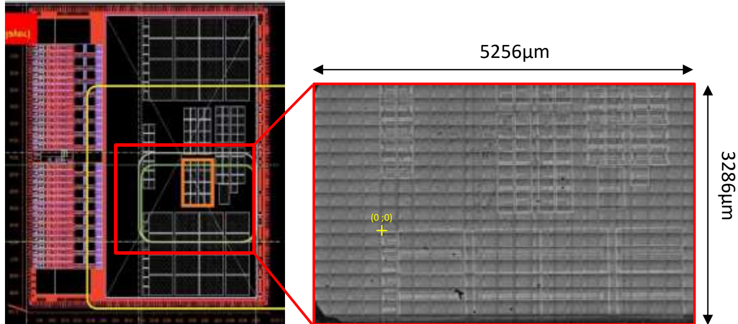


Figure 2-2 Chip orientation as seen with the camera

3 Laser Tests

3.1 Summary

The first part of the laser testing was performed on the SAMPA "V2" which is sensitive to SEL.

Because the threshold energy was not known, to avoid long automatized scan at under threshold energy, the first scans were done manually. It allows aiming directly the most likely sensitive structure in a most effective way. With an energy of 276pJ, first events have quickly appeared on the memory array of the Pedestal SRAM. After having found a point sensitive to SEL, we have reduced the energy in order to find the energy threshold. The SEL threshold energy was measured between 117pJ and 124pJ.

The SEL threshold energy was then measured for different power supply voltages. As expected, by reducing the power supply voltage, the SEL threshold energy increases (less sensitive). For example, at nominal voltage 1.25V, we generate SEL with a laser pulse energy of 124pJ. By reducing the voltage down to 1.16V, we need increasing the laser pulse energy up to 172pJ to generate SEL in a same point on the Pedestal SRAM.

The SEL threshold energy was also measure for different pattern written in the Pedestal SRAM. The default pattern is an alternation of 0 and 1 [0101]. We have also tried all in 1 [1111] and

all in 0 [0000]. The pattern [0000] seems to be less sensitive to SEL but it was not clearly reproductive.

After having investigate the Pedestal SRAM, we have moved on the Data SRAM. No SEL was detected on this area.

Because SEU was also detected during the test, we have decided to measure SEU threshold energy on Pedestal SRAM (between 48pJ and 62pJ) and on Data SRAM (between 34pJ and 48pJ).

The SEU threshold energy was also measure for different pattern written in the Pedestal SRAM. The pattern [0000] seems to be a little less sensitive to SEU.

The second part of the experiment was performed on the SAMPA "V4". As expected, no SEL was detected on the new Pedestal SRAM with a laser pulse energy of 1,035nJ.

Because SEU was also detected during the test, we have decided to measure SEU threshold energy on Pedestal SRAM (between 48pJ and 55pJ) and on Data SRAM (between 48pJ and 55pJ).

The SEU threshold energy was also measure for different pattern written in the Pedestal SRAM. The pattern [0000] seems to be a little less sensitive to SEU.

The SEU threshold energy was measured for different power supply voltages. Contrary to SEL, by reducing the power supply voltage, the SEU threshold energy decreases (more sensitive). For example, at nominal voltage 1.25V, we generate SEU with a laser pulse energy of 55pJ. By reducing the voltage down to 1.144V, we can decreasing the laser pulse energy down to 46pJ to generate SEU in a same point on the Pedestal SRAM.

To finish, we have tried to scan two zone with an energy of 1,035nJ to investigate SEFI but no event was detected.

3.2 Results

Two main zones have been inspected. There are shown in red on figures below.

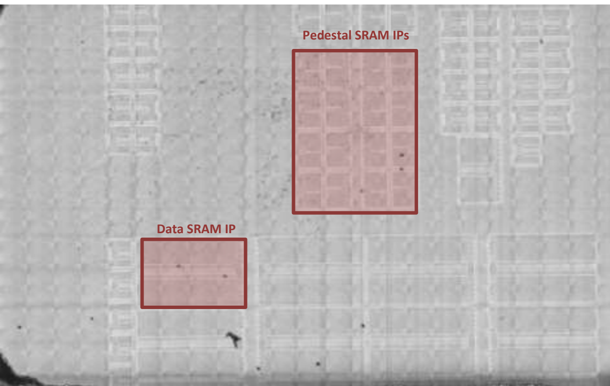


Figure 3-1 inspected zones on SAMPA "V2"

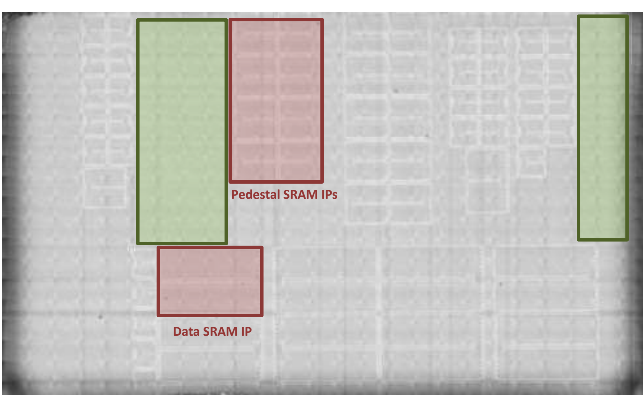


Figure 3-2 inspected zones on SAMPA "V4"

Run #	Chip #	Scanned area	Laser parameters		Scan parameters					Results	Comments
			Energy (Incident on DUT)	Repetition. Rate (Hz)	Point 1* (µm;µm)	Size X (µm)	Size Y (µm)	dX (µm)	dY (µm)		
SAMPA "V2"											
1	1	Pedestal SRAM	276 pJ	2	Manual scan					SEL	Triggered in the memory array
2	1	Pedestal SRAM	276 pJ	2	$\begin{pmatrix}1700.6\\359.6\end{pmatrix}$	Random move around this point				SEL	
3			138 pJ							SEL	
4			103 pJ							No SEL	
5	1	Pedestal SRAM	172 pJ	2	Manual scan					No SEL	
6	1	Data SRAM	172 pJ	2	Manual scan					No SEL	
7			276 pJ							No SEL	

Run #	Chip #	Scanned area		Laser parameters		Scan parameters					Results	Comments
				Energy (Incident on DUT)	Repetition. Rate (Hz)	Point 1* (µm;µm)	Size X (µm)	Size Y (µm)	dX (µm)	dY (µm)		
SEL threshold energy												
8				150 pJ							SEL	
9				138 pJ							SEL	
10	1	Pedestal SRAM		131 pJ	2	$\begin{pmatrix}1700.6\\359.6\end{pmatrix}$	Random move around this point				SEL	
11				124 pJ							SEL	
12				117 pJ							No SEL	
Pattern effect on SEL												
13											SEL	Pattern [0101] (default)
14	1	Pedestal SRAM		131 pJ	2	$\begin{pmatrix}1700.6\\359.6\end{pmatrix}$	Random move around this point				SEL	Pattern [0000] (not found during the first pass)
15											SEL	Pattern [1111]
Power supply voltage effect on SEL												
16				131 pJ							SEL	Power supply: 1.25V (nominal)
17				131 pJ							No SEL	Power supply: 1.23V
18				144 pJ							SEL	Power supply: 1.23V
19				144 pJ							No SEL	Power supply: 1.20V
20				158 pJ							SEL	Power supply: 1.20V
21				158 pJ							No SEL	Power supply: 1.16V
22	1	Pedestal SRAM		172 pJ	2	$\begin{pmatrix}1700.6\\359.6\end{pmatrix}$	Random move around this point				SEL	Power supply: 1.16V (Not found during the first pass because the current limitation was set too high 500mA compare to the nominal consumption 270mA). For the rest of the experiment, the current limitation was set at 400mA.
23				172 pJ							No SEL	Power supply: 1.11V
24				186 pJ							No SEL	Power supply: 1.11V

Run #	Chip #	Scanned area	Laser parameters: Energy (Incident on DUT)	Laser parameters: Repetition. Rate (Hz)	Scan parameters: Point 1* (µm;µm)	Scan parameters: Size X (µm)	Scan parameters: Size Y (µm)	Scan parameters: dX (µm)	Scan parameters: dY (µm)	Results	Comments
Automatic scan in the memory array of the Pedestal SRAM with SEL trigger signal monitoring											
25	1	Pedestal SRAM	131 pJ	10	$\begin{pmatrix}1698.2\\351.0\end{pmatrix}$	40.1	20.9	1	1		
26								0.5	0.5		
SEU threshold energy on Pedestal SRAM											
27	1	Pedestal SRAM	131 pJ	2	$\begin{pmatrix}1700.6\\359.6\end{pmatrix}$	Random move around this point				SEU	
28			117 pJ							SEU	
29			103 pJ							SEU	
30			89 pJ							SEU	
31			75 pJ							SEU	
32			62 pJ							SEU	
33			48 pJ							No SEU	
Pattern effect on SEU											
34	1	Pedestal SRAM	48 pJ	2	$\begin{pmatrix}1700.6\\359.6\end{pmatrix}$	Random move around this point				No SEU	Pattern [0101] (default)
35			48 pJ							No SEU	Pattern [0000]
36			48 pJ							No SEU	Pattern [1111]
37			62 pJ							SEU	Pattern [1111]
38			62 pJ							No SEU	Pattern [0000]
39			75 pJ							SEU	Pattern [0000]
40			69 pJ							SEU	Pattern [0000]
41			65 pJ							SEU	Pattern [0000]
42			62 pJ							No SEU	Pattern [0000]

Run #	Chip #	Scanned area	Laser parameters		Scan parameters					Results	Comments
			Energy (Incident on DUT)	Repetition. Rate (Hz)	Point 1* (µm;µm)	Size X (µm)	Size Y (µm)	dX (µm)	dY (µm)		
SEU threshold energy on Data SRAM											
43	1	Data SRAM	131 pJ	2	$\begin{pmatrix}292.6\\-35.2\end{pmatrix}$	Random move around this point				SEU	
44			117 pJ							SEU	
45			103 pJ							SEU	
46			89 pJ							SEU	
47			75 pJ							SEU	
48			62 pJ							SEU	
49			48 pJ							SEU	
50			34 pJ							No SEU	
Automatic scan in the data array of the Data SRAM with SEL trigger signal monitoring											
51	1	Data SRAM	690 pJ	10	$\begin{pmatrix}281.1\\-48.1\end{pmatrix}$	44.8	21.9	1	1	No SEL	
SAMPA "V4"											
SEU threshold energy on Pedestal SRAM											
52	2	Pedestal SRAM	131 pJ	2	$\begin{pmatrix}1025.7\\653.5\end{pmatrix}$	Random move around this point				SEU	
53			117 pJ							SEU	
54			103 pJ							SEU	
55			89 pJ							SEU	
56			75 pJ							SEU	
57			62 pJ							SEU	
58			48 pJ							No SEU	
59			55 pJ							SEU	
Pattern effect on SEU											
60	2	Pedestal SRAM	55 pJ	2	$\begin{pmatrix}1025.7\\653.5\end{pmatrix}$	Random move around this point				SEU	Pattern [0101] (default)
61			55 pJ							No SEU	Pattern [0000]
62			55 pJ							SEU	Pattern [1111]
63			62 pJ							SEU	Pattern [0000]

Run #	Chip #	Scanned area	Laser parameters		Scan parameters					Results	Comments
			Energy (Incident on DUT)	Repetition. Rate (Hz)	Point 1* (µm;µm)	Size X (µm)	Size Y (µm)	dX (µm)	dY (µm)		
Power supply voltage effect on SEU											
64	2	Pedestal SRAM	55 pJ	2	$\begin{pmatrix}1025.7\\653.5\end{pmatrix}$	Random move around this point				SEU	Power supply: 1.25V (nominal)
65			48 pJ							SEU	Power supply: 1.22V
66			41 pJ	10						No SEU	Power supply: 1.22V
67			41 pJ							No SEU	Power supply: 1.192V
68			41 pJ							No SEU	Power supply: 1.144V
69			44 pJ							No SEU	Power supply: 1.144V
70			46pJ							SEU	Power supply: 1.144V
SEU threshold energy on Data SRAM											
71	2	Data SRAM	131 pJ	10	$\begin{pmatrix}299.6\\-50.7\end{pmatrix}$	Random move around this point				SEU	
72			117 pJ							SEU	
73			62 pJ							SEU	
74			48 pJ							No SEU	
75			55 pJ							SEU	
76			51pJ							SEU	
77			48pJ							SEU	Same configuration as run #74 but not same result: due to error bar of the measure
Automatic scan in the memory array of the Pedestal SRAM with SEL trigger signal monitoring											
78	2	Pedestal SRAM	1.035nJ	10	$\begin{pmatrix}1010.2\\640.2\end{pmatrix}$	41.3	21.3	1	1	No SEL	
Automatic scan for SEFI inspection											
79	2		1.035nJ	10	$\begin{pmatrix}40.2\\44.0\end{pmatrix}$	851.5	2038	851	10	No SEFI	
80	2		1.035nJ	100	$\begin{pmatrix}3980.7\\48.5\end{pmatrix}$	466.6	2033	10	2033	No SEFI	

*The coordinates of the Point 1 correspond to the bottom left corner of the scanned zone.

4 Conclusions

As expected, SEL was detected on SAMPA prototype “V2” and not on SAMPA prototype “V4”.

Only the Pedestal SRAM was sensitive to SEL and the SEL threshold energy has been measured between 117pJ and 124pJ.

We have also shown that by decreasing the power supply voltage, the SEL sensitivity decreased.

SEU sensitivity has also been investigated. SEU threshold energy was measured as twice lower than SEL threshold energy.

We have also shown that when the pattern all 0 is written in SRAM, the structure seems to be less sensitive.

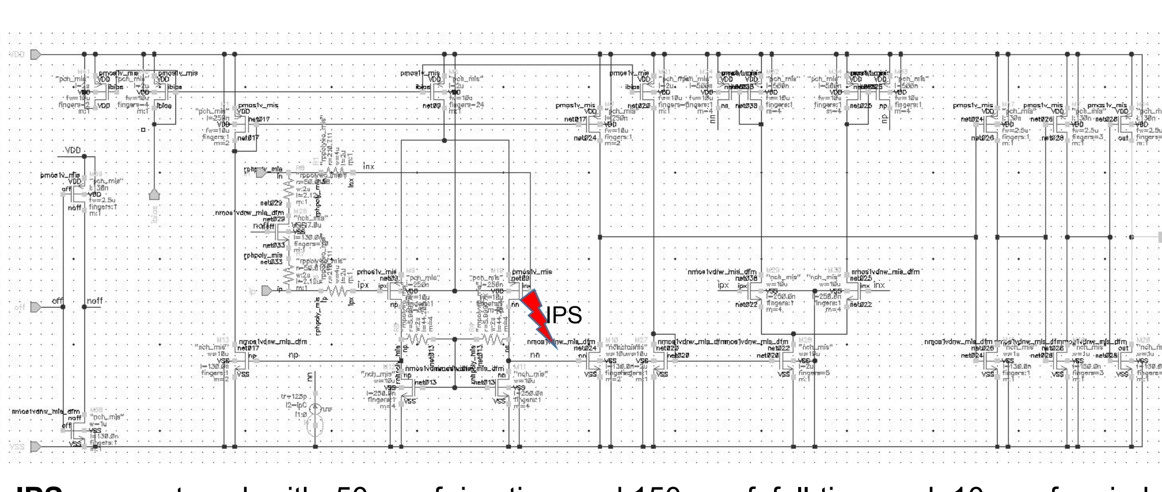
To finish, no SEFI was detected.

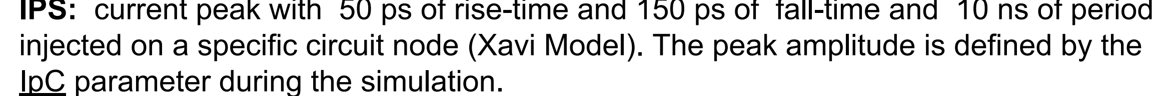
We cannot exclude that other sensitive points can be present on the scanned areas. Indeed, the presence of dirt on the backside surface could have hid some zones of the circuit.

Appendix H

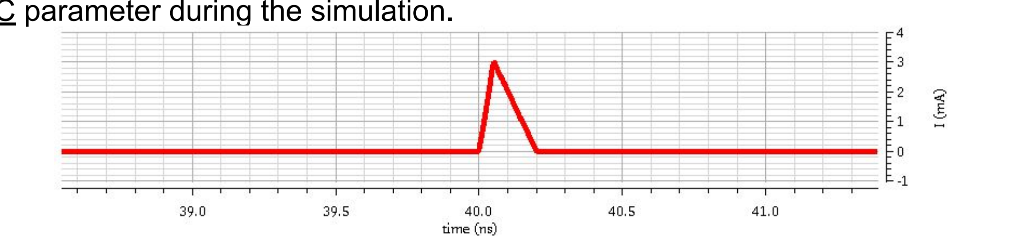
Single Event Transient simulations of the SAMPA SLVS receiver

Simulations of the SLVS receiver SET



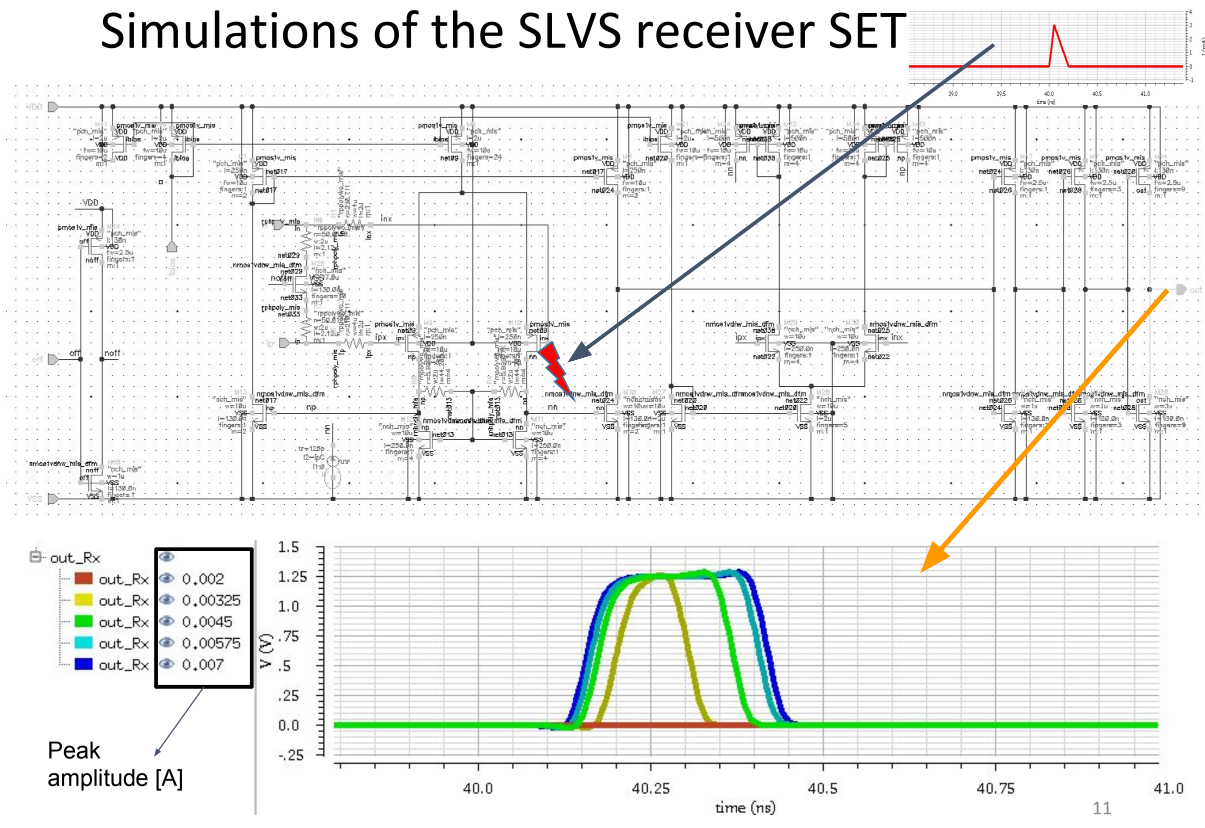


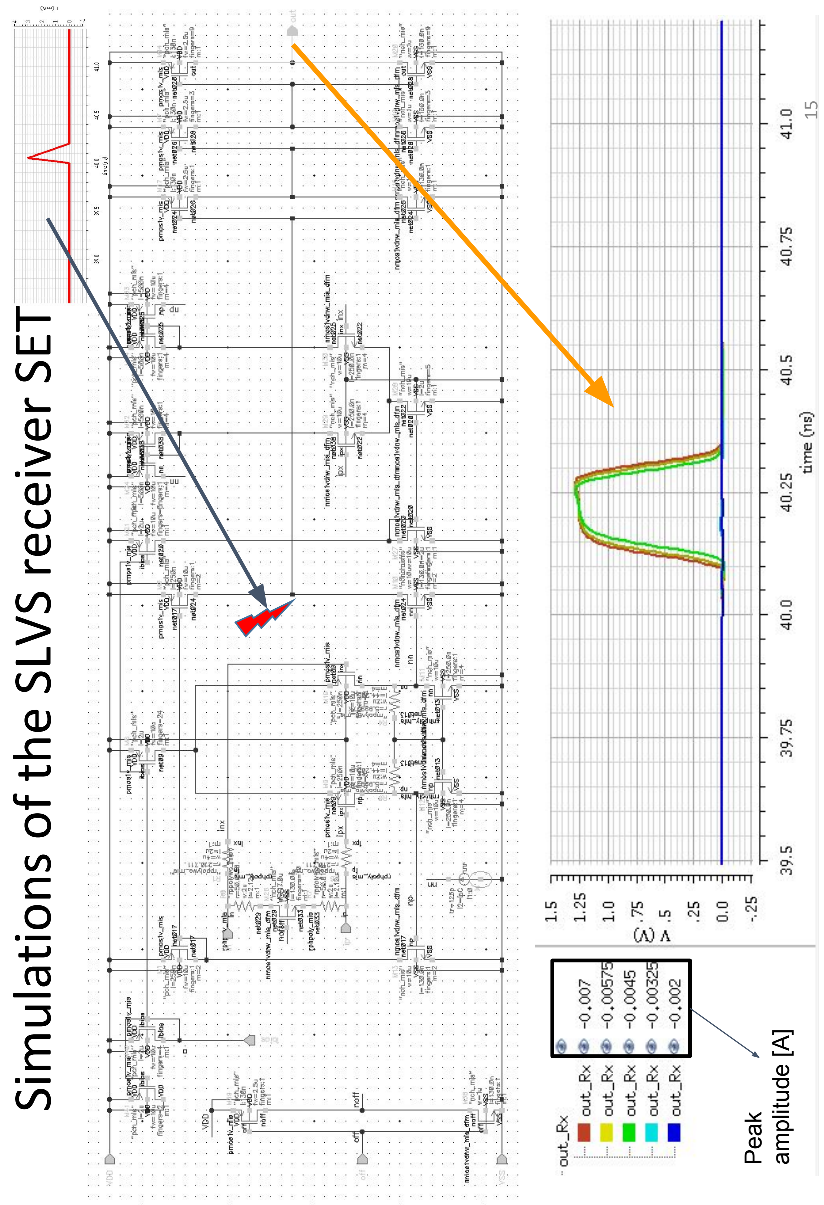
IPS: current peak with 50 ps of rise-time and 150 ps of fall-time and 10 ns of period injected on a specific circuit node (Xavi Model). The peak amplitude is defined by the <u>IpC</u> parameter during the simulation.

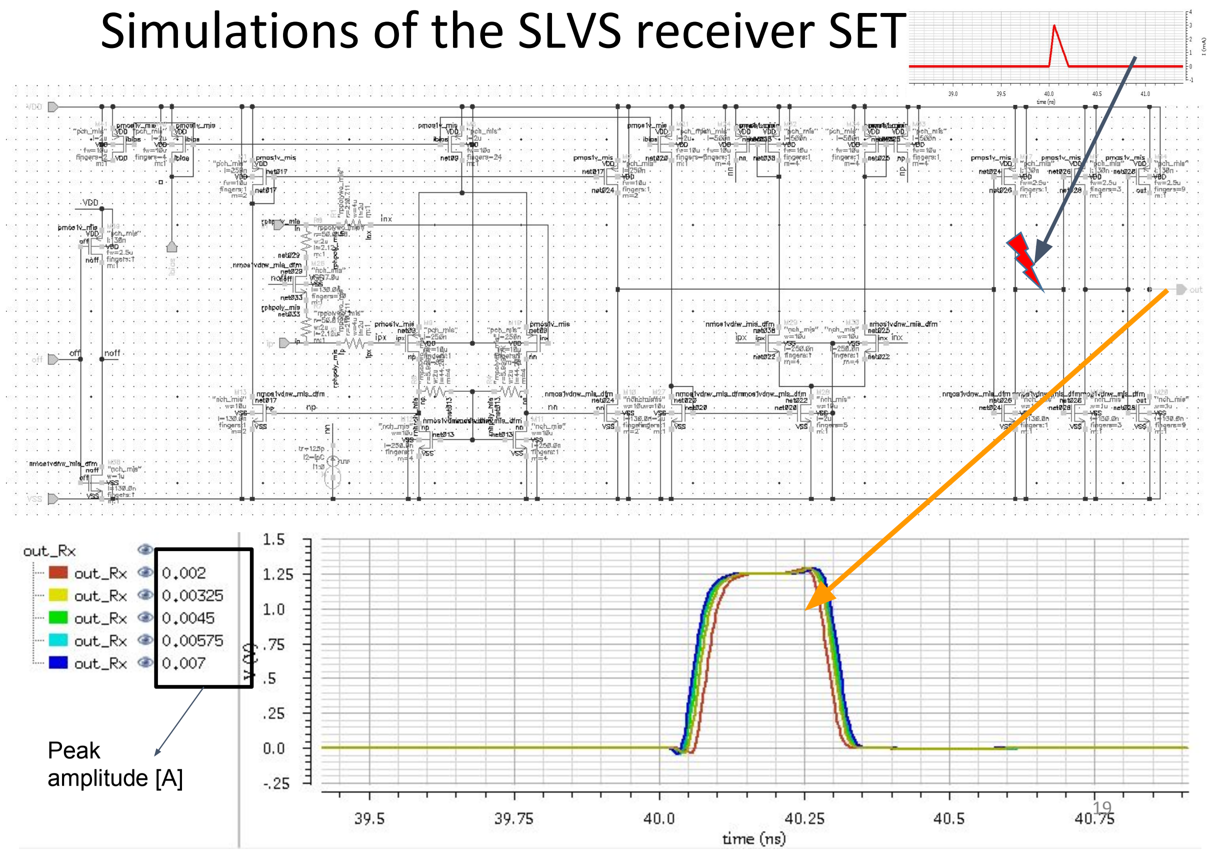


10

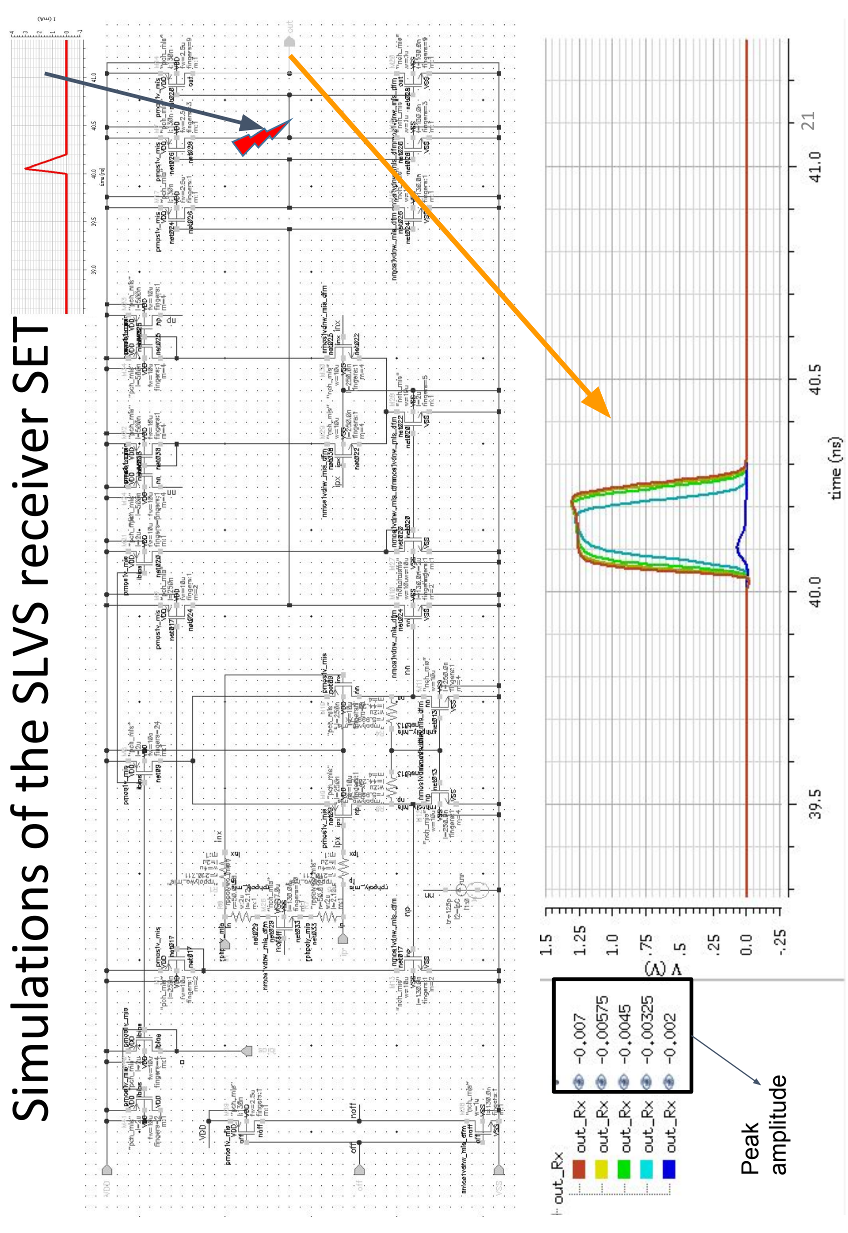
Simulations of the SLVS receiver SET




Simulations of the SLVS receiver SET
out_Rx
out_Rx -0.007
out_Rx -0.00575
out_Rx -0.0045
out_Rx -0.00325
out_Rx -0.002
Peak amplitude [A]
V (V)
time (ns)
39.5
39.75
40.0
40.25
40.5
40.75
41.0
1.5
1.25
1.0
.75
.5
.25
0.0
-.25



Simulations of the SLVS receiver SET
out_Rx
out_Rx 0.002
out_Rx 0.00325
out_Rx 0.0045
out_Rx 0.00575
out_Rx 0.007
Peak amplitude [A]
V (V)
time (ns)


Simulations of the SLVS receiver SET
out_Rx
out_Rx -0.007
out_Rx -0.00575
out_Rx -0.0045
out_Rx -0.00325
out_Rx -0.002
Peak amplitude
V (V)
time (ns)
1.5
1.25
1.0
.75
.5
.25
0.0
-.25
39.5
40.0
40.5
41.0
21

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