Developing MOS structures in gallium oxide for high-power electronics and energy savings applications

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Abstract

Metal-oxide-semiconductor capacitors (MOSCAP) based on the β phase of gallium oxide (β–Ga_2O_3) were pursued for future power electronic devices. Two surface orientations of β–Ga_2O_3 were investigated, i.e. (010) and (-201), while for the oxide layer aluminium oxide (Al_2O_3) was deposited using atomic layer deposition (ALD). From the current–voltage (IV) and capacitance-voltage (CV) measurements, it was found that the sample with the (010) surface orientation showed better rectification and lower density of interface states. On the basis of this result, MOSCAPs based on (010) β–Ga_2O_3 were fabricated and post deposition annealing employed, and the results were compared with a more mature material for power electronics, namely 4H–silicon carbide (4H–SiC). From the current-voltage (IV) and capacitance-voltage (CV) measurements, the β–Ga_2O_3 MOSCAP samples exhibit smaller flatband voltage than 4H–SiC MOSCAPs and did not show any kink in depletion. It was also demonstrated that the increase of the annealing temperature improves the interface states between 4H–SiC and Al_2O_3, but conversely, it degraded the MOSCAP properties in β–Ga_2O_3. Information on bulk and interface defect states of β–Ga_2O_3 and 4H–SiC MOSCAP was obtained from the peak of the Deep Level Transient Spectroscopy (DLTS) spectra, and thermal dielectric relaxation current (TDRC) was also attempted. Signatures were obtained from the DLTS spectra originating from defects present in the bulk and closer to the interface. Furthermore, H^+ irradiation was used to examine general defect states and intrinsic defects states of β–Ga_2O_3. A peak appeared in the recovery process in response to irradiation. This irradiation induced peak indicate an intrinsic origin, and labeled E2* in a recent study(1). Finally, MOS field effect transistors (MOSFETs) and metal semiconductor FETs (MESFETs) have been attempted for wider understanding the β–Ga_2O_3 for power devices.

Contents

PART I – THEORY

1 INTRODUCTION

The majority of modern devices include semiconductor components that provide basic operation to electronic devices, such as rectifiers and switches. In particular, semiconductor devices based on silicon have been widely studied. However, silicon-based device performance often meets its limitation in high temperature and high power applications as used in power electronics. For these reasons, new semiconductor materials have been explored since the 1950s, especially materials with a wide bandgap (2). Hence, wide bandgap semiconductor materials such as SiC and GaN have been intensely studied and used as substitutional candidates. These materials perform better than Si-based devices at high temperatures, voltages, and switching speeds (3-8). However, as devices continue to develop it is essential to explore new materials that can be applied to power devices and to establish their capabilities.

Recently, gallium oxide (Ga_2O_3) has emerged as a next-generation semiconductor material, with potential applications including gas sensors, solar blind photodetectors, and solar cell coating, in addition to power devices (9-12). Gallium oxides can have polymorphic states of α–, β–, γ–, δ–, and ε–, of which β–Ga2O3 is the most stable within the temperature range below the melting point (13),(14). In addition, the possibility of doping at room temperature and the ability to grow large single crystals in bulk by the melt growth method during substrate fabrication have been recognised as strong virtues in the production process. β–Ga_2O_3 has a bandgap of 4.5–4.9 eV (15), which is higher compared to that of GaN, GaAs, and 4H–SiC, which have a bandgap of 3.4, 1.4, and 3.3 eV, respectively. Furthermore, theoretical calculations predict that β–Ga_2O_3 should exhibit less on-resistance and a higher breakdown voltage than Si, GaN, GaAs, and 4H–SiC (16). These properties underpin the status of β–Ga_2O_3 as a promising candidate for power semiconductor devices.

This thesis attempts to investigate the property of beta-gallium oxide as a power device by fabricating metal-oxide-semiconductor (MOS) capacitors, study bulk and interface related electrically active defects, and suggest a path to develop metal-oxide-semiconductor field effect transistor (MOSFET). In the MOS structure, comparative experiments are carried out under the same conditions as the conventional 4H–SiC substrate, with a focus on the extraction of the characteristics of the MOSFET using gallium oxide. I–V and C–V curves are obtained to determine the electrical properties, and the values of the extracted parameters are calculated. In addition, the features of bulk and interface characteristics are examined by deep-level transient spectroscopy (DLTS) and thermally dielectric relaxation current (TDRC). In addition, defect states in β–Ga_2O_3 bulk are investigated using proton irradiation. Fabrication of MOSFETs and MESFETs are also attempted.

2 BACKGROUND

This chapter provides an overview of the basic theory related to the subject of this thesis. Therefore, this chapter considers the structure of a solid (crystal), and the reasons for defects present within it. Subsequently, the characteristics obtained by the MOS and MOSFET from the junctions are investigated. Defects are a useful concept when describing the driving of non-ideal devices in the future.

2.1 Structure of a solid

This section is based on the textbook by Callister(17), Kittel(18), and Hu(19) discussing basic solid state physics.

Crystal structure is the most fundamental concept for classifying solid materials. It is composed of atoms or ions arranged regularly as small repeating entities called primitive unit cells, which consist of a basis and lattice. A lattice is a three-dimensional array of points and a basis is a group of atoms that placed in the same lattice. In other words, the atomic group is called basis, and the set of mathematical point that basis is placed is called lattice. In a crystalline material, atoms are positioned in an array with three-dimensional periodicity. These small repeating units are termed unit cells. This indicates symmetry of the crystal structure, which means that the position of the atoms in the crystal can be determined by translation along each of its edges. Thus, the unit cell plays an important role in determining the virtual geometry and the position of atoms in the crystal. The structure of the crystal depends upon bonding with the nearest neighbouring atoms. The most energetically stable case is the close packing of the atoms. This is usually represented by rounded spheres whereby each sphere represents an ion core. The three most common models in nature are face-centred cubic, body-centred cubic, and hexagonal close-packed.

Crystal systems

As there are a lot of possible configurations of the crystal structure, it is convenient to define groups according to the arrangement of the unit cells or the atoms. First, the geometry of the unit cell is defined by six variables. The x, y, and z axes are aligned parallel to the three directions from the corners, where a, b, and c represent the unit cell lengths, and interaxial angles are defined by α, β, and γ. These are termed the lattice parameters of the crystal structure. Accordingly, seven different combinations of crystal systems exist with different a, b, and c and α, β, and γ.

Point coordinates: crystallographic points, directions, and planes

Crystallographic points, directions, and planes are defined by indexing schemes. In terms of point locations and directional indices, they are defined with coordinates and vector projections on each of the coordinate axes respectively. With the reciprocals of axial intercepts, the planar or Miller indices (as hkl) are decided.

In these three dimensions, space groups are classified under seven crystal systems along with lattice types. The space groups which pertain to the seven crystal systems consist of 14 Bravais lattices and 32 crystallographic point groups. Accordingly, space groups are further delineated in the translational symmetry of the unit cell, which has operations such as rotation, reflection, and

inversion. On account of the constituents of translation and the screw axis in the space group, a glide plane exists. These combinations of symmetry operation bring about the definition of 230 space groups with crystal symmetries. Based on this geometric property of solids, crystallography has been studied by, for example X-ray diffraction for determination of crystal structures and to enable visualisation.

2.2 Defects in crystals

The above description of crystals neglects the structures and symmetries of crystal defects and imperfections. The material properties of a perfect crystal structure without any defects is more easily predicted than the properties of a crystal with defects, however, substantial imperfections exist in real bulk crystals. Thus, these defects play an important role in determining the properties of the materials.

The classification of defects depends largely on dimensionality. From the lowest to the highest dimensional defect, point defects, line defects, area defects, and volume defects can be defined. These four types of defects are each triggered by a different mechanism. A point defect may exist due to vacancies, interstitials, and impure atoms, while two-dimensional (area) defect and three-dimensional (volume) defects result from, for example, stacking faults, grain boundaries, precipitates and voids respectively.

Point defects are especially important to explain doping and diffusion. For single crystalline materials, 1, 2 and 3 dimensional defects may be sufficiently supressed, and point defects become particularly diffuse. In addition, they are highly relevant for bulk electronical properties with several mechanisms of electrical charges. In the following, intrinsic and extrinsic defects are explained separately.

2.2.1 Intrinsic defects

Intrinsic defects consist of two types of point defects. This defect type occurs where atoms are missing from their original locations, resulting in a vacancy, or when an atom occupies an interstitial site.

Above 0 K, defects occur in a crystal structure. The formation of defects is related to thermodynamic phenomena, as intrinsic point defects exist due to the increase in the configuration entropy of crystal. All solids tend to become thermodynamically stable by introducing disorder or defects.

$$G = H - TS \tag{2. 1}$$

Where G is the Gibbs free energy, H enthalpy, T absolute temperature, and S entropy. For temperatures above 0 K, Gibbs free energy is reduced by introducing defects.

Two types of stoichiometric defect formation can be defined. One is the Schottky defect, which is formed by a vacancy–vacancy pair. In this process, no mass is transferred, and the ratio of cations and anions does not change. As an example, the Schottky defect reaction of Ga_2O_3 is:

$$\emptyset \rightleftharpoons 2V_{Ga}^{-3} + 3V_O^{+2} \quad (2.2)$$

Where $\emptyset$ denotes the null reactant, V the vacancy on the original site, and $-$ and $+$ indicate negative and positive charge, respectively. Thus $2V_{Ga}^{-3}$ describes two vacancies of $Al^{+3}$and $3V_O^{+2}$ indicates three oxygen ion vacancies. In this process, the concentration of both charges is in the equilibrium state.

The second type of point defect is the Frenkel defect, which is formed by a vacancy–interstitial pair. It forms a vacancy site on the cation or anion sublattice, in accordance with the same lattice of an interstitial site.

$$\emptyset \rightleftharpoons V_{Ga}^{-3} + Ga_i^{+3} \rightleftharpoons V_O^{+2} + O_i^{-2} \quad (2.3)$$

In this equation, i indicates the interstitial site. This indicates that a vacancy is created when a cation or anion leaves its original site in the sublattice. Other types of interstitial defects include self-interstitials that contain only the same atoms in the lattice, and impurity interstitials that are present in the off-lattice.

2.2.2 Extrinsic defects

An extrinsic defect refers to a defect driven into the bulk for a specific purpose, or impurities. This defect type can be roughly classified under two titles; foreign atoms and impurities. A foreign atom is intentionally introduced impurities like dopants, while an impurity signifies that its addition is not intentional.

If the foreign atom is placed on an interstitial site then it is termed an interstitial impurity; and where the foreign atom occupies a lattice site, it is called a substitutional solute or impurity. Atoms that typically are found on interstitial sites are relatively small, for instance carbon, nitrogen, and hydrogen. Therefore, types of solute atoms are highly dependent on size, while the larger size of atom is located in a substitutional site. Extrinsic defects can affect the characteristics of carriers, such as doping which changes of conductivity in the semiconductor, and are a useful tool for semiconductor applications and engineering, as they can generate various electrical properties and enhance mechanical strength.

2.3 Semiconductor physics

The characteristics of semiconductor materials arise from their different junctions, which are highly effective when implementing a switching function without a mechanical device. This has been studied in various ways to improve performance. Therefore, understanding the electrical characteristics of semiconductors is the first step to understanding power devices. This section considers the crystal structure of semiconductors, as dealt with in the textbook by Streetman et al.(20).

2.3.1 Energy band and band structure

Electrons in an atom are confined to a series of discontinuous energy levels (energy values). Continuity of independent atoms causes overlapping of the quantum mechanical wave function, so that a band is formed. That is to say, there is a range of energy values that an electron can use in a solid. In the case of semiconductor materials, the energy band structure is fundamentally insulator-like at 0 K. The gap between the occupied and non-occupied states at 0K is the bandgap. When the uppermost filled band is called valence band, and the unoccupied band is called conduction band. The valence band is completely filled with electrons, and the conduction band is empty. However, since semiconductors have a smaller band gap (E_g) than insulators, electrons can excited to a conduction band when they are subjected to thermal or optical energy. Therefore, the number of electrons that can contribute to conduction in the semiconductor can be greatly increased.

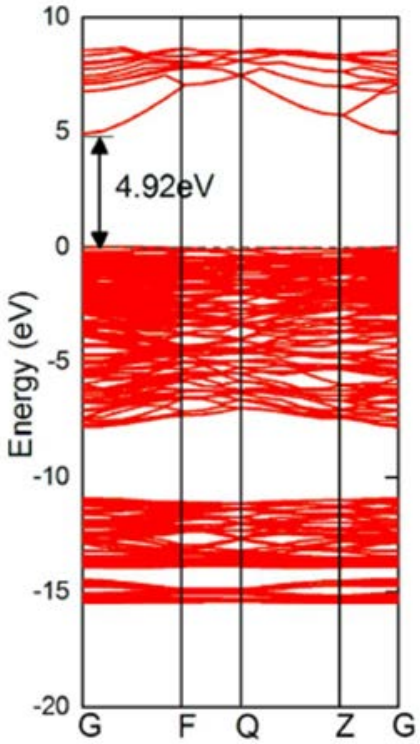


Figure 2. 1 The results of DFT with β–Ga_2O_3. This illustrates the direct bandgap between conduction and valence bands of 4.92 eV at point *G*. This value is larger than for Si, SiC, and GaN. (21)

Figure 2. 1 shows the band structure of β–Ga_2O_3 using the density functional theory (DFT) from Dong, L. P et al (21). The usable energy states are plotted using the wave vector k in the reciprocal space. This results from the calculation of the dispersion relation $E_n(k)$ for each band, n. For this study, points are selected in the reciprocal space corresponding to the crystal direction before energy is drawn as a function of k.

Research on the bandgap of gallium oxide is still continuing. According to other first-principles studies of Ga_2O_3(14, 22), the conduction band minimum is found at the gamma point, but since the valence band maximum is almost flat, there are various opinions on this. Thus, studies still display

uncertainty on whether the bandgap is direct or indirect. On the other hand, the calculated band gap is reported to be about 4.5-4.9 eV. This is a larger gap than for Si (1.1 eV), GaN and SiC (3.3 eV and 3.4 eV respectively), which are the most widely used semiconductor materials for power electronics. Large band gap enable the implementation of devices with high breakdown voltage and high efficiency.

2.3.2 Charge carriers

The electrons in the solid follow the Fermi–Dirac distribution.

$$f(E) = \frac{1}{1 + e^{\frac{(E-E_F)}{kT}}} \tag{2. 4}$$

Where k is the Boltzmann constant, E_F is the fermi level, and the function $f(E)$ is a Fermi–Dirac distribution function, which represents the probability that the electrons are occupying at absolute temperature T. The above equation has a value of 1 if $E<E_F$ at absolute temperature 0, which means that electron states are fully occupied at the energy level satisfying $E<E_F$ condition since $f(E) = \frac{1}{1+\frac{1}{\infty}} = 1$. However, under the condition of $E>E_F$, $f(E) = \frac{1}{1+\infty} = 0$, the probability of finding an electron becomes zero. For any of the temperature T, $E=E_F$ is expressed as the occupancy

$$f(E_F) = \left[1 + \frac{e^{(E_F-E_F)}}{kT}\right]^{-1} = \frac{1}{1+1} = \frac{1}{2} \tag{2. 5}$$

This means that the Fermi level is an energy level of half probability of electrons being filled at any temperature T. In the n-type semiconductor material, the electron density of the conduction band is larger, so that the distribution function $f(E)$ is located above the intrinsic semiconductor. In the case of a p-type semiconductor, the opposite is true.

2.3.3 Carrier concentration

In order for current to be generated in a semiconductor device, electrons must be excited from the valence band into the conduction band. The energy required to excite the electrons is equal to or larger than the bandgap. The electrons excited by the conduction band move freely in the available state, and leaving the unoccupied state of electrons in the balance band. This state is called a hole. When other electrons enter the place of hole, the hole contributes to current by moving in the other direction as a positive carrier. At temperatures above 0 K, the electron's thermal energy distribution provides a rate at which electrons are excited into the conduction band.

To obtain the total electron concentration, the integral of the entire conduction band is used. This integration result is simply the same as multiplying the effective state density at conduction band energy sate (E_c) with the occupancy probability at E_c; $n_0 = \mathrm{n}_c f(E_c)$. Here, $f(E_c)$ can be simplified

and expressed as $f(E_c) = \frac{1}{1+\frac{e^{-(E_c-E_F)}}{kT}} \simeq e^{\frac{-E_c-E_F}{kT}}$. Therefore, the electron concentration of the conduction band and the hole concentration of the valence band are:

$$n_0 = N_c e^{-(E_c-E_F)/kT} \quad (2.\ 6)$$

$$p_0 = N_v e^{-(E_F-E_v)/kT} \quad (2.\ 7)$$

Where N_c and N_v indicate the effective density of states in each band.

$$N_c = 2\left(\frac{2\pi m_n^* kT}{h^2}\right)^{\frac{3}{2}} \quad (2.\ 8)$$

$$N_v = 2\left(\frac{2\pi m_p^* kT}{h^2}\right)^{\frac{3}{2}} \quad (2.\ 9)$$

Here, m_n^* and m_p^* denote the effective mass for electrons and holes, respectively, and h is the Planck constant. In an intrinsic semiconductor, E_F is located at some intrinsic energy level E_i near the centre of the energy bandgap. The intrinsic electron and hole concentrations are $n_i = N_c e^{-(E_c-E_i)/kT}$ and $p_i = N_v e^{-(E_i-E_v)/kT}$. This can be expressed as per the equations below:

$$n_0 = n_i e^{(E_F-E_i)/kT} \quad (2.\ 10)$$

$$p_0 = N_v e^{-(E_F-E_v)/kT} \quad (2.\ 11)$$

By applying equations (2. 6) and (2. 7) in the equilibrium state, the product of n_0 and p_0 is constant for a certain material and temperature. Thus from $n_0 p_0$ and $n_i p_i$ it is possible to obtain $N_c N_v e^{-Eg/kT}$. Moreover, since carriers are generated in pairs, $n_i = n_p$. Therefore, $n_i = \sqrt{N_c N_v} e^{-Eg/2kT}$. The relationship between electron and hole concentrations and the intrinsic carrier concentration can be written as:

$$n_o p_0 = n_i^2 \quad (2.\ 12)$$

2.3.4 Defect levels

The defect levels present inside the band gap of a semiconductor can capture and emit carriers. Thus, the defect levels can act as donors or acceptors, i. e. either donating or accepting an electron. In addition, by interacting with the conductive band or valence band, they can affect the electrical properties of the material. Defect levels close to the conduction or valence band are considered as shallow, and typically used to modify the change carrier concentration, while deep levels can act as recombination or trapping centres. For this reason, the study of the deep level both in the bulk and

at the interface is an important when studying device characteristics and quality. Hence, the electrical properties of deep levels are considered in Chapter 5.3.

This section builds a base for the elaboration of deep level transient spectroscopy (DLTS), based on the work of Blood and Orton (23).

At the interface or a surface the crystal structure is disrupted, resulting in unsatisfied dangling bonds. Therefore, a comparatively large amount of charge states are generated at the interface between semiconductor and for example an oxide layer, and electrons and holes are likely to be captured or emitted. Four types of defects or charges are usually present at the semiconductor and oxide layer interface: fixed oxide charge (Q_f), interface trapped charge (Q_{it}), mobile oxide charge (Q_m), and oxide trapped charge (Q_{ot}).

In addition, these charge states of the interface traps tend to depend on voltage. Therefore, they affect the C–V trace. For example fixed charge causes a shift of the flatband voltage, while the interfacial states affect the slope of the C–V trace during depletion.

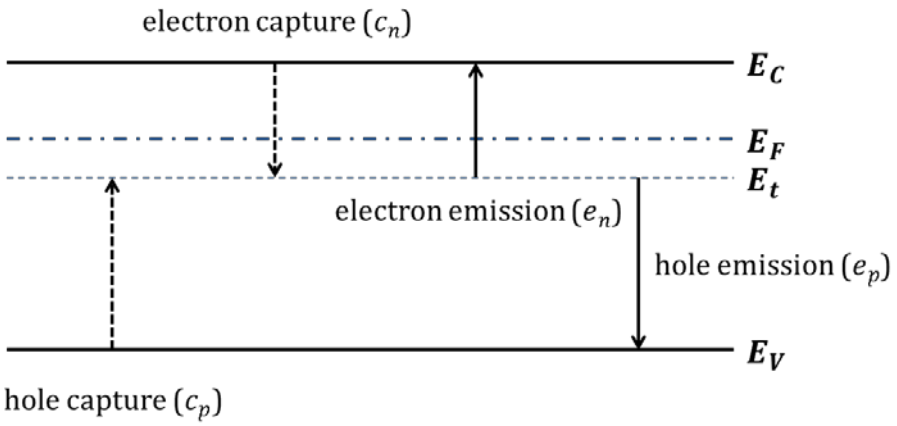


Figure 2.1 Emission and capture of carriers in the deep trap in the n type semiconductor.

A state within the band gap can interact with the conduction and valence band, where four processes are identified. Figure 2.1 illustrates the possible electronic processes occurring in the deep trap. Carriers can be captured or emitted to the conduction or valence band when they obtain thermal or radiation energy. From the left, the figure shows hole capture (c_p) from the valence band, electron capture (c_n) from the conduction band, electron emission (e_n) to the conduction band, and hole emission (e_p) to the valence band. Generally, where the trap is located near the middle of the band gap, a recombination centre is found, which reduces the lifetime of a carrier when applied in optical devices. Thus, understanding traps is one of the important factors when fabricating and evaluating an MOS device.

The capture process is characterized by a capture cross-section, σ. The process of capture and emission depends on the occupancy of carriers. e_n and c_p processes are occupied by electrons at n_t

state, while e_p and c_n are unoccupied by electrons at the (N_t-n_t) state, where N_t and n_t are the concentration of deep centres and electron occupancy of the trap at any moment, respectively.

Capture rate

The capture rate is characterised by the electron flux across an area per unit time. Assuming a free electron density n has a thermal velocity $\langle v \rangle$ in $(N_t - n_t)$ with cross-section σ_n. The difference of occupancy in a short time interval Δt is:

$$\Delta n_t = \sigma_n \langle v \rangle n (N_t - n_t) \Delta t \tag{2. 13}$$

And electron capture rate per unoccupied state is:

$$c_n = \frac{\frac{\Delta n_t}{\Delta t}}{N_t - n_t}$$

$$c_n = \sigma_n \langle v \rangle n \tag{2. 14}$$

In practice, c_n and $c_p$largely depend on doping of the sample. In other words, the free carrier concentration is determined by the above equation.

Emission rate

The emission rate can be described in terms of electron occupancy using the velocity equation:

$$\frac{-dn_t}{dt} = (c_n + e_p)(N_t - n_t) - (e_n + c_p) n_t \tag{2. 15}$$

In the thermal equilibrium state, $\frac{dn_t}{dt} = 0$ and$\frac{dp_t}{dt} = 0$, thus the rates of emission and capture of electrons and holes must be equal, leading to:

$$e_n n_t = c_n (N_t - n_t) \tag{2. 16}$$

$$c_p n_t = e_p (N_t - n_t) \tag{2. 17}$$

By rearranging the equation with respect to the thermal equilibrium occupancy $\hat{n}_t$ one obtains:

$$\frac{\hat{n}_t}{N_t} = \frac{c_n}{c_n + e_n} = \frac{e_p}{e_p + c_p} \tag{2. 18}$$

Another expression related to the occupancy is contributed by the Fermi–Dirac distribution function:

$$\frac{\hat{n}_t}{N_t} = \left\{1 + \frac{g_0}{g_1}\exp\left(\frac{E_t - E_F}{kT}\right)\right\}^{-1} \quad (2.\ 19)$$

Where g_0 is the degeneracy of the unoccupied state and g_1 indicates the occupied state by an electron. It can be omitted since the ratio of them is close to 1. This equation can be written with equation (2. 16) and (2. 17).

$$\frac{e_n}{c_n} = \exp\left(\frac{E_t - E_F}{kT}\right) \quad (2.\ 20)$$

$$\frac{e_p}{c_p} = \exp\left(\frac{E_F - E_t}{kT}\right) \quad (2.\ 21)$$

From these two equations, the ratio of capture to emission rate is obtained. Thus, the capture and emission of electrons and holes is influenced by the position of the Fermi level, since the capture rate is affected by the free carrier concentration, as described in equation ((2. 6). In the case of a non-degenerate semiconductor in thermal equilibrium, trap density for electrons n_t, and trap density for holes p_t are given by the following equations:

$$n_t = N_t\left[1 + \left\{\frac{-(E_t - E_F)}{kT}\right\}\right]^{-1} \quad (2.\ 22)$$

$$p_t = N_t\left[1 + \left\{\frac{-(E_V - E_t)}{kT}\right\}\right]^{-1} \quad (2.\ 23)$$

The trap occupancy is determined by the Fermi–Dirac function. To obtain the electron and hole emission rates, equation (2. 14) is placed into equations (2. 20) and (2. 21):

$$e_n(T) = \sigma_n\langle v_n\rangle N_c\, exp\left(-\frac{E_c - E_t}{kT}\right) \quad (2.\ 24)$$

$$e_p(T) = \sigma_p\langle v_p\rangle N_v\, exp\left(-\frac{E_t - E_v}{kT}\right) \quad (2.\ 25)$$

The two equations above express emission rates e_n and e_p with the capture cross-section and energy separation of the trap energy level from the band edge. To provide further information about capture and the emission processes, temperature dependence is introduced. The thermal velocity $\langle v_n\rangle$ and density of states N_c are described as

$$\langle v_n\rangle = \left(\frac{3kt}{m^*}\right)^{\frac{1}{2}} \quad (2.\ 26)$$

The capture cross-section is applied by the activation energy, and when σ is extrapolated to infinite temperature (σ_∞),

$$\sigma(T) = \sigma_\infty exp\left(-\frac{\Delta E_\sigma}{kT}\right) \quad (2.27)$$

The temperature dependence of e_n(T) can be explained as:

$$e_n(T) = \gamma T^2 \sigma_{na} exp\left(\frac{-E_{na}}{kT}\right) \quad (2.28)$$

Where $\gamma = 2\sqrt{3}(2\pi)^{\frac{3}{2}}k^2 m^* h^{-3}$ and $\sigma_{\text{na}} = \frac{g_0}{g_1}\sigma_\infty$. Hence, $\frac{e_n}{T^2}$ with T^{-1}makes a trap signature plot. E_{na} is defined as $(E_c - E_t) + \Delta E_\sigma$, and assumes that $E_c - E_t$is temperature independent. In the case of σ_{na}, as described earlier, this implies that $T = \infty$ and is affected by the degeneracy ratio. This is modified when $(E_c - E_t)$ is temperature dependent. However, E_{na} and σ_{na} do not appear exactly as the expected values for the actual capture cross-section, σ_n. This is explained by thermodynamics; the activation energy is due to the enthalpy of ionization formation, and the apparent cross-section σ_{na} contains entropy (24). Although E_{na} and σ_{na} do not directly represent energy levels and capture cross-sections, they can be used for signatures in traps.

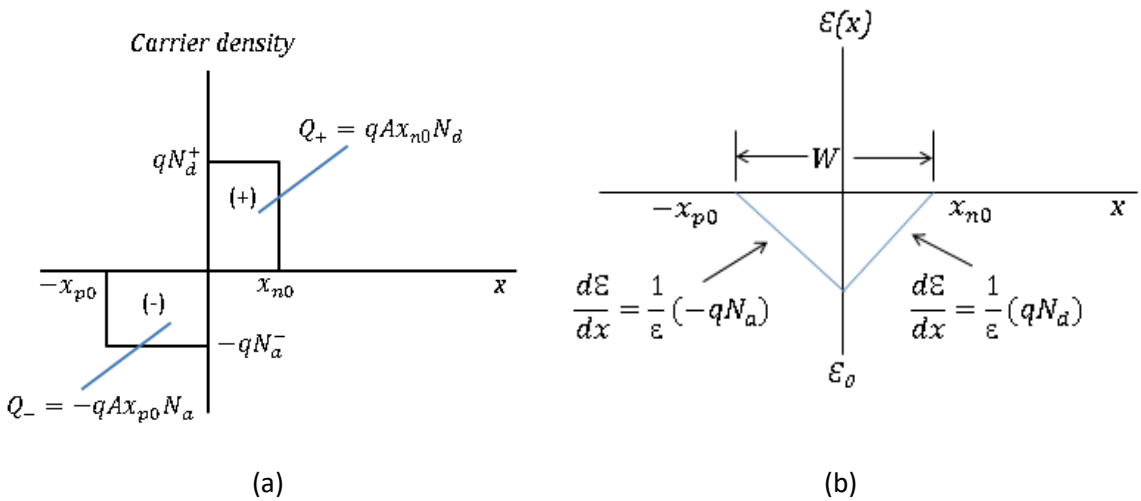
2.4 P–N junction

The majority of electronic devices, the junction of semiconductor materials with different carriers are utilized. First, consider the junction between a p-type and n-type semiconductors. In such a junction in thermal equilibrium will balance the diffusion of charge carriers across the junction.

The electric field $\mathcal{E}$ is increased until the actual current becomes zero in the equilibrium state. This electric field appears in an area W near the junction, and an equilibrium potential difference V_0 between the p and n side arise. This region W is called the depletion region, and the potential difference V_0 is called the contact potential. The contact potential across W is a built-in potential barrier, and this barrier is necessary to maintain equilibrium in the junction. At the junction, this transition region may be asymmetrically positioned depending on the doping concentration on the p and n side. Assume that there are no free carriers at the transition region, then the carrier density will be $Q_- = Q_+$. This relationship can be written as:

$$qAx_{p0}N_a = qAx_{n0}N_d \quad (2.29)$$

Where A is the cross-section of sample, x_{p0} and x_{n0} are the penetration distance of the space charge region into the p-type and n-type material, and N_a N_d indicate the ionised acceptor and donor, respectively. Therefore, the width W of the transition region is the sum of x_{p0} and x_{n0}.



(a) (b)

Figure 2. 2 Carrier density in the transition region (a) at equilibrium state and (b) electric field distribution.

Now, examine the electric field distribution in this depletion region. Assuming that all of the dopant impurities are ionised, we obtain two uniform space charge regions using the Poisson equation.

$$\frac{d\mathcal{E}}{dx} = \frac{q}{\varepsilon}N_d, \qquad 0 < x < x_{n0} \tag{2. 30}$$

$$\frac{d\mathcal{E}}{dx} = -\frac{q}{\varepsilon}N_a, \qquad -x_{p0} < x < 0$$

As can be seen in Figure 2.2 (b), the electric field increases with x on the n-type side, and decreases on the p-type side. In addition, at x = 0 the electric field $\mathcal{E}_0$ has the maximum value, and $\mathcal{E}(x)$ in the transition region is negative everywhere. The value of $\mathcal{E}_0$ can be obtained by integrating one side of equation (2. 30), and therefore the maximum value of the electric field is as follows:

$$\mathcal{E}_0 = -\frac{q}{\varepsilon}N_d x_{n0} = -\frac{q}{\varepsilon}N_a x_{p0} \tag{2. 31}$$

Since the electric potential $\mathcal{E}$ at the arbitrary point x has a negative value for the potential gradient, the relationship with built-in potential V_0 and electric field is:

$$\mathcal{E}(x) = -\frac{dV(x)}{dx} \; or \; -V_0 = \int_{-x_{p0}}^{x_{n0}} \mathcal{E}(x)dx \tag{2. 32}$$

As can be seen from the above equation, the contact potential difference is the area of triangle of $\mathcal{E}(x)$ and x. The equation can be rewritten by relating the contact potential difference to the width of the depletion region:

$$V_0 = -\frac{1}{2}\mathcal{E}_0 W = \frac{1}{2}\frac{q}{\varepsilon}N_d x_{n0} W \tag{2. 33}$$

In this state, a balance of charges must be achieved. Thus, $x_{n0}N_d = x_{p0}N_a$ and W is $x_{p0} - x_{n0}$. Equation (2. 33) and these conditions produce $x_{n0} = \frac{WNa}{(N_a+N_d)}$. Applied to the above equation,

$$V_0 = \frac{1}{2}\frac{q}{\varepsilon}\frac{(N_a N_d)}{N_a + N_d}W^2 \tag{2. 34}$$

When rearranged for W, it can be seen that the equation for the width of the potential region is composed of the contact potential difference, the doping concentration, and the terms of the integers that are already known; q and ε (equation (2. 35))

$$W = \sqrt{\frac{2\varepsilon V_0}{q}\left(\frac{N_a + N_d}{N_a N_d}\right)} = \sqrt{\frac{2\varepsilon V_0}{q}\left(\frac{1}{N_a} + \frac{1}{N_d}\right)} \tag{2. 35}$$

When a reverse bias $V_r$is applied, this built-in voltage increases by qV_r and decreases when the forward bias $V_f$is applied. Thus the barrier is adjusted along with the applied voltage.

Now, consider junctions with forward and reverse bias applied. Diffusion currents in toward bias, across the barrier prevail, but this current is negligible in the case of reverse bias. This is because the barrier increases with the bias V_r with built-in voltage. On the other hand, the drift current is relatively insensitive to the height of the potential barrier. The minority carriers participating in this current are generated by thermal excitation of the electron–hole pair (EHP) near the junction. This current can be significantly increased by exciting the EHP optically, as done in photodiodes. The total current through the junction is the sum of these two components; diffusion and drift current components.

At the forward bias $V = V_f$ increases the probability that the carrier will diffuse by a factor $exp\left(\frac{qV}{kT}\right)$, while at the reverse bias $V = -V_r$ decreases. Therefore, when any bias is applied, the diffusion current is simply $|I| \exp\left(\frac{qV}{kT}\right)$.

Therefore, the total current I is the diffusion current minus the absolute value of the generation current:

$$I = I_0(e^{\frac{qV}{kT}} - 1) \tag{2. 36}$$

In the above equation, V can be positive or negative, and $I_0$is the reverse saturation current. When V is positive and larger than a minority of kT/q, the exponential term is greater than 1. Thus, the current is exponentially increased within V_f. If V is negative (V_r), the current becomes $-I_0$ and saturates at a large V_r.

An ideal diode follows this equation, but for real diodes, it is necessary to consider the carriers that are generated and recombined in the transition region. If the width W of the transition region is not small enough compared to the carrier diffusion length $L_n = \sqrt{D_n \tau_n}$ and $L_p = \sqrt{D_p \tau_p}$, then significant recombination is produced in this region. The current due to recombination is proportional to n_i^2/N_d and n_i^2/N_a, and increases with $exp(\frac{qV}{kT})$. This discordance can be expressed:

$$I = I_0'(e^{\frac{qV}{nkT}} - 1) \tag{2. 37}$$

with the ideality factor *n*.

To examine capacitance from the junction, start from the charge Q value from equation (2. 29), which is expressed in terms of doping concentration and transition region width. If the overall width W of the transition region is divided into x_{n0} and x_{p0},

$$x_{no} = \frac{N_a}{N_a + N_d} W, x_{p0} = \frac{N_d}{N_a + N_d} W \tag{2. 38}$$

And the charge of each side of the dipole is as follows:

$$|Q| = qA \frac{N_d N_a}{N_d + N_a} W = A \left[2q\epsilon (V_0 - V) \frac{N_d N_a}{N_d + N_a} \right]^{\frac{1}{2}} \tag{2. 39}$$

With the general formula of capacitance, $C = \left| \frac{dQ}{dV} \right|$, and equation (2. 39),

$$C_j = \left| \frac{dQ}{d(V_0 - V)} \right| = \frac{A}{2} \left[\frac{2q\epsilon}{V_0 - V} \frac{N_d N_a}{N_d + N_a} \right]^{\frac{1}{2}} \tag{2. 40}$$

C_j is the voltage variable capacitance, since it is proportional to $(V_0 - V)$. The parallel plate capacitor formula is obtained from the equations of $C_j$and W:

$$C_j = \epsilon A \left[\frac{2}{2\epsilon (V_0 - V)} \frac{N_d N_a}{N_d + N_a} \right]^{\frac{1}{2}} = \frac{\epsilon A}{W} \tag{2. 41}$$

Similar to the parallel plate capacitor, the width W of the depletion region corresponds to the plate separation of the conventional capacitors. Asymmetrical junctions, for example p^+–n junctions, have a different depletion region width due to the difference of doping concentration. The capacitance for the lower doped side, n, becomes:

$$C_j = A \sqrt{\frac{\epsilon q}{2(V_0 - V)} N_{a,d}} \tag{2. 42}$$

2.5 Metal–semiconductor junction

2.5.1 Schottky contacts

Generally, a rectifying contact between a metal and the semiconductor is referred to as Schottky barrier diode. In the case of n-type semiconductors, charge transfer occurs until the Fermi level coincides with the metal having a larger work function. The contact potential V_0 arises and found the difference in work function between metal and semiconductor. The resulting barrier is called a Schottky barrier (ϕ_B), and the height ϕ_B of the potential barrier is $\Phi_m - \chi$, where Φ_m is work

function of metal, and χ is electron affinity. A depletion region W is formed near the junction, and the junction capacitance is $A\epsilon_s/W$ – as in the p–n junction when the p⁺–n type junction is formed. The height of this barrier and the current are regulated according to the applied voltage similar to the in p-n junction.

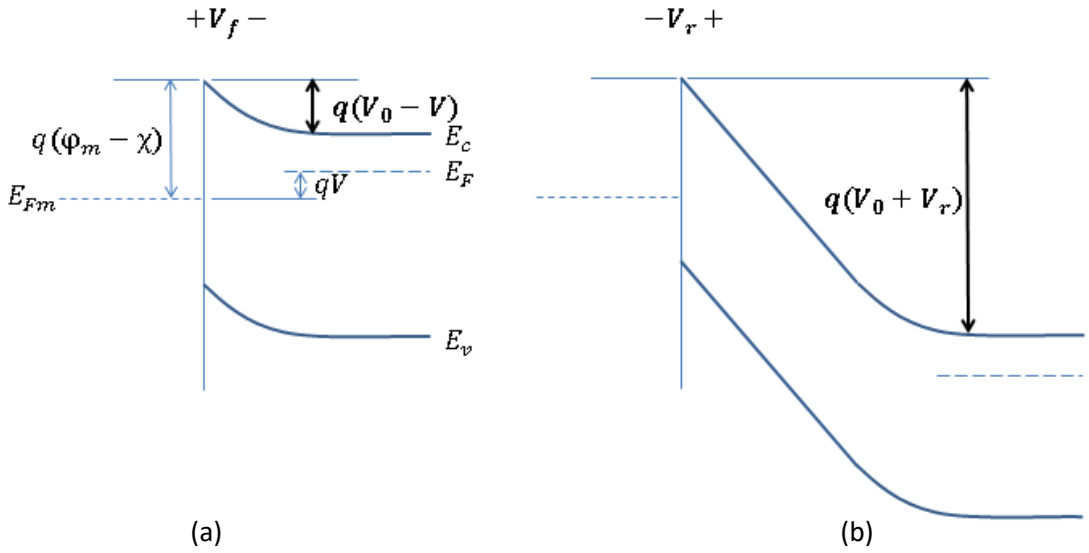


Figure 2. 3 Schottky barrier of metal and n-type semiconductor differences, displayed with applied voltage.

However, in contrast to p-n junctions, these characteristics make the Schottky diode rectifying. The absence of charge accumulation during the time delay due to the injection of minority carriers demonstrates that Schottky barrier diodes are suitable for high-frequency and high-speed switching devices.

2.5.2 Ohmic junctions

Unlike Schottky contacts, Ohmic contact does not provide rectification. This property is a appropriate condition to use for contacts that must react linearly and quickly to an applied voltage. For example, the contact area of the device should have low resistance for the migration of the carriers with the bias. In the case of metal contact with n-type semiconductors, charge is supplied from the semiconductor with work function condition $\Phi_m < \Phi_s$. Electrons are transferred from the metal to the semiconductor to match the Fermi level in the equilibrium state and relatively increase the electron energy of the semiconductor. In this case, the barrier is low and easily overcome by the voltage.

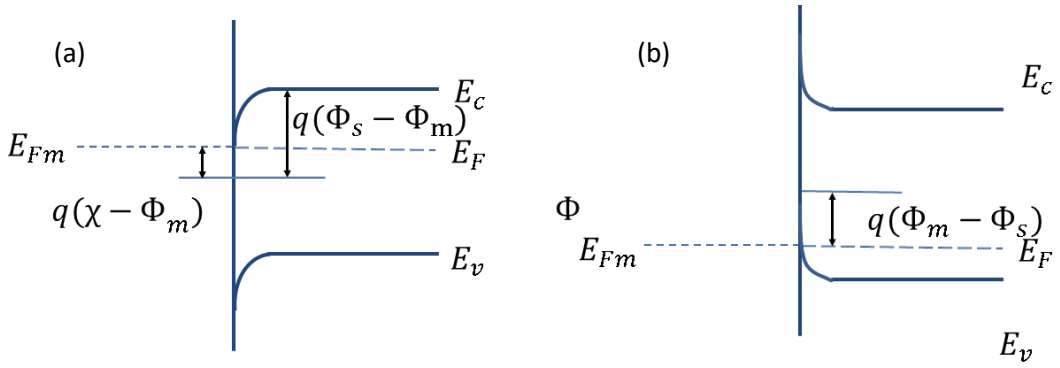


Figure 2. 4 Ohmic contact of metal–n-type semiconductor (a), and with p-type semiconductor (b). Ohmic contact formed with condition $\Phi_m < \Phi_s$ for n-type semiconductor, and $\Phi_s < \Phi_m$ for p-type semiconductor.

2.6 MOS and MOSFET

The metal-oxide-semiconductor structure (MOS) is achieved by deposition a metal contact and an oxide layer on a semiconductor. It has the properties of a capacitor and utilized in field effect transistors (MOSFET). This chapter describes the principles of the transistor using the MOS stack and the field effect transistor with an MOS structure.

2.6.1 MOS capacitor

Here, an ideal MOS capacitor with an n-type semiconductor is assumed. Figure 2. 5 indicate different modes of operation and assuming an n-type semiconductor substrate.

When a positive voltage is applied to the gate, the state is called accumulation since electrons of the semiconductor substrate are attracted to the oxide–semiconductor interface. Depletion occurs when a negative voltage is applied to the gate. The applied negative voltage pushes the mobile electrons back towards the substrate, and eventually the semiconductor is depleted at the interface. The voltage dividing the accumulation and depletion regions is called a flatband voltage (V_{FB}) (Figure 2. 5 (c)). Applying a larger negative voltage across the threshold voltage (V_{TH}) results in a positively charged inversion layer at the oxide–semiconductor interface in addition to the depletion region, where minority carriers dominate.

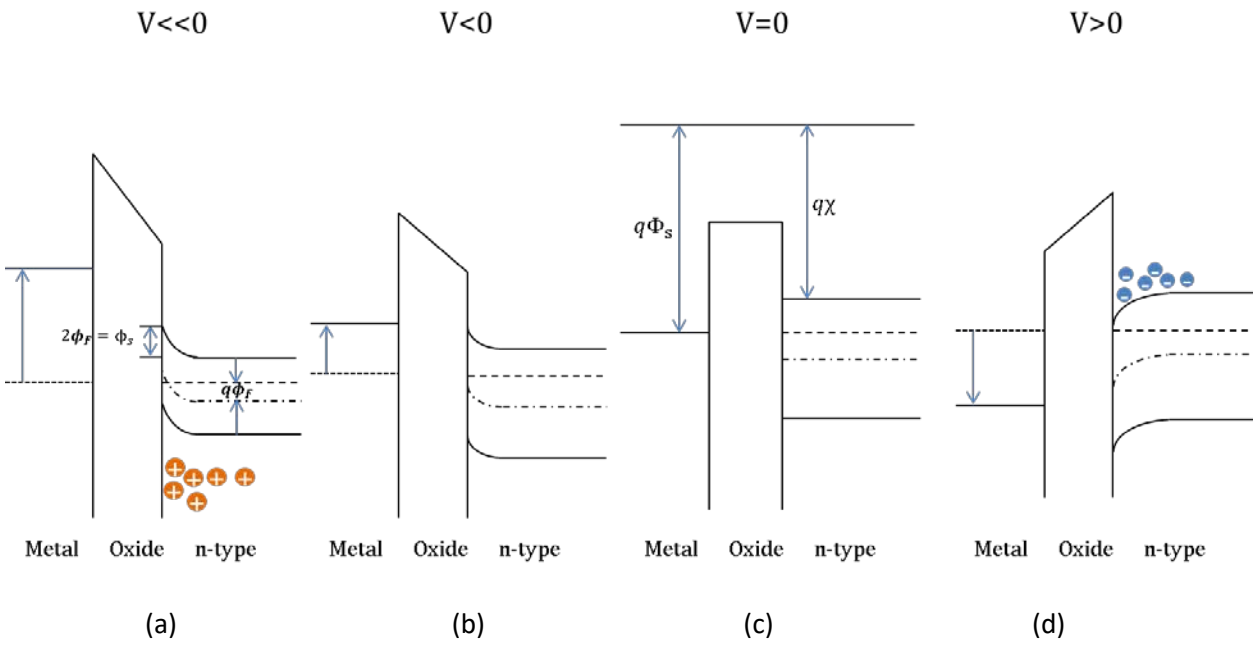


Figure 2. 5 Ideal operation of an MOS capacitor in accordance with applied voltage and n-type semiconductor (20), showing (a) inversion, (b) depletion, (c) flatband, and (d) accumulation state.

Flatband condition

For an ideal capacitor, the work function of the metal and semiconductor are the same, $\Phi_m = \Phi_s$, but not in actual devices due to for example fixed and mobile charge in the oxide, and imperfect surface states. In the ideal situation, surface electric field in the substrate at the flatband state is zero. Therefore, the electric field within the oxide also becomes zero. The voltage V_{FB} satisfying this condition is:

$$V_{FB} = \Phi_m - \Phi_s \tag{2. 43}$$

Accumulation

If the voltage applied to the gate V_g is larger than V_{FB}, the band of the semiconductor is pushed downwards, and produces the state of being able to accumulate electrons (Figure 2. 5, (d)). Therefore, when V_G is not the same as V_{FB}, and V_{ox} (oxide voltage) is not zero.

$$V_G = V_{FB} + \phi_s + V_{ox} \tag{2. 44}$$

The conditions satisfying the flatband are $V_G = V_{FB}$, $\phi_s = V_{ox}$ and it should satisfy the (2. 44) as well. In surface accumulation, however, the value of ϕ_s is quite small and can be ignored. Thus V_{ox} in the surface accumulation is $V_{ox} = V_G - V_{FB}$. With the application of Gauss's law, $\epsilon_{ox} = -Q_{ac}/\varepsilon_{ox}$, the equation about oxide voltage become equation(2. 45). Where ϵ_{ox} is an electric field caused by the

potential difference generated across the oxide layer, and Q_{ac} and ε_{ox} represent the accumulated charge at the surface and oxide permittivity, respectively.

$$V_{ox} = \epsilon_{ox} T_{ox} = -\frac{Q_{sub}}{C_i} \tag{2. 45}$$

This equation is generally used for capacitance ($V=Q/C$). C_i and Q_{sub} indicate oxide (insulator) capacitance per unit area and charge in the substrate.

Depletion

When a more negative V_G than V_{FB} is applied, a depletion region is formed near the surface. As a result, there are less electron and hole densities in this region. Here, equation(2. 45) implies that:

$$V_{ox} = -\frac{Q_{sub}}{C_i} = -\frac{Q_{dep}}{C_i} = \frac{qN_d W}{C_i} = \frac{\sqrt{qN_d 2\varepsilon_s \phi_s}}{C_i} \tag{2. 46}$$

Where $\phi_S = \frac{qN_d W^2}{2\varepsilon_s}$ anddepletion region width $W = \sqrt{\frac{2\varepsilon_s \phi_s}{qN_d}}$.

Threshold condition and strong inversion

It more negative voltage is applied, the surface becomes inverted and is no longer a depletion region. In fact, the surface becomes a p-type. The condition for the threshold is $-2\phi_F$, a threshold voltage is defined as the difference between intrinsic and Fermi levels:

$$V_{TH} = V_{FB} + (-2\phi_{\mathrm{F}}) - \frac{\sqrt{qN_d 2\varepsilon_s 2\phi_F}}{C_{OX}} \tag{2. 47}$$

This implies that the hole density at the surface is equal to that of the electron density of the substrate, for applied voltages above V_{TH}, strong inversion occur. Here $\phi_F$is given by

$$q\phi_F \equiv \frac{E_g}{2} - (E_c - E_F) = kTln\frac{N_d}{n_i} \tag{2. 48}$$

At the inversion state, the net bias ($V_G - V_B$. V_B is substrate bias) across MOS structure is composed of a threshold voltage V_{TH}, across the insulator voltage $V_{OX,}$ and a voltage appearing across the depletion region of the semiconductor surface, $2\phi_F$ (equation(2. 47)). The surface potential at the threshold conditions:

$$\phi_s = -2\phi_F = 2kTln\frac{N_d}{n_i} \tag{2. 49}$$

The depletion region increases with voltage until a strong inversion occurs, but upon reaching a higher voltage, a stronger inversion layer is formed rather than an increasing depletion region. At this time, the maximum depletion region width is as follows:

$$W_m = \sqrt{\frac{2\varepsilon_s 2\phi_F}{qN_d}} = 2\sqrt{\frac{\varepsilon_s kT ln\left(\frac{N_d}{N_i}\right)}{q^2 N_d}} \quad (2.\ 50)$$

2.6.2 MOSFET Transistor

The metal-oxide-semiconductor field effect transistor (MOSFET) is used to control on/off in devices by controlling gate terminals, or to amplify small AC signals. Because of this amplification and switching function, it is used in many electronic devices. It is operated by a channel generated from the control of the current on the semiconductor between source and drain. The gate determines the conductivity of the device, and the source and drain terminals are separated from each other and are connected to the heavily doped region. The voltage applied to the drain also plays an important role, and the gate channel is blocked by an oxide layer (insulator). MOSFETs are divided into depletion mode and enhancement mode, depending on whether the channel is generated as a default.

In the case of an n-channel MOSFET, both depletion mode and enhancement mode are generally fabricated. In the case of a p-channel MOSFET, however, this is generally only applicable to enhancement mode transistors. The structure and fabrication methods of the two modes are similar, but are distinguished by the feature that the threshold voltage is adjusted according to the implanted ion during the manufacturing process. Ion implantation is used to control the threshold voltage in accordance with an intended amount of doping. For example, when B^+ is implanted into a p-type channel silicon device, the threshold voltage increases depending on the dose, since the implanted ions change the effect of the charge Q_d in the depletion region, and V_{TH} also changes accordingly. If the dose of ion implantation continues to increase to this state, V_{TH} becomes positive and depletion mode is active. As a result, the difference between the two modes is divided by whether the inversion mode is 'normally-on' or 'normally-off'. The enhancement mode and depletion mode transistors are normally-off, normally-on devices, respectively.

An enhancement mode transistor is normally in the off state when the gate voltage is zero, and the device operates when a sufficient gate voltage is applied to induce a conductive channel. In the case of a depletion mode transistor with an n-channel device, since the channel is already formed at the gate voltage of 0, a negative gate voltage must be applied to enable the off state of the device. Therefore, this can be utilised in the IC circuit to appropriately insert these transistor modes to enhance the selectivity of the cell.

Figure 2. 6 shows an enhancement mode MOSFET structure is assumed, with a p-type source and drain, and an n-type channel.

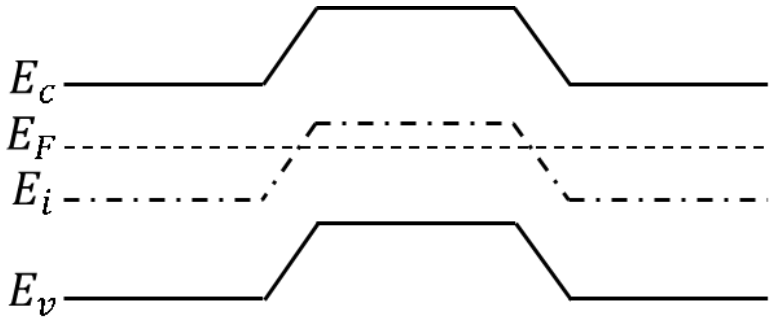


Figure 2. 6 Energy band of n-p-n transistor.

The energy band of the MOSFET is shown in Figure 2. 6. The different energy states between source/drain and gate will play the role of a potential barrier when the electrons pass from the source to the drain. This barrier is the internal potential of the p–n junction between the source and the drain.

The operation of the device depends on the voltage across the terminals. First, if the voltage V_{GS} between the gate and the source is less than the threshold voltage V_{TH} ,($V_{GS} < V_{TH}$), then no conduction of carriers occurs. In an actual device, however, it is possible for some electrons in the source to undergo a high energy flow into the drain in this condition. The current caused by this inversion current is called subthreshold leakage. If V_{GS} is greater than V_{TH} and the voltage between drain and source, V_{DS}, is less than V_{GS} - V_{TH}, electrons create a current between drain and source beyond the potential on the lower gate. The case of $V_{GS} > V_{DS}$ is similar, but if $V_{DS} > V_{GS} - V_{TH}$, a portion of the channel disappears, because the drain voltage is higher than the gate voltage. This is because the depletion region formed near the channel becomes wider into the channel near the drain, and the effective channel cross-sectional area is limited. This area is called the pinch-off. If the pinch-off point is exceeded, the I_D is only slightly increased, even if V_D increases. Therefore, beyond this point, the current becomes saturated. A more detailed description of voltage and current relationships is given in section 5.1 Current–voltage (IV) curve properties.

2.6.2-1 MOSFET output characteristics (saturation)

The current–voltage characteristic of the MOSFET can be determined by the characteristics of the current and voltage at the drain (I_D-V_D) as a function of the gate voltage V_G. It is assumed that the characteristics are obtained below the saturation state, and that the I_D is essentially kept constant above the saturation state. The applied gate voltage V_G is equal to the voltage across the insulator V_i, with the voltage across the depletion region of the semiconductor ϕ_s added to the flatband voltage. Thus the voltage applied on the gate area can be expressed by:

$$V_G = V_{FB} + \phi_s - \frac{Q_s}{C_i} \qquad (2.51)$$

Where Q_s is the charge induced in the semiconductor because of V_G, which consists of the mobile charge Q_n and the charge fixed in the depletion region Q_d, so that the induced charge can be expressed with respect to the mobile charge as follows:

$$Q_n = -C_i\left[V_G - \left(V_{FB} + \phi_s - \frac{Q_d}{C_i}\right)\right] \tag{2.52}$$

Now consider the situation where drain voltage V_D is applied. When V_D is applied, a voltage drop V_x occurs. Where x is the each point of the channel away from the source. Thus, the potential $\phi_s(x)$ is the sum of V_x and the surface potential ($2\phi_F$, at strong inversion), where ϕ_F is the bulk Fermi potential.

$$Q_n = -C_i\left[V_G - V_{FB} - 2\phi_F - V_x - \frac{1}{C_i}\sqrt{2q\varepsilon_s N_a(2\phi_F + V_x)}\right] \tag{2.53}$$

If the change of $Q_d(x)$ according to the bias V_x is neglected, the conductance of the differential element d_x at point x is given by:

$$I_D dx = \bar{\mu}_n Z|Q_n(x)|dV_x \tag{2.54}$$

Where Z is the depth of the channel and $\bar{\mu}_{n(h)}$ is the surface electron (or hole) mobility. Now, integrating this equation over the channel length L:

$$\int_0^L I_D dx = \bar{\mu}_n Z C_i \int_0^{V_D}(V_G - V_T - V_x)dV_x \tag{2.55}$$

$$I_D = \frac{\bar{\mu}_n Z C_i}{L}\left[(V_G - V_T)V_D - \frac{1}{2}V_D^2\right]$$

Where $\frac{\bar{\mu}_n Z C_i}{L}$ decides the conductance and transconductance of the MOSFET. However, when a voltage is applied to the drain, the charge in the depletion region at point x, $Q_d(x)$, must be expressed together in the equation since the charges change along with V_x. Therefore, the characteristics of the drain current can be obtained from (2.53) and (2.54) as follows:

$$I_D = \frac{\bar{\mu}_n Z C_i}{L} \times\left\{\left(V_G - V_{FB} - 2\phi_F - \frac{1}{2}V_D\right)V_D - \frac{2}{3}\frac{\sqrt{2\varepsilon_s q N_a}}{C_i}\left[(V_D + 2\phi_F)^{3/2} - (2\phi_F)^{3/2}\right]\right\} \tag{2.56}$$

Now a correlation of the drain voltage and the drain current can be considered. At low drain voltages equation (2.55) or (2.56) can be followed. Thus I_D is drawn linearly according to the V_D.

However, as the drain voltage increases, the mobile charge Q_n near the drain decreases as the voltage across the gate oxide decreases. As a result, the channel is pinched off near the drain, and the current is saturated. Under this saturation condition, the drain voltage is given by:

$$V_D(sat) \simeq V_G - V_{TH} \tag{2.57}$$

Once it is saturated, the drain current remains constant even when a larger drain voltage is applied. To obtain I_D at this state, equation (2.57) can be substituted into(2.55), then equation (2.58) is obtained.

$$I_D(sat) \simeq \frac{1}{2}\bar{\mu}_n C_i \frac{Z}{L}(V_G - V_{TH})^2 = \frac{Z}{2L}\bar{\mu}_n C_i V_D^2(sat) \tag{2.58}$$

However, for devices with short channel lengths, the above equation should be modified. In the pinch-off region, the carriers can move over most of the channels due to the short channel length. In this case, the drain current is given by the channel width (Z) multiplied by the channel charge per unit area and the saturation rate, where v_s is the velocity when the carrier is saturated:

$$I_D(sat) \approx ZC_i(V_G - V_{TH})v_s \tag{2.59}$$

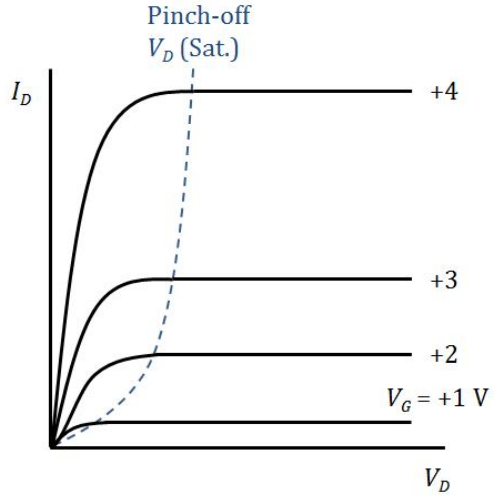
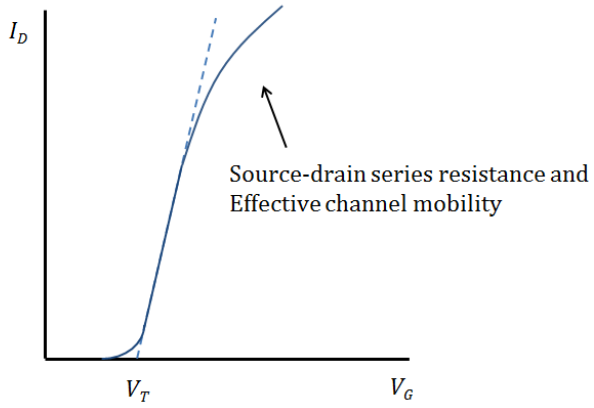


Figure 2. 7 Drain current and voltage relationship for the enhancement mode MOSFET (20). At the low drain voltage, drain current linearly increases, while after pinch-off it is saturated.

2.1.2-2 MOSFET transfer characteristics (linear)

Transfer characteristics are shown by plotting gate bias (input) and drain current (output) for a fixed drain bias. Equation (2.55)implies that I_D -V_G is a straight line, however in real MOSFET, the

drain current linearly increases at low gate bias, and sub-linearly increases at high gate bias. This deviation from linearity indicates an electric field-dependent mobility and a series resistance between source and drain. In addition, the transfer conductivity is zero below the threshold voltage (V_{TH}) and decreases after a certain maximum at the point I_D -V_G, due to the deterioration of the source–drain series resistance and effective channel mobility.



2.1.2-3 MOSFET mobility models

The mobility of carriers in the channel of the MOSFET differs from that in the bulk of the semiconductor due to the scattering mechanism in this area. For this reason, mobility is bound to decrease. Furthermore, where carriers are present in the channel, they are located very close to the semiconductor and oxide interface. Therefore, it is scattered by the surface roughness and the Coulomb interaction generated from the fixed charge in the gate oxide. Thus, the deterioration of this mobility increases with the bias applied to the gate, as high bias leads the carrier closer to the interface, and they are affected by the roughness of the interface. This degradation of mobility with gate bias is simply expressed using a drain current expression:

$$I_D = \frac{\bar{\mu}_n Z C_i}{L\{1+\theta(V_G - V_T)\}}\left[(V_G - V_T)V_D - \frac{1}{2}V_D^2\right] \tag{2.60}$$

Where θ is the mobility degradation parameter. Due to the $V_G - V_T$ term in the denominator, the I_D according to high V_G increases in a sub-linear manner.

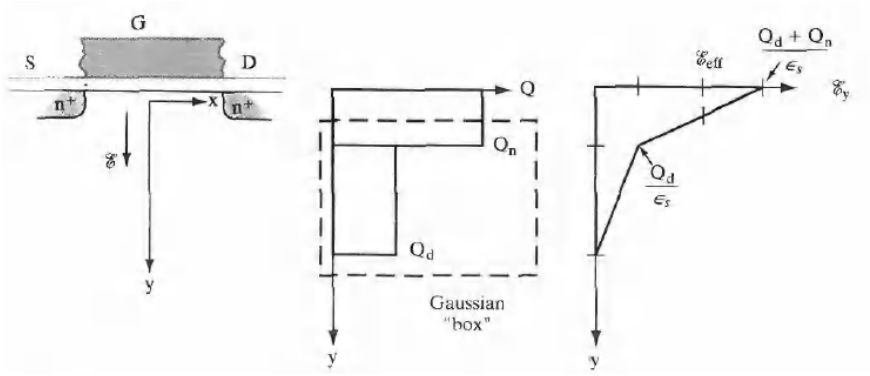


Figure 2. 8 Ideal charge distribution in the inversion and depletion layer from (20).

As a function of depth (y axis) in the MOSFET channel, the idealised charge distribution and the transverse electric field in the inversion and depletion layers are shown in the Figure 2. 8. Here the dotted box is the Gaussian box, where Gauss's law can be applied.
The average transverse electric field for electron and hole in the middle of the inversion region is given by:

$$\mathcal{E}_{\text{eff}} = \frac{1}{\epsilon_s}\left(Q_d + \frac{1}{2}Q_n\right) \tag{2.61}$$

$$\mathcal{E}_{\text{eff}} = \frac{1}{\epsilon_s}\left(Q_d + \frac{1}{3}Q_n\right) \tag{2.62}$$

In addition, the drain bias and longitudinal electric field also affect the mobility. The carrier drift velocity increases linearly with the electric field until it reaches a certain electric field $\mathcal{E}_{sat}$ and the velocity saturates at v_s.

$$\text{v} = \mu\mathcal{E} \qquad \text{for } (\mathcal{E} < \mathcal{E}_{\text{eff}}) \tag{2.63}$$

$$\text{v} = \text{v}_\text{s} \qquad \text{for } (\mathcal{E} > \mathcal{E}_{\text{eff}}) \tag{2.64}$$

The maximum longitudinal electric field near the drain end is approximated by dividing the voltage drop along the pinch-off region ($V_D - V_D(sat)$) by the length of this region.

$$\mathcal{E}_{\text{max}} = \left(\frac{V_D - V_D(sat)}{\Delta L}\right) \tag{2.65}$$

2.7 β–Ga_2O_3

β–Ga_2O_3 is one of several polytypes of Ga_2O_3. It has monoclinic crystal structure, and one of several materials to be used as conducting transparent semiconducting oxides (TSO) (14). As mentioned in

Chapter 1, it has been studied as a promising material for power devices and optoelectronic devices due to the its unique electrical properties, especially its wide bandgap and high breakdown voltage (25). Furthermore, its fabrication is adequate for low-cost and high-quality bulk mass production, for example using melt growth techniques like edge-defined film-fed (EFG) and Czochralski growth (26, 27).

2.7.1 Brief review of the properties of β–Ga_2O_3 as a semiconductor for power devices

Similar to that of other oxide semiconductors, β–Ga_2O_3 exhibits a native n-type conductivity. It has a bandgap of about ~4.8eV which is higher than those of SiC and GaN. For the n-type doping, Sn, Si and Ge are used by forming shallow donors with carrier concentrations in the range of 10^{15}~10^{19} cm^{-3}.

In addition, On-resistance(R_{ON}) as a function of the breakdown voltage(V_{br}) shows that β–Ga_2O_3 has much larger V_{br} with lower R_{ON} than other commercially available semiconductor materials, such as 4H–SiC, GaN. The value of breakdown field (MV/cm) is 8 or β–Ga_2O_3, 2.5 for 4H–SiC and 3.3 for GaN (16). Thus β–Ga_2O_3, can have lower conduction loss under the same Vbr condition. For these characteristics, β–Ga_2O_3 is considered a suitable material for unipolar devices such as field effect transistors (FET) (15).

However, β–Ga_2O_3 has some limitations. Low thermal conductivity (28 98) ,low hole mobility, and difficulty in formating p-type conductivity. Also, it is difficult to control the source drain current by the depletion mode MOSFET, since the depletion region cannot efficiently extend in the bulk with N_D ~$10^{17}cm^{-3}$.

Higashiwake et al (16) investigated that the MESFET based on β–Ga_2O_3 shows a possibility for FET device with β–Ga_2O_3. The pinch-off and on/off drain current ratio were observed but two main problems were found. High contact resistance was formed in the source and drain regions and drain current (I_d) on–off ratio was limited by leakage current. After that, depletion-mode β–Ga_2O_3 MOSFET was studied by Higashiwake et al (29). First, 20 nm of alumina was deposited on MBE-grown Sn-doped β–Ga_2O_3 as a gate insulator. The device performed considerably better than the MESFET, particularly I_d on-off ratio appeared ten orders of magnitude. The off-state leakage also was very low and V_{br} was high as 370V. In addition, MOSFET with implanted in Si + implanted S/D electrode and channel layer shows even better performance. The drain current density corresponding to V_G was higher than the previous MOSFET device. And the V_{br} was 415V (30).

Through these studies, it was clear that source and drain ohmic contacts and compensation for low current densities in the channel region played an important role in improving the performance of β–Ga_2O_3 power device.

PART II – EXPERIMENTAL METHODS

This part describes the experimental methods used in this thesis. Two deposition techniques were used for MOSCAP fabrication. Atomic layer deposition (ALD) was used to deposit a uniform Al_2O_3 layer, and physical vapour deposition (PVD) was used for metal contact deposition. In addition, more fabrication techniques have been used for MOSFETs. The lithography was performed before each deposition and reactive ion etching (RIE) step to form the desired area to be etched and deposited. In addition, ALD for Al_2O_3 deposition is used as well as CVD for SiO_2 deposition were used in MOSFETs. For the Ohmic contacts of source and drain regions of MOSFETs, Silicon ion implantation was used.

3. EXPERIMENTAL METHODS

3.1 Deposition

3.1.1 Chemical deposition (ALD)

Atomic layer deposition (ALD) was used for deposition of the oxide layer. The ALD technique is commonly used for the development of a thin film with uniform material layers. This is a chemical vapour deposition method, as it uses chemical reactions between precursors and the substrate. ALD has several important advantages compared to other deposition techniques. The deposition film has excellent uniformity and selectivity, even on large substrates, with the desired thickness. The formation of thin films by ALD uses a gas phase chemical reaction, which is self-limiting (self-terminating), and a sequential reaction taking place on the substrates. This film growth occurs by continuous cycling the process steps until a desired thickness is obtained. The precursors react via self-limiting surface reactions, so that the thickness can be controlled by cycles and the uniform quality of the thin film can be fabricated. This method also offers dense and controlled nanometre-scale thicknesses. Overall, these properties offer a strong advantage for producing electrical devices.

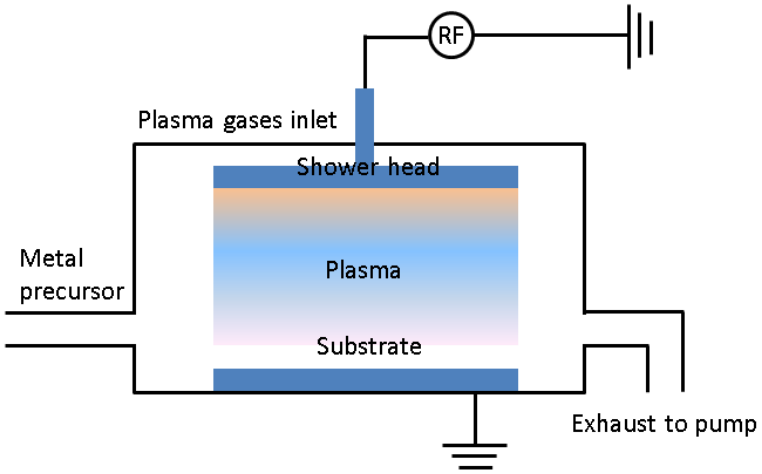


Figure 3. 1 Schematic diagram presenting the ALD reactor. This figure is modified from Kariniemi, M., 2012 (31).

Typical process conditions are 0.1 to 10 mbar or atmospheric pressure, and a temperature range of 50 to 500°C. Figure 3. 1 shows a simple schematic of the ALD reactor.

Al_2O_3 with ALD

The ALD process for an Al_2O_3 thin film is conducted via several steps with trimethylaluminium (TMA, $Al(CH_3)_3$) and an H_2O precursor. When the prepared substrate is placed in the chamber and the desired temperature and pressure are reached, the TMA precursor is injected into the chamber and reacts with hydroxyl groups on the substrate. TMA reacts until the surface is passivated, as it cannot react with itself or dissociate. As a result, once all of the hydroxyls on the surface have reacted the process is terminated. Hence this process is 'self-limiting'. In this step CH_4 is produced as a reaction product. Subsequently, excess TMA and methane are pumped out. Next, an H_2O pulse is injected as an oxidant into the reaction chamber and reacts with a methyl group, producing Al-O bridges. This process is expressed as a chemical exchange between TMA and H_2O (32).

$$2Al(CH_3)_3 + 3H_2O \rightarrow Al_2O_3 + 6CH_4 \qquad (3.1)$$

Hereby one cycle of Al_2O_3 formation is performed, and the thickness of the Al_2O_3 oxide layer is controlled by this cycling process. Ideally this A/B sequence forms a monolayer on the film.

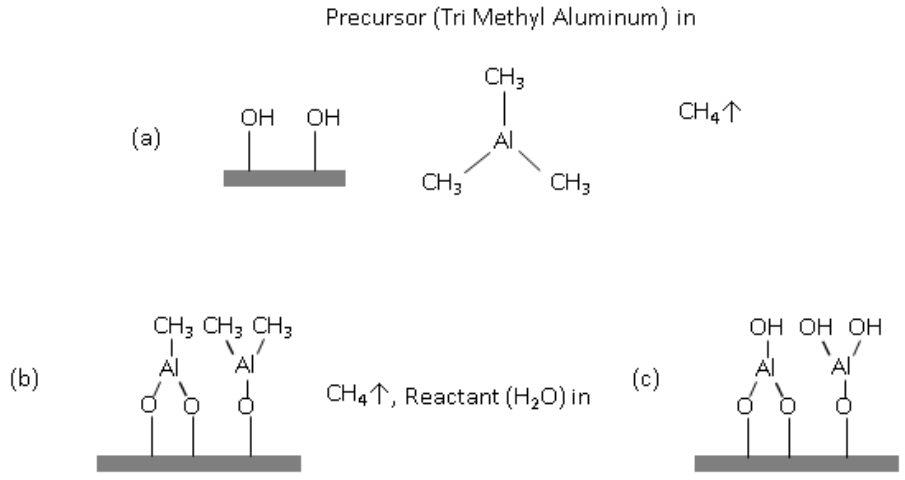


Figure 2. 9 Process of Al_2O_3 deposition from TMA and H_2O. This process is repeated until the desired thickness is achieved.

3.1.2 Chemical deposition 2 – plasma-enhanced chemical vapour deposition (PECVD) RF discharges

Plasma-enhanced chemical vapour deposition utilize a plasma generated by the radio frequency (RF) using a high-frequency alternating current (AC). The use of AC has the advantage of effectively sustaining discharge at the electrode surface. Since the cathode and the anode are changed at a high

rate, the possibility of accumulating positive ions on the electrode surface is reduced, and the discharge can be continued. This is advantageous when the electrode is non-metallic or ceramic rather than a conductor. The sources within this radio frequency range are typically 13.56 MHz. Furthermore, this induces ionization up to 100 times faster than in the case of DC, and facilitates atomic decomposition. If the frequency is greater than 10 kHz, ions do not adapt to the voltage change, but in the case of electrons, they accelerate and strike the surface of the electrode. This results in a negative charge for the plasma, and a dark space is created for each electrode region. The resulting DC voltage drop is shown in Figure 3. 1.

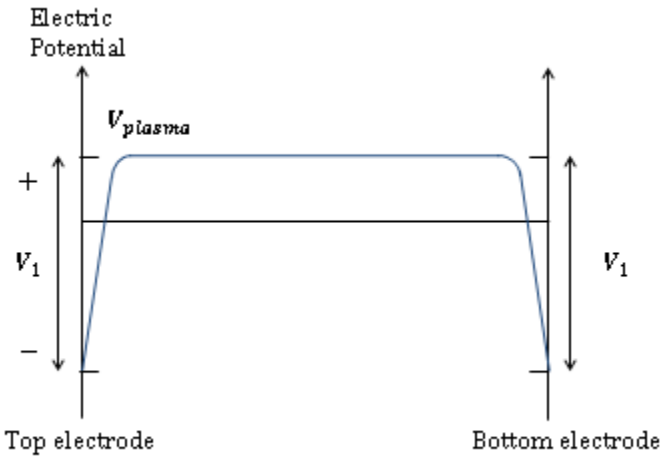


Figure 3. 1 DC voltage as a function of position in an RF plasma (33).

Here, the equation for V_1 and V_2 is:

$$V_1 \equiv V_{plasma} - V_{top}$$
$$V_2 \equiv V_{plasma} - V_{bottom} \quad (3.\ 2)$$

and in the asymmetric chamber, the equation is:

$$\frac{V_1}{V_2} \approx \left[\frac{A_2}{A_1}\right]^4 \quad (3.\ 3)$$

A_1 and A_2 are the area of the two electrodes. This equation is called *Child's law*. By increasing the area ratio of the electrodes, it is possible to obtain a higher ion bombardment energy by increasing the voltage difference between the plasma and the lower electrode.

The SiO_2 insulation thin film is fabricated from plasma-enhanced chemical vapor deposition (PECVD). This is widely used to make SiO_2 thin films in microelectromechanical systems (MEMS) and IC (34). This benefit is generated because ion bombardment on the surface due to plasma helps the adspecies to diffuse along the surface. Therefore, PECVD can produce a film at lower temperatures than conventional CVD (35). The RF frequency used here is less than 1 MHz, and as

noted above, the oxide can be deposited at 13.56 MHz. Depending on the temperature of the wall, it is divided into a cold wall parallel plate or a hot wall parallel plate.

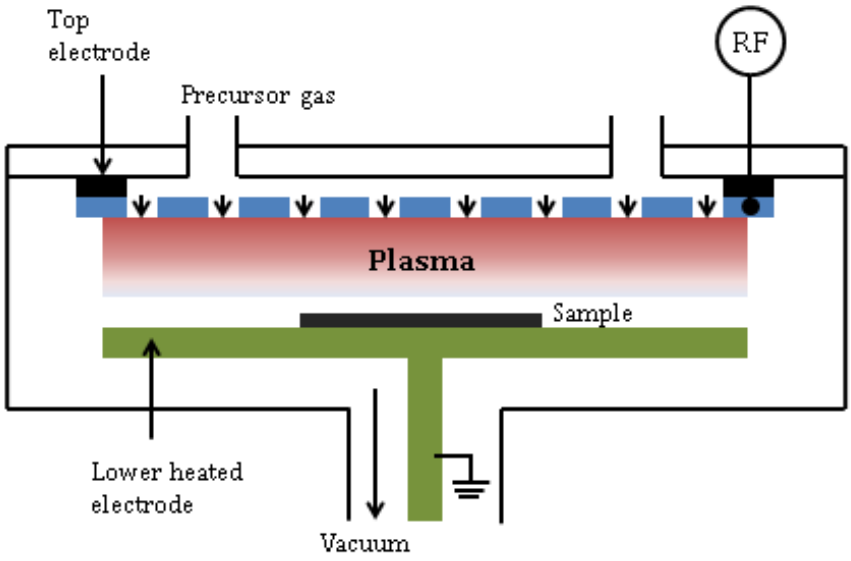


Figure 3. 2 The PECVD setup, adapted from (35).

Gases are injected through the showerhead on the edge or top electrode, and are exhausted around the centre or edge. The precursors are injected into the reaction chamber and form ions and radicals in the plasma. These radicals diffuse to the substrate surface and adsorb onto the surface. Thereafter, the reactants chemically react on the surface to form the desired solid film. The by-product exits the chamber by desorption and diffusion. In order to enable such diffusion-reaction-desorption process, the free energy difference between the reaction gas and the reaction product must be large so that the reaction can be performed spontaneously. The film should be solid and the remaining reaction product should be volatile (36). Silicon dioxide thin film formation by the PECVD method is generated using SiH_4 and N_2O gases via the process of $SiH_4(g) + N_2O(g) \rightarrow SiO_2(s) + N_2(g) + 2H_2(g)$.

3.1.3 Physical deposition – electron beam evaporation

Electron beam evaporation is a common physical deposition technique (PVD) used to form metal films. The major advantages of this method are that it can be used on metals with high melting points, and it offers high selectivity for substrates. Furthermore, this method exhibits better performance in terms of the purity of the result compared to other resistance-heated evaporators, since it essentially evaporates the material after melting, while simultaneously the temperature of crucible is kept low.

This method has limitations in terms of step coverage, however, this drawback can be utilised when it comes to the lift-off process in lithography or forming contact electrodes. Simply, a shadow mask conceals the undesirable region of the substrate, so that the material cannot physically reach the

substrate. Through this method it is possible to develop pattern on the substrate with PVD. Furthermore, by using several crucibles multilayer formation are allowed.

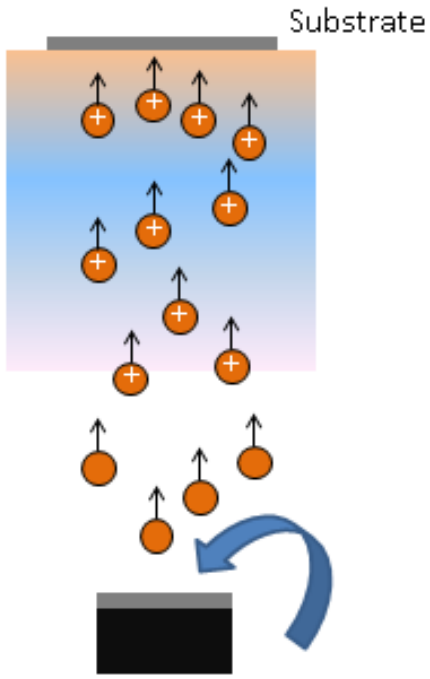


Figure 3. 2 The process of e-beam evaporation. This schematic is modified from Vijayalakshmi, K., Sivaraj, D., 2016 (37).

Evaporation takes place in a high vacuum, since atoms in vapour have to travel to and reach a surface in the chamber. The deposition process comprises three main parts: evaporating the material through the electron beam, ionising the evaporated particle, and collision on the substrate to form deposition. In the first step – evaporation – a current is applied to a hot electron filament for thermionic emission, and provokes the bumping off and acceleration of electrons from the filament. The electrons are focused toward a crucible by a magnet. In the majority of cases, metal materials melt before they begin to evaporate.

Now the material vapours are ready to travel to the substrate. Before they reach the substrate, they are ionised in plasma so that they can accelerate and collide with the substrate. Collision with high energy helps material to travel to the substrate, and enables the formation of the film. One consideration about electron beam evaporation is radiation damage, since the relaxation of excited electrons in the melted material generates X-rays, which may bring about substrate damage. However, subsequent thermal annealing steps can help to remove this damage.

3.2 Ion implantation

The base of a bipolar transistor and channel of a MOSFET requires accurately controlled doped profiles, since they ensure base and threshold voltages, or ions may be doped in cases where Ohmic contacts are needed, such as sources and drains. Ion implantation uses ionised impurity atoms, which are accelerated through an electrostatic field to hit the wafer surface, and is a suitable method to meet the demands of doping profiles in semiconductor transistors. The dose and penetration depth of impurity are controlled by ion current measurements and an electrostatic field. Hence, ion implantation offers an injected dopant profile in the substrate to some extent. One speculated shortcoming of ion implantation is that incident ions damage the lattice of the semiconductor. This damage might be difficult to recover in the case of very shallow or deep profiles. Compared to a diffusion process, the throughput of ion implantation has limitations for high-dose implants and is expensive. Ion implantation systems consist of three main parts: the ion source, the acceleration tube, and the end station.

Ions with a large energy are injected towards a thick target, which brings about scattering and collision. Eventually, the ions are stopped after losing their energy. The total distance travelled by ions in the semiconductor is the range, R. In the case of interest, a uniform beam, the quantity termed 'average depth' is used. This quantity is the project range, R_p. Once the electronic stopping S_e and nuclear stopping S_n are known, the project range $R_p$can be obtained by performing integration.

The energy loss per unit length from electronic stopping is:

$$S_e = \left.\frac{dE}{dx}\right|_e = k_e\sqrt{E} \tag{3. 4}$$

Where $k_e$is a proportional constant depending on the charge number and mass of the incident and target ions.

Ion interaction is considerably different to electron interaction, so a different model is used. Ion interaction can penetrate thousands of angstroms of semiconductor crystals with a relatively large scattering angle, since incident and target ions have almost the same order of mass. Scattering depends on the impact parameter, masses, and relative positions of the two ions. As they enter, the ions are uniformly distributed over the surface of the wafer. Thus, the result appears as a statistical distribution of depths. This statistical distribution function for the amorphous target ideally follows Gaussian distribution.

As mentioned earlier, to find R_p, S_n must be determined. It increases with ion energy and has a maximum value at some energy, since the collision time at high velocity provides insufficient time for energy loss. Hence the maximum value of S_n is:

$$\mathrm{S_n^0} \approx 2.8\times10^{-15} eV - cm^2 \frac{Z_i Z_t}{Z^{\frac{1}{3}}} \frac{M_i}{M_i + M_t} \tag{3. 5}$$

Where

$$Z = \left[Z_i^{\frac{2}{3}} + Z_i^{\frac{2}{3}} \right]^{\frac{3}{2}} \tag{3. 6}$$

Now, the project range and the standard deviation of the projected range are obtained by:

$$R_p = \int_0^{R_p} dx = \int_{E_0}^{0} \frac{dE}{\frac{dE}{dx}} = \int_{E_o}^{0} \frac{dE}{S_n + S_e} \tag{3. 7}$$

$$\Delta R_p \cong \frac{2}{3} R_p \left[\frac{\sqrt{M_i M_t}}{M_i + M_t} \right] \tag{3. 8}$$

During ion implantation, the crystal in the substrate is damaged by the transfer of energy. The ions injected into the substrate with high energy cause two types of scattering, due to interaction with the atoms constituting the substrate crystal: elastic scattering, due to collisions with nuclei, and inelastic scattering, due to interactions with electrons around atoms.

There is one thing to consider when ion implantation is performed on single-crystal materials. This is because the phenomenon called channeling, which occurs when ion velocities parallel to the crystal orientation exist. Channeling is due to the low density of electrons in the channel and the ineffectiveness of nuclear stopping, so ions can travel a long distance with low energy loss. This eventually produces defects or impurities and forms a significant tail in the injection distribution. In order to suppress this phenomenon, it is necessary to change the angle of the wafer to lengthen the other crystal planes or to destroy the lattice in the pre-implantation step.

The energy transfer develop the ion into the sample may induce considerable defects in the sample. In particular, collisions with nuclei can deliver enough energy to the target atoms to cause atomic displacements. In general, the transition of the collision energy to nuclear energy is much greater than the binding energy of the atom in the lattice. As a result of such damage, a damage region is formed inside the substrate. The mass of the ions determines the structural characteristics of these impairments. Thousands of lattice defects may be caused by a heavy ion, because as the quantity of implanted ions increases.

Following ion implantation, the implanted ions themselves may not all act as impurities. In order for the impurities to be electrically activated, they must be situated in a substitutional site in the substrate crystal; since the substrate crystal no longer has its original bonding structures, impurities due to implanted ions also do not play their original role. This state can be recovered through annealing. The purpose of annealing is to repair the ion-induced damage (e. g. recrystallisation), and the implanted ions move to the substitutional position in the crystal to serve as a dopants (activation). However, during annealing at highly elevated temperatures, the

compound may decompose or undesirable diffusion may occur in the implanted species. This undesired diffusion can be minimised by optimising time and temperature.

3.3 Lithography

For the process of building a dense integrated circuit or transistor, many sophisticated and elaborate processes are established. The semiconductor industry has made progress in accordance with Moore's and Hwang's laws. Photolithography is a key technology that has played a major role in increased integration.

The basic structure of the lithography system optically exposes a wafer with a mask. The optical source is located on the topmost area and the light travels through the aperture, shutter, and mask with a specific height.

Optical lithography has three major print methods: contact, proximity, and projection. UV is widely used as a light source, and the initial lithography process used contact and proximity printing methods; however, contact printing has a problem whereby the mask or film can be damaged by dust due to physical contact on the wafer. In terms of the proximity printing method, the light source (UV) is diffracted at the edge area of the mask pattern due to the space between the mask and the wafer, thus invading the shadow region. Therefore, projection printing is widely used.

Resolution and depth of focus in projection printers

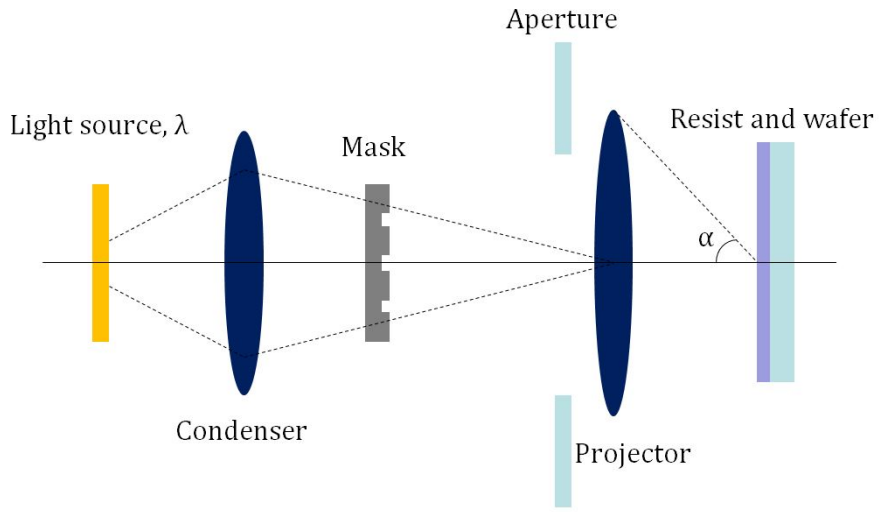


Figure 3. 3 Projection printer structure. Contact printing has a high risk to have damages on mask and film.

Two important parameters in this process are the resolution and depth of focus. First, the resolution is a limitation for collecting and reimagining light. This can be expressed by $W_{min} = k_1 \frac{\lambda}{NA}$, where $k_1$is the process-related coefficient, *NA* is the numerical aperture, and λ is the wavelength of the light source used. As can be seen from the preceding equation, it is possible to utilise fine patterns using short wavelengths and a high NA, but the depth of focus (DOF), which is a measure of vertical alignment of the wafer, must also be considered. The DOF is defined as $= k_2 \frac{\lambda}{NA^2}$,

where k_2 is another process-related coefficient. Lithography equipment is limited in continuously increasing the value of *NA*, and the adjustment of process factors such as k_1 and k_2 is limited by the sensitivity of the photoresist, mask production, and the difficulty of the process. Current lithography techniques have evolved towards a tendency to use short wavelengths.

Photoresist

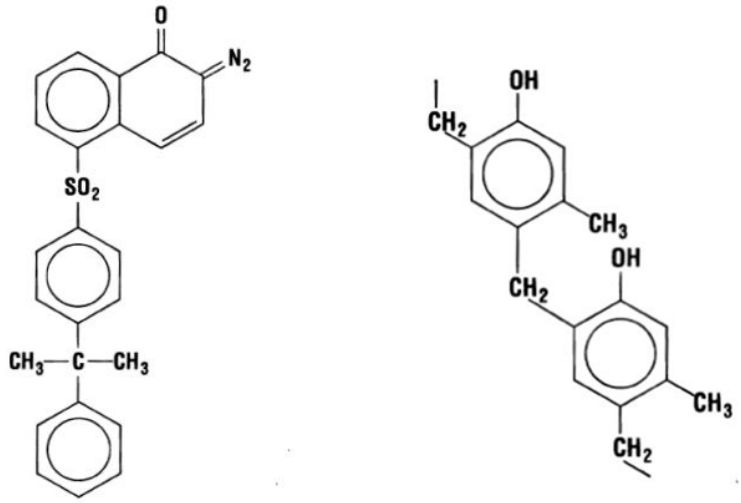


Figure 3. 4 Diazoquinone(left) and novolac(right). Diazoquinone acts as an inhibitor and reduces the dissolution rate when exposed to a developer, and novoloc is used for adhesive

Photoresist, the medium used to transfer circuit designs to wafers, is divided into two categories. Positive resist is the case where light is dissolved by the developing solution, and negative resist is the opposite situation. The composition of the photo resist (PR) includes a polymer that modifies solubility during exposure, a solvent for the liquid medium, a sensitiser for chemical changes in the polymer, and additives for the desired process results. In this paper, S1813 – a positive resist – was used to fabricate MOSFETs. Positive resist has the advantage that the portion not exposed to light is not attacked by the developer. S1813 resist consists of electronic-grade propylene glycol monomethyl ether acetate (solvent), mixed cresol novolac resin(polymer), cresol, diazo photoactive compound (sensitiser), and fluoroaliphatic polymer esters. A positive photoresist, such as S1813, typically uses a DQN (the photoactive compound diazoquinone and matrix material) resist. The novolac that forms part of the DQN is readily dissolved in aqueous solutions, usually used as an adhesive, and organic solvents are added to achieve viscosity. Diazoquinone acts as an inhibitor and reduces the dissolution rate when exposed to a developer. Figure 3. 5 illustrates the photolysis process due to UV exposure.

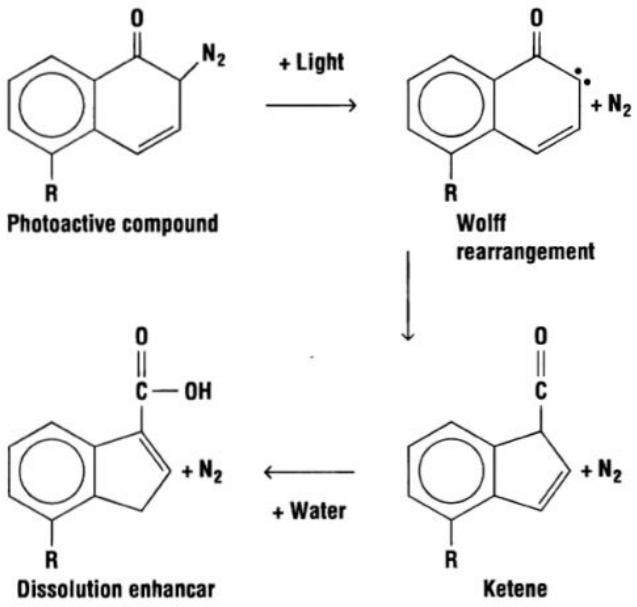


Figure 3. 5 The process of DQN dissolution.

The DQN molecule is encompassed by R. In this photoactive compound (PAC), the N2 molecule of the carbon ring leaves a highly reactive carbon site when exposed to UV light. Therefore, the oxygen atom is covalently bonded with the carbon outside the ring to compensate for this. This process is called Wolff rearrangement, and as a result, ketene is produced. The final rearrangement occurs within water, where the OH group bonds with external carbon atoms. This reaction eventually produces carboxylic acid. This causes dissolution in base solutions and typical developer solutions such as water-diluted KOH or NaOH.

As such, several steps are required to obtain the desired pattern via various chemical changes. First, an adhesion promoter such as hexamethyldisilazane (HMDS) is used to turn the wafer surface into a hydrophobic surface, and the photoresist is rotated according to the specific rpm. Thereafter, soft bake is performed at a low temperature (typically 90–110°C) to remove the organic solvent, and subsequently the exposure process is performed. Following this, baking and developing occur again. When development is completed, the developer is removed and hard baking occurs at a temperature slightly higher than the glass transition temperature of the PR to prevent its deformation.

In this study, maskless lithography is used to fabricate MOSFET devices. This equipment uses a method of transferring light pixel by pixel without using a mask. Therefore, it provides the advantage that the time and cost of mask production can be reduced.

3.4 Reactive ion etching (RIE)

Reactive ion etching (RIE) is a type of dry etch that uses plasma to perform anisotropic etching. This method is used to scale down for MOSFET, etching Si and SiO_2 effectively (38, 39). The degree of anisotropy can be expressed as $A_f = 1 - \frac{l}{h_f} = 1 - \frac{R_{lt}}{R_{vt}} = 1 - \frac{R_l}{R_v}$ where h_f represents the thickness of the layer to be etched, l is the etched side length of the bottom of the photo resist, and R_{lt} and R_{vt} are the etch rates of the lateral and vertical surfaces, respectively. For an isotropic etch, this value is zero and the anisotropic etch has a value of one. There are two types of RIE system: parallel-plate and hexode batch, according to the style of wafer arrangement and the location of ground electrodes. The parallel-plate RIE system for SiO_2 is used for this study.

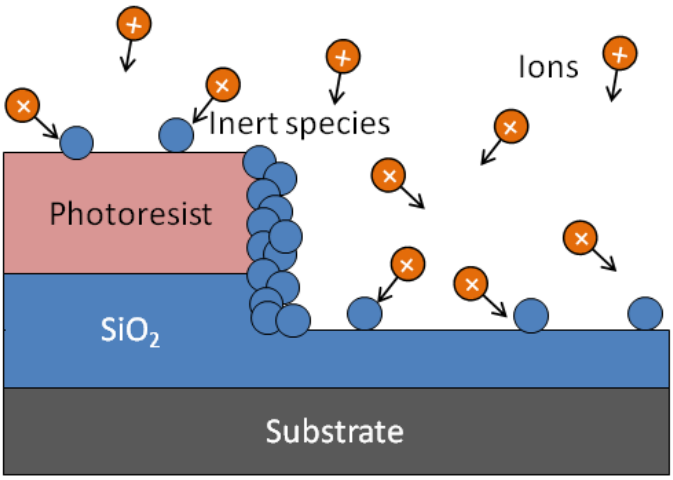


Figure 3. 6 Anisotropic etching of SiO_2 with sidewall passivation. The etching process occurs in CF4 plasma. This figure is adapted from Campbell, S, A (33).

Dry etching utilises the chemical reaction in plasma and contains reactive radicals and targets on the wafer surface. First, the feed gas species diffuse and react on the surface. When the ion and radical generate bombardment on the surface, the physical reaction that takes place in the RIE uses the collision mechanism similarly to sputtering. Ions with a significant amount of energy impose on the substrate surface, and the high momentum of these particles is sufficient to break the bond energy of the etchant. Hence, there is a possibility of defect occurrence due to this process. Therefore, RIE can be said to use both physical and chemical reactions for etching. For the selective etching of Si or SiO_2, CF_4 plasma is generally used. Substrate surface atoms are bonded with two F atoms in fluorine plasma, and a few atoms with a thick, fluorinated skin may exist. In the plasma, reactions between CF_4 and e^- forms CF_3+F+e^-, while reaction with the SiO_2 substrate generates primarily desorbed volatile SiF_4 and O_2 gas. Here, the etching rate is mostly affected by pressure in a non-linear fashion. A small amount of oxygen is also used to raise the etch rate, due to the fact that the injected oxygen reacts with carbon atoms to form CO or CO_2, which further helps the C–O bond to replace the broken Si–O bond (40). During this process, thin non-volatile fluorocarbons are polymerised on the sidewalls, and due to the vertically applied electric field the Si and SiO_2 can be etched anisotropically (41).

For more accurate anisotropic etching, hydrogen may be used. As H is added to the CF_4 plasma, the etch rate is reduced because the hydrogen reacts with fluoric radicals to form HF. Nonvolatile fluorocarbon films are deposited to enhance anisotropy, in addition to selectivity for selective etching of SiO_2 where SiO_2 and Si exist on the same substrate. This polymerisation process depends on the ratio of fluorine to carbon, and can be injected in the form of H_2 or CHF_3 (42).

4. SAMPLE PREPERATION

In order to measure and compare characteristics as a power device, MOS capacitors and MOSFETs are fabricated in a MiNa clean room. A beta-gallium oxide substrate and SiC substrate were used for the MOS capacitor, and devices were fabricated using the same conditions and time.

4.1 Fabrication preparation – wafer and cleaning

For β–Ga_2O_3 MOS capacitance, a 10×15 mm substrate was purchased by Tamura Corporation (Japan). The surface alignment was in the (010) direction with 0.5±0.3 mm thickness, and the melt growth 'edge-defined film-fed growth' (EFG) method was used. β–Ga_2O_3 naturally has n-type characteristics and the wafer contains unintentional impurity dopant (UID). The effective donor concentration of those samples is $N_D \approx 1{\sim}5{\times}10^{17}/cm^{-3}$, indicating that it is an n–type semiconductor. For β–Ga_2O_3 MOSFET, a 2-inch wafer from the same company and the same growth method was used. The donor concentration is $N_D \approx 3.2{\times}10^{17}/cm^{-3}$, and surface orientation is (-201) with 0.68±0.02 mm thickness.

4H–SiC substrates were prepared for using comparable criteria to the beta-gallium oxide substrate MOS capacitor. The samples has a ~10 μm epitaxial layer with a net carrier concentration of $1.0{\times}10^{15}/cm^{-3}$, grown by chemical vapour deposition on a 4° off-axis (0001) doped n–type SiC substrate from Cree Research Inc.

Before and after each deposition step, cleaning was carried out and the samples were immersed in acetone, isopropanol, and DI water for 2 minutes, 10 minutes, and 10 minutes respectively in an ultrasonic bath. After each cleaning step, samples were dried with a nitrogen (N_2) gas flow.

4.2 Fabrication for MOS structure

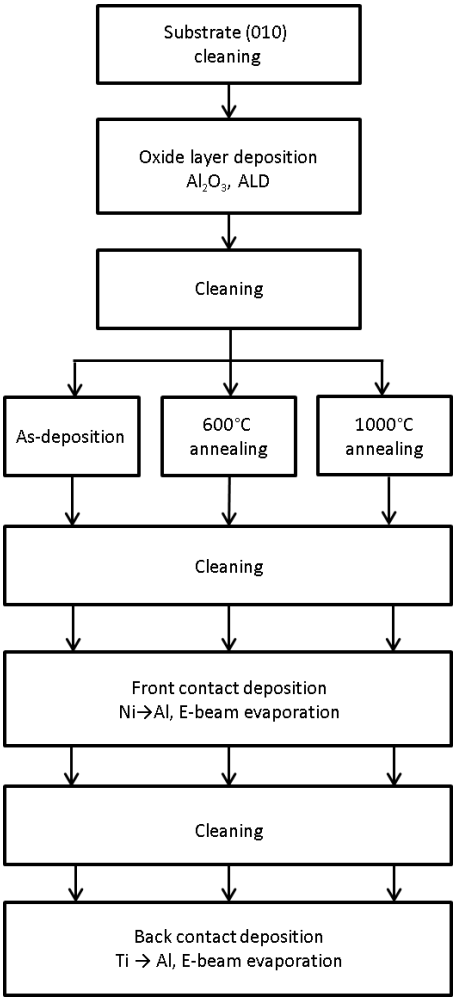


Figure 4. 1 Flowchart of MOS capacitor fabrication.

The Figure 4. 1 briefly shows a block diagram of the MOS capacitor fabrication process. After oxide layer deposition, three different annealing conditions were conducted on β–Ga_2O_3 and SiC samples. The first condition was As-deposited, and in the second and third conditions the samples were annealed after oxide layer deposition at 600°C and 1,000°C, respectively. This resulted in a total of six different capacitors.

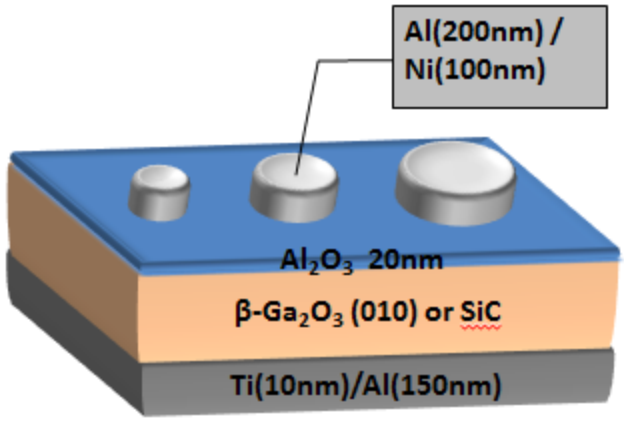


Figure 4. 2 Fabricated MOS structure. The MOS structures were fabricated through the same process on the (010) β–Ga_2O_3 and SiC substrates.

Oxide layer and annealing

After cleaning the prepared substrate, a thin Al_2O_3 oxide film was deposited with Beneq's TFS 200 ALD equipment for the oxide layer on the β–Ga_2O_3 and SiC substrates. During deposition, the temperature in the reactor chamber was 200°C, and high-purity trimethylaluminium ($Al(CH_3)_3$, TMA) and H_2O were used as a precursor. Following the deposition of the oxide layer, heat treatment was carried out in a furnace for 1 hour with 150 ml/min of nitrogen atmosphere to make different heat treatment conditions. Except for the As-deposited condition, heat treatment was performed at 600°C and 1,000°C.

Contact

Electrodes were deposited by an e-beam on the front and back surfaces of β–Ga_2O_3 and Al_2O_3 for the formation of electrodes. First, a front contact deposition was executed. The deposition was performed with approximately 1.6×10^{-6} Torr of chamber pressure. As shown in Figure 4. 2 Fabricated MOS structure 100 nm nickel was deposited first, followed by 200 nm aluminium. For the formation of the front Schottky contact, a mask was used during e-beam evaporation. This mask had three different hole sizes, thus three contact sizes were generated. The smallest dot had a diameter of 200 μm, while the medium and largest dots had diameters of 480 μm and 800 μm respectively. For the back contact (Ohmic contact), 10 nm of titanium was deposited first, followed by 150 nm of aluminium deposition. The condition of this deposition was in the same manner as the previous deposition. In order to contact to measurement apparatus, silver paste was applied on the back contact of samples.

5 ELECTRICAL EXPERIMENTAL CHARACTERISATION TECHNIQUES

5.1 Current–voltage (IV) curve properties

The current–voltage graph intuitively shows the rectification of the device (43), and the device drive attribute of a MOSFET can be determined through output and transfer characteristics. The difference between enhancement mode and depletion mode transistors depends on whether they are normally off or on. Thus, for a depletion mode transistor, the device can be turned off by extending the depletion region. Here the description about device characteristics based on the MOSFET of p–type semiconductor and the enhancement mode conditions. The output characteristic is given by a different gate bias and is plotted in terms of drain current and drain bias. The transfer characteristics are also shown graphically for the gate bias versus the output drain current for a fixed drain bias. How the charges respond according to the applied voltage, and thus how the current and voltage appear, are described in chapter 2.6.2.

5.2 Capacitance–voltage (C–V) characterization of MOS structure and Schottky barrier.

As mentioned in chapter 2.6 MOS and MOSFET, operations of MOS structure devices are roughly divided into four parts according to bias (accumulation, depletion, inversion and strong inversion). The surface potential (ϕ_s) becomes zero at V_{FB}, and thus, potential at the accumulation part is close to zero (The ϕ_s in Figure 2. 5(a)). In other words, in the MOS structure with the n–type semiconductor, ϕ_s gradually increases because the depletion region occurs as the bias changes to the negative bias direction. Where the threshold voltage, which separating the depletion region and the inversion region, ϕ_s becomes the maximum value $2\phi_F$ (where $\phi_F$is the bulk fermi potential). This phenomenon can be displayed as an intuitive graph by capacitor measurement according to the voltage change, and the measurement result is able to calculate a large amount of information about the charge.

Assume the C–V curve is obtained by varying the DC bias while measuring the capacitance with a low frequency. In the accumulation region, the capacitance of the MOS structure is given by the oxide layer. In depletion, however, the capacitance consists of two series capacitors in the oxide (insulator) capacitor *Ci*, and the depletion layer capacitor C_{dep}. The capacitance in the depletion region is inversely proportional to the width of the depletion region, and is proportional to the permittivity of the substrate. Thus, the total capacitance connected in series with equation (2. 46) is given by:

$$\frac{1}{C} = \frac{1}{C_i} + \frac{1}{C_{dep}} \qquad (5.\ 1)$$

$$\text{where} \quad C_{dep} = \frac{\varepsilon_S}{W}$$

The C–V curve can also be used to determine the doping concentration, gate oxide thickness, flatband voltage, threshold voltage, and so on, which can be provided by capacitance–voltage measurements. In 1960, J. Hilibrand and R.D. Gold developed a formula to measure the impurity and doping profiles of semiconductor junctions from capacitance–voltage measurements (44).

$$\frac{1}{C^2} = \frac{2}{q\varepsilon_s N_d A^2}(V_0 - V) = aV + b \tag{5. 2}$$

From the capacitance equation of an asymmetric Schottky barrier, the above equation ((5. 2) is obtained. Donor concentration (N_d) can be found from the slope, and the built-in voltage of the junction is found at the intersection with the horizontal axis of the $1/C^2$ line.

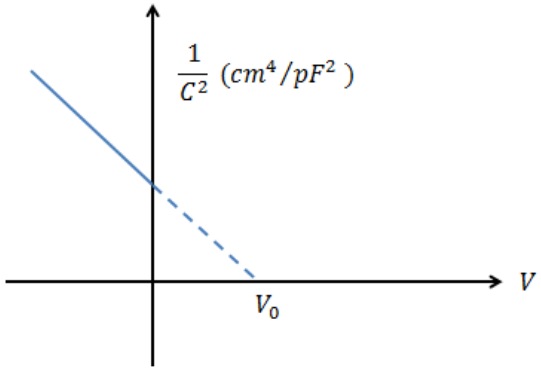


Figure 5. 1 $1/C^2$ vs. applied voltage. This slope is widely used to determine the carrier concentration (20).

For more accurate measurements, $2kt/q$ should be included in the intercept value in order to describe the majority carrier tail towards the depletion region. When the substrate concentration is obtained by the above method, the flatband capacitance can be determined from this and the device length, which depends on the doping.

$$C_{FB} = \frac{1}{\frac{1}{C_{OX}} + \frac{L_D}{\varepsilon_s}} \tag{5. 3}$$

By using this method, various parameters of the fabricated device can be obtained. The equation for the flatband in the ideal capacitance is given in equation (2. 43). In actual devices, however, additional components such as the interface region or the charge of the depletion region must be added.

$$V_{FB} = \phi_{ms} - \frac{Q_i}{C_i} \tag{5. 4}$$

$$V_{TH} = \left(\phi_{ms} - \frac{Q_i}{C_i}\right) - \frac{Q_d}{C_i} + 2\phi_F \tag{5. 5}$$

Therefore, equation (2. 43) can be written as (5. 4)(5. 4), and equation (2. 49) can be written as (5. 5). Eventually, the actual interface or charge inside the oxide will affect the MOS measurement results. For example, the fast interface state density D_{it} and the mobile ionic charge Q_m can be determined from these measurements. The fast interfacial state can be attributed to the low

frequency capacitance C_{LF} in response to a low frequency (usually 1 to 1,000 Hz), and so can be represented as the difference between the low and high frequencies at the threshold voltage.

$$D_{it} = \frac{1}{q}\left(\frac{C_i C_{LF}}{C_i - C_{LF}} - \frac{C_i C_{HF}}{C_i - C_{HF}}\right) cm^{-2}eV^{-1} \quad (5.\ 6)$$

Moreover, when positive and negative biases are continuously applied, the content of mobile ions can be determined from the following equation by using the principle that the flatband voltage is measured differently due to mobile ions:

$$\mathrm{Q_m} = C_i(V_{FB}^{-} - V_{FB}^{+}) \quad (5.\ 7)$$

5.3 Deep level transient spectroscopy (DLTS)

As discussed in section 2.3.3 Carrier concentration, defects in deep levels are bound to exist inside semiconductor devices. In section 2.3.4 Defect levels, the relationship between carrier emission, time, and temperature was also handled. Accordingly, DLTS is a well-known method that is able to characterise deep levels in terms of trap signatures. The idea was first introduced by Lang, 1974 (45). This section focuses on the majority carriers along the classical DLTS model, and assumes the depletion region resulting from the Schottky barrier (or p + n junction). Thus, a number of traps serve as places where electrons are trapped.

For the calculation of carrier emission rate from the depletion region, DLTS uses bias to adjust this region for inducing trap charge and emission. The change in the depletion region and the resulting movement of the carrier eventually lead to a variation of the capacitor. In DLTS, the trap signature is obtained by using the temperature dependence of the emission rate and temperature, as explained in a later sub-section. A trap filled by a pulse applied to the diode induces a continuous emission that is transient with temperature, and the results corresponding to the trap are shown as peaks.

Figure 5. 2 shows the relationship between bias and capacitance. The bias is given between a bias close to zero and a reverse bias V_r, and the pulse interval is time t_r. Near zero bias, the bias is maintained for time t_f, where the traps are filled by the majority carriers. If a reverse bias is applied here, as the depletion region expands, the carriers filled in the traps are emitted at an emission rate e_n. Due to these carrier changes, the capacitance creates an exponential transient.

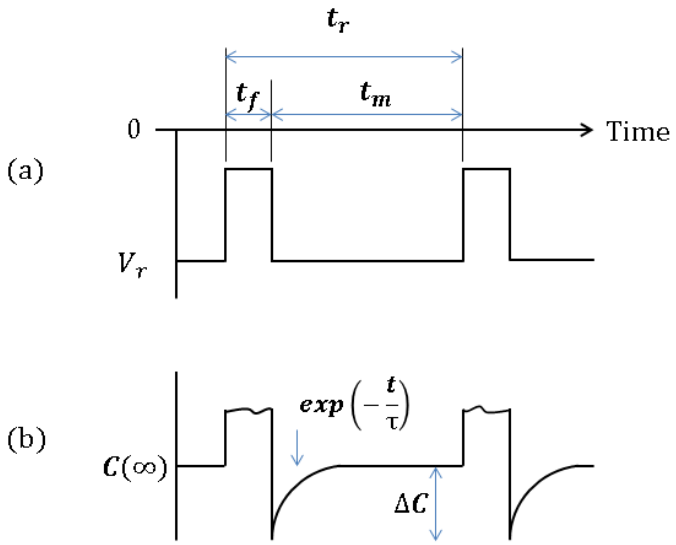


Figure 5. 2 The relationship between (a) diode bias and (b) diode capacitance of a DLTS system (23).

5.3.1 Response of capacitance transient in the depletion region

As the name suggests, DLTS measures 'transients', which are short time variations within the state. First of all, assume that the emission rate is in equilibrium. Here the trap occupation variation is described according to time ($n_t(t)$). The time dependence of electron trapping in the trap was investigated in the above equation (2. 15), and this formula can be altered as follows:

$$\frac{dn_t}{dt} = a(N_t - n_t) - bn_t \tag{5. 8}$$

Where

$$a = \sum rate\ of\ electron\ gain\ (c_n + e_p)$$
$$b = \sum rate\ of\ electron\ loss\ (e_n + c_p)$$

In the case of $n_t = n_t(0)$ when $t = 0$, the general solution to equation (5. 8) is:

$$n_t(t) = \frac{a}{a+b}N_t - \left\{\frac{a}{a+b} - n_t(0)\right\} exp[-(a+b)_t] \tag{5. 9}$$

This equation indicates that occupancy relaxes exponentially with the rate constant $(a + b)$ to steady state occupancy. For the boundary of infinitely long time, steady state occupancy concentration is described ($t = \infty$):

$$n_t(\infty) = \frac{a}{a+b} N_t \tag{5. 10}$$

Generally, $n_t(t)$ can be written as

$$n_t(t) = n_t(\infty) - \{n_t(\infty) - n_t(0)\} \exp\left(-\frac{t}{\tau}\right) \tag{5. 11}$$

Where the time constant τ is $\tau^{-1} = (a+b) = e_n + c_n + e_p + c_p$. Two situations must be considered; the traps are fully occupied at $t = 0$, or initially empty:

$$n_t(t) = \frac{a}{a+b} N_t - \frac{b}{(a+b)} N_t exp[-(a+b)t], \qquad (n_t(0) = N_t) \tag{5. 12}$$

$$n_t(t) = \frac{a}{a+b} N_t \{1 - exp[-(a+b)t]\}, \qquad (n_t(0) = 0) \tag{5. 13}$$

$n_t(t)$ increases with time t. Assuming that all traps in the depletion region are filled during the voltage pulse, then the emission rate of the thermal emission process is:

$$\left(-\frac{dn_t}{dt}\right) = e_n n_t(t) \tag{5. 14}$$

The above equations and assumptions illustrate the consequences of the emission rate due to abrupt changes in the depletion layer. The reason for explaining the emission in the depletion region is that no other processes need to be considered when the majority carrier emission process occurs. The majority carrier capture rate is neglected due to the absence of free charge carriers in this region. Therefore, only the electron emission rate in the trap exhibits meaningful behaviour with reverse bias. While it is possible to characterise both majority and minority carrier traps, the process for the majority carrier is exemplified because the traps of minority carriers are very small compared to those of majority carriers. Thus, the emission of electrons from the trap is considered. Equation(2. 15) indicates the rate of change of trap occupation. Since this is applied to only one electron, if it is integrated:

$$n_t(t) = n_t(0) e^{-e_{n(T)t}} \tag{5. 15}$$

In the emission process, a donor-like trap is neutral, as a negative charge is associated with occupation, while the trap becomes positive in the unoccupied state. For a donor-like carrier trap, the net space charge density is expressed as; $\rho(t) = e(N_d + N_t - n_t(t))$. This value can be applied to equation (2. 42), the charge density in the capacitance equation, so the time-dependent capacitance is built at reverse bias.

$$C(t) = C(\infty) \sqrt{1 - \frac{n_t(t)}{N_d + N_t}} \tag{5. 16}$$

At time = ∞, all electrons are emitted and the capacitance is:

$$C(\infty) = A\sqrt{\frac{\varepsilon_r \varepsilon_0 e(N_d + N_t)}{2V}} \tag{5. 17}$$

When the trap concentration is $N_t \ll N_d$, the capacitance variation $\Delta C(t) = C(t) - C(\infty)$is written as:

$$\frac{\Delta C(t)}{C(\infty)} = -\frac{n_t(t)}{2N_d} \qquad (N_t \ll N_d) \tag{5. 18}$$

Referring to equation (5. 12), a the sum of electron gain rates, and b the sum of electron loss rates, can be replaced by 0 and e_n respectively for more accurate representation. This is re-formulated as:

$$\frac{\Delta C(t)}{C(\infty)} = -\frac{N_t(t)}{2N_d}\exp(-e_n t) \qquad (N_t \ll N_d) \tag{5. 19}$$

The graph obtained by measuring the actual DLTS was applied to the above equation to determine the concentration of the trap.

5.3.2 DLTS signal generation

As shown in Figure 5. 2, the capacitance of the diode has a region that varies exponentially along the bias. The τ in Figure 5. 27 is equal to the value of e_n^{-1}. If the constant for this time is equal to the known preset time constant τ_{ref}, the equipment provides the rate window output. This time also serves as an important filter in the DLTS technique (46).

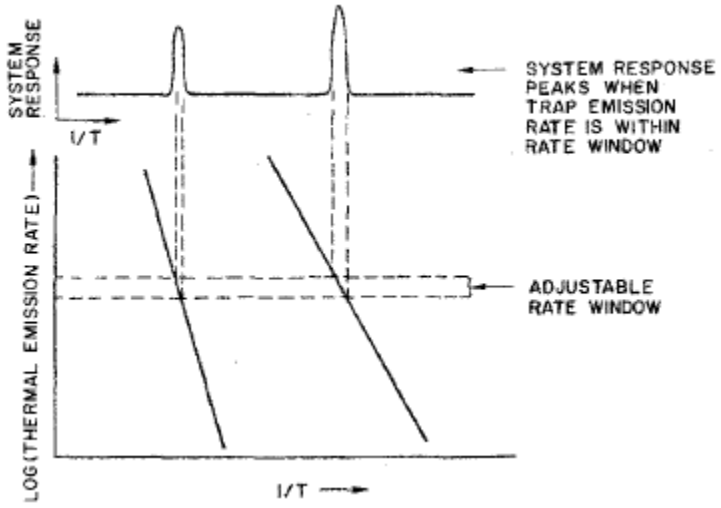


Figure 5. 3 Peaks corresponding to the match of time filter and emission rate. This figure is adapted from (45).

That is, the rate window allows the output signal only when the transient has a time constant that matches the centre of the time window. This is illustrated in Figure 5. 3. There are many ways to construct this time filter, but the most widely used and most common method is the 'double boxcar' method.

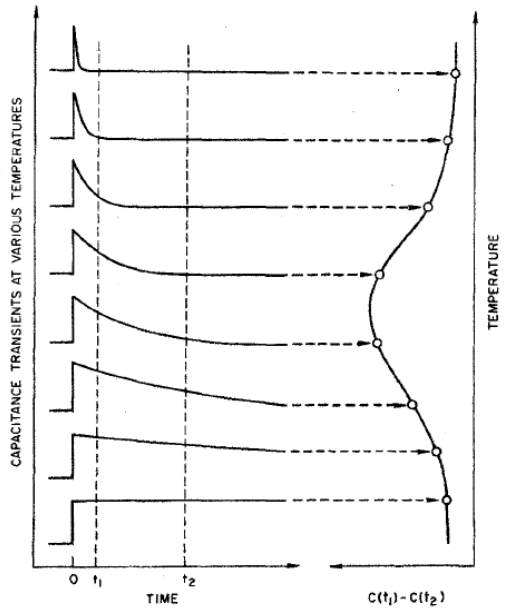


Figure 5. 4 Generation of a signal in the double boxcar model, which indicates the rate window. This figure is adapted from (45).

This dual boxcar model converts the capacitance changes detected at times t_1 and t_2 into signals when the capacitance transient is placed in a fast response situation, $C(t_1) - C(t_2) = \Delta C$, as shown in Figure 5. 4. The emission rate can be determined from the position of the peaks using the formed peak and weighting function. In this study, the lock-in weighting function is used. The weighting function can be involved in the sensitivity, selectivity, and noise of the signal. Hence, by using an appropriate weighting function, the signal overlap at two levels can be separated, or a noise reduction effect can be obtained. This weighting function is applied to the signal of the window (equation (5. 21)).

$$\omega(t) = \begin{cases} 1 & t_d + 2^{i-1}\tau < t \leq t_d + 2^{i}\tau \\ -1 & t_d < t \leq t_d + 2^{i-1}\tau \end{cases} \quad (5.\ 20)$$

Where t_d in the above equation is delay time before the start of the capacitance reading, and τ is the time interval between each measurement. This mode implies that the first half of the capacitance measured in the time window is negative and the second half is positive (47). The signal of the i-th window number with capacitance measurement point n_i is obtained by the following equation.

$$S_i(T) = \frac{1}{n_i} \sum_{t=t_d}^{t_d+t_i} \Delta C(T,t)\omega(t) \quad (5.\ 21)$$

Where t_i is the duration of the measurement in the window. This weighting function determines the value of the emission rate at the temperature corresponding to the peaks, and several windows are used for the temperature dependence of the emission rate. By plotting S versus temperature for different time windows, a DLTS spectrum can be obtained. In the experiment for this study, the signal measured in lock-in weighting function, the number of measurements point was $n_i = 2^{\mathrm{i}}$.

Table 5. 1 shows the nine rate windows used in this study and the window length at 50 ms time intervals.

5.3.3 Data extraction from DLTS

Emission rate and capture cross-section

The signals from DLTS allow meaningful results to be derived from the relationship between its emission rate and temperature. From this relationship, an Arrhenius plot can be drawn to determine the enthalpy of ionisation formation and the capture cross-section. As shown in Figure 5. 4, the DLTS signal has a result of $dS(T)/dT = 0$ at the peak. The emission rate in (2. 28) can be modified as follows in terms of enthalpy and entropy:

$$e_n(T) = \sigma_{na}\langle v_n\rangle N_c exp\left(\frac{-\Delta H}{kT}\right) \tag{5. 22}$$

This equation can be expressed as follows with temperature independent constants β (48):

$$e_n(T) = \sigma_{na}\beta T^2 exp\left(\frac{-\Delta H}{kT}\right) \tag{5. 23}$$

Where βT^2 is:

$$\beta T^2 = \langle v_n\rangle N_c = \sqrt{\frac{(3kT)}{(m_n^*)}}\,2\left(\frac{2\pi m_n^* kT}{h^2}\right)^{3/2} = \sqrt{\frac{3k}{m_n^*}}\,2\left(\frac{2\pi m_n^* kT}{kT}\right)^{3/2} T^2 \tag{5. 24}$$

Equation (5. 23) contains the emission rate and capture cross-section. Taking the logarithm of both sides of this equation yields an Arrhenius plot of $ln(e_n/T^2)$ versus $1/T$. This plot indicates ΔH by the slope, and the capture cross-section from the y-intercept.

Trap concentration

As mentioned in equation (5. 19), this equation can be substituted into equation (5. 21) to obtain the concentration of the trap from the signal. Thus, the following equation can be obtained:

$$S_i(T) = \frac{C(\infty)N_t}{2N_d}\left\{\frac{1}{n_i}\sum_{t_j=t_d}^{t_d+t_i} e^{-e_n t}\,\omega(t)\right\} = \Delta C_0 F_i \tag{5. 25}$$

F_i is a numerical factor under a given time window. From equation (5. 25), the concentration of traps is given by:

$$N_t = \frac{2N_d S_{i,peak}\left(T_{peak}\right)}{C_p(\infty)F_i} \tag{5. 26}$$

Window (i)	Number of measurement points ($n_i = 2^i$)	Window length (t_i, s)	e_n^{max} (s^{-1})	t_d (s)	$e_n^{max} t_i$	F_i
1	2	0.1000	14.4896	0.5	1.4490	0.1249
2	4	0.2000	9.0859	0.5	1.8172	0.1549
3	8	0.4000	5.2450	0.5	2.0980	0.1760
4	16	0.8000	2.8529	0.5	2.2823	0.1888
5	32	1.6000	1.4941	0.5	2.3906	0.1959
6	64	3.2000	0.7656	0.5	2.4498	0.1997
7	128	6.4000	0.3876	0.5	2.4808	0.2017
8	256	12.8000	0.1951	0.5	2.4967	0.2026
9	512	25.6000	0.0979	0.5	2.5050	0.2031

Table 5. 1 The calculated values of parameters for DLTS signal used in this study (47-49).

5.4 Thermal dielectric relaxation current technique (TDRC)

The thermal dielectric relaxation current technique (TDRC) was first studied by J.G. Simmons and G. W. Taylor in 1974 (50). The basic idea of this measurement method is to detect the flow of electrons from the surface traps as the MOS device changes from the non-steady state to the steady state, as it is switched from the accumulation mode to the deep depletion mode with temperature (51). This concept is derived from the thermally stimulated current (TSC) technique (52, 53). The following account of TDRC theory is taken from J.G. Simmons and G.W. Taylor, 1973.

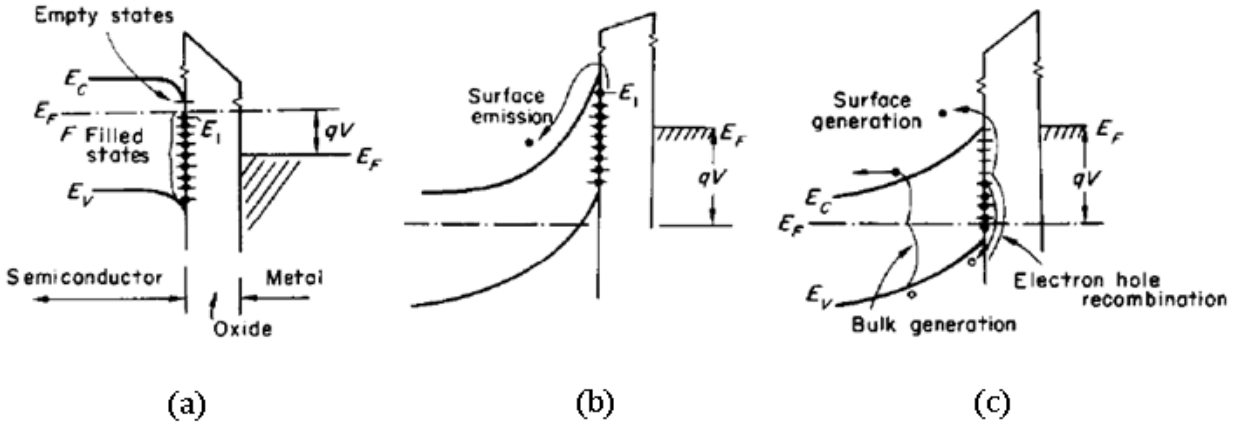


Figure 5. 5 n-type MOS device of (a) accumulated mode with filled states under the Fermi energy level; (b) deep depletion mode with low temperature. Here, due to the low temperature, electrons cannot escape from interface traps ($T = T_0$); (c) where $T > T_0$, electrons are emitted from interface traps. From J.G. Simmons and G.W. Taylor, 1973 (50).

First, as shown in Figure 5. 5 n-type MOS device of (a) accumulated mode with filled states under the Fermi energy level; (b) deep depletion mode with low temperature. Here, due to the low temperature, electrons cannot escape from interface traps ($T = T_0$); (c) where $T > T_0$, electrons are emitted from interface traps. From J.G. Simmons and G.W. Taylor, 1973 (50).(a), a charging bias is

applied to the MOS device at a high temperature (usually room temperature) to allow the device to reach the accumulated mode. Thus, majority carriers are captured in the trap states at the interface. This bias is continuously applied until the device is sufficiently cooled. When the low temperature T_0 is reached, as the temperature rises again at a certain rate, the bias is converted to discharging. This bias leads the device to depletion, causing the emission of the majority carriers (Figure 5. 6). An increase of temperature accompanies the ramp rate β. Thus, linearly changing temperature with time t is:

$$T = \beta t + T_0 \tag{5. 27}$$

In this paper, T_0 is 50 K and the rate of temperature rise is 2 K/min.

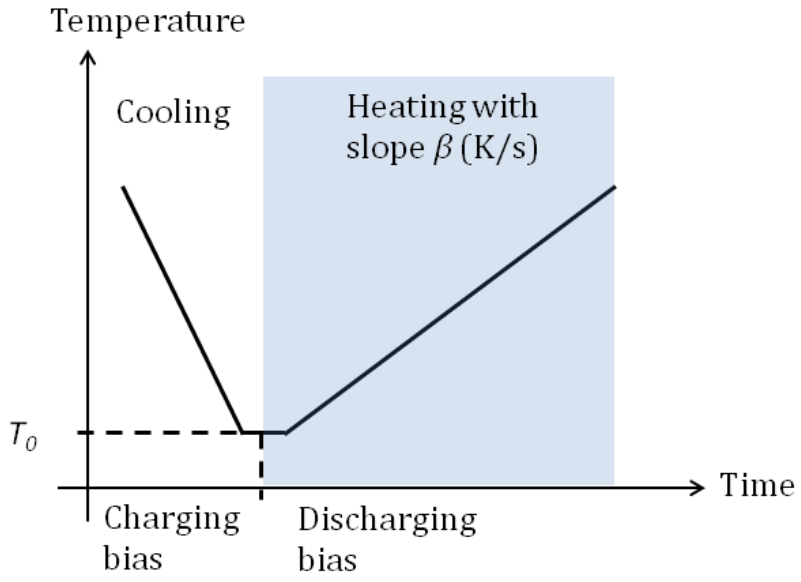


Figure 5. 6 Temperature variation over time for TDRC measurement (53).

5.4.1 Emission and generation of majority carriers

In the non-steady state, the current caused by the expansion of the deep depletion region is divided into two situations. First, electrons are emitted from the highest filled energy level in the upper half of the band gap. The current is then generated by traps in the lower half of the band gap.

The current from surface traps located in the upper half of the band gap is given by:

$$I = \frac{AC_{ox}\dot{Q}_t}{C_{ox} + C_d} \tag{5. 28}$$

Where C_{ox} and C_d are the capacitance of the oxide and the depletion region of the semiconductor, respectively. A is the device area, and $\dot{Q}_t$ is the emission rate of surface state charges. The emission rate of electrons per unit area from filled traps at an incremental energy range δE in an n-type substrate is as follows:

$$\frac{d(\delta n_t)}{dt} = -e_n n_t dE = -e_n \delta n_t \tag{5. 29}$$

Where n_t is the number of trapped electrons per unit area per unit energy, and e_n is the emission coefficient of electron traps. The general equation of the above equation is given by:

$$\delta n_t = N_{it}(E)\exp\left(-\int_0^t e_n dt\right) dE \tag{5. 30}$$

Where N_{it} denotes the energy distribution of interface states. By placing equation (5. 27) into (5. 30), the total emission current $\dot{n}_t$, integrate over the band gap $E_c \sim E_v$ by substituting the equation becomes:

$$\dot{n}_t = \int_{E_v}^{E_c} N_{it}(E) e_n \exp\left(-\frac{1}{\beta}\int_{T_0}^{T} e_n dT\right) dE \tag{5. 31}$$

The charge emission rate of the surface state from this total emission current can be expressed as $q\dot{n}_t = \dot{Q}_t$, so that equation (5. 31) is applied to equation(5. 28):

$$I = \frac{AC_{ox}q}{C_{ox}+C_d}\int_{E_v}^{E_c} N_{it}(E) e_n \exp\left(-\frac{1}{\beta}\int_{T_0}^{T} e_n dT\right) dE \tag{5. 32}$$

The function $P(E,T)$ can be introduced to extract N_{it}, and to increase the accuracy of any trap distribution of the integral part of the above equation. The function $P(E,T)$ is:

$$P(E,T) = e_n \exp\left(-\frac{1}{\beta}\int_{T_0}^{T} e_n dE\right) \tag{5. 33}$$

The graph obtained by substituting (5. 33) into equation (5. 32) appears as a peak with a maximum value in energy E_m as a function of $E_C - E_{it}$ and temperature T, i.e. $\frac{\partial P(E_m,T)}{\partial E} = 0$. The relationship between energy E_m and temperature T is given by:

$$\frac{T}{\beta}\int_{T_0}^{T}\frac{e_n}{T} dT = \frac{kTe_n(E_m,T)}{\beta(E_c - E_m)} = 1 \tag{5. 34}$$

The relationship between this energy $E_c - E_m$ and temperature T_m can be deduced to be linear from $e^{\frac{\Delta E}{kT_m}} = \frac{\upsilon\sigma_n N_c k}{\beta \Delta E}$. Therefore, the straight line for this relation is $\Delta E = CT_m - D$, with slope C, which is built from a plot of $\frac{\Delta E+D}{T_m}$ $vs\log_{10}(v/\beta)$ and depends on v and β (where $v = \upsilon\sigma_n N_c$). The intercept D is given by $D \simeq 0.0155$. From the plot, $\frac{\Delta E+D}{T_m}$ is defined as $Blog_{10}\left(\frac{s}{\beta}\right) + Z$, where the slope B and intercept Z are defined as 1.92×10^{-4} and 0.32×10^{-3}, respectively, by J.G. Simmons and G.W. Taylor in 1972 (54). Hence, ΔE with an approximation about temperature in the emission process is given by:

$$\Delta E(T) = T\times10^{-4}\left(1.92\log_{10}\left(\frac{v}{\beta}\right)+3.2\right)eV/K\ -0.0155\ \text{eV} \quad (5.\ 35)$$

With the unit of eV, where v, the attempt-to-escape frequency, is:

$$v = N_c v_{th}\sigma_n \quad (5.\ 36)$$

5.4.2 Data extraction from TDRC

The number of trapped electrons N_t and v can be obtained by two temperature maxima from plotting the two different I–T characteristics with two different heating rates β in equation (5. 35). The trap density is obtained from the area of the curve:

$$N_t = \frac{2\times area}{q\beta} \quad (5.\ 37)$$

While v, the attempt-to-escape frequency, is defined as:

$$v = 10^{y} \quad (5.\ 38)$$

Where $y = \frac{T_2\log_{10}\beta_2 - T_1\log_{10}\beta_1}{(T_2-T_1)}$

5.5 Experimental setups

An HP4280A 1MHz and BOONTON 7200 capacitance meter were used to measure the CV and DLTS. This instrument applies a bias to the sample and measures the capacitance versus time transients. For the DLTS, filling pulse applied from Agilent 81110A 165/660MHz pulse generator. To mount the sample to the instrument, Ag paste applied on ground plate which is a nickel coated sapphire plate film. The temperature sensor is also glued on the ground plate. The temperature for cooling process is controlled by LakeShore 331 with temperature range of 20–350K, and LTC-21 for the heating process for 120–700K. The cryostats were always kept in vacuum by turbomolecular pump. The controlling and measurement were performed by Labview™ programmes and the connection was made by the GPIB bus.

For the IV and TDRC measurements, A keithley 6487 picoammeter/voltage source was used for measuring current while applying the bias. The sample also mounted on the ground plane. MOSFET measurement is performed with Pegasus S200FA (Wentworth Laboratories). The current applied by keithley 6487 and 2440 5A SourceMeter was used for applying bias.

PART III – Results and discussion

6. Results and discussion

To investigate the Ga_2O_3 based MOS structures for power electronic devices, and in particular to determine the quality at the interface, several electrical characteristics are measured. Current–voltage measurement (IV) and the capacitance–voltage measurement (CV) are tools that can directly show the characteristics of the device. Thus these measurements are discussed first, and then, techniques to investigate defects at the interface and in the bulk were performed, including thermal dielectric relaxation current (TDRC) and deep level transient spectroscopy (DLTS).

Experiments were conducted on MOS capacitors fabricated according to the procedure in chapter 4. The thickness of the Al_2O_3 gate oxide layer deposited by ALD was measured by an ellipsometer and the thickness was approximately 19.6 nm for all MOS capacitor (MOSCAP) and MOSFET samples.

First of all, the IV and CV on different surface orientations of β–Ga_2O_3 (010) and (-201) are compared. The β–Ga_2O_3 grown by EFG method and the wafer contains UID. The effective donor concentration is $N_D \approx 1{\sim}5{\times}10^{17}/\mathrm{cm}^{-3}$. And the 4H–SiC contains around 10μm epitaxial layer with $1.0{\times}10^{15}/\mathrm{cm}^{-3}$ of carrier concentration. Next, the thickness dependence of the Al_2O_3 layer on 20nm and 100nm of β–Ga_2O_3 (010) are also compared as measurement results of (010) surface orientation show better performances. Based on these results, three types of heat treatments were arranged on β–Ga_2O_3 (010) and 4H–SiC. Here 4H–SiC is used for the reference as it is a well-known substrate. After the IV and CV, DLTS were followed by TDRC and DLTS to investigate defect states in the bulk and interface.

The types and conditions of the samples used in the experiments are summarized in the Table 6. 1.

	β–Ga_2O_3	**4H–SiC**
IV/CV	(010) β–Ga_2O_3 with 20nm Al_2O_3 (-201) β–Ga_2O_3 with 20nm Al_2O_3	–
IV/CV	(010) β–Ga_2O_3 with 20nm Al_2O_3 (010) β–Ga_2O_3 with 100nm Al_2O_3	–
IV/CV TDRC DLTS	(010) β–Ga_2O_3 with 20nm Al_2O_3 – As–deposition (010) β–Ga_2O_3 with 20nm Al_2O_3 –600°C annealing (010) β–Ga_2O_3 with 20nm Al_2O_3 –1000°C annealing	4H–SiC with 20nm Al_2O_3 – As–deposition 4H–SiC with 20nm Al_2O_3 – 600°C annealing 4H–SiC with 20nm Al_2O_3 – 1000°C annealing
H^+ irradiation	(-201) β–Ga_2O_3 – no irradiation (-201) β–Ga_2O_3 – $3{\times}10^{13}$ cm^{-2} dose (-201) β–Ga_2O_3 – $6{\times}10^{13}$ cm^{-2} dose (-201) β–Ga_2O_3 – $1{\times}10^{14}$ cm^{-2} dose	–
MOSFET and MESFET fabrication	(-201) β–Ga_2O_3 with 20nm Al_2O_3	–

Table 6. 1 The sample for experiments

6.1 Electronic characteristics of β–Ga_2O_3 MOS capacitors

Current-voltage (IV) and capacitance-voltage (CV) measurements were carried out on each diode for all samples at room temperature. On each sample, several diodes are found with three different contact areas – 200µm, 480µm and 800µm of diameters. The oxide layer with Al_2O_3 was deposited by ALD and Ni/Al Schottky and Ti/Al Ohmic contacts were fabricated by PVD. The criteria for good performance samples was a low reverse current density from IV, high oxide capacitance from CV and a low conductance in the accumulation region from the conductance–voltage measurement (GV). In regard to the shadow mask, it has been heavily used, resulting in contacts that deviate somewhat from a perfect circle. Thus, this may have an affected on the actual size of the diode, and may influence the extracted parameters.

The purpose of the IV and CV measurements is to assess the quality of the structure. Defects at or near the interface, and in the oxide layer, may degrade the device properties and are of utmost importance. Therefore, it was preceded before the study of defects in bulk and interface to understand the feature of the device. Here, this has mainly been investigated using CV curves. As mentioned in section 5.1, $1/C^2$ as function of V and voltage sweeping are plotted to estimate bulk carrier concentration and interface properties.

6.1.1 IV and CV on the (010) and (-201) surface orientations of β–Ga_2O_3

Two types of different surface orientations of β–Ga_2O_3 are evaluated. IV and CV are measured using diode contacts with an area of 1.81×10^{-3} cm^2 and measured in 500mV/s.

Current–voltage and capacitance–voltage measurements

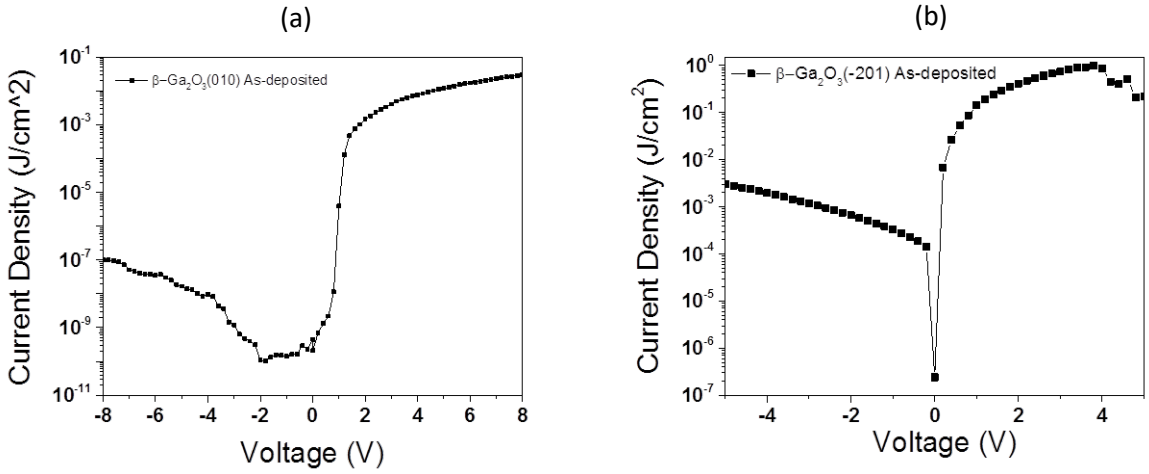


Figure 6. 1 The IV characteristics of β–Ga_2O_3 with a (010) (a) and (-201) (b) surface orientation. (a) is IV from (010) orientation sample, and (b) is from (-201) orientation sample. Both IV indicate current rectification with forward bias (positive voltage).

IV on both (010) (Figure 6. 1(a)) and (-201) β–Ga_2O_3 (Figure 6. 1(b)) MOS samples clearly show current rectification and n–type semiconductor behavior. The most noticeable point is the difference in current rectification magnitude. (010) β–Ga_2O_3 has rectification of around six orders of magnitude, however, (-201) sample shows only three orders of magnitude, and a considerably

higher reverse leakage current compared to that of the (010) sample. This is probably due to the difference in interface quality where the surface orientation of beta-gallium oxide plays a key role (55). In the Figure 6. 1 (a), the IV from (010) orientation, the increased current appears on the forward bias region (positive voltage) and saturated after around 1.5V. On the reverse bias region in negative voltage has relatively low current density. The current density difference between forward and reverse bias is over five orders of magnitude. The IV of (-201) orientation sample shows also increased current density along with forward bias, however, larger reverse current appears on the negative bias. The difference of current density in forward and reverse is only three orders of magnitude and overall current density is quite large. Thus, (010) sample has a better IV character. To further investigate the features of the MOS structure, capacitance–voltage measurement was performed.

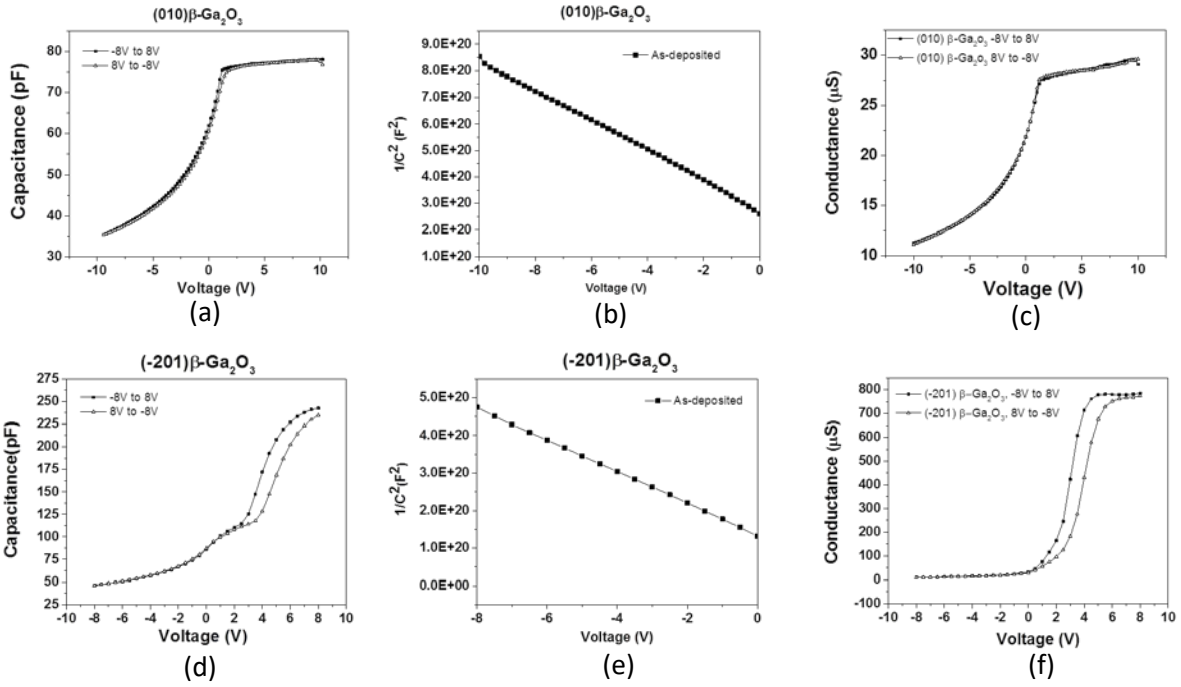


Figure 6. 2 the CV curve from different surface orientation samples of β–Ga_2O_3 (a), (d). Donor concentration calculated from $1/C^2$ vs applied voltage (b), (e) and conductance vs voltage(c), (f).

Figure 6. 2 shows the CV and GV on MOSCAP of (010) and (-201) β–Ga_2O_3. The samples are measured from -10V to 10V first, followed by the reverse measurement from 10V to -10V to see a hysteresis of the capacitance. The samples are n-type substrates, therefore, accumulation regions are observed at positive voltage range for all samples. First of all, an interesting observation is that CV of (-201) β–Ga_2O_3 sample (Figure 6. 2 (d)) reveals a kink in the voltage range from 0V to 4V, and hysteresis from 3V. This kink appears in the measurements on all contacts of the MOS sample with (-201) orientation. Interestingly, the IV of the (-201) substrate MOS (Figure 6. 1(b)) also indicates a distortion above 4V. In terms of GV at Figure 6. 1(f), the kink is not seen, but saturates after 4V.

Moreover, for MOS with (010) β–Ga_2O_3 substrates, the value of oxide capacitance is 80pF, which is smaller than the capacitance of (-201) orientation sample as its oxide capacitance is 250pF. These calculated values are lower than the oxide value with given oxide thickness. By the equation $C_{ox} = \varepsilon_{ox}/t_{ox}$, 20nm Al_2O_3 indicates 720pF for the same dot area MOS. However, there is no kink and the hysteresis is barely seen. The origin of this kink is uncertain and is open to various interpretations. For example, it may indicate that there is a recharging process at the β–Ga_2O_3 surface as a weak accumulation appears.

In addition, the CV curve offers information about charges at the interface between oxide layer and semiconductor, and from the oxide near the interface. The presence of mobile charge can be detected by sweeping the voltage. The difference of flatband voltage in the hysteresis of the (201) β–Ga_2O_3 sample is larger, so this sample can be assumed to contain more mobile charges. There are several reasons why depletion region has kink and higher conductance in (-201) samples, apart from the quality problem of the surface of the 201 sample. First, the gate oxide may not be uniform enough to keep the current stable. This can be the reason for the leakage current in IV and the instability of capacitance due to the non–uniform oxide thickness and quality. In addition, there is a possibility that the MOS structure may have been damaged during repeated experiments.

From the figure 6. 2 (b), (e) donor concentration (N_D) (equation (5. 2)) and built-in voltage (V_{bi}) are obtained. The donor concentration was found to be 1.97×10^{17} cm^{-3} and 1.34×10^{17} cm^{-3} on (010) and (-201) samples, respectively. These values match the donor concentration provided by the sample vendor, $1\sim5\times10^{17}$ cm^{-3}. A difference in the substrate charge carrier concentration may influence the CV and IV characteristics, however, the difference is considered to be insignificant, suggesting that the (-201) substrate has lower quality at the interface. In addition, the built-in voltage is calculated at 4.87V, 3.23V on (010) and (-201) samples respectively. As the contacts of the samples are formed using identical material (100nm of Ni, 200nm of Al), the difference of built-in voltage indicates that their surface potential is different. In sum, MOSCAP with (010) substrate shows a more stable outputs.

6.1.2 (010) β–Ga_2O_3 MOS with different Al_2O_3 oxide layer thickness 20nm and 100nm

Current–voltage and capacitance–voltage measurements

In previous experiments it was determined that (010) surface orientation exhibited a more stable device properties compared to that of the (-201) sample. In addition, a shift towards positive voltages in CV curve was observed for the (-201) orientation, and considered to imply the existence of charges at the interface of the oxide–semiconductor.

In order to investigate the difference by thickness of the oxide layer, Al_2O_3 was deposited by ALD on the (010) β–Ga_2O_3 substrate by 20nm and 100nm respectively, and the results of IV and CV are plotted in figure 6. 3.

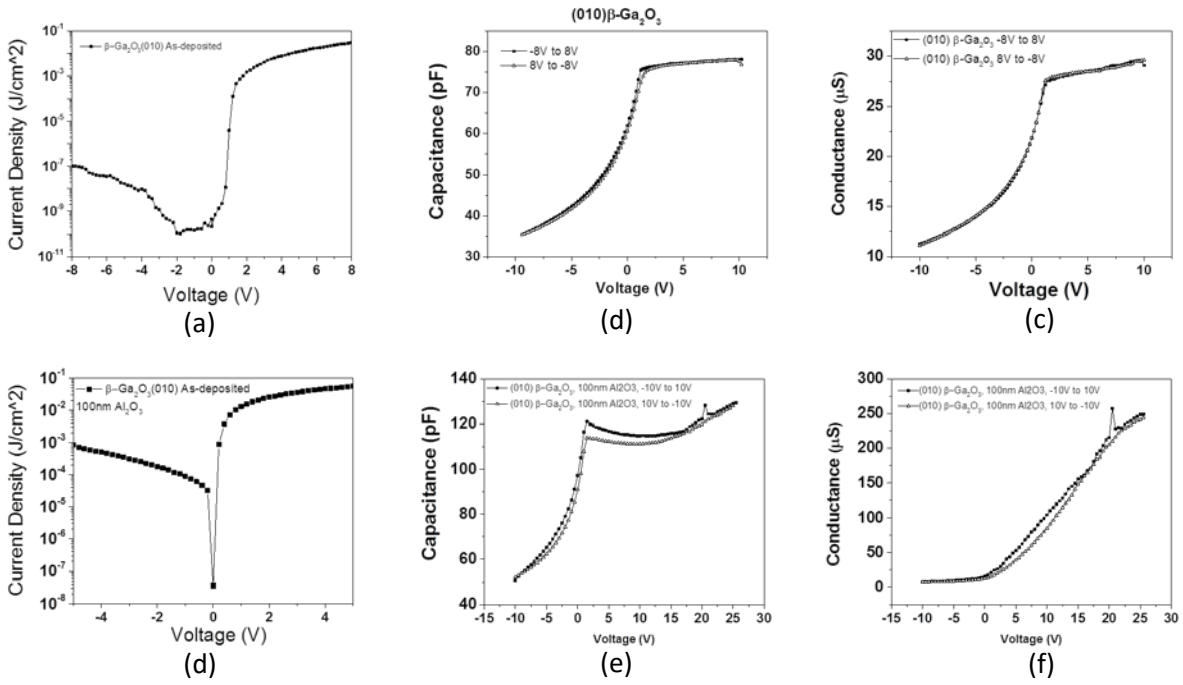


Figure 6. 3 IV(a), CV(b), GV(c)for 20nm Al_2O_3, and for 100nm Al_2O_3 (d-f) on the (010) β–Ga_2O_3 substrate MOS capacitor.

Comparing the IV curves of the 20nm (Figure 6. 3 (a)) and 100nm (Figure 6. 3 (d)) Al_2O_3 oxide , the result from 100nm Al_2O_3 shows a higher current density with a reverse bias value of $\sim 10^{-4}$ compared that of to 10^{-7} for the 20nm layer. CV and GV graphs show also distinct differences. It can be seen that the capacitance in the accumulation region of the CV graph (Figure 6. 3 (e)) is not constant and the conductance from the GV graph (Figure 6. 3(f)) continues to increase over 0V. Based on the two graphs and IV, it can be assumed that a significant leakage current is present this sample. This may be explained by a non-uniform layer, or the presence of pinholes leading to a higher conduction between the metal electrode and the sample. The latter hypothesis may also explain the difference in measured capacitance compared to the calculated value.

6.1.3 Comparison of the performance of (010) β–Ga_2O_3 and 4H–SiC MOS capacitor

4H–SiC is a well-known and widely studied material for use in power electronics. Thus, since 4H–SiC has been studied for a long time as a device for high power and high temperature, it is instructive to compare the β–Ga_2O_3 MOS structure, and in this case the (010) surface orientation, with a similar structure based on 4H–SiC. The results are shown in figure 6. 4. The value of N_D and V_{bi} voltage from the 4H–SiC sample is extracted from figure 6. 4 (c), and found to be $2.25\times10^{15}$and 5.36V respectively, and the V_{bi} is higher than β–Ga_2O_3 substrate samples.

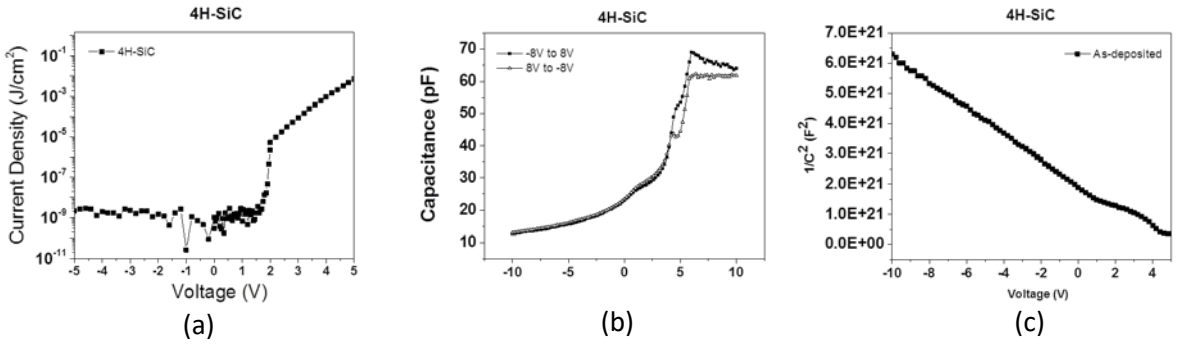


Figure 6. 4 IV(a), CV(b), and $1/C^2$ of 4H–SiC MOS sample.

The current density in figure 6. 4 (a), a voltage difference between reverse and forward bias appeared from 10^{-9} to maximum 10^{-5} and clearly shows current rectification. Thus, a significant difference between the behavior of the Al_2O_3 deposited on 4H–SiC and β–Ga_2O_3 is observed. The oxide layer deposited on 4H–SiC is closer to what is expected from a MOS structure, where the current across the oxide layer is low. In the CV measurement, the oxide capacitance is 63∼70pF, which is lower than as–deposited β–Ga_2O_3 substrate sample. The most noticeable difference in the 4H–SiC CV graph (Figure 6.4 (b)) is the kinks observed for positive voltages up to ∼5V. Before the capacitance reach to the accumulation, two kinks were found at around 1.8V and 5V in the depletion region. This phenomenon has previously been reported, not only with Al_2O_3 (56), but also with the SiO_2 oxide layer (57). The kink in the depletion region may be associated with poor channel mobility in the MOS structure, or a trapping or recharging process in the 4H–SiC/Al_2O_3 interface. Depending on the substrate material the difference between IV and CV is clearly evident. It assumed that the growth of Al_2O_3 is different on β–Ga_2O_3 and 4H–SiC as the IV of 4H–SiC indicates less leakage current. Initially, it was assumed that it was caused by pinholes or any other similar causes that allows for large leakage current, but pinholes or equivalent was not observed by the optical microscopy.

6.1.4 Influence of annealing on (010) β–Ga_2O_3 and 4H–SiC MOS

In fact, in 4H–SiC substrate MOS devices, there are many studies that show the annealing process being performed after the deposition of the oxide layer has reduced the interface trap density (D_{it}) (58) while improving bulk of Al_2O_3 and interface properties with above 900-1000°C(59-61). It is further known that the amorphous oxide is crystallized by annealing during deposition, which has a positive effect on the performance. Encouraged by these findings, various annealing temperatures were studied for the β–Ga_2O_3 samples. Thus, samples of three conditions of As-deposited, 600°C annealing and 1000°C annealing were prepared on (010) β–Ga_2O_3 and 4H–SiC MOSCAPs. According to a study by M. Avice 2007 (59), Al_2O_3 and 4H–SiC capacitor annealing in N_2 gas atmosphere reduced hysteresis and near–interface traps (N_{it}) in CV. Compared to the O_2 gas atmosphere, N_2 also has the advantage of preventing the formation of other oxides at the interface.

Therefore, the annealing in N_2 gas atmosphere was expected that the kink in the 4H–SiC MOS depletion region would be reduced, improving in CV characteristics. The β–Ga_2O_3 substrate was also annealed under the same conditions and the characteristics were compared.

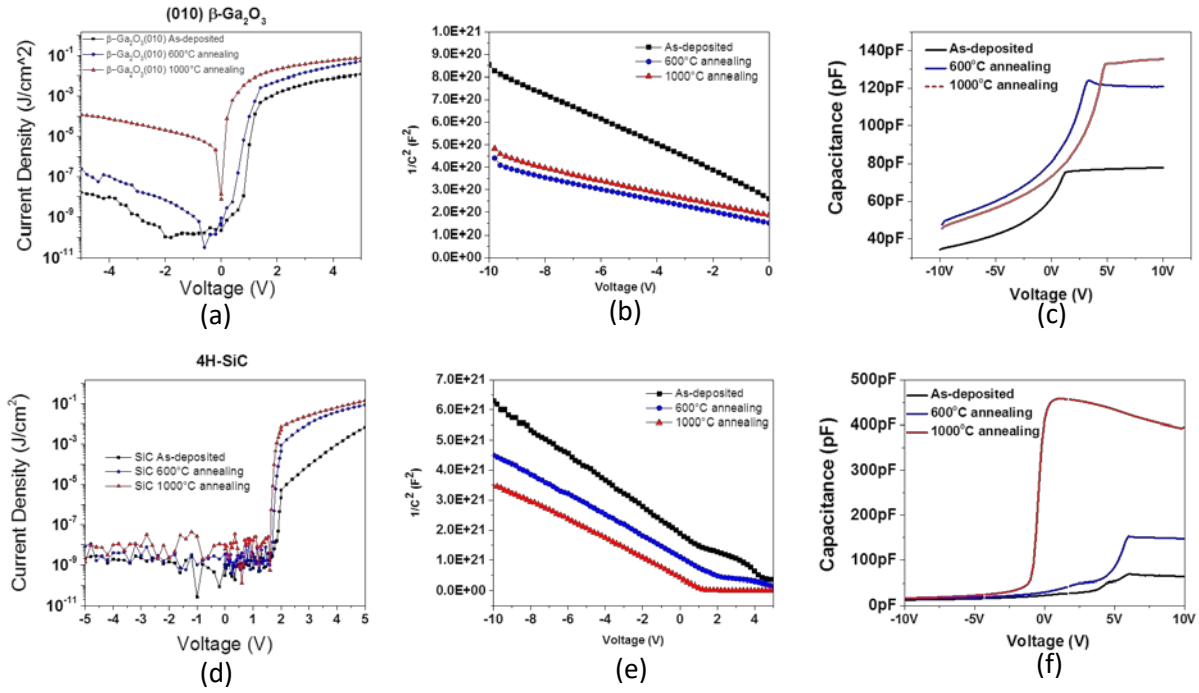


Figure 6. 5 (a), (b), (c) are IV, CV, 1/C^2 of β–Ga_2O_3, and (d), (e), (f) are of 4H–SiC. The black colour is for As–deposited, blue colour for 600°C annealing and red colour for 1000°C annealing conditions.

Firstly, in the reverse bias region the IV was noisy, especially in case of 4H–SiC substrate samples (Figure 6. 5 (a) and (d)). The increased noise in the reverse bias region is thus due to current values at the limit of the measurement equipment. The rectification ability of β–Ga_2O_3 is shown in order of 10^7, 10^6, and 10^2 for as–deposited, 600°C, and 1000°C annealed sample, respectively. On the other hand, higher rectification ranges and less reverse current density are observed for the 4H–SiC MOSCAP samples with order of 10^4, 10^6, and 10^7 with increasing annealing temperature.

In the CV measurement in figure 6. 5 (c) and (f), the capacitances of the β–Ga_2O_3 and 4H–SiC based MOS structures clearly increases along with the annealing temperature. The values of the oxide capacitances of β–Ga_2O_3 MOS samples are ~78pF, 122pF and 135pF for as-deposited, 600°C annealing sample, and 1000°C annealing sample, respectively. 4H–SiC MOSCAPs indicate the oxide capacitance values of 70pF, 145pF and 450pF respectively. However, oxide capacitance per unit area is obtained by the dielectric constant of an oxide material divided by the oxide thickness ($C_{ox} = \varepsilon_{ox}/t_{ox}$). By calculation, the oxide capacitance of 20nm Al_2O_3 is 720pF. Thus, for all cases the samples show lower oxide capacitance than the value of an ideal 20nm Al_2O_3 sample. This means that the actual thickness of the oxide is different. In effect, the actual average oxide layer obtained

with an elipsometer was 19.6 nm before the annealing process. Also, it may be that some charges or compounds where generated at the interface, which prevented the capacitance of the ideal Al_2O_3 insulator from being obtained. In addition, both of the substrates show increased oxide capacitance with increasing annealing temperature. This may be due to the fact that when Al_2O_3 is first deposited to ALD, it is deposited amorphously, and that is Al_2O_3 being crystallized by the annealing process. The crystallization can affect both the oxide thickness and ε_{ox}, so the differences are possible.

However, in terms of flatband voltage (V_{FB}), contradictory results appear for the two different substrate MOS devices. The flatband voltages are found to be 1.20V, 3.40V and 4.80 V from the CV graph of β–Ga_2O_3 MOS, while the values of 4H–SiC are 6.0V, 6.0V and 0.9V respectively. Generally, flatband voltage shift occurs due to the fixed charges, oxide trapped and mobile ionic charge at interface. Thus, the normalized capacitance–voltage graph in Figure 6. 6 clearly shows that there is charge distribution across the MOS structure and at the interface of Al_2O_3/β–Ga_2O_3 and 4H–SiC.

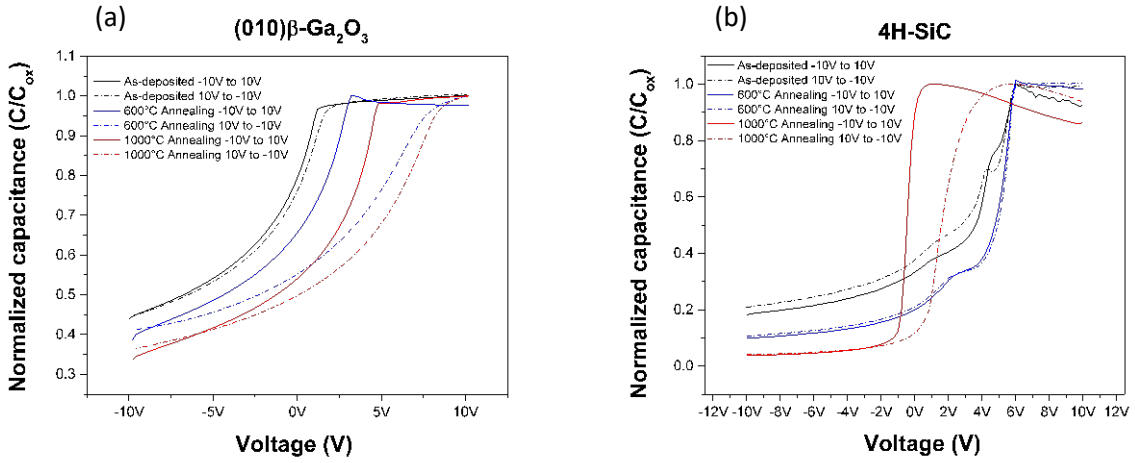


Figure 6. 6 Normalized capacitance of (010) β–Ga_2O_3 (a) and 4H–SiC(b).

Further, a hysteresis phenomenon is observed when sweeping the bias voltage from different starting polarities, which indicates that the mobile charge is more present in the annealing samples. Figure 6. 6 shows normalized capacitance in voltage sweeping from -10V to 10V and 10V to -10V. The hysteresis and shift of V_{FB} were found in all samples, especially the annealed samples. The shift of V_{FB} generally means trapping of charges such as sodium ions contained in the oxide layer. (010) β–Ga_2O_3 MOS samples were shifted toward the positive voltage direction by the annealing temperature, whereas the 1000°C annealed 4H–SiC MOS sample was shifted toward the negative voltage direction. The hysteresis phenomenon was most pronounced in the β–Ga_2O_3 600°C annealed sample and 4H–SiC 1000°C sample. Interestingly, in the 4H–SiC sample the kink disappeared when the temperature was increased. The as-deposited 4H–SiC MOSCAP clearly shows two kinks, but for the 600°C annealed sample, the kink observed at around 5V disappeared, and the 1000°C annealed sample shows no kinks. This may indicate that the defects recover from the inside

of the oxide depending on the annealing temperature. (not shown) The hysteresis and differences in V_{FB} are observed in GV as well.

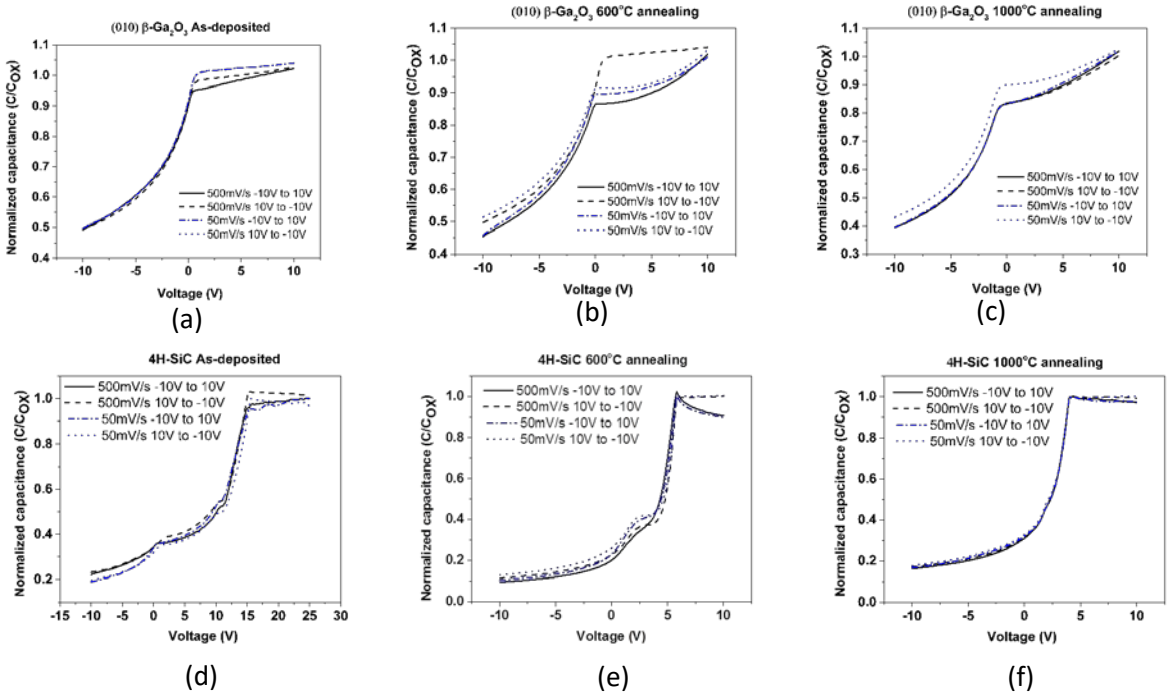


Figure 6. 7 Normalized CV curves measured from -10V to 10V and 10V to -10V. (a), (b) and (c) are CV in β–Ga_2O_3, (d), (e) and (f) are CV in 4H–SiC. Black lines indicate the CV measured in 500mV/s, blue lines are measured in 50mV/s.

Normalized CV measurements are performed using a 1MHz probing signal and a fast (500mV/s) and slow sweep rate (50mV/s) (Figure 6. 7). First of all, all samples have been repeatedly stressed by IV, CV, TDRC, and DLTS measurements, and damage to the structures may therefore be anticipated. Particularly, degradations are observed in accumulation part with lower and unstable capacitances (not shown due to the normalization) and lower hysteresis differences. In addition as-depostied 4H–SiC sample shows the shifted flatband voltage to positive direction, compare to initial CV measurement (Figure 6. 6 (b), 6.0V to 15.2V).

The slow sweep rate measurements (the blue lines in figure 6. 7) in all samples result in a small reduction of the hysteresis. β–Ga_2O_3 samples showed less variation with sweep rate in as-deposited sample, and less change in capacitance of accumulation region. On the other hand, the 4H–SiC sample showed that the 1000°C annealed sample had the least change with sweep rate.

From this experiment, it was expected to see the 'deep depletion' according to the sweep rate, and that mobile charges in the oxide may have sufficient time to migrate. The deep depletion is a phenomenon that when the time constant of the carrier generation–recombination is large with the fast sweep rate, the inversion region is not formed completely due to the fast voltage sweep and the

depletion region becomes larger. This is presumably because the sweep rate is not sufficiently low or, the kinetic energy of the minority carrier was sufficient. However, since the state of the sample has deteriorated, it is difficult to say that the graph can indicate about the characteristics of the sample.

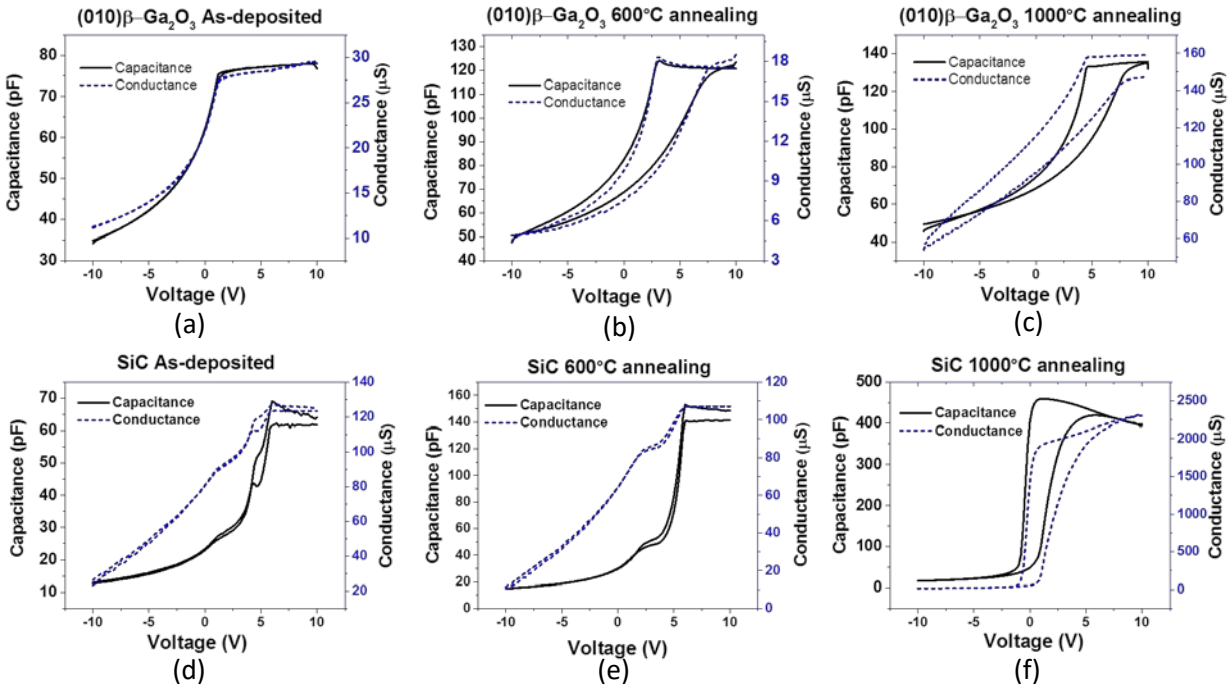


Figure 6. 8 Conductance–voltage graph for As–deposited(a, d) and 600°C (b, e) and 1000°C annealed samples (c, f). Hysteresis of conductance is observed also at annealed samples, and flatband voltage shifted to the positive direction along with voltage sweep from -10V to 10V, 10V to -10V.

The figure 6. 8 indicates GV and CV graphs from as–deposited, 600°C, and 1000°C samples. First, the voltage is applied from -10V to 10V and immediately followed by -10V to 10V to evaluate hysteresis. As a result, a distinct hysteresis is observed. As seen from the above figure, the capacitance and the conductance show a similar hysteresis behavior. Note that the samples annealed at 1000°C have high conductance values even at low voltage on both (-201)β–Ga_2O_3 and 4H–SiC MOS. The capacitance in accumulation region in 1000°C annealing of 4H–SiC sample (Figure 6. 8(f)) is decreased after peak of oxide capacitance, but the conductance is increased. This phenomenon is expected that it occurs due to leakage current as the applied voltage increases.

From the CV measurements several fundamental parameters of the device structure can be extracted. It also contains information about defects, especially in the interfacial and shallow oxide region, since the width of the depletion region is adjusted upon the applied voltage. The donor concentration N_D, flatband voltage V_{FB}(read-out) and threshold voltage V_{TH}(equation(2. 47))are calculated on each samples. In addition, effective density of oxide charge N_{eff} is obtained by dividing the effective oxide charges (Q_{eff}) by q ($1.6\times10^{-19}C$).

$$Q_{eff} = \frac{C_{ox}(\phi_{\mathrm{ms}} - V_{FB})}{A} \quad (6.\ 1)$$

Furthermore, slow traps near the β–Ga_2O_3/4H–SiC and Al_2O_3 interface of oxide can be a causative of shifted flatband voltage. Equation (6. 2) is used for *STD*, where is ΔV_{FB} is the flatband voltage difference in hysteresis.

$$STD = \frac{\Delta V_{FB} C_{ox}}{qA} \quad (6.\ 2)$$

The characteristics of the device obtained from the CV are summarized in the table 6. 2.

		N_D (cm^{-3})	V_{FB} *(V, Read out)*	V_{TH} *(V)*	N_{eff} (cm^{-2})	*STD* (cm^{-2})
β–Ga_2O_3	As–deposited	6.25E16	1.20	-4.12	3.91E11	1.62E11
	600°C annealing	1.40E17	3.40	-2.32	1.46E12	2.27E12
	1000°C annealing	1.41E17	4.80	-0.92	2.26E12	1.97E12
4H–SiC	As–deposited	2.25E15	6.0	-2.79	9.53E11	4.52E10
	600°C annealing	3.47E15	6.0	-2.85	2.19E12	5.18E10
	1000°C annealing	1.44E16	0.9	-3.14	4.07E12	5.68E12

Table 6. 2 Parameters calculated from measured CV at (010) β–Ga_2O_3 and 4H–SiC samples with three different annealing conditions.

Both substrates exhibit an increase in N_D, N_{eff}, and *STD* with increasing annealing temperature. This indicates that the annealing temperature evidently causes degradation associated with the oxide layer near the interface. The values of N_{eff}, *STD* and the flatband voltage difference obtained from the hysteresis curves are plotted in figure 6. 9. On the gallium oxide substrate, the difference between N_{eff} and *STD* and V_{FB} was large in the two annealed samples. On the 4H–SiC MOSCAPs, as–deposited and 600°C annealed samples show similar results for N_{eff} and *STD*. However, the value increases significantly in the 1000°C annealing sample. It can be expected that as alumina crystallizes at the highest annealing temperature, the oxide near the interface are more affected by fixed and/or mobile charges. Thus, one can conclude that in contrast to that observed in 4H–SiC MOSCAPS, post–deposition annealing do not have a positive effect on the capacitance–voltage characteristics. This may be important if the device is to be operated at high temperatures.

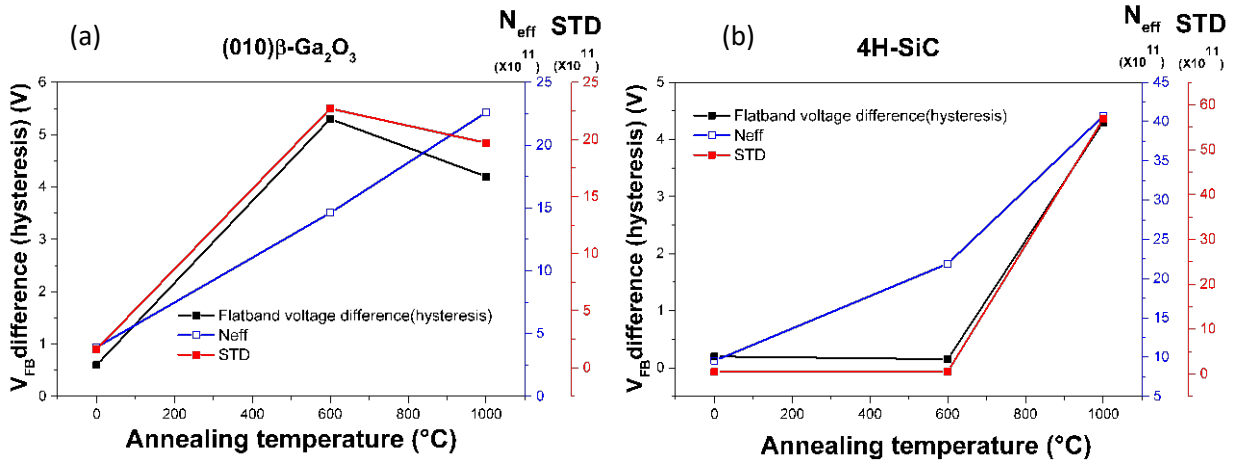


Figure 6. 9 Flatband voltage difference from hysteresis, effective oxide charge density and slow trap density. *N_{eff}* and *STD* are plotted in 1×10¹¹ per cm⁻³.

6.2 Bulk and interface defects

The results in section 6.1 reveal the need to investigate of electrically active defects at the interface of the Ga_2O_3 based MOS structures an in the bulk. In the present section, interface and bulk defects are investigated.

6.2.1 Defects based on CV

Interface trap densities (D_{it}) can be derived using several methods from the CV measurement. For example, a typical approach to study interface states using CV measurements is a high-low frequency method that extracts a D_{it} using a capacitance and surface potential change according to a different measurement frequency. This method follows equation(6. 3) (61).

$$D_{it} = \frac{1}{q}\left(\frac{C_{ox}C_{LF}}{C_{OX} - C_{LF}} - \frac{C_{OX}C_{HF}}{C_{OX} - C_{HF}}\right) \quad (6.\ 3)$$

Thus, three different measurement frequencies were used to find out D_{it} (figure 6. 10).

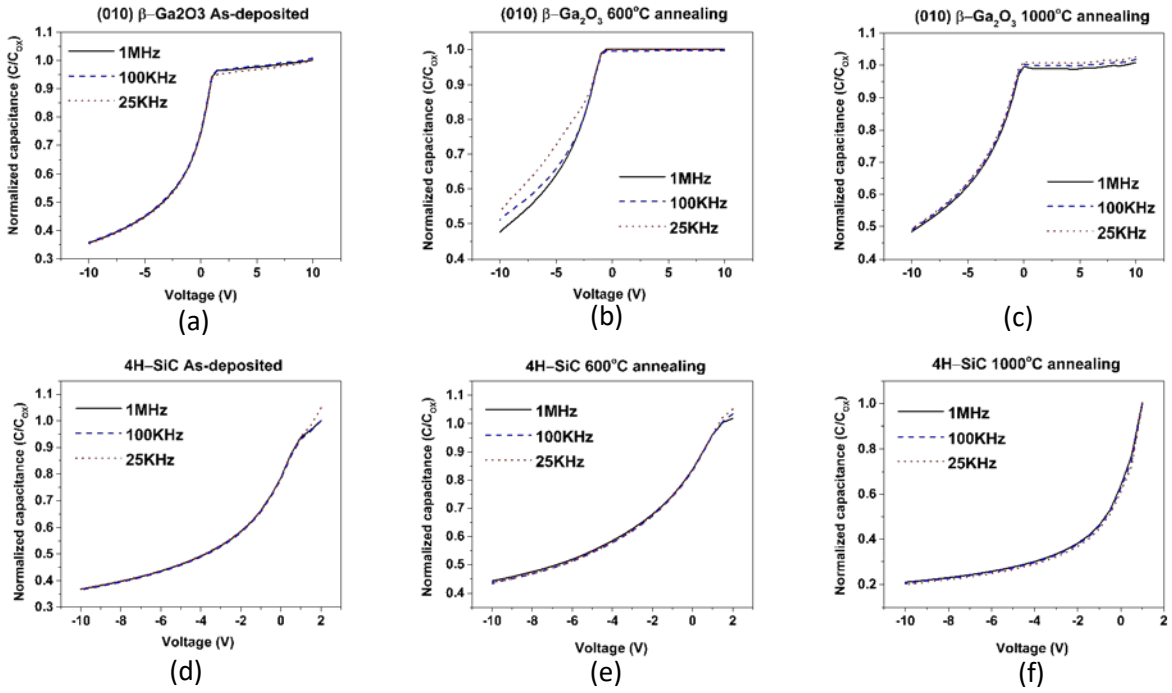


Figure 6. 10 CV measurements with various frequencies – 1MHz, 100KHz and 25KHz. The difference in capacitance according to the frequency is not shown conspicuously except for the 1000°C annealed β–Ga_2O_3 sample. With lower frequencies, CV curve for 4H–SiC samples was too noisy with high leakage after 2V.

However, it was not possible to reach the low frequency region for the present samples and the available equipment. The lowest bandwidth of equipment was attempted (20Hz), but it also did not present any difference in inversion area.

In another attempt to extract D_{it} from CV measurements, the Terman method was utilized. This method has an advantage that D_{it} is determined at the room temperature and using a single high frequency.

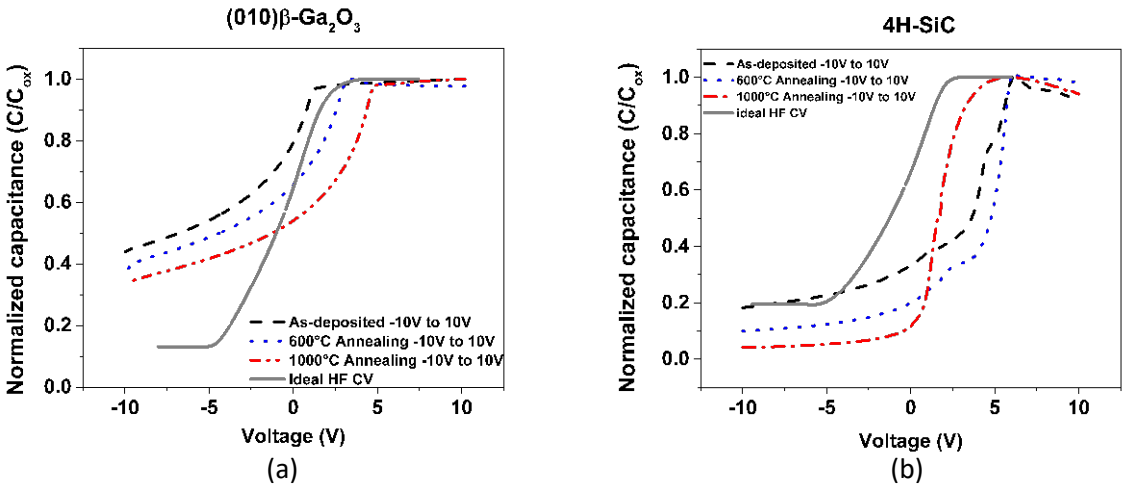


Figure 6. 11 Normalized CV curves with ideal high frequency CV curve (gray solid line)

Terman method starts by finding the surface potential (ϕ_s) in the ideal CV curve with respect to given high frequency capacitance (C_{HF}). Then the experimental C_{HF} is found, and the gate voltage (V_G) is extracted. From this process ϕ_s versus V_G will be obtained. The D_{it} can be determined from this curve with following equation (62).

$$V_G = V_{FB} + \phi_s + V_{Ox} = V_{FB} + \phi_s + \frac{Q_G}{C_{OX}} \tag{6. 4}$$

$$D_{it} = \frac{C_{OX}}{q^2}\left(\frac{dV_G}{d\phi_s} - 1\right) - \frac{C_S}{q^2} = \frac{C_{OX}}{q^2}\frac{d\Delta V_G}{d\phi_s} \tag{6. 5}$$

First, an ideal CV curve was calculated for this method. However, as discussed above, the oxide capacitance is significantly higher than the experimental CV curve, it was difficult to compare and obtain the stretched-out attribution directly. The normalized ideal CV curve was calculated and plotted with experimental CV curves in to find out the CV curve distortion.

The experimental CV curves in figure 6. 11 clearly reveal the stretched-out shapes compare to ideal CV curve. In particular, this distortion shows a larger difference in the 4H–SiC sample. This large distortion is known to be mainly attributed to fast surface states. It also causes an interface trap. However, in high frequency CV measurements, the interface trap is probably exhibit minimal distortion. It is because the time constant of fast surface state is short enough to respond to fast frequencies, and the interface traps have longer time constants.

For these reasons, it was not able to apply various CV techniques developed to find D_{it}. Therefore, TDRC and DLTS are used. These methods are well known for tracing the interface and bulk defect states.

6.2.1 TDRC Results

TDRC is well known for measuring D_{it} and near interface oxide traps (NIT_{ox}) as discussed in Chapter 5. First, traps at or near the interface were filled by applying a positive gate bias while the temperature was decreased from 300K to 50Kusing a cooling rate of 6K/min. Then the discharge process of the filled electrons was performed by increasing the temperature from 50K to 300K at a rate of 2K/min while maintaining a reverse bias. By applying a variety of filling biases during the cooling down, TDRC spectra are produced with defects state information and well known for measuring D_{it} and near interface oxide traps (NIT_{ox}).

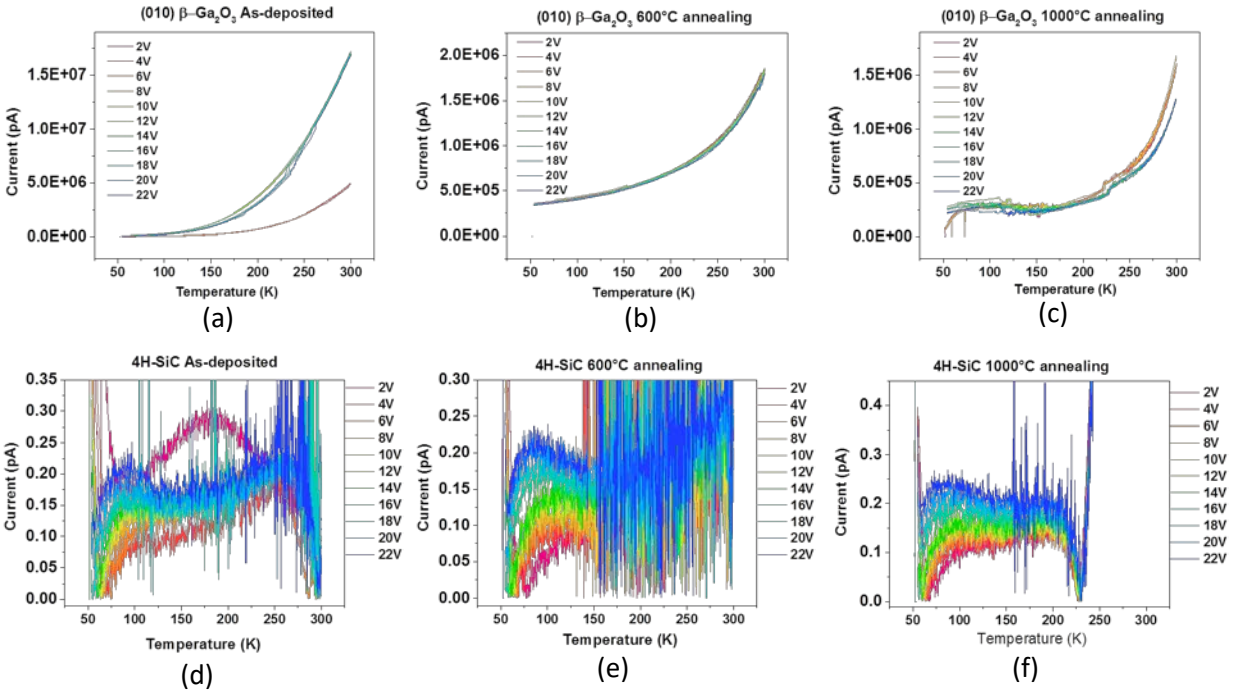


Figure 6. 12 TDRC results for (010) β–Ga_2O_3 (a), (b) and (c), for 4H–SiC (d), (e) and (f)

Figure 6. 12 is a TDRC graph measured on (010) β–Ga_2O_3 and 4H–SiC. The voltage in the cooling process was 2V steps from 2V to 22V. By applying the various forward biases, it was expected that the defect states would be filled depending on the applied forward bias voltage. The voltage for the heating process was -2V, so that the charges in the defect state could be released as the depletion region was created in the sample. However, meaningful information could not be obtained from the TDRC result. From the results of the β–Ga_2O_3 samples in figure 6. 12 (a), (b) and (c), although a change in current was observed with a cooling bias, in which significantly large currents were detected. Therefore, it is not considered to be a current from the defects states. Meanwhile, some slight peaks were observed in the silicon carbide sample (Figure 6. 12(d), (e) and (f)). However, the TDRC measured current is considerably low. These signals are assumed to be the noise level. In addition, there is no obvious variation in the pulse with different filling pulses. Thus, it is considered that detecting the defect states with the TDRC technique is difficult in these samples. Therefore, extracting information about interface defects using TDRC is challenging, and has not been pursued further. There are several possibilities for this problem. First of all, there may present a small amount of defects that are not able to be fully detected by spectra. However, the hysteresis curved from the CV measurements indicates otherwise. Another reason is that it was not able to probe the interface states, by insufficient filling during the cooling down.

6.2.2 DLTS Results

In addition to TDRC, DLTS was performed in order to extract information about defect states at the interface and in the bulk. To probe interface states with DLTS, a strong forward bias voltage was applied during the filling stage in the DLTS cycle, hereafter called interface spectrum. The DLTS spectrum gained was then compared with a conventional DLTS spectrum where a filling pulse below the reverse bias was applied, i.e. where only bulk defects were investigated, and hereafter called bulk spectrum. Thus, the reverse bias was set to V_R=-2V, and pulse bias set to V_P=1.5V and V_P=5V for bulk and interface spectrum, respectively. These two different pulse biases are used on the (010) β−Ga_2O_3 and 4H−SiC MOSCAP samples, and window number nine (with a length of 25.6 s) of each measurement is plotted in figure 6. 13 and figure 6. 15.

6.2.2.1 DLTS of bulk defect states

To the investigate the bulk of (010)β−Ga_2O_3, a pulse bias without reaching into forward bias during the filling sequence was used, by pulsing the depleted region down to -2V to 0.5V. Parameters such as measurement delay time and window length are shown in table 5. 1, and the results measured on each sample under this condition are plotted in figure 6. 13.

The (010) β−Ga_2O_3 MOSCAP samples shows distinct peaks at about 320K and 370K, which are conventionally labeled E2 and E3. In addition, the as−deposited and the 1000°C annealing samples (Figure 6. 13, black solid line and red dot line) contained broad and weak peaks after E2 peak temperature range, but the sample annealed at 600°C indicates a continuously increasing DLTS signal and the peak temperature for this trap signature was not reached. The E3 of the sample annealed at 600°C was overlapped by E2 (blue dash line in figure 6. 13), and higher and larger peaks appear at higher temperatures.

For comparison, samples based on 4H−SiC showed an increasing signal at high temperature above 550K, which appears only in the 1000°C annealing sample. In a paper about DLTS of 4H−SiC Schottky contacts, there are some references about defect states within Ec-0.10eV at temperatures within 50K (63, 64). It is believed that these are shallow nitrogen donors located at the cubic latitude site. However, the peak of spectra did not appear in the temperature range of 50K to 650K (shown in 8. Appendix).

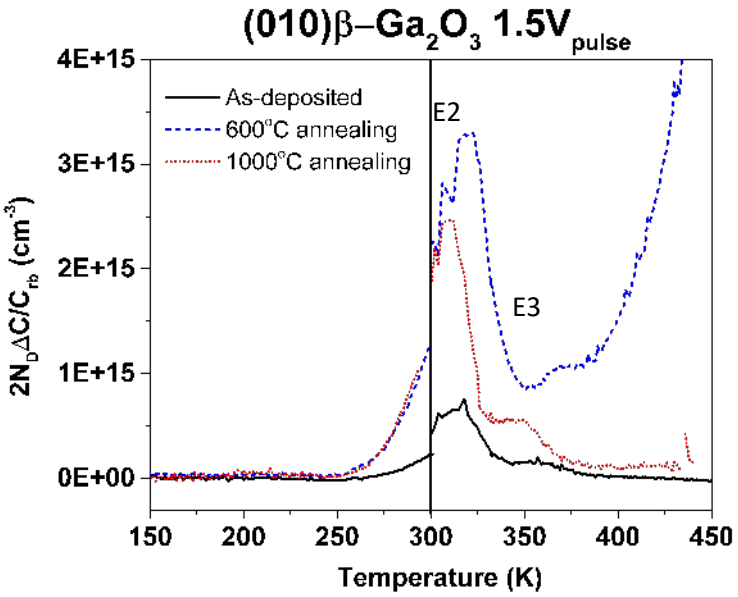


Figure 6. 13 DLTS signals from β–Ga_2O_3 samples. E2 and E3 peaks are clearly appeared, but the peaks in 600°C annealed sample seem to be overlapped.

Note that the DLTS measurements at low and high temperature were measured using different equipment, and this change in setup is indicated by a solid line at 300K in Figure 6. 13. The magnitude of the peak was calculated from the DLTS spectra, assuming a uniform defect profile, and expressed as the trap concentration related to the doping concentration calculated from CV.

$$N_t = 2N_D \frac{\Delta C_0}{C_p(\infty)} \tag{6. 6}$$

That is, the amplitude of the peak is directly proportional to the concentration of the traps (N_t). In the table 6. 3, the N_t of E2 peak of the (010) β–Ga_2O_3 sample shows the lowest value with 5.90×10^{14} cm^{-3} in the as–deposited sample, and the 600°C annealing sample has the highest trap concentration with $3.43\times10^{15}cm^{-3}$. This result is consistent with the trend of N_{eff} and *STD* results calculated from CV, which resulted in table 6. 2. The N_{eff} and *STD* values were also lowest for the as-deposited samples, while the 600°C annealed sample showed the highest values, even though the values extracted from the CV were overestimated. The tendency of trap concentration results at the E3 peak is also similar.

	Peak		E_t [eV]	σ_n [cm^2]	N_t [cm^{-3}]
β–Ga_2O_3	E2	As-deposited	0.80	1.45E-14	5.90E14
		600°C annealing	0.78	3.49E-15	3.43E15
		1000°C annealing	0.72	1.31E-15	2.35E15
	E3	As-deposited	0.95	4.34E-14	2.00E14
		600°C annealing	1.05	3.92E-13	1.04E15
		1000°C annealing	0.98	9.66E-14	5.24E14

Table 6. 3 Characterization of E2 and E3 peaks for bulk defect states. The enthalpy, capture–cross section and trap density are calculated from peaks of DLTS spectra.

To obtain the enthalpy and capture–cross sections of the traps, the Arrhenius plots corresponding to these peaks were plotted as figure 6. 14. As shown in table 6. 3, the defects corresponding to the E2 peak appear to be present at ~0.80 eV below E_C, and defects representing the E3 peak appear to be ~1.05 below E_C. The capture cross section shows the E2 peak in the range of 10^{-14} to 10^{-15} cm^2 and the E3 peak in the range of 10^{-13} to 10^{-14} cm^{-2}.

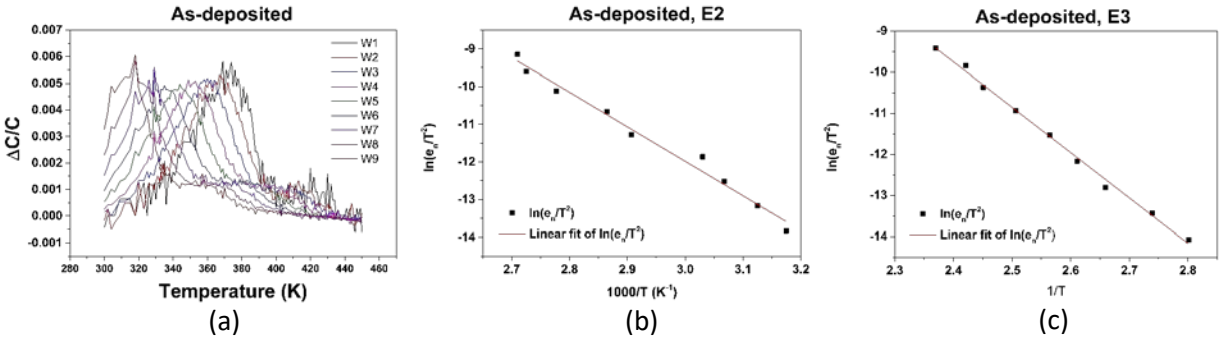


Figure 6. 14 (a) is the DLTS spectra of nine windows for the without forward bias of the as-deposited sample of beta-gallium oxide. An Arrhenius plot was made for each peak (b, c). The same operation was performed on all peaks.

The N_t of E2 on the (010)β–Ga_2O_3 MOS samples accounts for 0.95%, 2.45% and 1.67% percent of N_D for as-deposited, 600°C annealed and 1000°C annealed samples respectively. As the annealing temperature increased, the portion contributing to the trap became larger. The defect levels observed in figure 6. 13 have previously been reported in the literature, where both intrinsic and extrinsic origin of peaks in DLTS have been proposed (1, 65, 66). For E2, which is the dominating DLTS signature in our samples, it has been suggested that it may be the dominant compensation source for trapped electrons in bulk crystals (65). Recently, it was shown that the E2 level arise from substitutional Fe on Ga site, where Fe is a common impurity in particular bulk samples (1). In addition, traps located at E3 (Ec-1.04) and Ec-0.55(not shown in this thesis) were found to be mainly involved in Fe and Co (1). The average ionization energies of E2 and E3 in table 6. 3 are 0.76

eV and 0.99 eV. These values have showed similar ionization energies in Ingebrigtsen et al., (55) 0.76eV and 1.01 eV for E2 and E3 respectively.

6.2.2.2 DLTS of interface defect states

To potentially probe the interface states, the MOS structure was subjected to a forward bias (accumulation) during the filling sequence of the DLTS measurement, in contrast to that of the previous section where reverse bias always was maintained. As the depletion region collapse by applying forward bias and the majority carrier will be injected and accumulated near the junction, the interface region may be investigated.

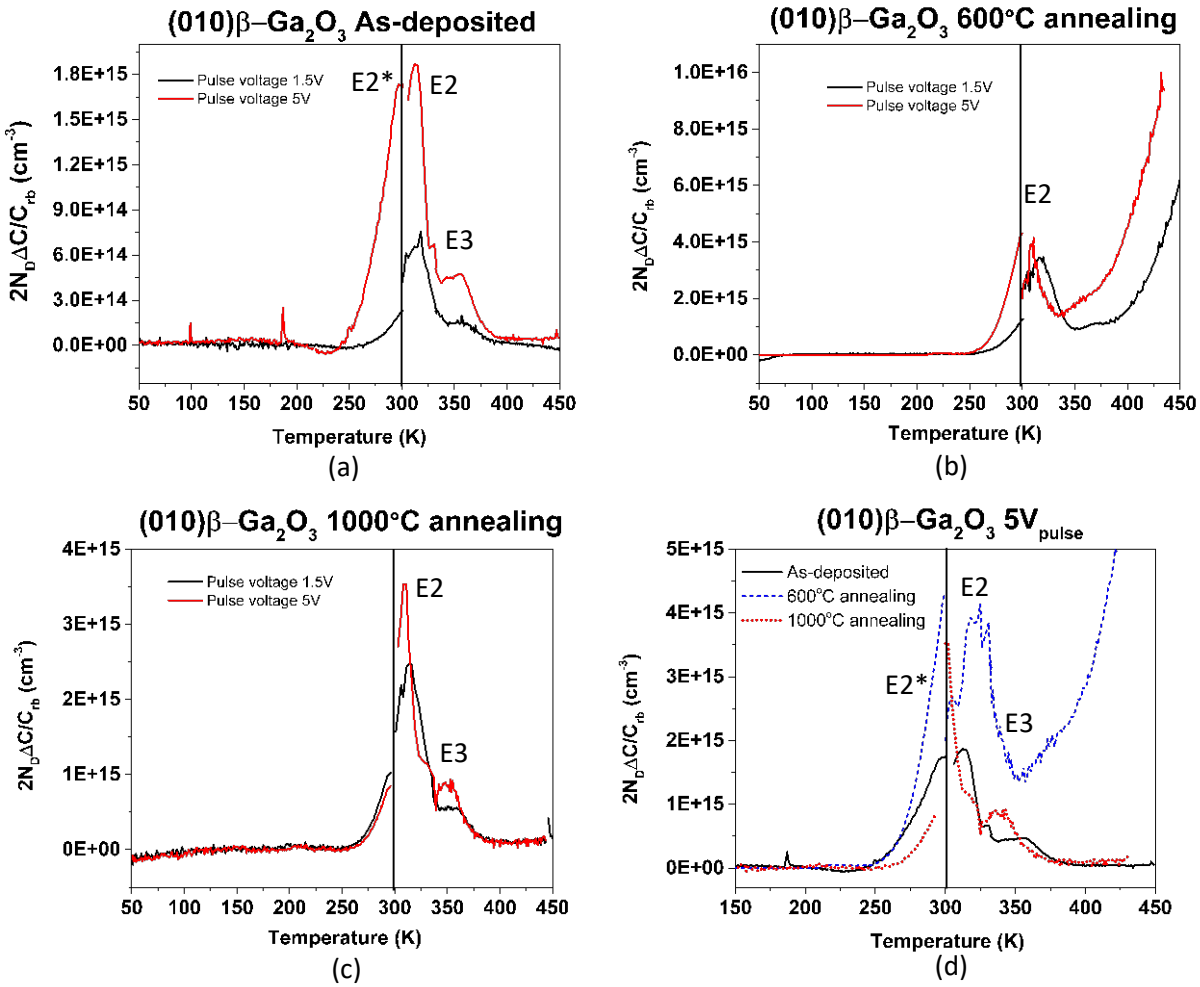
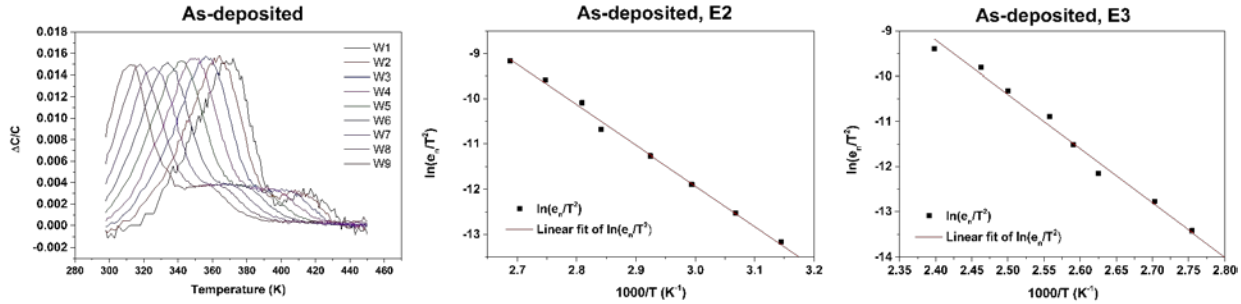


Figure 6. 15 DLTS spectrum of 9th window. The black lines are measured without forward bias, for bulk study. The red lines are measured with forward bias for interface study. (a) is for As–deposited sample, (b) is measurement of 600°C annealed and (c) 1000°C annealed (010) β–Ga_2O_3. (d) displays the signals for only $5V_{pulse}$ bias for the samples.

Figure 6. 15(d) shows DLTS spectra of the as–deposited, 600°C and 1000°C samples by a including forward bias (V_{pulse}=5V). As can be seen in the figure, DLTS spectra with forward biases also showed E2 and E3 peaks in the (010) β–Ga_2O_3 MOSCAPs. However, in both samples except the 600°C annealed sample, a weak shoulder phenomenon was observed in the E2 peak near 325 to 330K. The E2 peak traps were located at Ec-0.77 ~ 0.84 eV, and the E3 peak was within Ec-1.04~1.10 eV. (Table 6. 4) Therefore, there is another spectrum near Ec-1.00eV.

In addition, from the figure 6. 15(d), it is assumed that there is another peak near E2 at approximate 300K. This did not occur in the pulse biases that do not include forward bias. The peak occurring in this vicinity was named E2*, which was located at Ec-0.75 eV in previous studies and was estimated as an intrinsic defect state by iron impurities or mobile primary defect state, such as oxygen vacancy (1). E2 and E2* seem to be agglomerated, and probably exists around or near the interface. It indicates that the 5V of pulse voltage covers the interface region, and the intrinsic defect state of β–Ga_2O_3 at the interface is detected with this pulse bias.

Unfortunately, no peaks appeared on any of the windows in 4H–SiC MOS samples. The CV of the SiC sample has a kink phenomenon in the As–deposited and 600°C annealed samples, and the flatband voltage appears at about 5 V or more, so it is necessary to try using various V_R and V_P.



(a) (b) (c)

Figure 6. 16 DLTS spectra and Arrhenius plots for E2 and E3 in As-deposited sample. This work was done on all peaks found.

	Peak		E_t [eV]	σ_n [cm^2]	N_t [cm^{-3}]
β–Ga_2O_3	E2	As-deposited	0.77	7.18E-15	1.92E15
		600°C annealing	0.77	2.32E-15	8.44E15
		1000°C annealing	0.84	6.48E-14	3.39E15
	E3	As-deposited	1.04	7.14E-13	4.51E14
		600°C annealing	-	-	-
		1000°C annealing	1.10	3.54E-12	8.34E14

Table 6. 4 As in table 6. 3, the peaks were also characterized for the DLTS including forward biases. However, as shown in figure 6. 15 (b), it was difficult to detect the peak due to the larger peak close to E3 peak.

The N_t values of the (010) β–Ga_2O_3 samples calculated from the peaks account for 3.07%, 6.03% and 2.40% of the N_D. This means that N_t occupies a larger portion of the N_D than DLTS measurements without forward bias. Taken together, measurements including forward bias are considered to have similar defect states in the bulk and interface.

6.2.2.3 Proton irradiation for (-201) β–Ga_2O_3 samples

In addition to the interface between the semiconductor and the oxide layer, it is important to study the characteristics of the bulk. This is because the native and impurity related defects directly affect electrical and other properties. For example, studies on the electrical behavior of the intrinsic defects and impurities of β–Ga_2O_3, can set the stage for further research to optimize the performance of future devices. In order to investigate the defects observed in β–Ga_2O_3 further, an irradiation study was conducted.

Blanco, M.A., et al.'s study (67) shows that point defects such as oxide vacancies (V_O)or gallium interstitials (Ga_i) in gallium oxide can be mobile. This may imply that vacancy and interstitial defects can considerably affect the electrical properties of beta-gallium oxide. In a recent paper using proton irradiation, intrinsic E2* peaks near the E2 peak were studied (1, 68-70). This peak is found at about 317K, with an ionization energy of 0.75 eV which is particularly close to E2.

For the present study Schottky contacts on (-201) β–Ga_2O_3 bulk samples were utilized, and a 600keV proton beam with doses from 3×10^{13} to 1×10^{14} cm^{-2} . Furthermore, previous studies have shown that proton irradiation easily compensate the material, and annealing at 200-300^{o}C is required to study irradiation induced defects by DLTS (68, 69).

The sample production process is schematized in figure 6. 17. 150 nm of nickel was deposited with a PVD for Schottky contact. During deposition a circular contact is formed through the mask, which has the same size as the capacitor studied in this paper. The back side of the sample was deposited for Ohmic back contact with a Ti/Al of 10 nm and 150 nm, respectively. The implantation of H^+ ion was followed at room temperature with 600 keV H^+ ions, in which $3\times10^{13}cm^{-3}$, 6×10^{13} $cm^{-3}$and 1×10^{14} cm^{-3} of three different doses were used. The estimated projected range was ~4.3 μm, by Monte Carlo simulations with SRIM code (71). Vacancies were expected to be generated by the injection of H^+ ions and then the sample was annealed with a DLTS bias up to 620K to recover the charge carrier of the irradiated samples. The information about intrinsic defect states are expected by obtaining intrinsic vacancies peaks during the recovery process.

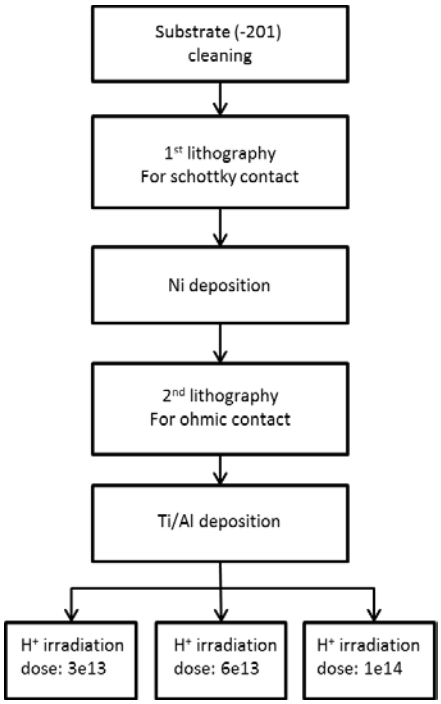


Figure 6. 17 Fabrication process of irradiation samples. Schottky contact formed with nickel deposition and three different H+ irradiation doses were used.

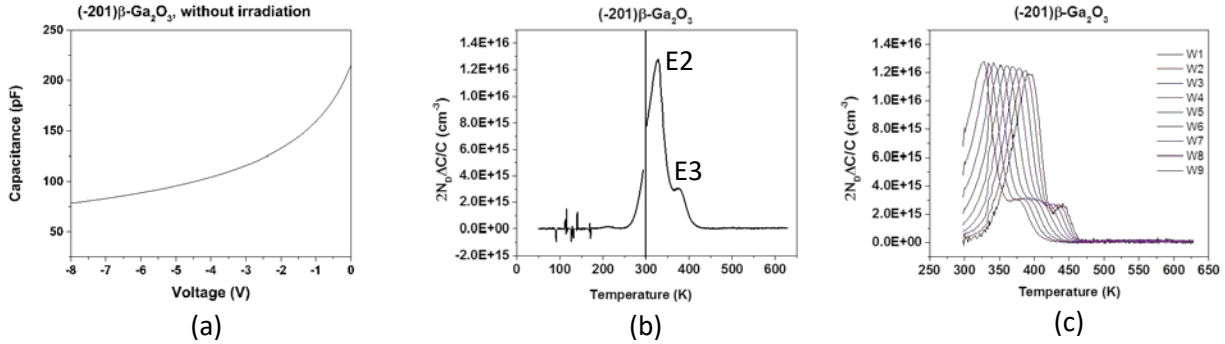


Figure 6. 18 *CV* of without irradiation and DLTS of window number nine (with a length of 25.6 s) in without irradiation sample from 50K to 630K (b) and spectra for E2 and E3 peaks (c).

Prior to irradiation, the carrier concentration was found to be 1.97×10^{17} cm^{-3}, it was obtained from figure 6. 18 (a). DLTS in figure 6. 18 (b)-(c) indicate the characteristic levels E2 and E3, where E2 exhibit a capture–cross section of 5.89×10^{16} cm^{2}, while the ionization energy is 0.74 eV.

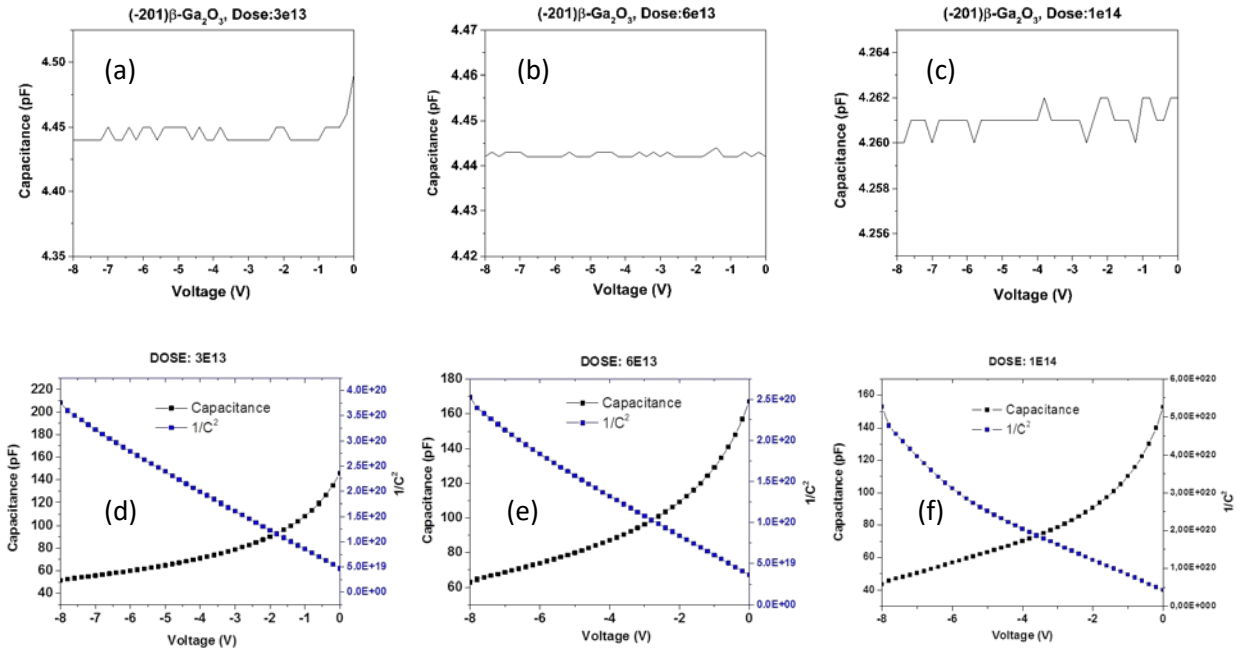


Figure 6. 19 CV after irradiation of smaples without irradiation (a), 3×10^{13} cm^{-2} (b), 6×10^{13} cm^{-2} dose (c) and 1×10^{14} cm^{-2} dose. And *CV*, $1/C_2$ after annealing to 600K (d), (e) and (f).

Figure 6. 19 is CV result for the samples after H^+ irradiations. Substantial reductions in the capacitance are observed after irradiation, where the samples display a capacitance of around 4pF. Thus, the samples are heavily compensated. Interestingly 4pF is corresponding to ~4μm of depletion region, which matches the implantation peak. It indicates that the origin of the carrier freeze-out is defects generated around the projected range of the implantation. The samples were then annealed as the samples were scanned in DLTS from room temperature up to 600K during, and the donor concentrations were obtained by measuring CV again to see the recovered carriers. After the recovery process, donor concentrations are calculated to be 9.11×10^{16} cm^{-3} for the 3×10^{13} cm^{-2} dose sample, 1.47×10^{17} cm^{-3} for 6×10^{13} cm^{-2} and 6.77×10^{16} cm^{-3} for 1×10^{14} cm^{-2} respectively. Thus, a partial recovery has been achieved in the samples.

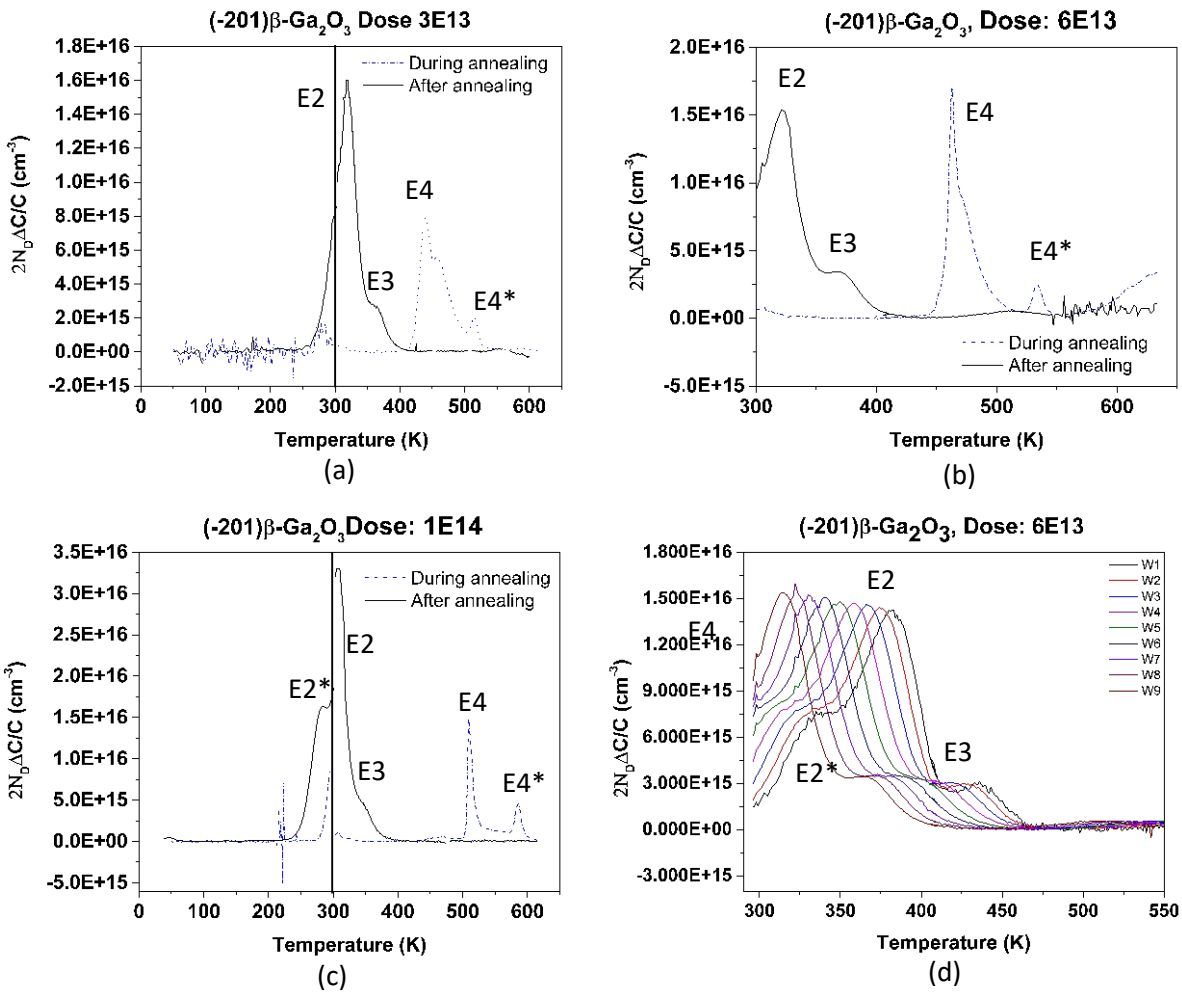


Figure 6. 20 The DLTS was performed to find out the difference in bulk between before and after the compensation. After the irradiation, DLTS was measured by annealing from 300K to 620K (Blue dotted line). V_{bias} applied to DLTS measurement was -8V and V_{pulse} was 7V. The DLTS was then measured while cooling the temperature from 620K to 300K (black solid line). (a) is the spectra of 3×10^{13} cm^{-2}dose, (b) is of 6×10^{13} cm^{-2} dose and (c) is 1×10^{14} $cm^{-2}$of dose. (d) is the nine spectra for the 6×10^{13} cm^{-2} dose sample.

DLTS before and after the recovery process during annealing is demonstrated with the figure 6. 20. At low temperatures of the sample irradiated to a dose of 6×10^{13} cm^{-2}, the DLTS signal is highly unstable, which is assumed to be a direct result of damage by the 600K annealing (not shown). However, a new defect level appear, labelled E2*, and found in the measurement of the 6×10^{13} cm^{-2} and 1×10^{14} cm^{-2} dose samples. According to a recent paper, the E2* peak has a particularly close ionization energy to E2 and its capture-cross section is larger an order of magnitude (1). The results of the values obtained from the peaks of each sample are given in table 6. 5. The E2* obtained at 1×10^{14} cm^{-2} dose is depicted also as close to E2, with an order of magnitude larger capture cross section. However, due to the damage that occurred during the low temperature of the DLTS measurement of the 6×10^{13} cm^{-2} dose, the peak for E2* was extracted only up to lock-in window four.

	Peak	Dose [cm^{-2}]	E_t [eV]	σ_n [cm^2]	N_t [cm^{-3}]
(-201)	E2*	6E13	-	-	-
β–Ga_2O_3		1E14	0.78	2.63E-13	1.83E16
	E2	Without irradiation	0.74	5.89E-16	1.24E16
		3E13	0.77	4.81E-15	2.53E15
		6E13	0.72	7.95E-16	1.49E16
		1E14	0.78	5.88E-15	3.11E16
	E3	Without irradiation	1.00	4.34E-14	2.90E15
		3E13	0.88	4.35E-15	2.53E15
		6E13	0.84	7.19E-16	3.28E15
		1E14	0.93	2.16E-14	4.20E15

Table 6. 5 Information corresponding to each peak of DLTS in irradiated sample after annealing.

In figure 6. 20, the most noticeable difference before and after annealing is the difference in peak positions and trap concentrations. The DLTS E2 trap concentrations measured during cooling (black solid lines in figure 6. 20) are similar to the trap concentration without the irradiation sample. On the other hand, the level marked E2* was observed in the low temperature DLTS. It is weakly present during annealing and shows a large increase during the cooling process. At the same time, new peaks at temperatures above 400K appear during annealing, and labelled E4 and E4*. However, the peaks almost disappeared while cooling down and the E4* peak was found at higher temperatures as the dose increased. However, it was difficult to obtain the peak of the DLTS spectra measured by annealing due to the annealing (recovery process) and various superposition signals.

Recently, E2 has been found to be related to iron in gallium site (Fe_{Ga})(1). There is no change in the E2 peak regardless on the H^+ dose. However, for the E2* peaks found at temperatures lower than E2, the change is evident with irradiation dose. This means that when beta-gallium oxide is irradiated and thermally stimulated, it forms a defect state corresponding to E2*, which indicate that an intrinsic defect is involved, but rather in a complex than being one of the primary intrinsic point defects(69). The generation of this intrinsic defect state and its recovery show that the carrier concentration can be recovered by the thermally activated process.

Another prediction is the mobility of primary defects. In other recent studies about migration barrier of vacancies in Ga_2O_3(67, 70), oxygen vacancy (V_O) is calculated as 0.5~1.7eV. This V_O tends to act as a deep donor (70, 72). Therefore, it is assumed that the peak corresponds to V_O or related complex. Its low migration energy is may allow these defects to mobile at relatively low temperatures such as 300K (67, 70).

6.3 Towards a β–Ga_2O_3 based field effect transistor

According to a study by M. Higashiwaki in 2012 and 2013 (16, 29), excellent device output was obtained in a metal-oxide-semiconductor and metal-semiconductor field effect transistor (MOSFET and MESFET) using a β–Ga_2O_3 substrate. This has spurred a tremendous research interest in Ga_2O_3 for power electronics and MOSFET/MESFET devices. In the case of the depletion mode MOSFET using Al_2O_3 20nm as an oxide layer, the drain current (I_d) of 39mA/mm was obtained when the gate voltage (V_g) of 4V was applied, and the I_d on/off ratio was over ten orders of magnitude. And the result of the three-terminal off-state (V_{br}) was 370V, which shows a good characteristic for a transistor. The MOSCAP study used a 20nm Al_2O_3 layer, and acted therefore as a starting point for the present work. In this work, MOSFET fabrication was built upon the (-201) β–Ga_2O_3 substrate due to sample availability. The device structure and fabrication was inspired by a Si based N-MOSFET design developed by Viktor Bobal and used in a lab course (FYS2210) at UiO (73). However, several modifications were developed to adapt the design for small Ga_2O_3samples. Figure 6. 21 provides a diagram of the sample preparation.

6.3.1 Attempt to (-201) β–Ga_2O_3 MOSFET

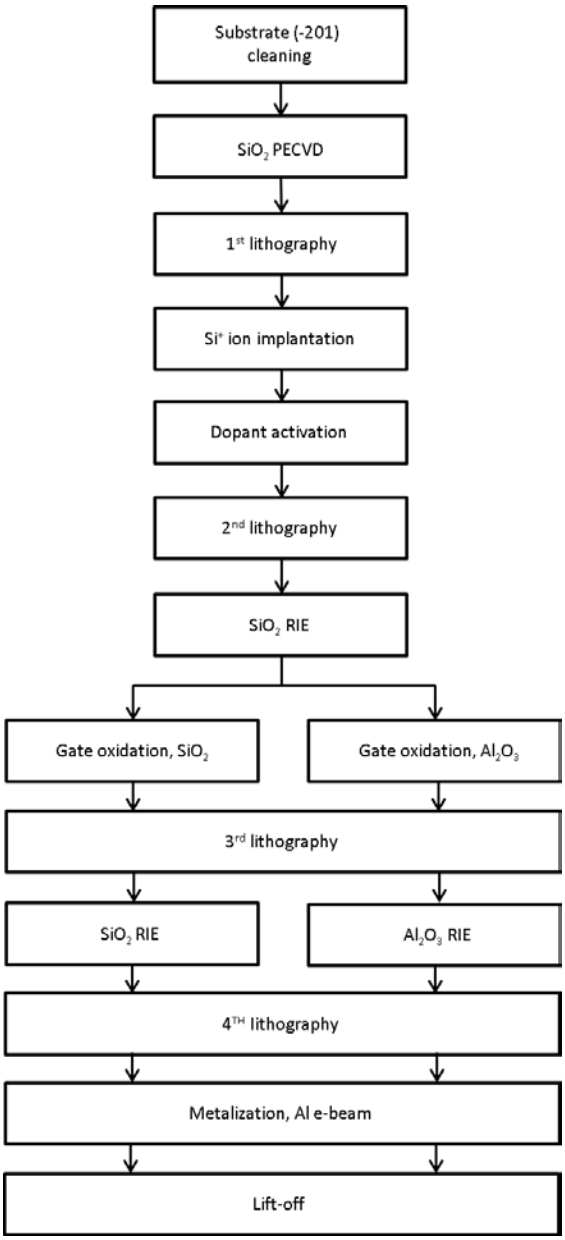


Figure 6. 21 MOSFET Process on (-201) β–Ga_2O_3 substrate.

First, after cleaning of the substrate, SiO_2 was grown by PECVD as a field oxide at 300°C with SiH_4 and N_2O gases. The final thickness of SiO_2 measured with ellipsometer was 186 nm. The first lithography step was then performed to open the source and drain regions. For the fabrication of this transistor device, a maskless lithography and a positive PR S1813 were used. The information about PR is described in section 3.3. Light was exposed at 15ms for all lithography steps. After lithography, to obtain low-resistance Ohmic contacts on the source and drain regions, Si^+ ion implantation was performed (29). The Si^+ ion implantation was injected at 35keV, and the dose was

1.50×10^{-14}cm^{-2}. After implanting the dopant, the samples were annealed in an N_2 gas atmosphere at 925°C for 30 minutes for dopant activation. This condition for dopant activation followed the 2013 work of Higashiwaki (29). Next, field oxide (SiO_2) on the gate region was removed using the second lithography step and RIE. The detailed process of SiO_2 etching, as described in section 3.4, was carried out in 1E-6 Torr. Subsequently, two types of gate oxide layer were formed on different substrates. Al_2O_3 20 nm was formed using ALD, but the SiO_2 oxide layer was formed by PECVD. Next, RIE was utilized again to remove the gate oxide of the source and drain regions, and SF_6, Ar, and O_2 gases were used for alumina etching. After the fourth lithography step for the deposition of the contact metal, 100nm aluminium was deposited by e-beam evaporation. Finally, a lift-off operation was conducted whereby the sample was immersed in an acetone solution to leave only the metal contact of the desired area. A cross-section of the completed sample is illustrated in figure 6. 22. After completing the MOSFET fabrication, the gate length was measured to be 27.41μm.

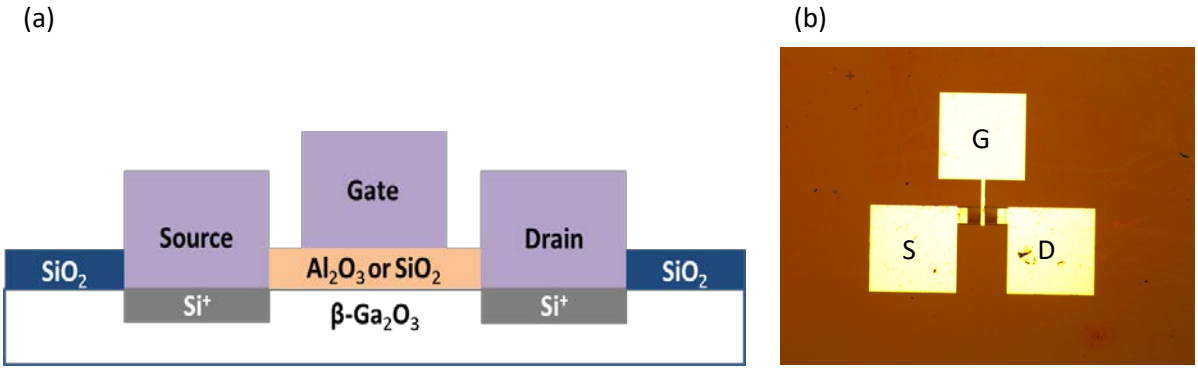


Figure 6. 22 (a) A MOSFET structure based on the process shown in Figure 4.3. Here SiO_2 was deposited as the field oxide, and Al_2O_3 and SiO_2 were used for the gate oxide on the different substrates. Si ions were implanted for the Ohmic contact of electrodes. (b) completed MOSFET. The gate is labelled 'G', 'S' for source and 'D' for drain.

However, the measured results did not show the I_d–V_d characteristic according to the gate voltage V_G. Through the result of MOSFET IV and the examination of the manufacturing process, several challenges and problems related to the fabrication was identified. First, the etching process was not done properly. Because I_d is measured similarly at source, gate and drain, without field effect (Figure 6. 23). This means that the silicon dioxide or alumina still remained on the substrate as an insulator, i.e. between the Si^+ implanted region and metal contact.

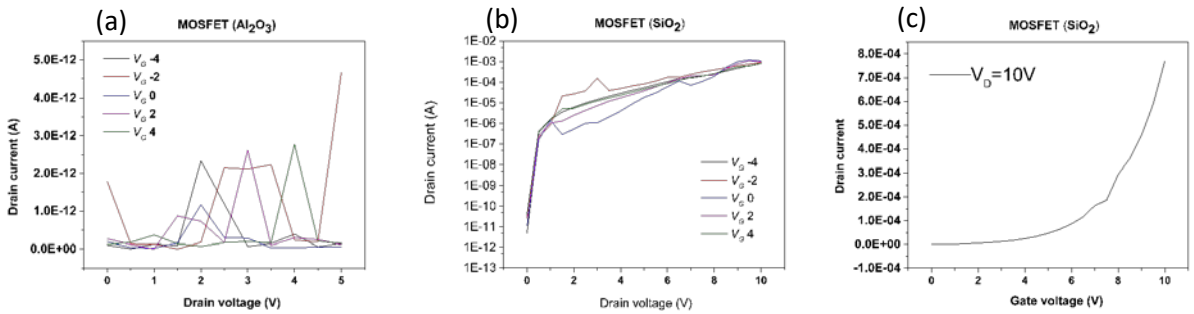
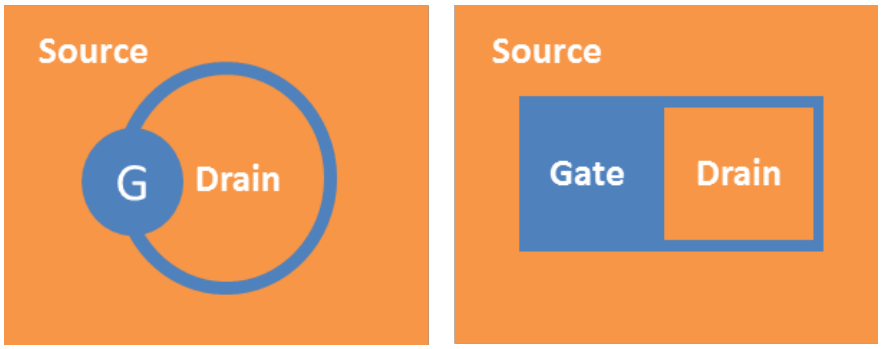


Figure 6. 23 The I_d–V_d results from 20nm of Alumina oxide layer MOSFET (a), 20nm of SiO_2 MOSFET(b) with (-201) β–Ga_2O_3. Al_2O_3 MOSFET shows low current, and SiO_2 MOS has saturated current over 1V, but the current does not modulated by applied gate voltage. (c) is the I_D–V_G on the same SiO_2 MOSFET with applying 10V on the drain. However, all the samples have no field effect.

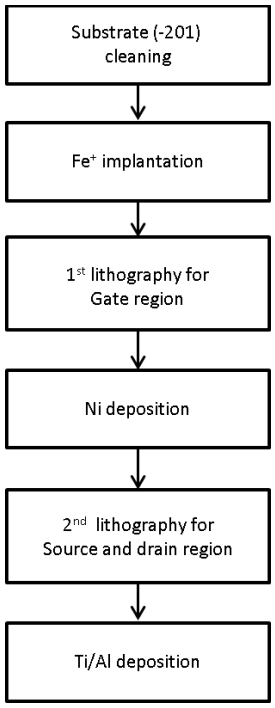
The reason for this problem is that the calculation of the etching rate does not match the actual etching rate. Secondly, there was inaccuracy in the lithography instrument. After the metal was deposited on the beta-gallium oxide substrate, the desired pattern was also lifted-off during lift-off process. It is therefore necessary to thoroughly check whether various chemicals such as photoresist, and lamps or other parameters of the lithography equipment are operating precisely. Thirdly, a depletion mode MOSFET relies on a sufficient depletion region between source and drain to affect the on-state. However, using a bulk sample with N_D~10^{17} cm^{-3} the depletion region does not extend sufficiently to change the source-drain current. Thus, a more appropriate approach is to utilize semiconductor on insulator (SOI) structures, however, this was not available during the thesis work.

6.3.2 Attempt to fabricate (-201) β–Ga_2O_3 MESFET

Since etching was a challenge for the MOSFET design, a MESFET sample was attempted with the closed loop design. In this MESFET manufacturing process, the oxide deposition step and etching step are not included.



(a)



(b)

Figure 6. 24 MESFET lithography design (a) and fabrication process (b). This process does not include oxide layer deposition and oxide etching steps.

First, the (-201) β–Ga_2O_3 substrate was cleaned and then Fe^+ was implanted through ion implantation, in order to form a buried insulating layer, while the top ~300nm remained conductive. Unlike MOSFET, MESFETs are controlled on/off by Schottky metal contacts. The depletion region underneath the metal contact is controlled by the applied voltage, which controls higher carrier mobility than MOSFET. However, turn–on bias tends to be limited by Schottky metal contacts. The MESFET requires the substrate isolation to adjust the injected carriers. Otherwise, carriers will spill–out from the channel toward the substrate. Thus, a process of growing or implanting a buffer layer is widely performed. In this paper, an isolated substrate layer was formed by implanting Fe^+ ions.

After the ion implantation on the (-201) β–Ga_2O_3 substrate, the lithography proceeds for the gate contact. The conditions used for lithography and metal deposition are the same as those for MOS capacitors. The gate electrode was made of Ni of 120nm, and a second lithography and Ti 10nm–Al 100nm deposition were used to produce the final sample.

However, due to the problem of lithography equipment, it failed to obtain the pattern at the lift-off step after metal contact deposition. Since any of patterns could be obtained through lithography, fabrication of complete MESFET was not available, and the full fabrication and device characterization remain as future work.

7. Summary and outlook

First of all, MOS capacitor based on β–Ga_2O_3 and 4H–SiC substrates with Al_2O_3 have been fabricated and investigated. Prior to comparison with the 4H–SiC sample, (010) and (-201) surface orientation samples of β–Ga_2O_3 was evaluated. IV showed rectification in both samples, but (010) samples showed less reverse current and high rectification. Any significant N_d difference was not observed between the two samples, but the (010) sample showed a smaller hysteresis curve and flatband voltage, and no kink phenomenon in the depletion region. Therefore, the sample prepared on the substrate with the (010) surface orientation shows better device characteristics.

Two different thickness of Al_2O_3 was then performed in order to evaluate the outputs by the 20nm and 100nm with IV and CV. The higher rectification and stable conductance at oxide capacitance were obtained at 20 nm Al_2O_3 sample. This means that there is less leakage current in 20nm samples, with better oxide quality than that of the sample of 100nm Al_2O_3 sample. The MOSCAPs with 20nm alumina and 4H–SiC substrates were then compared with three annealing conditions (As-deposited, and annealing at 600°C, 1000°C for 1 h). Interestingly, the characteristics evaluation of 4H–SiC and β–Ga_2O_3 samples tended to have opposite results. The hysteresis of β–Ga_2O_3 was increased with annealing temperature, which also increased the *STD* and the Q_{eff}. On the other hand, 4H–SiC showed a tendency to decrease with annealing temperature. This is presumably due to the crystallization of alumina.

TDRC and DLTS were performed to investigate defect states in the interface and bulk. In the case of TDRC, it was difficult to obtain meaningful measurement results. This was probably due to not being able to probe the defects, which was because of the low current, or because the measurement parameters were not suitable to detect the interface defects. However, bulk and interface characteristics were detected in DLTS. E2 and E3 peaks were seen in all samples. The concentration of the traps was higher for the annealed samples than for the as-deposited samples. Also, since the trap concentration of the interface is larger than the trap concentration of the bulk measurement, it is assumed that the biases are covering the bulk. In addition, the E2* peak was detected with the bias for interface at approximately 300K. This may mean that the $5V_{pulse}$ bias included interface defect states, and there was an intrinsic defect state at the interface region.

Since the properties of the device are also affected by the bulk properties, H^+ irradiation has been carried out to find out its intrinsic character. This experiment was done from DLTS measurements of samples with the conditions of 3 doses (3×10^{13} cm^{-2}, 6×10^{13} cm^{-2} and 1×10^{14} cm^{-2}). In the recovery process, the charge carrier compensation was observed in every sample. E2 * peak, known to be formed from an intrinsic V_{Ga}-like origin, was also obtained. This E2 * peak showed a tendency to increase with the H^+ irradiation dose.

Next, fabrication of MOSFET and MESFET was attempted, but unfortunately failed due to the mechanical problems of the lithography equipment and the software problems of the RIE equipment.

Further work on X-ray diffraction (XRD) should be conducted as it can identify amorphous thin films and crystallized thin films from the annealing. It would also be interesting to see a process of crystallization. In addition, a comparison of the diverse DLTS bias is suggested to investigate the kink of the depletion region and the interface. Furthermore, mass spectrometry would be helpful in studying the origin of defect states if DLTS is supported by this.

Further study on DLTS for the E2 * peak, shown with the forward bias, should be conducted as well. It would be offer a clue for understanding interface state, and it can serve to give further ideas for MOS structure fabrication and characterization.

β–Ga_2O_3 has an excellent potential for MOSFET devices, but there are some disadvantages to overcome. For example, bulk characteristics with only n-type, and insufficient N_D to generate the depletion region for the depletion mode of MOSFET. Therefore, various SOI structures or buffer materials need to be tried.

8. Appendix

Unfortunately, in the experiment with 4H–SiC MOSCAP samples, it was not possible to obtain a spectrum with a peak. A large increase in the spectrum was detected at temperatures over 520K in the 1000°C annealing sample. But due to the limitations of the equipment, measurements over 650K were impossible and no peak was obtained. The peak labeled EH7 is known to be caused by carbon vacancy (74). The spectra increased very weakly in the 600°C annealed 4H–SiC sample, and more clearly in the 1000°C annealed sample as the annealing temperature increased. This means that the carbon vacancies increase at ~1.5 eV below the conduction band with annealing temperature increasing.

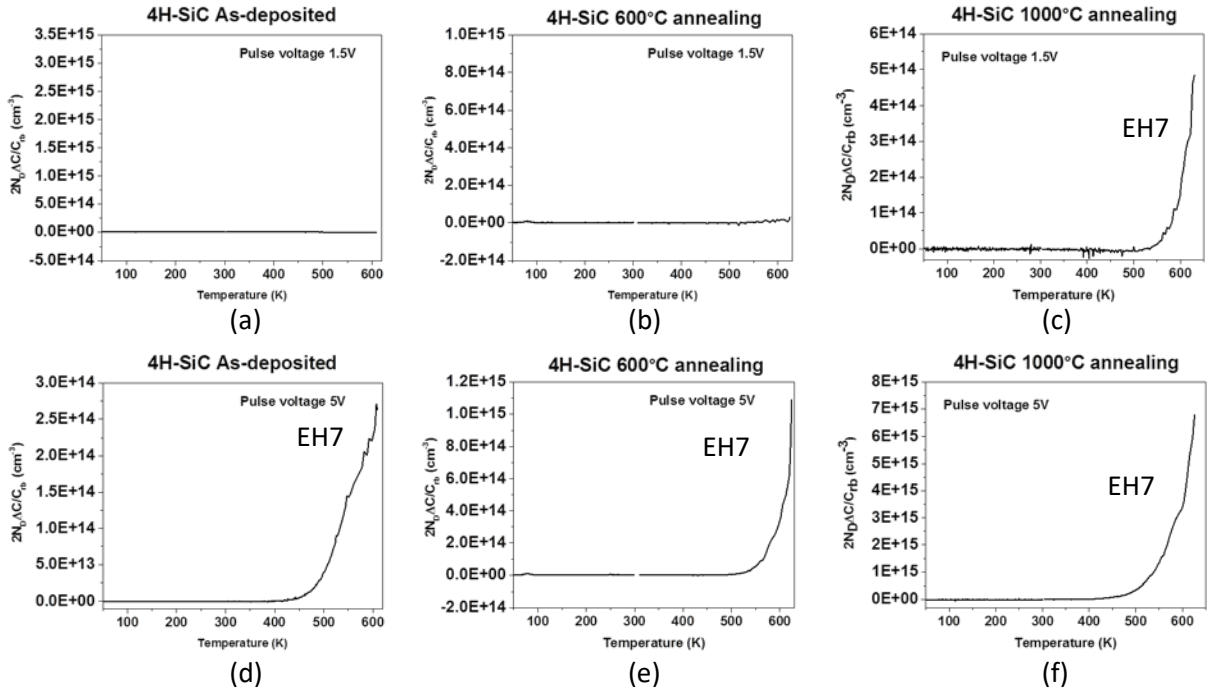


Figure 8. 1 DLTS spectrum of 9th window. (a), (b) and (c) is measured bulk, and (d), (e) and (f) is for interface.

4H–SiC MOS samples showed large increased spectra at over 500K with 5 V_{pulse} (Figure 8. 1(d-f). As–deposited samples, however, indicates that the defect states showed increase at lower temperatures, 450K (Figure 8. 1 (d)). This of the sample originated in a relatively shallow place. In the as–deposited sample and the 600°C annealed sample (Figure 8. 1(a), (b)), the results of DLTS with the bias for interface differ from the bias for bulk (Figure 8. 1(d), (e)). An increase in spectra between 500K and 600K is appeared with the interface spectrum. It indicates that there is a defect state in response to a pulse voltage of 5V. However, 3V is the area where the first kink occurs in the silicon carbide sample, so this may be the result of the defect states that makes up the kink. The 1000°C annealed sample has a larger spectrum than the reverse bias of 1.5V. The CV results show that the 1000°C annealed sample is accumulating at 3V, and therefore it may be agglomerated trap states of bulk and interface.

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