Exploration of ZnO and ZnMgO/ZnO Thin Film Transistors

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Thesis submitted in partial fulfillment of the requirements
for the degree Master of Science

UNIVERSITETETY OF OSLO

1.6.2015

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Abstract

Transparent semiconductor technology can improve the performance of thin film transistors (TFTs) in flat panel displays, making the product more energy efficient and cost effective. To achieve this, it is necessary to replace the commonly used material amorphous silicon (a-Si) with materials that have more suitable properties. With its large direct bandgap (3.3 eV at room temperature) and high exciton binding energy (60 meV), zinc oxide (ZnO) emerges as an attractive candidate for this kind of application. The present thesis explores TFTs made of ZnO and zinc magnesium oxide (ZnMgO) deposited with metal-organic chemical vapor deposition. X-ray diffraction (XRD) was used to investigate the crystallinity of the ZnMgO/ZnO samples. Further, two types of transistors have been considered. The first type makes use of ZnO as the channel material on a silicon substrate with silicon oxide (SiO_2) or silicon nitride (Si_3N_4) as gate dielectric, i.e. adapting so called bottom gate device architecture. The second type is a ZnMgO/ZnO hetero-structure TFT made on r- and c-sapphire as substrates with a top gate design. The hetero-structure fabricated on c-sapphire exhibited characteristics indicating the formation of a two-dimensional electron gas at the ZnMgO/ZnO interface due to its polar growth direction. On the other hand, the hetero-structure grown on r-plane has non-polar growth direction; no 2DEG at the interface. Plasma-enhanced chemical vapor deposition (PECVD) was used for deposition of the dielectrics to avoid the high concentration of fixed charges that was likely to result from thermal oxidation of boron doped p-type silicon wafers ($N_a \approx 10^{15}$ cm^{-3}). Insulator thickness and refractive index was measured by ellipsometry to check on the film quality and this varied with deposition parameters. C-V characterization was used to study the properties of the insulating layers by fabricating metal-insulator-semiconductor structures and optimal temperature, RF power and reactor pressure was found for deposition of SiO_2. In contrast, the results obtained from C-V measurements for optimal growth conditions of Si_3N_4 were less definite. IV measurements performed on the TFTs generally show a higher performance for transistors with SiO_2 as gate dielectric than with Si_3N_4. Threshold voltage, field effect mobility and on/off current ratio for the bottom gate TFTs were calculated from I-V characteristics and the TFTs show superior device characteristics. For the ZnMgO/ZnO TFTs the mobility ranged from 0.3 to 170 cm^2/Vs, with transistors on c-sapphire having higher mobility than those on r-sapphire, a fact attributed to the formation of a 2DEG. Threshold voltages were 2-4 V and on/off current ratios were in the range 10^3-10^4 for ZnMgO/ZnO TFTs.

Acknowledgements

I would like to thank my supervisor Andrej Kuznetsov for his insight and vision for my thesis. Vishnukanthan Venkatachalapathy helped me a great deal with setting up the working plan and with training on X-ray diffraction. He also did all depositions of ZnO and ZnMgO with MOCVD. I am indebted to him for his contribution. I would also like to thank both Viktor Bobal and Mikael Sjödin for training on several instruments and their frequent help in the MiNalab, without which the work in the laboratory would have been much more difficult. In addition I am grateful to Per Lindberg for his help with I-V measurements among other things and his willingness to always lend a helping hand or explain something to me if I did not understand it. Vincent Quemener gave me training for laser cutting and thermal evaporation. I thank him for that and for his helpful and friendly attitude. Others that have helped me during the work with my thesis are Naoya Iwamoto, Pekka Neuvonen and Ilia Kolevatov. I am thankful for all their help.

Finally I would like to thank Bengt Gunnar Svensson who through his course on semiconductor components introduced me to the field of semiconductor physics and with his enthusiasm inspired me to dive into this field and learn more about it.

1. Introduction

Transparent electronics is an area with a wide range of applications and is one of the most promising technologies for leading the next generation of flat panel displays due to its high electronic performance. Wide bandgap semiconductors can here play an important role, both as passive and active components, similar to the role of silicon in traditional transistor technology [1]. So far the dominant material for use in flat panel displays has been hydrogenated amorphous silicon. But thin film transistors of a-Si has low mobility as well as threshold voltage stability issues, and this has led to interest in alternative materials such as organic and metal oxide semiconductors [2]. One of the most promising of these materials is the group II oxide semiconductor zinc oxide (ZnO).

ZnO has properties that make it a suitable material for this kind of application. Importantly, its high electron mobility results in higher drive currents and faster operation of the device. In addition, the wide bandgap of ZnO renders it transparent to visible light, and consequently ZnO thin film transistors (TFTs) do not degrade after exposure to light the way transistors of amorphous silicon are prone to. Specifically, ZnO can be used as the active channel layer in TFTs which are part of the pixels in active matrix liquid crystal displays (AMLCD) and organic light-emitting device (OLED) displays. Deposition and growth of ZnO is usually done at relatively higher temperatures compared to a-Si, but it is also possible to deposit at lower temperatures, all the way down to room temperature. However, TFTs made by low temperature deposition of ZnO have been reported to have high operating voltages, resulting in higher power consumption in the device [3].

To improve performance and reduce the cost of silicon transistors used in digital circuits, the main tasks are reducing dimensions of the device and increasing the circuit density. TFTs on the other hand, require only low-density circuits applied over a large area, and improvement in performance is related to increasing energy efficiency and overall stability of the devices [2]. Improvement in both energy efficiency and stability of the device can likely be achieved by replacing a-Si with ZnO as the channel layer in TFTs.

The purpose of this thesis is to study and explore the advantages of ZnO based TFTs deposited by metalorganic chemical vapor deposition (MOCVD). Two types of transistors has been synthesized and characterized. The first type was a bottom gate TFT made on a substrate of silicon. An insulating layer (silicon oxide or silicon nitride) deposited by plasma-enhanced chemical vapor deposition functions as the gate dielectric and the Si is used as the gate in this transistor structure. The second type is a hetero-structure TFT consisting of ZnMgO and ZnO on a sapphire (Al_2O_3) substrate. This structure was made in order to demonstrate advantages of two-dimensional electron gas (2DEG) formed at the interface between ZnMgO and ZnO. Current-voltage characterization is used to determine important parameters of the TFTs, such as the field effect mobility, on-off current ratio and threshold voltage. A metal-oxide-semiconductor (MOS) structure was also made and characterized by capacitance-voltage measurements. The purpose of this was to study the properties of the insulating layer and extract the dielectric constant and threshold voltage.

2. Background and Theory

2.1. Zinc Oxide

Thin films of homo- and hetero-structures made of oxide semiconductors have properties that make them potentially attractive for use in future optoelectronic devices. ZnO is particularly interesting for these applications due to its direct wide band gap and the possibility of tailoring electronic, magnetic and optic properties via alloying, doping, hetero-structures and quantum wells, and nano-engineering. Tailoring of this type is required to make a number of important devices such as laser diodes, solar detectors, spintronic devices and, most importantly, thin film field effect transistors for use in transparent electronics [4].

Zinc oxide is a compound semiconductor made up of the group IIb element zinc (Zn) and the group VI element oxygen (O). There are five stable zinc isotopes and the three most frequently occurring are ^{64}Zn (48.89%), ^{66}Zn (27.81%) and ^{68}Zn (18.57%), whereas oxygen occurs almost exclusively as the ^{16}O isotope (99.76%). The electron configuration of Zn is $1s^2 2s^2 2p^6 3s^2 3p^6 3d^{10} 4s^2$ and that of O is $1s^2 2s^2 2p^4$. ZnO has a tetrahedral geometry with four equivalent orbitals in its crystal lattice caused by sp^3 hybridization of the electron states. Here, the valence band is made up of the bonding sp^3 states, while the conduction band consists of its antibonding counterpart. This gives a band gap of 3.4 eV (in the ultraviolet range) and a cohesive energy per bond at 7.52 eV, resulting in high thermal stability. The melting temperature of ZnO is 2242 K.

In the crystal lattice, each zinc atom is surrounded by four oxygen atoms and each oxygen atom is surrounded by four zinc atoms in a tetrahedral configuration. This structure is common for both III-V and II-VI semiconductors as well as some group IV semiconductors. The bonding of the structure is called covalent, but when there is a significant difference in electronegativity between the constituents, there may be a noticeable polarity in the bond. Space filling in this geometry is quite low, so the stabilizing factor is the rigidity of the binding sp^3 orbitals. In ZnO the tetrahedrons form bilayers made up of one zinc and one oxygen layer. Whether the tetrahedron arrangement results in a cubic or a hexagonal structure depends on how these layers are stacked [5].

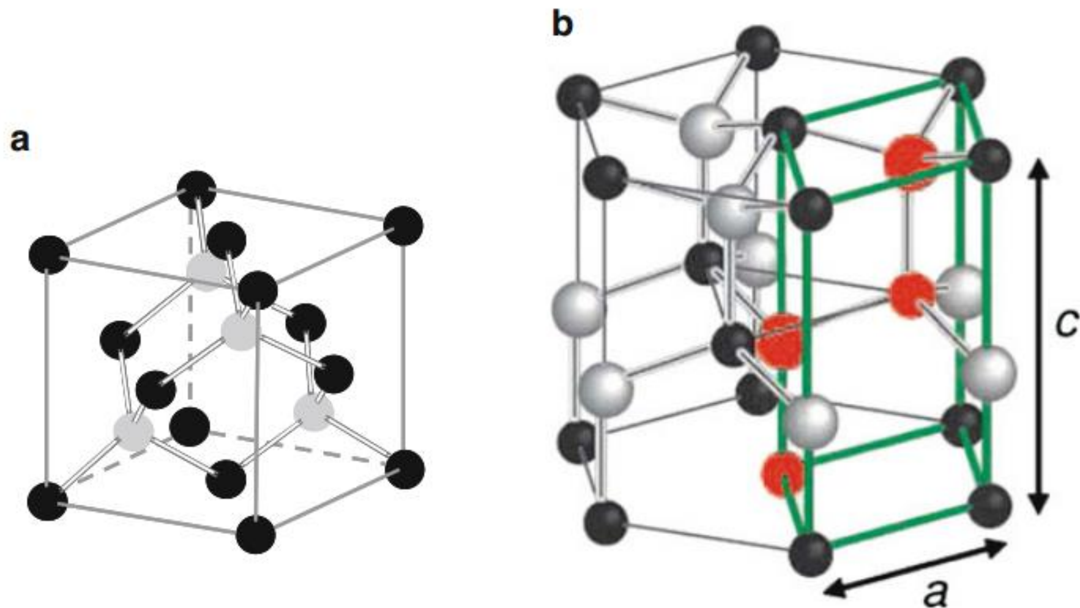


Figure 2.1: The two possible structures of ZnO, cubic zinc-blende (a) and hexagonal wurtzite (b). The red dots in figure b are the molecular base units (2 ZnO) and the green lines show the primitive unit cell [5].

The zinc-blende structure may be regarded as two interpenetrating face-centered cubic lattices, displaced by a distance equal to ¼ of the body diagonal axis, with the bonding orbitals oriented in the direction of the four body diagonal axes. Since the cubic unit cell is not the smallest periodic unit of the crystal, it is not the primitive unit cell. The primitive unit cell consists of an oblique parallelepiped containing one pair of ions, Zn^{2+} and O^{2-}.

Unlike the cubic zincblende, the hexagonal wurtzite crystal is uniaxial with its distinct axis directed along one of the bonding tetrahedral orbitals. This c-axis, as it is called, corresponds to a body diagonal axis of the zincblende structure. In the plane perpendicular to this axis, the translation vectors **a** and **b** have equal length and an angle of 120° between them. As opposed to the cubic structure, the primitive unit cell of wurtzite contains two pairs of ions, namely two ZnO units.

The preferred crystal structure for zinc oxide is the wurtzite structure with lattice constants a = b = 0.3249 nm and c = 0.5204 nm at ambient conditions. This preference is caused by the high degree of polarity of the bond between Zn and O in the structure. Oxygen has the second highest electronegativity of all periodic elements (only Fluorine has higher) while Zn has a relatively low electronegativity. Consequently, the bonding in ZnO is on the border between that of semiconductors, which is usually considered covalent, and that of the alkali halides, which is considered ionic, and thus zinc and oxygen in ZnO may well be considered as Zn^{2+} and O^{2-} ions. The ionic bond radius is 0.074 nm for Zn^{2+} and 0.140 nm for O^{2-} according to the Pauling scale giving a bond ratio of about 1:2. This high degree of polarity results in an effective charge Z* with reported values ranging from 1.00 to 1.30 and is, as mentioned, the reason that the wurtzite structure is favored over the zincblende for ZnO. Zinblende is common for tetrahedrally oriented bonds with lower polarity, such as for many II-VI semiconductors and in almost all III-V semiconductors. The only way to get cubic zincblende ZnO is by epitaxial growth on a zincblende substrate, for instance on GaAs (100) with a ZnS buffer [5].

Table 2.1 summarizes the properties of ZnO. The bandgap of ZnO is 3.3 eV at room temperature and can be tuned by adding Mg or Cd. Some of its electrical and optical properties, as well as energy band parameters like the effective masses of electrons and holes, are similar to those of GaN, and this material has already been used successfully in blue light emitting diodes (LED) and as a semiconductor laser diode. ZnO actually emits more intensely (about 4-5 times) and more efficiently than GaN at its band edge due to the fact that its binding exciton energy is more than twice the value of that of GaN. Excitons mediate the radiative recombination in ZnO and this should result in narrow emission linewidths. However, in GaN broad bandwidths are expected because in this material the recombination happens through band-to-band processes. This entails that ZnO can be used for a wide range of applications such as those mentioned above.

Basic Properties		**Crystal Lattice Parameters**	
Density (g/cm^3)	5.67	Crystal structure	Wurtzite
Molecular weight (atomic unit)	81.38	Lattice constants (Å)	a = 3.24 c = 5.20
Ion radii (Å)	r_{Zn}^{2+} = 0.60 r_O^{2-} = 1.40	Shear modulus (GPa)	50.0
Electronic configuration	Zn: [Ar]3d^{10} 4s^2 O: [He]2s^{2}2p^4	Stacking Fault Energy (mJ)	100
Thermal Properties		**Electrical Properties**	
Melting point (K)	2242	Bandgap (eV)	3.27 (300 K) 3.44 (6 K)
Thermal conductivity (W/m*K)	κ = 54	Electron Hall mobility (cm^2/Vs) Thin film Bulk single crystal	$\mu_{n\perp c}$ = 70 $\mu_{n/\!/c}$ = 170 $\mu_{n\perp c}$ = 150
		Effective mass of electrons (m_e)	m_n^* = 0.28
		Effective mass of holes (m_e)	m_p^* = 0.59

Table 2.1: Properties of ZnO [4].

Tuning the band gap can be done by alloying, but is most commonly done by using hetero-structures made of thin films. Mainly three periodic elements are used for this kind of band gap tailoring (see also section 2.2): Mg, V and Cd. Adding V or Mg broadens the band gap, while the addition of Cd narrows it. An advantage of using Mg is that it has an ionic radius similar to that of ZnO. In addition, widening of the band gap can be achieved in the same way as for III-V semiconductors (figure 2.2). By varying the Mg content from 0 to 100 %, the band gap of ZnMgO can theoretically be tuned all the way from 3.3 to 7.8 eV. This provides a cutoff wavelength range of 400 to 157 nm and this variation of band gap as a function of Mg content is larger than those found in AlGaN system. A drawback near the mixed phase region is the transition from hexagonal wurtzite to cubic structure at high contents of Mg.

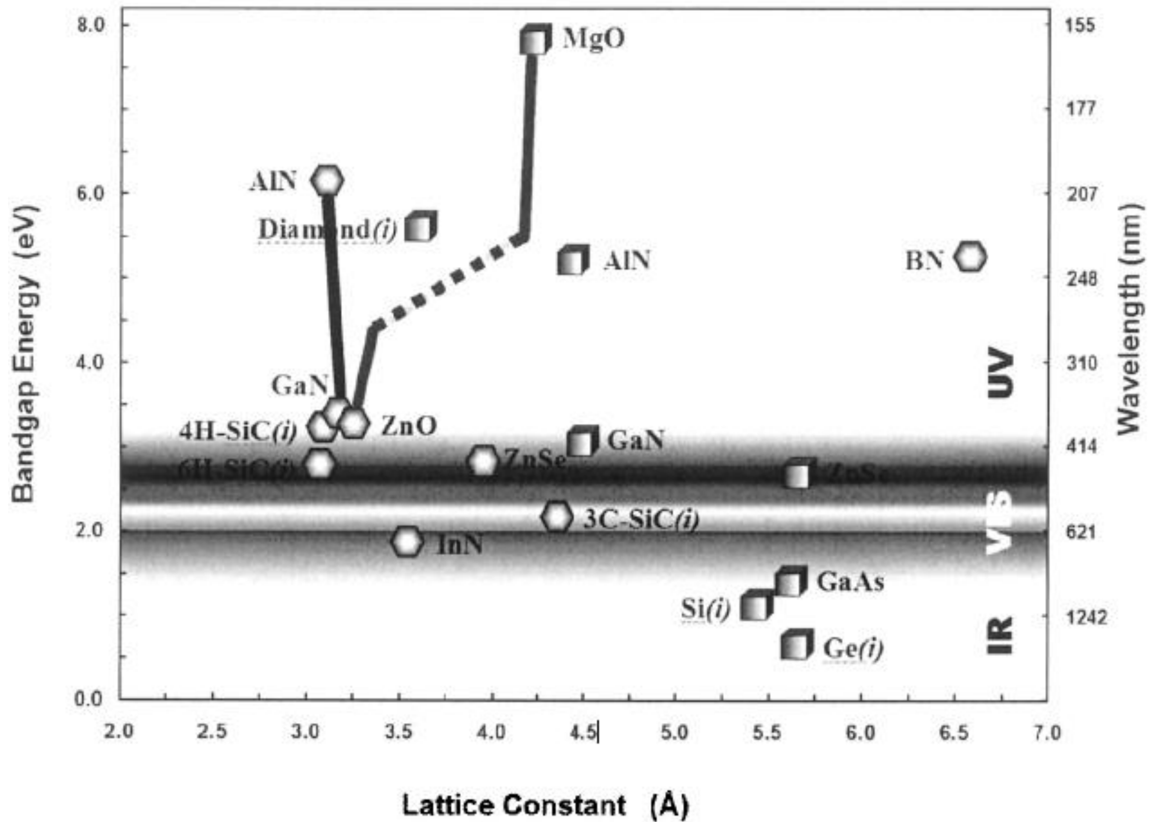


Figure 2.2: Band gap energy and corresponding wavelengths. Mg stands out as a particularly suitable material for band gap tailoring of ZnO [4].

There are some important advantages with regards to commercial production of ZnO compared to other semiconductors with similar properties. Monocrystalline ZnO of high quality is readily available with wafers having a diameter of 50 mm. Moreover, because of the differences in wafer growth processes, it is believed that the wafer production of ZnO will increase faster than that of GaN and other potential candidates for UV applications. The most common substrate for hetero-epitaxy is sapphire, despite its large lattice mismatch with ZnO (17%). On the other hand, the ZnO lattice matches closely to that of GaN (less than 2 % mismatch), which makes epi-GaN/sapphire the ideal substrate for hetero-structure junctions with minimal bandgap distortion. This makes hybrid device technologies more feasible. ZnO can be deposited at low temperatures with RF sputtering, chemical vapor deposition (CVD) and pulsed laser deposition (PLD), and the ionic nature of ZnO makes it possible to use both wet and dry etching in the device fabrication process.

2.2. Band gap tailoring

Band gap tailoring means being able to tune the band gap of a material through alloying, the use of hetero-structures or by implementing strained epitaxy. Tuning the band gap enables researchers and fabricators to tailor the performance of optoelectronic devices. The incompatible crystal structure and electronic configuration of MgO and ZnO makes the alloying of these two materials a challenge. As previously mentioned, MgO has a cubic crystal structure with a lattice constant a = 4.24 Å, whereas ZnO has a wurtzite structure with lattice constants a= 3.24 Å and b = 5.20 Å. MgO has a solid solubility of less than 4 % in ZnO according to binary phase diagrams. For other

semiconductors used in alloying, for instance AlGaN and AlGaAs, where the constituents have the same crystal structure, the alloy itself also end up having the same crystal structure.

Despite these supposed limitations (suggested by the phase diagrams), solid solubilities of 33 % for MgO in ZnO have been reported for thin films grown under metastable conditions. At percentages above 33, the MgO segregates from the ZnMgO lattice, and hence the band gap can be broadened to 3.9 eV and no higher. The solubility of MgO in ZnO films has been found to be a function of the growth temperature and this is established as a critical factor for stabilizing the purity and structure of the alloy. Phase separation and mixed phases caused by the lack of similarity between the structures is the main disadvantage with using the ZnMgO alloy for hetero-structures. For this reason, discontinuity when tailoring the band gap is to be expected. To get high quality $Zn_{1-x}Mg_xO$ films it is therefore necessary to minimize the phase separation region. In addition, the deposition technique will also affect whether the alloying will be successful or not [4].

2.3. Two-dimensional electron gas

Systems employing a two-dimensional electron gas (2DEG) are well-suited to show the degree of control and quality that can be achieved in a semiconductor system. A 2DEG can be formed via modulation doping or by piezoelectric effects in a semiconductor hetero-structure and this effect is the basis for the high electron mobility transistor (HEMT) and other devices. In polar semiconductors, such as ZnO or GaN, a high carrier concentration in a two-dimensional channel can be achieved through polarization effects as well as by using modulation doping. An advantage of ZnO over GaN for use in HEMT is that ZnO has a higher saturation velocity. However, there are some challenges that need to be overcome for high-quality ZnO HEMT structures to be used in commercial devices.

The purpose of the 2D channel is to separate the conducting charges from ionized impurities in order to avoid scattering and thereby increase the mobility. At carrier concentrations above 10^{18} cm^{-3} at room temperature, the dominant form of scattering is impurity scattering, but at lower carrier concentrations polar optical phonon scattering will dominate. The structural quality of the ZnO itself will also affect the outcome. In thin films, for instance, the structural properties will depend on the growth of an MgO buffer layer. There have been reports of Hall mobilities about twice as high as those for bulk ZnO for undoped ZnO grown by laser molecular beam epitaxy (440 $cm^2 V^{-1}s^{-1}$ compared to 230 $cm^2 V^{-1}s^{-1}$ at room temperature and 5 000 $cm^2 V^{-1}s^{-1}$ compared to 2 200 $cm^2 V^{-1}s^{-1}$ at 100 K for thin film and bulk ZnO respectively) [5].

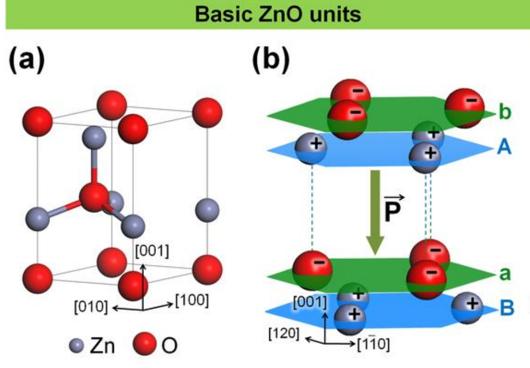


Figure 2.3: (a) ZnO unit cell, including the tetrahedral-coordination between Zn and its neighboring O. (b) ZnO has a noncentrosymmetric crystal structure that is made up of alternate layers of positive and negative ions, leading to spontaneous polarization $\vec{P}$. [6]

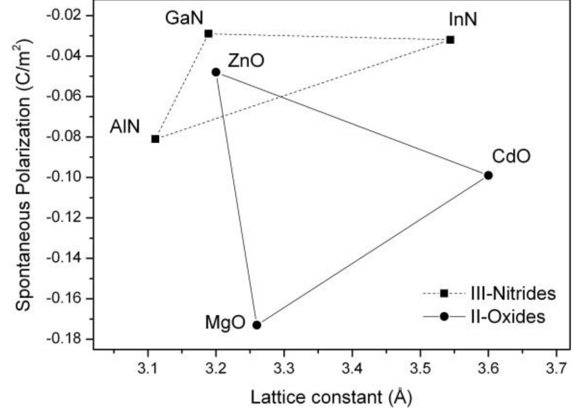


Figure 2.4: Spontaneous polarization in III-Nitrides and II-Oxide alloys according to a Vegard-like rule. [7]

ZnO crystal structure does not possess a center of symmetry, accompanied by a simultaneous shift in positive and negative charge centers within the primitive unit cell. Displacement of these charges results in a dipole moment within each unit cell. In crystals, spontaneous polarization arises due to the ionic character of the bonds between atoms and their asymmetric positions within the structure. In the bulk of such crystal, the net polarization charge within each unit cell is cancelled by neighboring unit cells resulting in a net polarization charge only at the top/bottom surfaces. However, for noncentro-symmetric crystals with a composition varying along the direction of the dipoles, a fixed (bound) polarization charge builds-up because the neighboring dipoles in the graded alloy are not of the same magnitude anymore, and thus no longer cancel each other. To maintain the overall charge neutrality, the bound polarization charge accumulated in the crystal must be compensated by mobile (free) charge carriers, which can be provided from the surface states. The lack of inversion symmetry in wurtzite II-Oxides along with the large ionic component of (Zn,Mg,Cd)-O bonds gives rise to very strong polarization effects, comprised of spontaneous and piezoelectric contributions. The strength of the electric field caused by spontaneous (P_{SP}) and piezoelectric (P_{PZ}) polarizations in strained heterojunctions, e.g. ZnO/ZnMgO, can be ascribed in terms of sheet charge density as

$$\sigma = P_{SP(ZnMgO)} - P_{PZ(ZnMgO)} - P_{SP(ZnO)} \tag{2.1}$$

In its turn, P_{PZ} is due to strain caused by the lattice mismatch between MgO and ZnO material and can be defined as:

$$P_{PZ} = 2\varepsilon_{xx}\left(e_{31} - e_{33}\frac{C_{13}}{C_{33}}\right) \tag{2.2}$$

Here, the strain is defined as $\varepsilon_{xx} = (a_{ZnMgO} - a_{ZnO}) / a_{ZnMgO}$, a stands for lattice constant, C_{13}, C_{33} are elastic and e_{31}, e_{33} are piezoelectric constants. Lattice parameter in II-Oxides varies as a function of alloy compositions as shown in Figure 2.4. Assuming ZnO as a starting composition, the lattice parameter increases for Zn(Mg)O system. Taking both the spontaneous and piezoelectric polarization effects into account, the polarization discontinuity in a coherently strained $Zn_{1-x}Mg_xO$

is expressed as $P^{SP+PE}(x) = 0.029x$ (C/m) and the built-in (intrinsic) electric field is given by $E(x) = Ax$, where $A = 3.95$ MV⁄cm [8] and x is the Mg content in ZnO. [6,7,8]

An example of a structure used to investigate a 2DEG is shown in figure 2.5.

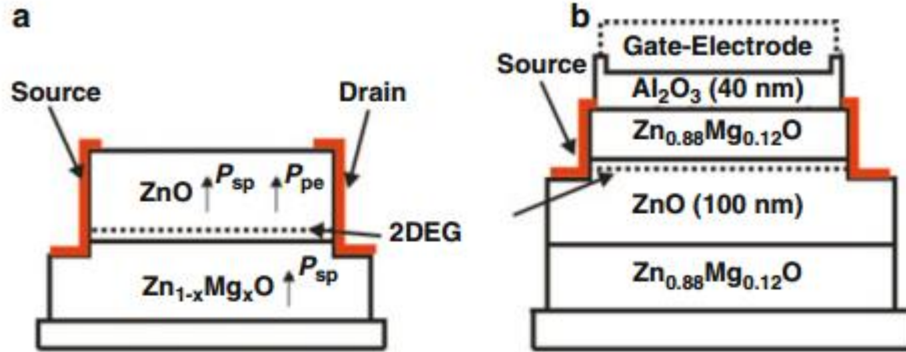


Figure 2.5: Depiction of structures used to investigate a 2DEG. Figure a) shows a structure without a gate to control the 2DEG, figure b) shows a structure with a gate to modulate channel conductivity [5].

The mismatch in spontaneous polarization between ZnO and ZnMgO causes the 2DEG to form in the part of the ZnO layer that is closest to the ZnMgO beneath it (figure 2.5 a). By changing the Mg concentration and the doping in the barrier, it is possible to control the concentration of charge carriers (i.e. electrons) in the 2DEG. There are two possible configurations when fabricating a 2DEG: one with oxygen-polar ZnO on top of ZnMgO, the other with zinc-polar ZnMgO on top of ZnO. As a consequence, being able to control the polarity of the material during growth is highly important. For oxygen-polar ZnO field effect transistors a mobility of 5 000 cm^2/Vs has been measured, while for structures on zinc-polar ZnMgO a mobility as high as 14 000 cm^2/Vs has been achieved. [5]

2.4. Thin Film Transistors

Conventional transistors use single-crystal wafers as the starting point for fabrication. This gives pn-junctions with high mobility and low leakage, but also imposes some important restrictions, especially in conjunction with integrating multiple active materials on one substrate, and particularly if the substrate is required to be larger or more flexible than the standard wafer. An example where this is a requirement is in light-emitting diodes (LED) or active matrix liquid crystals (AMLCD) used as pixels in flat panel displays. To drive the light emitting or transmitting devices, transistors are required at every pixel. This means having 10^6 transistors on an area of between $0.25m^2$ and $1m^2$. In this case, as opposed to use in digital circuits, the transistors do not have to be high performance transistors packed together as densely as possible, but a low on-resistance is desirable due to power considerations. In addition, because these transistors are made for display applications, it would be a major advantage if they could be made transparent. The development of thin film transistors has been made with these goals specifically in mind.

The work with developing thin film transistors was started in 1962 by Paul Weimer when he worked for RCA. The structure of TFTs today resembles that of Weimer's original device, but the materials used are different.

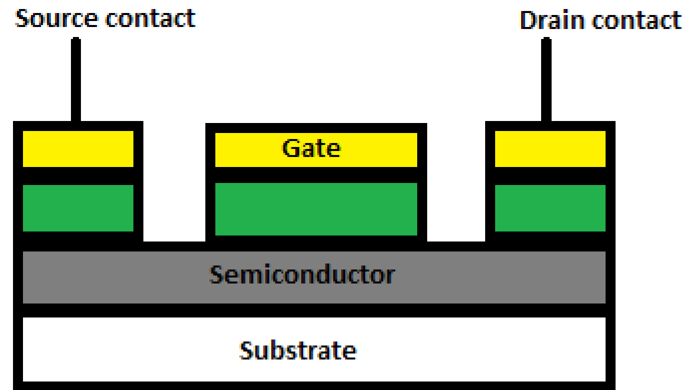


Figure 2.6: Cross-sectional view of a top-gate thin film transistor. The layers are gate metal and contacts to source and drain (yellow), insulator (green) and semiconductor material (grey). Source and drain are the regions in the semiconductor below the contacts and the insulating layer.

The basic elements of the TFT are a gate electrode, source and drain contacts, an active semiconductor layer and a gate insulator. It is possible to make both n-channel and p-channel devices, but the main focus has been on making n-channel devices. The structure is far simpler than other transistor structures used today, such as CMOS-transistors, and complicated isolation structures are not required since simple mesa isolation is sufficient. Low resistance ohmic contacts are normally not used because the thermal cycle of this device is severely limited. Instead, a large contact resistance is accepted while the barrier height is made as small as possible by choosing a material with an appropriate work function. However, in display applications the channel length is typically around 10 µm, and high performance contacts are not required when channels of this length with poor mobility are used. [9].

Unlike in a MOSFET, there is no inversion layer during operation of a TFT. Instead, the channel is formed by accumulation of charges in the interface between the insulating layer and the semiconductor. Still, the TFTs obey the same basic principles as a FET made of monocrystalline silicon, and have a similar I-V characteristic.

Figure 2.7 shows a schematic depiction of a bottom-gate thin film transistor. The channel consists of a layer of a-Si, poly-Si or ZnO, and has electrodes for efficient carrier injection and extraction (source and drain respectively). The gate is separated from the channel by an insulating layer and, as in a MOSFET there are two regimes in which the transistor operates: the linear region and the saturation region. First the current depends linearly on the voltage and Ohm's law is valid. This is the case for low drain voltages ($V_D << V_G$). But as the drain voltage increases, the potential in the channel will vary and at a certain point (i.e. saturation) inversion is no longer achieved. The channel is closed off and no more current will flow even if the voltage is increased (but charges will still be swept over from source to drain by the field, so there is a constant current). This happens when $V_D > V_G – V_{TH}$. In this region the I-V curve will be flat.

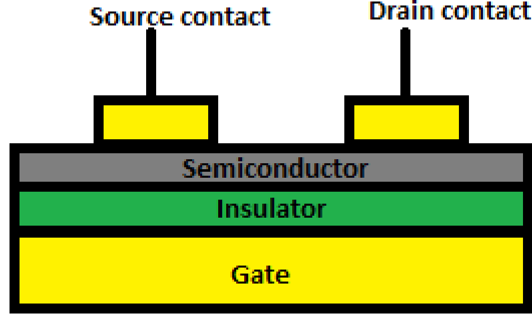


Figure 2.7:Cross-sectional view of a bottom-gate thin film transistor.

We assume a gradual channel approximation and that y is the direction parallel to the channel and x is perpendicular to the channel. In addition, the carrier density per unit area depends on y and the potential V(y) which is in turn dependent on the potential at the drain, V_{DS}. Given a gate voltage higher than the threshold voltage, V_T, the relationship between the mobile ion charge Q_i and the gate voltage can be written as

$$Q_i = -C_i(V_{GS} - V_T) \tag{2.1}$$

When the transistor operated in the linear region ($V_{DS} << V_{GS}$), the drain current can be written as

$$I_{DS} = C_i\, \mu_n\, \frac{W}{L}\, (V_{GS} - V_T)\, V_{DS} \tag{2.2}$$

As mentioned, the induced carriers in the inversion region will eventually disappear as the gate voltage is increased. Pinch-off occurs when $V_D = V_G - V_{TH}$ and the current reaches saturation at this voltage. In the saturation region (where $V_D > V_G - V_{TH}$) the following equation applies:

$$I_{DS} = C_i\, \mu_n\, \frac{W}{2L}\, (V_{GS} - V_T)^2 \tag{2.3}$$

The field-effect mobility can be extracted from the equation above. Contact resistance effects and gate-voltage dependent mobility may cause deviations from the gradual channel approximation [2].

Because transparent devices are wanted, thin layers and transparent metals such as indium tin oxide have been used [6]. Semiconductors that are transparent themselves, such as zinc oxide, have also been proposed for thin film transistors, and studies have shown promising results with regard to the performance of these transistors and the properties of ZnO [10].

There are three main challenges that need to be overcome to achieve adequate TFT performance. The first is developing a semiconductor material with a sufficiently high mobility which can be deposited by using low temperature deposition techniques. The second is producing an insulator with low charge density and low interface state density that is to be deposited on the semiconductor. The final challenge is making reliable metal contacts with low resistance.

The most commonly used material in commercial TFTs has been hydrogenated amorphous silicon (a-Si:H). Deposition is done by high frequency plasma-enhanced chemical vapor deposition (PECVD) with silane and hydrogen as precursors. The process is set up to be oxygen-free because oxygen degrades the performance of the TFTs significantly. A-Si has a high number of defect states in the bandgap caused by unsatisfied bonds in the material. To passivate these defects it is common to hydrogenate a-Si, hereby reducing the concentration of these states from 10^{20} cm^{-3} to 10^{16} cm^{-3}. Deposition temperature for a-Si is typically around 180° C. If the temperature exceeds 400° C, dehydrogenation will take place and this will lead to poor electrical performance for the device. Alternatively, nanocrystalline silicon can be made under the same conditions by heavily diluting with hydrogen, resulting in a slightly higher performance. By depositing at a higher temperature (around 600°C) or annealing after deposition, one can get polysilicon instead, which has higher mobility than a-Si. However, this precludes many substrates from use because of the high temperature that is required. Another alternative is laser annealing, but despite its effectiveness, this method is too costly for large scale use [9].

The prevalence of thin film transistors made of a-Si:H is primarily caused by the ease of manufacturing these transistors over areas of several meters at a side at low cost. Also, the fact that a-Si:H TFTs can be produced at relatively low temperatures make them compatible with substrates such as glass and metal foil, further lowering their overall cost of fabrication [2].

Silicon nitride is the insulator that has been used most frequently for thin film transistors. It is usually deposited by PECVD with silane and hydrogen as precursors. The Si_3N_4 layer acts as a diffusion barrier for several impurities, including but not limited to sodium, oxygen and water. Formation of particles in the plasma can lead to shorts in the film, so care must be taken to avoid this. One way is to use a bilayer gate in order to avoid pinholes and other types of defects which may propagate through the film layer. Normal processing conditions produce a Si_3N_4 film with a hydrogen content of around 20 to 40 %. There are usually traps present in stoichiometric Si_3N_4 and these are saturated by the hydrogen when using PECVD for deposition. To achieve interfaces with low state densities, a higher deposition temperature and/or RF power is generally required. There have been reports of Si_3N_4 layers with interface state densities as low as $2x10^{11}$ $eV^{-1}cm^{-1}$.

Currently, the contact resistance provided by contacts for a-Si:H is around 1 to 0.1 Ωcm^2, which is seven orders of magnitude higher than that of CMOS-transistors. This limitation is caused by the difficulty related to doping a-Si:H heavily. It has been shown, for instance, that by reducing the resistivity of the a-Si:H layers from 100 to 10 Ωcm, the contact resistance decreased from 30 to 0.1 Ωcm^2, the latter value corresponding to a carrier concentration of 10^{17} to 10^{18} cm^{-3}. It is common to deposit the doped layers between the channel layer and the contact and then etch to remove the doped layer from the channel region. An etch stop is deposited between the doped and undoped layers to prevent etching into the channel layer itself, but this has to be done before depositing the second a-Si:H layer. One way to accomplish this is by using the gate electrode itself as a mask and illuminate from the bottom in a semi-self-aligned manner. This results in exposure of the areas that are not above the gate and produces an image of the gate in the resist that is semi-self-aligned with the gate. This is essentially proximity printing with all the limitations this entails. Many thin film transistors have large contacts to compensate for the high contact resistance and use a voltage supply that provides tens of volts to give the DC current required to drive the pixel. The drawback by doing this is that the capacitance that has to be switched during operation increases and hence power consumption increases. An alternative is to do a fully self-aligned implant salacide process similar to the one used for state-of-the-art CMOS. Low implant activation and silicidation temperatures are required because a-Si:H degrades at 300

°C. By using this process, the source and drain will be self-aligned to the gate, thereby reducing the overlap capacitance. In addition, the series resistance will also be reduced.

It is also possible to use organic materials to make thin film transistors. An advantage with this is that the devices can be made at very low temperatures. Moreover, they can potentially be made without using any lithography or vacuum processing, instead using roll-to-roll printing technology to make complete transistors or even entire circuits. The major overall advantage with using organic materials is the potential for very low cost circuits, and when they are combined with organic light emitting diodes, fully integrated circuits and optoelectronic systems can be made. Printing resolution and accuracy would limit the minimum gate lengths to around 20 µm, but when considering the advantages, this is an acceptable trade-off. This is a relatively new area within thin film electronics and it is rapidly evolving. As is the case for other TFT materials, some challenges for organic TFTs are mobility, stability, interface states and contact resistance [9].

2.4.1. ZnO Thin film Transistors

There has been a lot of interest in ZnO in recent years because of its potential to replace a-Si:H as the semiconductor of choice for use in thin film transistors. ZnO has several attractive properties for this application, such as a wide bandgap, high transparency and good electrical transport. The improvement of the quality and control of conductivity in both epitaxial and bulk ZnO has led to an increase in interest for using this material in transparent electronics (as well as in short wavelength light emitters). Doped ZnO conducts current well and is highly transparent to visible light, properties making it suitable for use as transparent electrodes in flat panel displays. Its electrical and optic properties are comparable to that of widely used Indium tin oxide (ITO), but ZnO is less expensive, non-toxic, is thermally stable and also maintains stability in hydrogen plasma. Thin film transistors of ZnO provide high field-effect mobility and offers possible architecture and process simplifications compared to that of a-Si TFTs because of ZnO's insensitivity to visible light. ZnO deposition with low temperature deposition techniques may enable the fabrication of devices on plastic substrates, something that would reduce the cost of production considerably. These properties make ZnO TFTs an interesting alternative for pixel switches in display schemes such as AMLCDs, OLEDs and similar technologies.

A major difference between TFTs of a-Si and ZnO is that the characteristics of the former will degrade after being exposed to visible light, whereas the latter will not be affected. This means that measures to shield the channel layer against light exposure are not required for ZnO TFTs. Transparent TFTs of ZnO is compatible with high voltage, high temperature and it has a high radiation tolerance, all of which are desirable properties in this type of device. It is possible to grow high quality, crystalline ZnO films at low temperatures on substrates such as amorphous glass. Consequently, ZnO-based TFTs have been demonstrated by using several different growth techniques for the ZnO deposition.

To study the performance of TFTs, some important parameters to look at are threshold voltage, field-effect mobility and the on/off current ratio [3]. This is described in more detail in the section about I-V characterization.

2.5. Ohmic and Schottky contacts on ZnO

Ohmic contacts are required in order to operate the device. Unlike other wide band gap semiconductors, it is easier to achieve ohmic behavior when depositing metals on ZnO than schottky-type behavior. For I-V and C-V characterization, as well as deep level transient spectroscopy (to identify defects and its energy levels in the band gap), being able to fabricate reliable Schottky diodes is a prerequisite.

ZnO oriented in the (0001) direction has an electron affinity of 4.1 eV. If we assume that the Schottky-Mott model is valid and use the work function for each of the following metals, this would result in a Schottky barrier height of 1eV for gold (Au), 0.16 eV for silver (Ag), 1.02 eV for palladium (Pd) and 1.05 eV for nickel (Ni). However, the actual, published values differ from these theoretical ones significantly. Au has been found to have a barrier height of 0.66 eV and Pd a barrier height of 0.60 eV. The quality of the Schottky contacts is in great part caused by the surface preparation, and by using a subsequent etching, high quality contacts can be made.

To measure the homogeneity of contacts made of Au, Ag, Pd and Ni, they can be analyzed by using electron beam-induced current. Reliable values for the barrier heights have only been obtained for homogenous contacts. The surface polarity of ZnO and its effect on barrier heights of Pd and Pt diodes have also been observed, but no such effect has been seen when analyzing Au and Ag diodes.

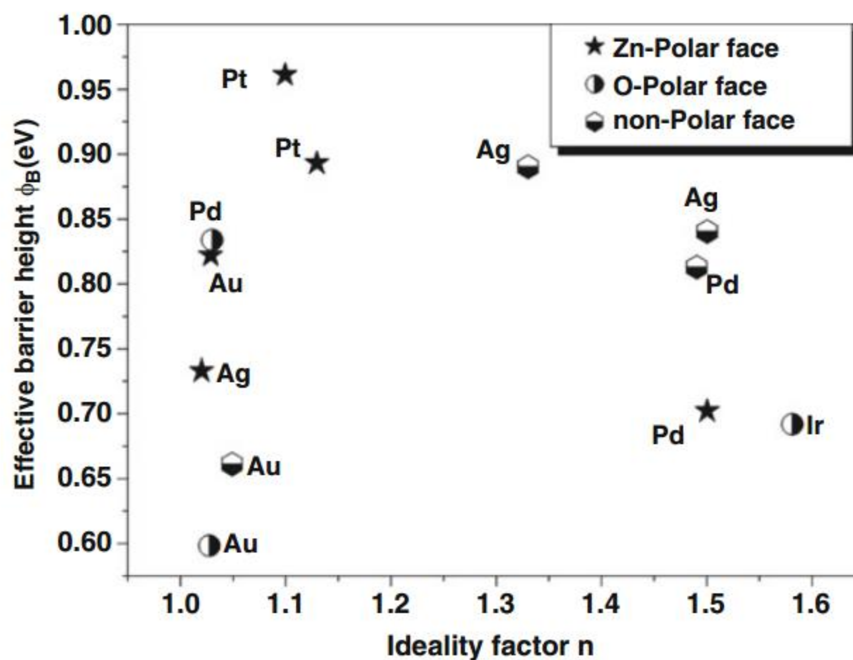


Figure 2.8: Barrier heights as a function of ideality factor for Schottky diodes for different metals on ZnO [4].

Diodes made of ZnO and Pd or Ag has been shown to provide the highest Schottky barrier heights, with 1.02 eV for Pd and 0.77 eV for Ag. By looking at metal-ZnO contacts with depth-resolved cathodoluminescence spectroscopy researchers have found that the barrier height and the ideality factor is influenced by native defects in the ZnO crystal and defects introduced through metallization. For contacts made of ZnO and Au, the behavior can be changed from ohmic to rectifying via the treatment of H_2O_2. This transition is believed to be caused by a reduction of surface OH termination and a vacancy defect being formed, thus leading to reduced conductivity close to the surface.

The quality of ohmic contacts made by depositing metals on ZnO is largely determined by the doping concentration of ZnO. Making ohmic contacts of high quality on n-type ZnO is not difficult because its doping concentration can be very high. Contacts of Au/Ti (titanium) (annealed in nitrogen at 300◦C after deposition) exhibiting ohmic characteristics and having contact resistances in the range of 10^{-4} Ωcm^2 have been reported [5]. Another alternative is non-alloyed Al (aluminium)/Pt contacts. A contact resistance of 10^{-4} Ωcm^2 can be achieved on ZnO with a carrier concentration of about 10^{18} cm^{-3}. This dependence on doping concentration is also present in contacts of Ti/Al/Pt/Au. Contact resistances ranging from $3x10^{-4}$ to $8x10^{-7}\Omega cm^2$ are obtainable, with carrier concentrations ranging from $7.5x10^{15}$ to $1.5x10^{20}$ cm^{-3} [5].

Making ohmic contacts for p-type ZnO is a lot more difficult, mostly because the work done to achieve this has been severely limited by the difficulty of obtaining p-type ZnO in the first place. Surprisingly, ohmic contacts of Au/Ni with contact resistances around 10^{-4} Ωcm^2 on ZnO:Sb have been reported [5]. Questions regarding doping type and measurement consistency have been raised, but the use of Ni could be related to the fact that NiO is intrinsically p-type, an uncommon property for oxide semiconductors [5].

Even without surface treatments Au contacts on ZnMgO will form a Schottky barrier. In [11] Schottky diodes with good rectification factor were obtained with deposition of Au on ZnMgO after basic cleaning and etching.

3. Previous Work

Initial attempts at making TFTs with channel layers of ZnO goes back as far as the 1960s. For instance in 1968, a TFT made of lithium-doped ZnO was demonstrated by Boesen and Jacobs. This device had evaporated SiO_x dielectric and contacts made of aluminum, but exhibited poor electrical characteristics. More significant interest for ZnO based TFTs, and particularly for active matrix organic light emitting diodes (AMOLED), has only appeared more recently with the work of Hosono, Wager, Carcia and Fortunato [1]. In 2003, Hoffmann et al. reported fully transparent TFTs with performance similar to that of a-Si and in some aspects even superior to the commonly used TFT material, with for example a measured mobility of 2.5 $cm^2 V^{-1} s^{-1}$. The processing temperatures for ZnO for these devices were quite high, ranging from 450 to 600 ^oC, but the work of Carcia et al. made use of radiofrequency (RF) magnetron sputtering for deposition of ZnO and were able to achieve similar electrical performance when depositing ZnO at room temperature. In this case a substrate of silicon was used for fabrication of transistors, so the devices were not fully transparent. However, a similar degree of transparency in the optical region was achieved. After 2004 several improvements in the realm of ZnO TFTs have been made. Improved performance has been achieved, mainly with regards to mobility, even when using low temperature deposition techniques; production of the ZnO layers have been done with non-vacuum processes; fully transparent devices have been made with room temperature deposition; new methods for extracting the mobility in the TFTs have been found and the application of ZnO TFTs as UV photodetectors has been realized.

Although, most of the work has been focused on binary semiconductors, more complex structures such as a single crystalline $InGaO_3(ZnO)_5$ (GIZO) semiconductor layer as channel layer in TFTs can also be found in literature (Nomura et al. in 2003). The transistors exhibited good characteristics, with a mobility of 80 $cm^2 V^{-1} s^{-1}$, a -0.5 V turn-on (threshold) voltage and an on/off current ratio of 10^6. Despite the fact that a very high temperature (1400 ^oC) was used to achieve this performance, the research made a huge impact in the field of TFTs because it proved that high performance TFTs are possible with oxide semiconductor-based materials. The following year Nomura et al. demonstrated transparent TFTs on a flexible substrate using temperatures close to room temperature for deposition. A GIZO layer deposited with pulsed laser deposition was used as the semiconductor, and although the performance of these devices was nowhere near the single crystalline TFTs made previously by the same authors, a saturation mobility of 9 $cm^2 V^{-1} s^{-1}$, threshold voltage of 1-2 V and on/off current ratio of 10^3 was achieved. After this demonstration, the amount of papers making use of GIZO and similar structures soared and from 2010 this technology has been applied in the industry to produce displays. By analyzing the 200 publications making use of GIZO TFTs two important things can be noted. The first is that the main deposition technique for these devices (>90 %) is sputtering and the second is that devices with acceptable performance can be produced at temperatures below 150 ^oC [1].

Hetero-structure TFTs made of double-layered oxides, for instance ZnMgO/ZnO have also been made, often with the specific purpose of forming a two-dimensional electron gas at the interface between ZnO and ZnMgO. In 2006 Shigehiko Sasa et al demonstrated high performance field effect transistors made of a $Zn_{0.6}Mg_{0.4}O/ZnO$ hetero-metal-insulator-semiconductor structure with Al_2O_3 as a dielectric. Field effect mobility of 62 cm^2/vs and a threshold voltage of -7.2 V were achieved [12].

4. Experimental Methods

4.1. Processing Techniques

4.1.1. Plasma-enhanced chemical vapor deposition

Many applications require the deposition of thin films at low substrate temperatures. This means the energy necessary to drive the reactions has to come from something other than heat. The most important non-thermal energy source is radiofrequency (RF) plasma [9]. Plasmas are used in several different processes including sputtering, etching and deposition of thin films [13].

Plasma is a gas where a fraction of the atoms have been split into ions and electrons (i.e. ionized). In process reactors the ionization fraction is usually from around 0.001 % to 10 %. Plasmas are electrically conductive, and because the electrons have a very low mass, they respond faster to changes in the electric field than ions, making electrons the primary charge carriers in plasmas. The most common way to generate plasma for plasma-enhanced chemical vapor deposition (PECVD) is by using an RF electric field. The electrons are easily accelerated by the field without significantly increasing the temperature of the plasma, whereas the heavier ions are unable to respond to the quick changes in direction and remain relatively still. Electronic energies in the plasma range from 0.1 to 20 eV and are sufficient to break chemical bonds or excite molecules via collisions between gas molecules and electrons. These inelastic collisions cause excitation or ionization and the species generated do not have the energetic reaction barriers of the parent precursor. Hence, films can be formed by the reactive ions at far lower temperatures than those necessary for thermal CVD. The reactions in a PECVD reactor are shown in figure 4.1 below.

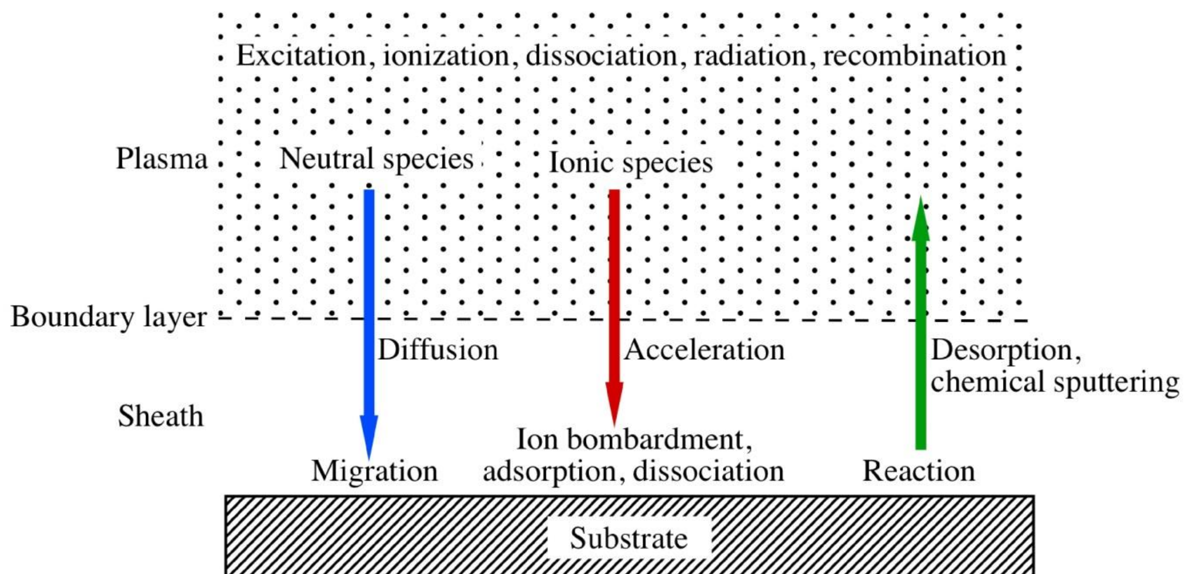


Figure 4.1: Reactions in the PECVD chamber [13].

Processes that happen in thermal CVD also occur in the PECVD reaction chamber. In addition, ionized species – which are produced by dissociation of parent precursors – diffuse to the substrate surface. These ions have lower chemical activation energies as well as a higher sticking

coefficient to the substrate. As a consequence, the PECVD reaction is not dominated by any of the precursor molecules which also diffuse to the surface, but rather the reactive species at the surface [13].

The advantage of plasma-enhanced chemical vapor deposition (PECVD) is, as mentioned, that depositions can be done at a much lower temperature than other forms of CVD. For thermal CVD the reactions occur in the range of 700 to 900 ^{o}C, whereas in PECVD the equivalent reactions take place between 250 and 350 ^{o}C [13].

In addition, PECVD provides energy by using ion bombardment of the substrate surface, thereby allowing the reactants to travel further along the surface at low temperature. This makes the process very effective at filling small features. [9]

There are several advantages with using PECVD compared to thermal CVD. At the high temperatures which are required for thermal CVD the metal interconnects may melt and significant diffusion of dopants occurs. This is avoided with the lower temperature deposition of PECVD. In addition, because a fairly low pressure is necessary to maintain plasma, the reaction is controlled by surface kinetics, thus yielding higher film uniformity than for thermal CVD. However, there are disadvantages with PECVD, such as damage of the film caused by the bombardment of ions during deposition, and difficulties with controlling the stoichiometry. The reason for these difficulties is variations in the bond strengths of the different precursors. In silicon nitride for instance, the bond in a N_2 molecule is stronger than the Si-H bond and this tends to make Si_3N_4 films made with PECVD silicon rich [13].

PECVD reactor types

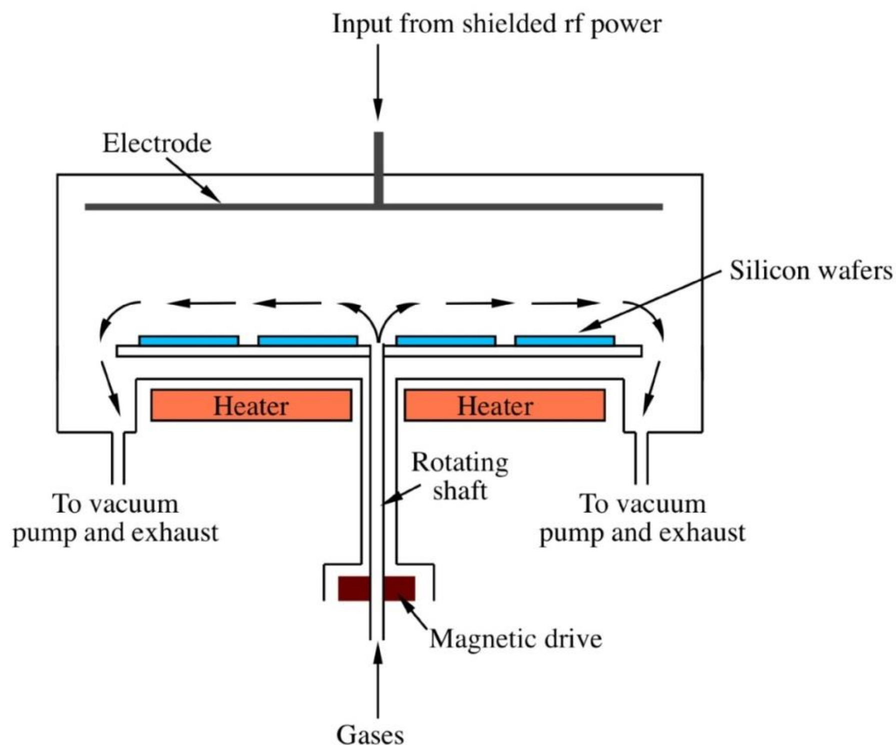


Figure 4.2: Cold wall parallel-plate reactor [13].

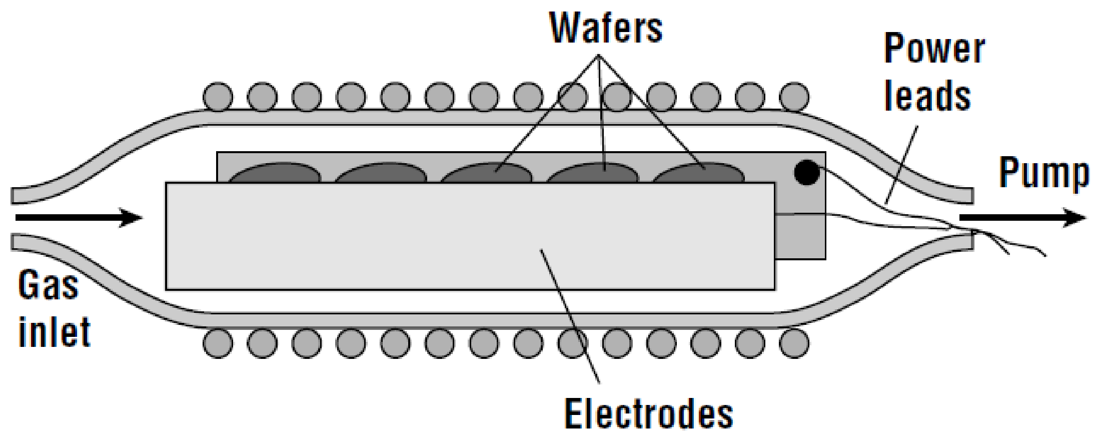


Figure 4.3: Hot wall parallel-plate reactor [9].

In figure 4.2 and 4.3 two different kinds of PECVD reactors are depicted. Although deposition is possible at 13.56 MHz, most of the systems use frequency less than 1 MHz [6]. Figure 4.2 shows a basic cold wall parallel-plate reactor. This was the first type of reactor used for PECVD. The wafers are placed on a plate acting as the lower electrode which normally has a potential of zero (i.e. ground potential). The gases are either injected at the reactor edges and then pumped out through the center, or radially injected from the center and pumped out at the edges. During processing the wafers are rotated by the magnetic drive to ensure that the substrate position is randomized. A more uniform plasma distribution can be achieved by introducing the gases through holes in the upper electrode, and some newer reactors make use of this concept [9]. This is the type of reactor available at MiNaLab, University of Oslo.

With increasing wafer size the use of cold wall parallel-plate reactors in large scale production of integrated circuits has decreased because of the low throughput and uniformity related to these systems. However, for deposition on GaAs this kind of reactor remains the preferred type.

Today, the hot wall parallel-plate reactor (figure 4.3) is generally preferred to the cold wall design in large scale production of integrated circuits with PECVD. This design is similar to a low pressure chemical vapor deposition (LPCVD) tube where the wafers are placed vertically on graphite electrodes. The temperature in the chamber during growth is much lower than for an LPCVD process. However, the throughput, though higher than that of a cold wall reactor, is much lower than for a LPCVD system. Gas depletion/uniformity and particle problems affect the processes in both hot wall PECVD and conventional thermal CVD systems. This has led to renewed interest in cold wall PECVD reactors. By setting up several deposition stages into one vacuum system or running more than one single-wafer chamber in parallel with another, an increase in the system’s throughput can be achieved.

Another way to make high quality layers on low temperature substrates is by using high-density plasmas. One way to achieve this is to use an electron cyclotron resonance (ECR) reactor to dissociate one or more of the precursors. High-density plasmas are for instance used to dissociate N_2 into atomic nitrogen which subsequently reacts with silane and forms Si_xN_y avoiding ion bombardment almost entirely. A large substrate temperature is not required for the reaction to happen since the reactivity of the atomic species is so high. Silane can be injected outside the plasma and silicon dioxide films of high quality have been deposited at temperatures down to 120 ^{o}C.

The high density plasma has a low pressure (~0.01 torr) which results in long mean free paths leading to poor step coverage. This can be remedied by continuous sputtering of the deposited species by allowing ion bombardment of the surface, giving a proper filling of high aspect ratio features. In general this is one of the most used applications of the technology, and particularly for deposition of SiO_2 this has been very useful. A drawback with HDP is its high concentration of particles. A solution which has been proposed recently is creating particle traps or chamber surfaces that are particle absorbent. The deposition rate of ECR is low, but can be improved by designing systems where several plasma injectors are placed in parallel in a single vacuum chamber.

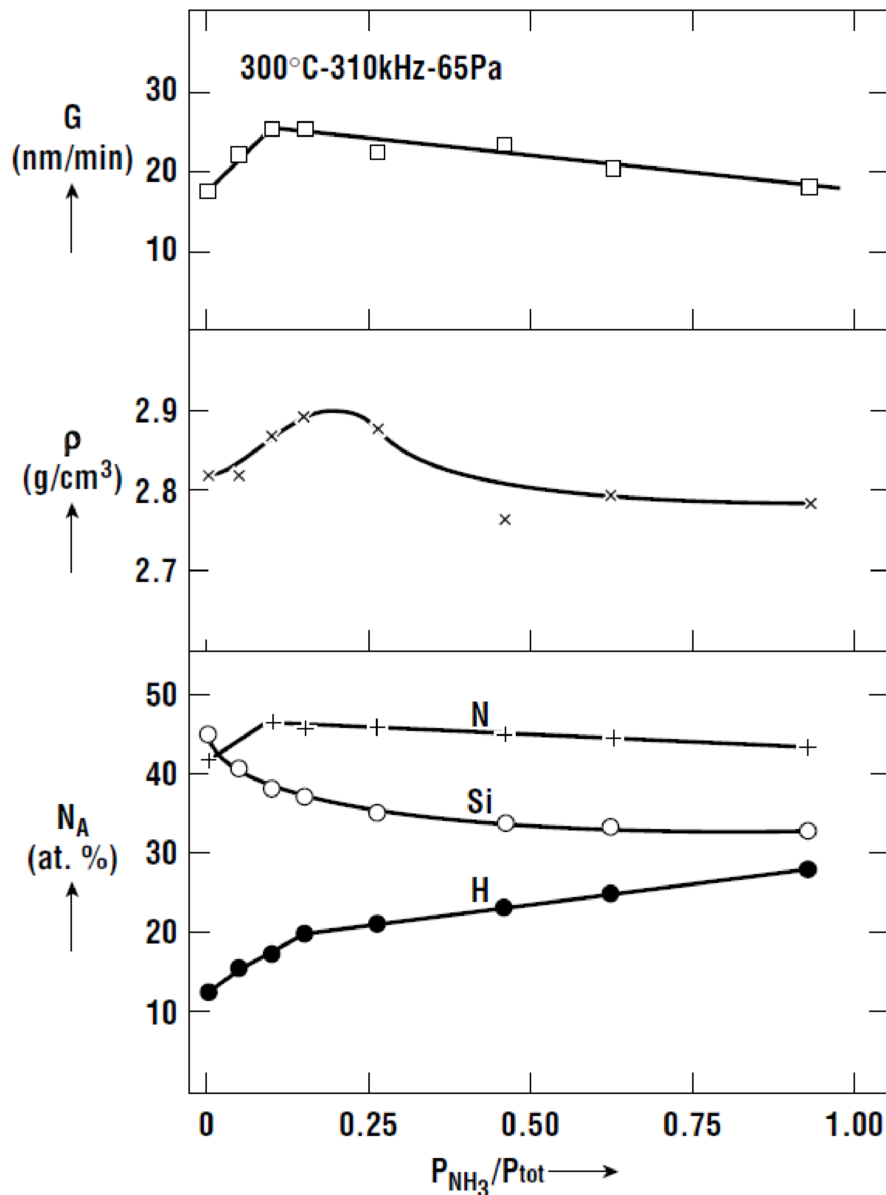


Figure 4.5: Deposition rate, density and stoichiometry of Si_3N_4 deposited by PECVD [9].

As can be seen in figure 4.5, the deposition rate does not depend strongly on the gas composition. The peak in density is around the value for stoichiometric silicon nitride, in other words a Si/N ratio of ¾. If the ammonia flow is increased, the concentration of hydrogen will also increase, and

for Si_3N_4 deposited with PECVD the hydrogen concentration is usually around 20 %. This increase can be counteracted by heating up the substrate or by using N_2 instead of NH_3 [9].

4.1.2. Metal-organic chemical vapor deposition

Metalorganic Chemical Vapour Deposition (MOCVD) was introduced by Manasevit and Simpson in the 1960s. At the time they were trying to find a method for depositing GaAs and other optoelectronic semiconductors onto sapphire and similar substrates. Other techniques, such as Liquid Phase Epitaxy (LPE) and chloride Vapour Phase Epitaxy (VPE) were not suitable for growth on a substrate where the surface was very chemically different from the material to be deposited. Manasevit and Simpson found that by using combinations of alkyl organometallics for the group III element and hydrides for the group V element, they could deposit GaAs on several different substrates. It took some time before the technique became significant in terms of production; in the 1980s a lot of work had been put into in improving the purity of the precursors and this made the technique very successful. After this, in contrast with the pioneering work of Manasevit and Simpson, considerable effort was focused on making high quality epitaxial layers on lattice-matched substrates. Because of this high quality epitaxial nature of the films the technique is also called Metalorganic Vapour Phase Epitaxy. However, it is important to note that MOCVD can include polycrystalline growth and this cannot be referred to as epitaxy.

The simplicity in delivering the reactive precursors in an MOCVD reactor and the versatility of the technique are characteristics that have taken MOCVD from relatively small use in research to far more extensive use in both research and production. The technique is used for narrow band gap semiconductors, such as $Cd_xHg_{1-x}Te$, and, more recently, wide band gap semiconductors such as ZnO [14].

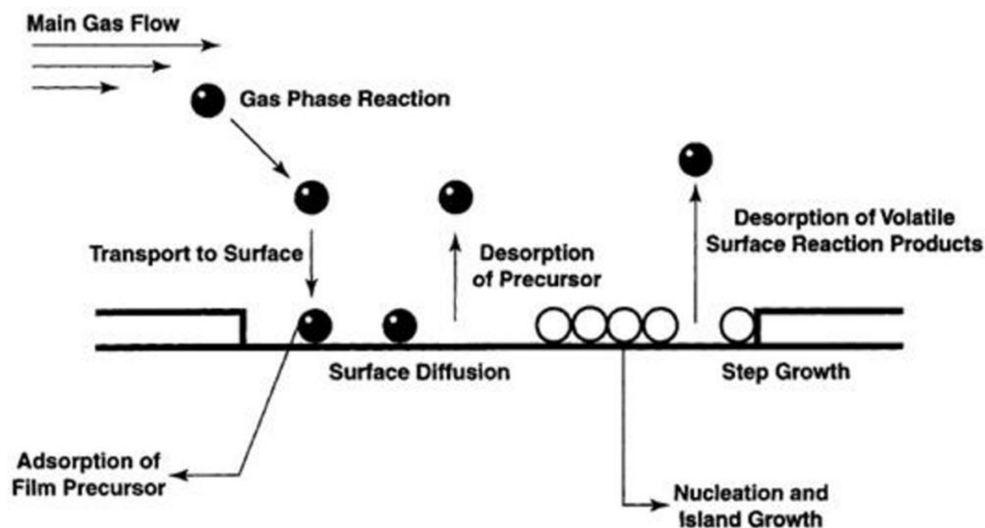


Figure 4.6: Illustration showing the transport and reaction processes in a MOCVD reactor [15].

The reactions in the above illustration can be explained in the following way:

Gas phase diffusion: Transport of reactant gases into the reaction chamber.

Gas phase reaction: Reactions which generate the constituent species for deposition.

Surface transport and absorption: Transport of these constituent species to the surface and absorption on the surface.

Surface diffusion: Diffusion of the species on the surface.

Desorption: Volatile species evaporate or are desorbed from the surface.

Nucleation and growth leading to film formation: Vapor phase condensation, solidification of liquids and gases.

Gas exhaustion: Transport of the by-products to the exhaust outlet Illustration showing the transport and reaction processes in a MOCVD reactor [15].

II-VI MOCVD

MOCVD of II-VI compounds generally takes place at much lower temperatures than for III-V compounds. This has led to research on alternative precursors, energy-assisted growth, and growth kinetics. The principles for making II-VI semiconductors with MOCVD is basically the same as for making III-V semiconductors and the same reaction chambers can be used. However, different precursors are necessary because of the lower growth temperature, especially for the group VI elements.

For II-VI semiconductors alkyl groups are normally used both for the group II and the group VI element. Pre-reactions make it difficult to use hydrides, especially when incorporating dopants. Using combined precursor sources has been an area of extensive research, but it is not in use for making high quality epitaxial layers. This is because it is difficult to control the stoichiometry of the material by adjusting the precursor ratio [14].

Growth rate

To gain an understanding of what happens in the MOCVD process, the chemical reactions that take place in the reaction chamber are important to consider. Pyrolysis is the most common chemical reaction and is related to thermal decomposition of volatile metal-organic radicals and oxygen source for growing the semiconductor oxide material. Thermodynamics is an important driving force for deposition of desired material formed by the pyrolysis process. The maximum value for growth rate is set by thermodynamic calculation, but the rate also depends on mass transport which in turn affects the thickness uniformity of the film. Mass transport consists of two parts, diffusion; the motion of individual atoms or molecules, and hydrodynamics; the motion of a group of gases as a whole, for instance viscous flow and convection. Generally, thermodynamics and kinetics both contribute to the process of thin film deposition by MOCVD. Kinetics is dependent on heterogeneous surface reactions and movement of reactants to the substrate surface. These movements include adsorption of reactants, desorption of products and surface diffusion. Heterogeneous reactions between gases and the solid result in material film growth on the surface. Figure 4.7 shows the three growth regimes associated with kinetics, mass transport and thermodynamics.

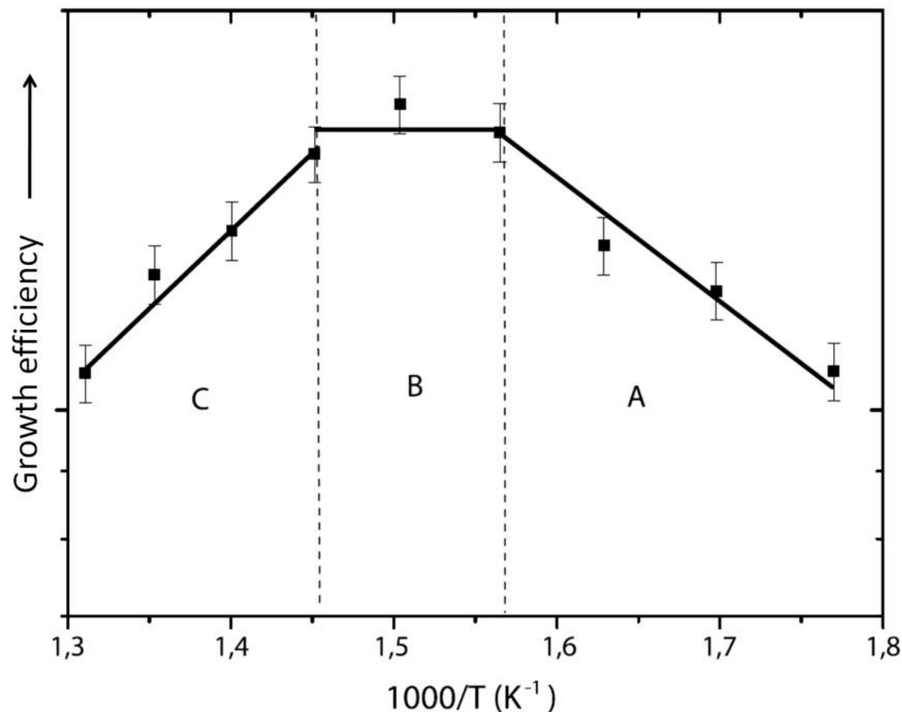


Figure 4.7: The graph shows the different growth regimes for ZnO using diethylzink and tertiary-butanol as precursors [15].

In the first regime (A in figure 4.7) the growth is limited by surface kinetics, and thus controlled by the reaction of DEZn and t-BuOH on the surface. This region is from about 292 to 366 ^{o}C.

At temperatures higher than this full pyrolysis efficiency is achieved and the growth becomes mass transport limited. Here, the growth rate does not depend on the temperature; it is determined by the concentration of the precursors. This regime is called the diffusion regime. The diffusion coefficient of the gaseous alkyls depends weakly on temperature, but is moderated by the boundary layers caused by the fluid dynamics through the chamber.

The third regime (C in figure 4.7) is characterized by a decreasing growth rate due to evaporation and desorption of precursors and occurs at temperatures above 416 ^{o}C. In this regime, the temperature becomes so high that pyrolysis occurs and this results in material deposition of particles. Consequently, deposition on the wall of the reactor, spontaneous nucleation and a higher desorption rate of reactants disturbs the deposition on the substrate, and hence, growth rate is reduced.

Kirchner et al [15] compared the growth rate of ZnO on c-plane sapphire when using diethylzinc (DEZn) as zinc precursor and three different oxygen precursors, iso-propyl alcohol (i-PrOH), nitrous oxide (N_2O) and tertiary-butanol (t-BuOH). It was found that the growth rates for all the oxygen sources under study had similar dependence on pressure (see figure 4.8), but differed highly as a function of temperature (refer figure 4.9). For t-BuOH the growth rate was nearly constant from 380 to 510 ^{o}C, and the optical quality of the layers grown with this precursor was found to be superior to those grown with i-PrOH. For i-PrOH a maximum ZnO growth rate occurred at 380 ^{o}C. However, ZnO growth occurred only at temperatures > 550 ^{o}C with N_2O as oxygen source. To get high quality layers, it was necessary to achieve a flat surface via proper thermal treatment of the substrate before growth. In addition, the flow rate of the precursors should be high for optimal growth [15].

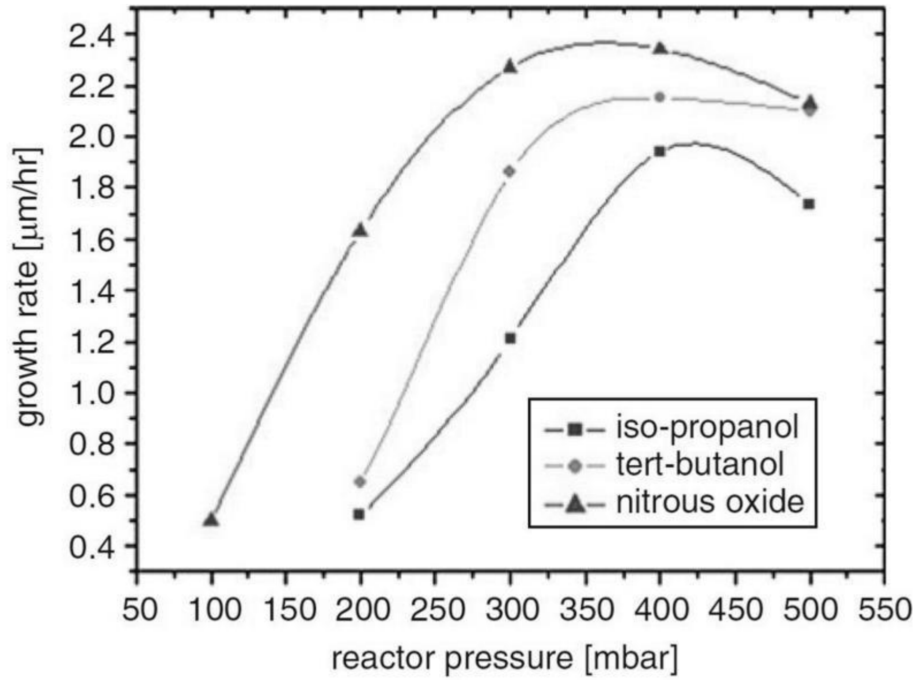


Figure 4.8: Graph showing the growth rate of ZnO as a function of reactor pressure [15].

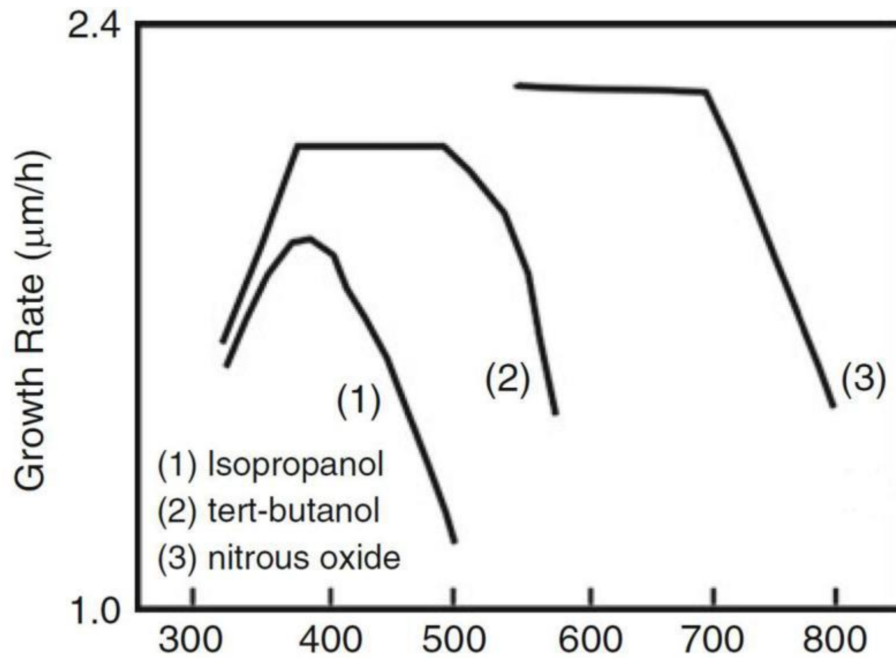


Figure 4.9: Growth rate of ZnO as a function of temperature. The growth regimes depicted in figure 4.7 can also be observed here [15].

MOCVD Reactor at MiNaLaB, UiO

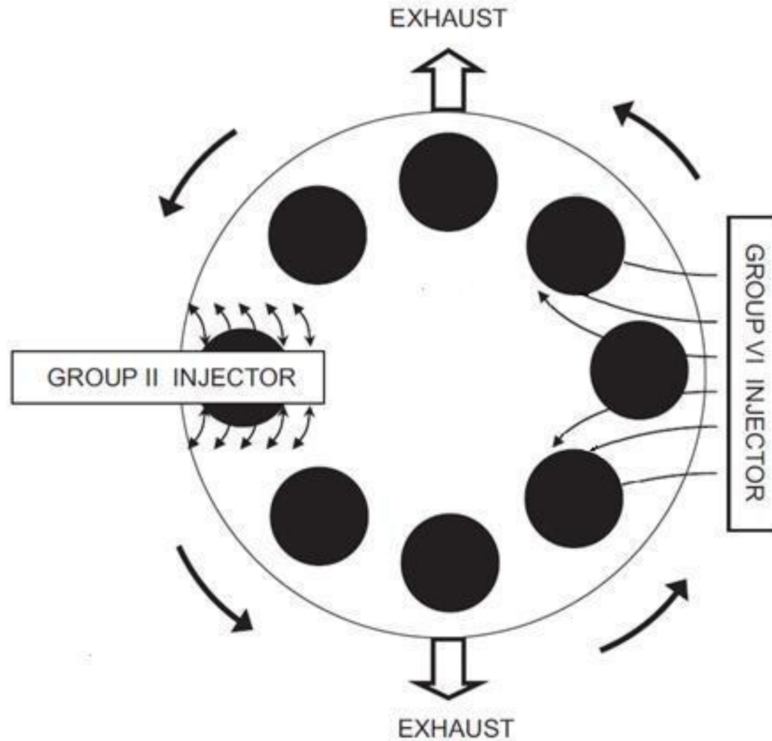


Figure 4.10: Illustration of an EMF vector flow MOCVD reactor. The gases come in through separate inlets and hence mixing of the reactants is avoided [15].

There are several different types of MOCVD reactors, but they all have some basic functions in common. Activation energy for the process must be provided and the diluent gases and reactants must be allowed to flow to the reaction zone. In addition, a specific reactor temperature and pressure must be maintained during the process, and the by-products removed from the chamber as the reaction proceeds. All these functions should be implemented as effectively, as safe and with as much control as possible during operation. Most importantly, the reactors are classified based on the injection of precursors in to the reactor. The precursors are carried by an inert gas such as N_2 or Ar and directed into a heated zone where the substrate is placed. The basic idea is to reduce the parasitic reactions (pre-reactions near the reactor wall and other places) and maximize the reactions at the growth front, i.e. on the substrate.

The MOCVD reactor in the MiNaLab uses the system depicted in figure 4.10, and this method of flow modulation for deposition is called vector flow epitaxy. The two types of precursors (group II and IV) are introduced through separate inlets and reacts on the surface of the wafers. These are located on a rotating susceptor platen. In the reaction chamber there is a radial injector for the group II precursor, and a tangential injector for the group VI precursor. The rotation of the platen ensures that the precursors are distributed evenly on the substrates and are ideally kept separate throughout the reaction, exiting the chamber through separate outlets. Pre-reactions in the reaction chamber, which can be a big problem in other types of reactors, are prevented by alternate dosing with the different precursors and their full consumption in the reaction chamber. Moreover, this type of reactor runs at nearly atmospheric pressure. The operation of the reactor is thus simplified by maximizing the reactant partial pressure leading to an efficient use of precursors [15]. Figure 4.11 and 4.12 show the schematics of the gas handling system and gas flow schematics of vector flow modulated MOCVD at the facility in the MiNaLab.

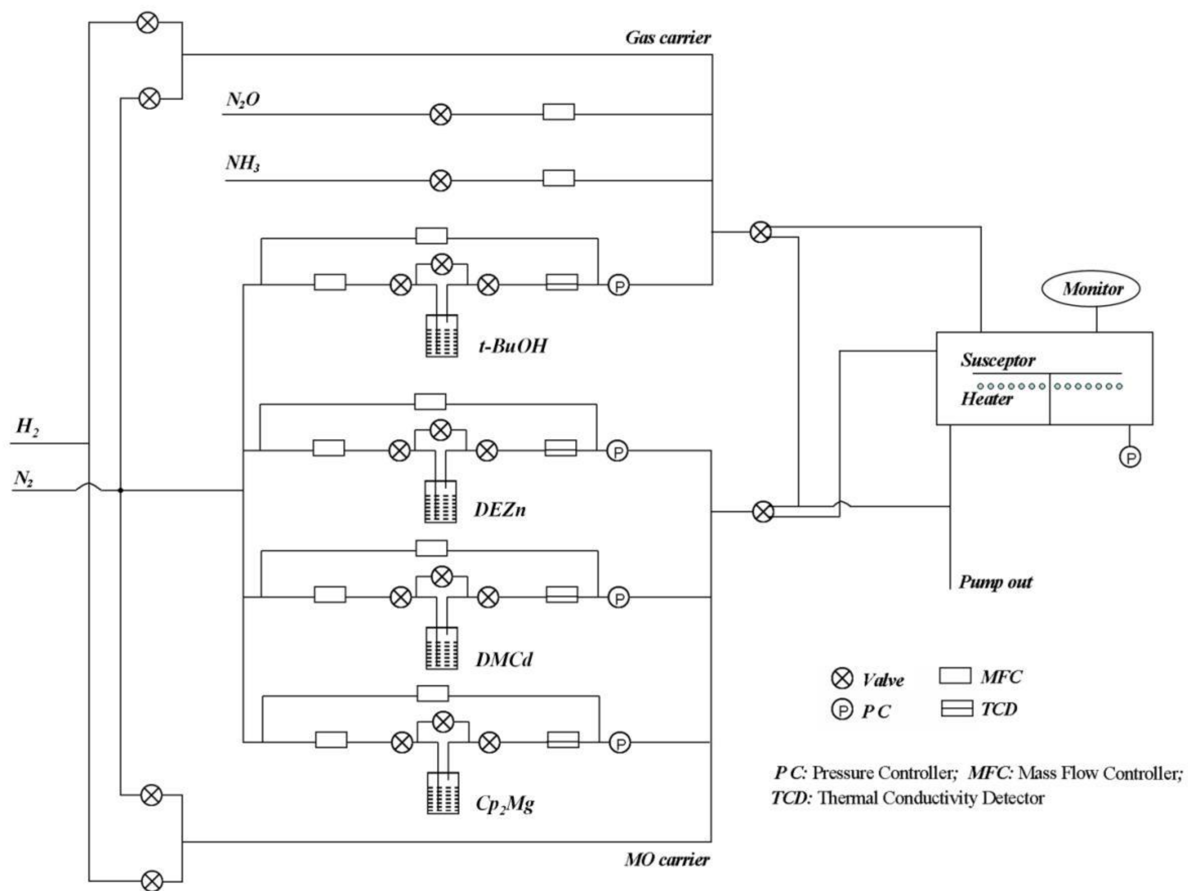
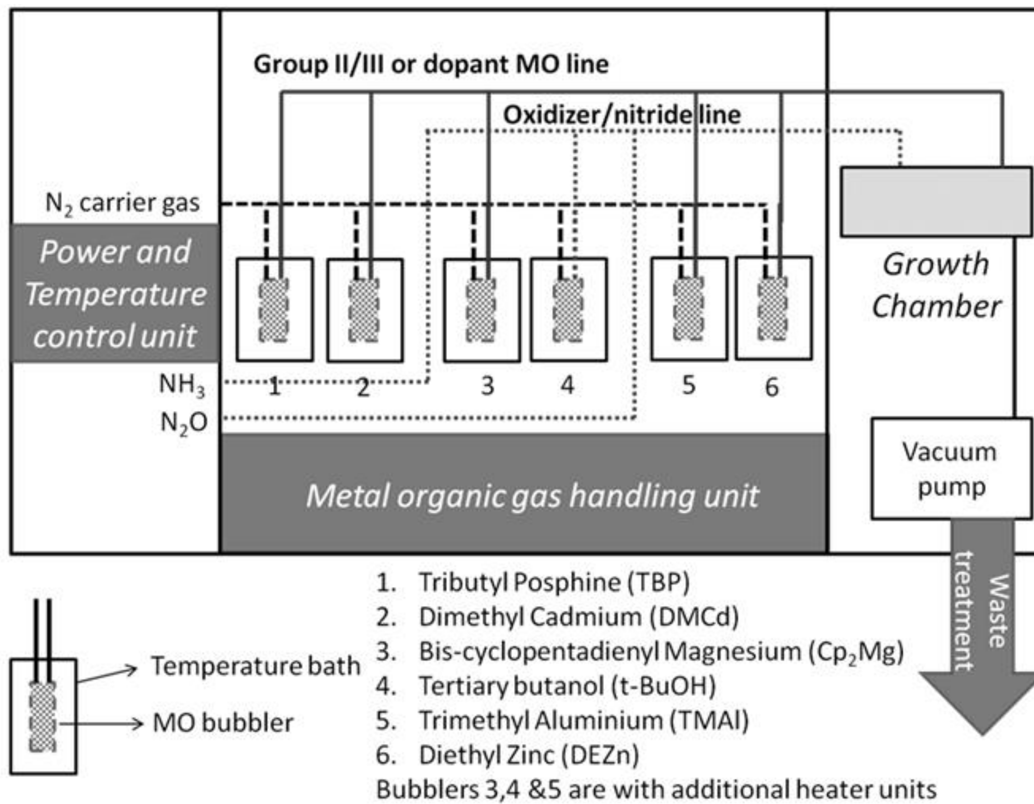


Figure 4.11: Gas flow schematics of vector flow modulated MOCVD tool at MiNaLab/UiO [15].



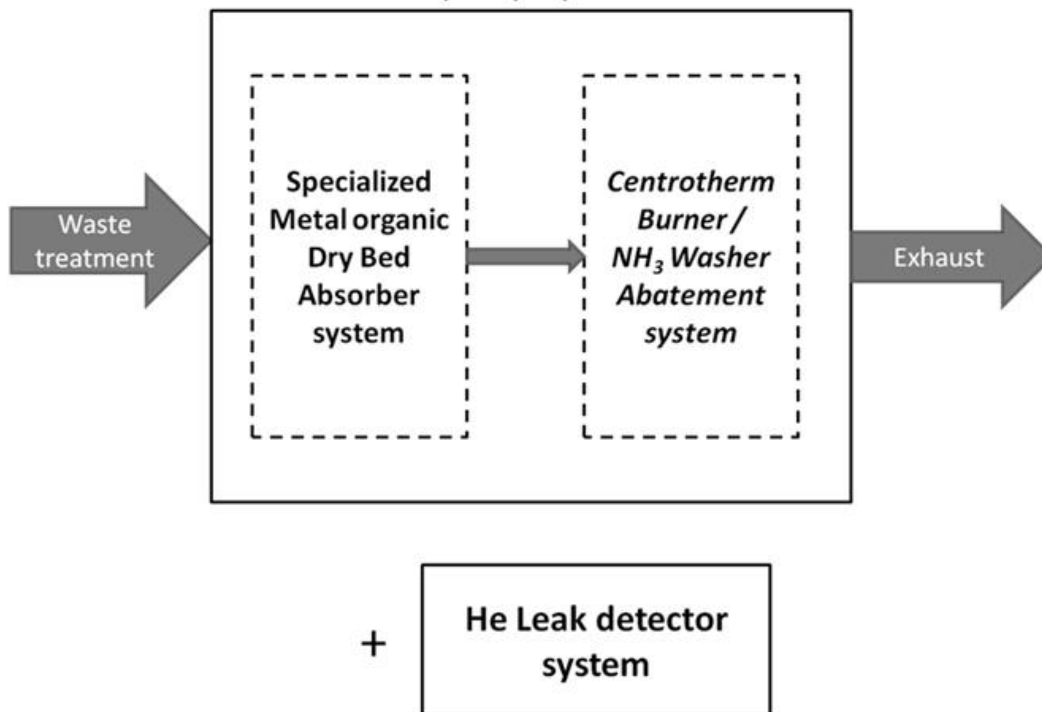


Figure 4.12: Schematics of gas handling system layout of MOVPE tool and exhaust waste treatment facility available at MiNaLab/UiO [15].

The MOCVD is a complex technique and herein lies both its strength and its weakness. Given the right precursor it is possible to grow just about any inorganic material. However, the development is empirical and therefore many of the reaction mechanisms in the process are poorly understood.

Despite this, the technique has made significant contributions to the compound semiconductor industry. For instance, the variety of large LED displays owes its existence to MOCVD. The work of Manasevit and Simpson paved way for later research by demonstrating the potential for growing many different types of materials with the technique, and the ease of growing GaAs/AlGaAs layers encouraged researchers to expend considerable effort with growing the more difficult materials [14].

4.1.3. Thermal evaporation

Deposition of films by evaporation is done by heating the evaporant (the material to be deposited) above its melting point (or slightly below given a low enough vapor pressure) in a low pressure chamber. The low pressure ensures that the evaporated species can travel in straight lines towards the substrate at a high velocity and be deposited on its surface. The source material can be heated by resistive heating, RF heating or with a focused electron beam.

Aluminum is one of the metals most frequently deposited with thermal evaporation. It is often deposited as the metal in metal-oxide-semiconductor (MOS) structures and it is used for metallization in integrated circuits. With a resistivity of ~μΩ-cm for aluminum and its alloys, it satisfies the low-resistance requirements. In addition, Al easily adheres to silicon dioxide making it a suitable metallization material for MOS structures based on this insulator [16].

Evaporation was the dominant technique for depositing metal layers in the early days of semiconductor fabrication. Today it has been replaced by sputtering and, in some cases, electroplating in silicon technologies, but it remains an important tool in research and for III-V semiconductor technologies. There are basically two reasons why other techniques have been preferred in recent times. Firstly, evaporation has poor step coverage, which means that its ability to cover surface topology is limited; on the vertical walls the film may become discontinuous. While the transistor dimensions have steadily decreased, the thickness of the different layers has stayed essentially constant. A consequence is that the topology imposes stricter restrictions on coverage of the deposition technique. Secondly, producing alloys with evaporation is also a challenge and some technologies require these to form efficient contacts or metal lines. III-V semiconductor technologies exploit the poor step coverage of thermal evaporation by depositing a metal layer on the photoresist after lithography. Rather than etching, the metal layer is dissolved (usually in acetone) along with the unexposed photoresist and hence lifted off the sample. Instead of using alloys, it is common to deposit thin layers of several different metals. It would be difficult to etch this kind of metal stack, but by using lift-off instead this problem is avoided.

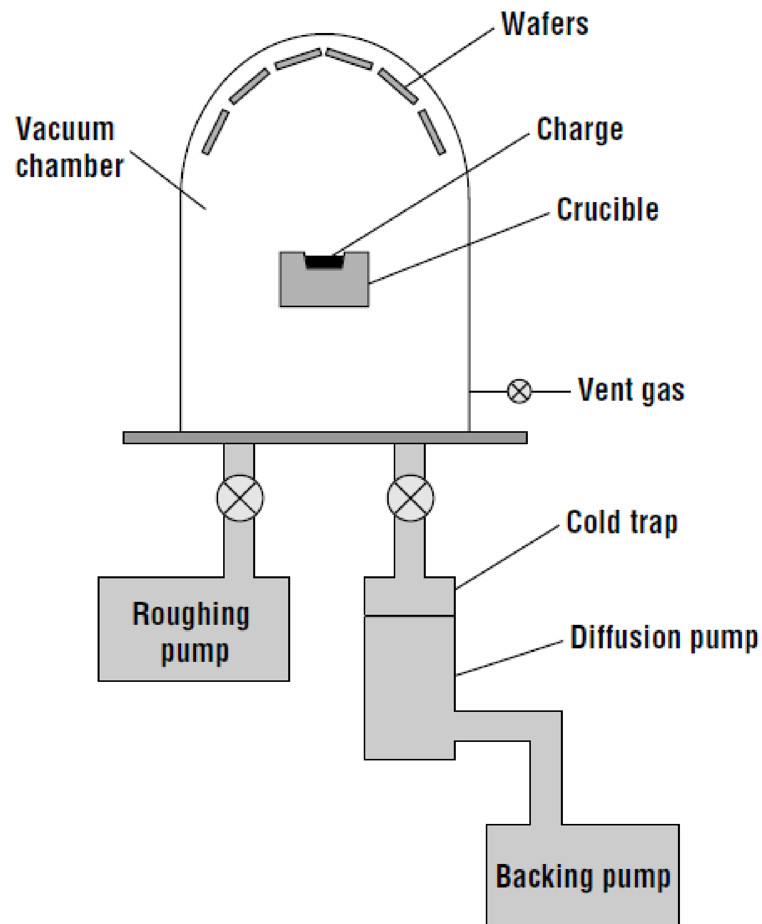


Figure 4.11: Schematic depiction of a simple thermal evaporator setup [9].

Figure 4.11 shows a simple thermal evaporator. The samples are placed in a chamber which is then pumped down to high vacuum by either a diffusion pump or a cryopump. A diffusion pump employs a cold trap to avoid streaming of pump oil vapors back into the chamber. The sample to be coated is placed above the crucible containing the evaporant and during deposition this crucible is heated until the target material starts to evaporate. The vapor then travels to the sample above the crucible and forms a coat of metal on its surface. There may be as many as four different crucibles inside one evaporator, making it possible to deposit several different metals on a sample without the need to break the vacuum when starting a new deposition. In addition, it is possible to operate more than one crucible at a time to make alloys, and up to 24 wafers can be suspended in a frame above the target material. In order to start and stop the depositions abruptly, mechanical shutters are employed.

When looking at phase diagrams for evaporation, one is interested in how the behavior of a single material depends on the temperature and pressure which the material is exposed to. All evaporations of this kind take place at pressures below 1 Torr, a range which is so narrow that any pressure effects as well as the existence of multiple solid phases can be safely ignored.

Heating the target material brings it through each phase, from solid to liquid and from liquid to gas. At every temperature there is an equilibrium vapor pressure P_e. When the heated material goes from solid phase directly to gas phase, the process is called sublimation. Evaporation is the process from liquid phase to gas phase and in semiconductor fabrication, this process usually involves molten samples where the high vapor pressures achieved through heating of the target

produce the desired deposition rate. Figure 4.12 is a diagram which shows how the equilibrium vapor pressure of a variety of different elements depends on temperature. By varying the temperature one can achieve a wide range of vapor pressures.

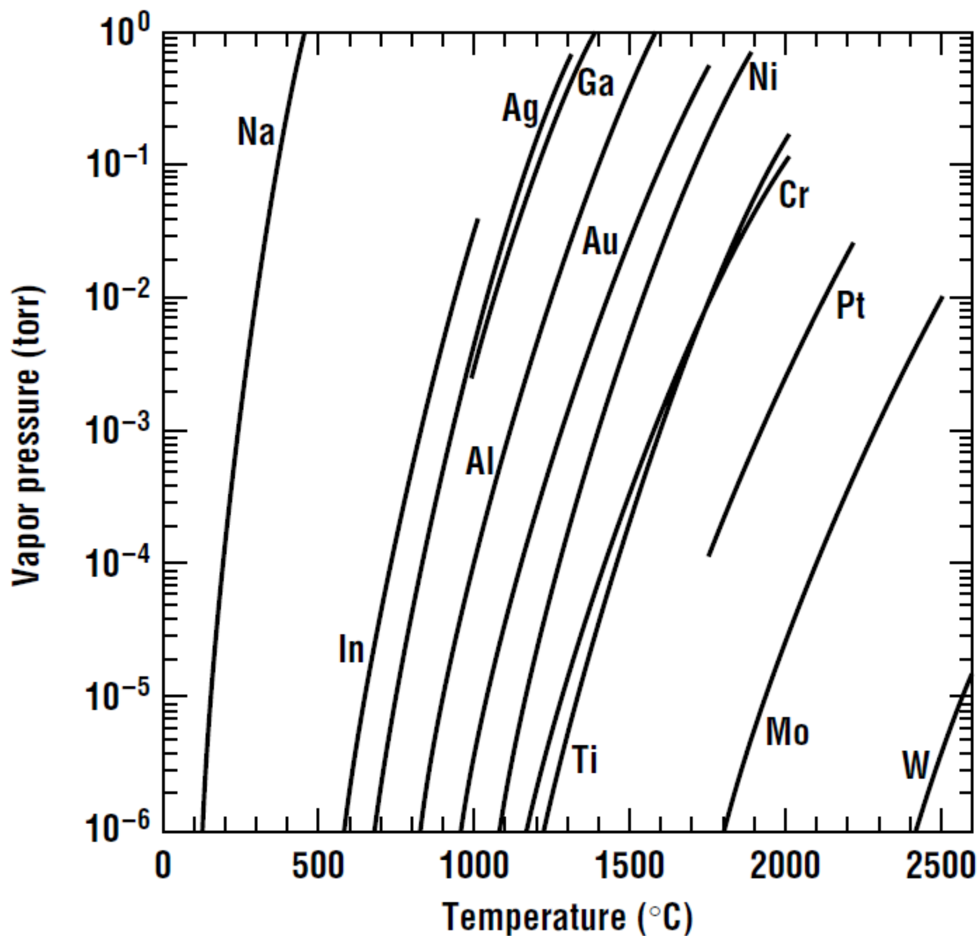


Figure 4.12: Equilibrium vapor pressure for some commonly used evaporants [9].

The vapor pressure of a liquid target material is given by the formula:

$$P_e = 3 \times 10^{12}\ \sigma^{3/2} T^{-1/2} e^{\Delta H_v/NkT} \tag{4.1}$$

Where σ is the surface tension of the evaporant, ΔHv is the enthalpy of evaporation, T is the temperature, k is Boltzmann's constant and N is Avogadro's number. The vapor pressure of the evaporant needs to be at least 10 mTorr in order to get an acceptable deposition rate. Some metals have to be heated up to very high temperatures to achieve a sufficiently high vapor pressure; some examples are Ti, W, Ta and Mo. These belong to a class called refractory metals and because of their high melting points; they have low vapor pressures at low to moderate temperatures. Tungsten, for instance, has to be heated up to 3000 °C to reach a vapor pressure of 10 mTorr. Evaporating this class of materials means special equipment is required. Depositing a material such as aluminum is far easier as this metal will reach a vapor pressure of 10 mTorr at just 1250 °C.

Thermal evaporation makes use of three different kinds of heating methods, namely, resistive, inductive and electron beam systems. The simplest of these is the resistively heated system. If we

have a high vacuum chamber with power feedthroughs, an evaporator can be constructed by using just a small coil and a simple variable transformer. Here, the charge (evaporant) is a solid bar placed upon the heated element (figure 4.13A). To avoid the charge becoming molten - causing it to drip through the coil –adjustment of the input power is necessary. Another way is to use a crucible which is heated resistively, such as the one depicted in figure 4.13B.

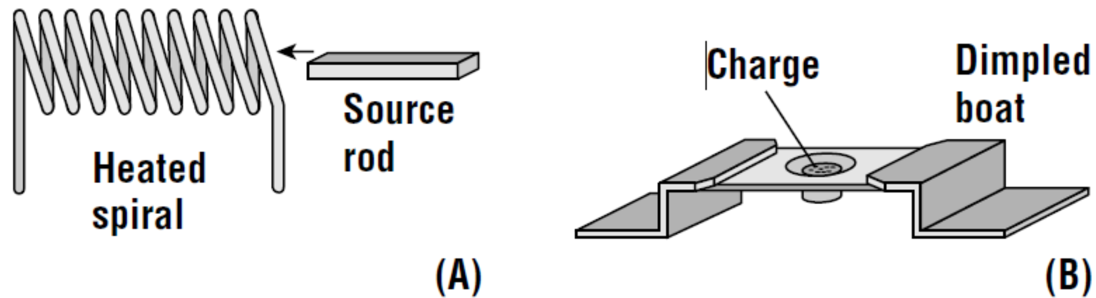


Figure 4.13: Sources used in thermal evaporation by resistive heating. Figure A shows a rod and a heating coil of refractory metal, while figure B shows the more commonly used boat where the source metal is placed in a dimple in the middle of the boat [9].

For deposition of aluminum, a sufficient vapor pressure can be achieved by using a relatively low power input. However, if deposition of a refractory metal is the objective, there are often no suitable heating elements that can be used for resistive heating. One of the problems with resistive heating is that the filament wire has to be at least as hot as the evaporant and this causes outgassing and evaporation of the wire material. By using inductive heating instead, temperatures high enough for deposition of refractory metals can be obtained. The source material is placed in a crucible, usually of boron nitride, and a coil is wound around the crucible. By running RF power through the coil, the crucible is heated up via induction of eddy currents. To keep the coil at a low temperature (<100 °C) it can be cooled by water, hereby preventing evaporation of the coil material.

Inductive heating can be utilized for deposition of refractory metals, but the problem of contamination of the source from the crucible itself remains. One way to counteract this effect is by only heating the charge while simultaneously keeping the crucible cool. This can be achieved through the use of an electron beam system. Such a system (figure 4.14A) consists of a wire loop of heated tungsten (W) which surrounds a thin rod of material with a high electric potential relative to the wire. The end of the rod is heated by electrons boiling off the wire which in doing so impacts the material rod, thereby producing an atomic beam. When using thermionic emission electron guns, the chamber will be contaminated by the hot electron filaments. This is especially important when very high vacuums are used during operation. A disadvantage in this process is that there is a possibility of deposition of filament material on the wafer surface.

In most e-beam evaporators, an intense, high energy beam is produced by an electron gun placed under the crucible. The filament is placed in such a way as to minimize the deposition of the filament material on the wafer surface. In order to make the electron beam incident on the charge surface, the beam is bent 270° by using a strong magnetic field (figure 4.14B). By scanning the beam across the source material, a significant fraction of the surface can be melted. When the heating is done this way, the hot portion of the charge is effectively self-contained by the cooler portion.

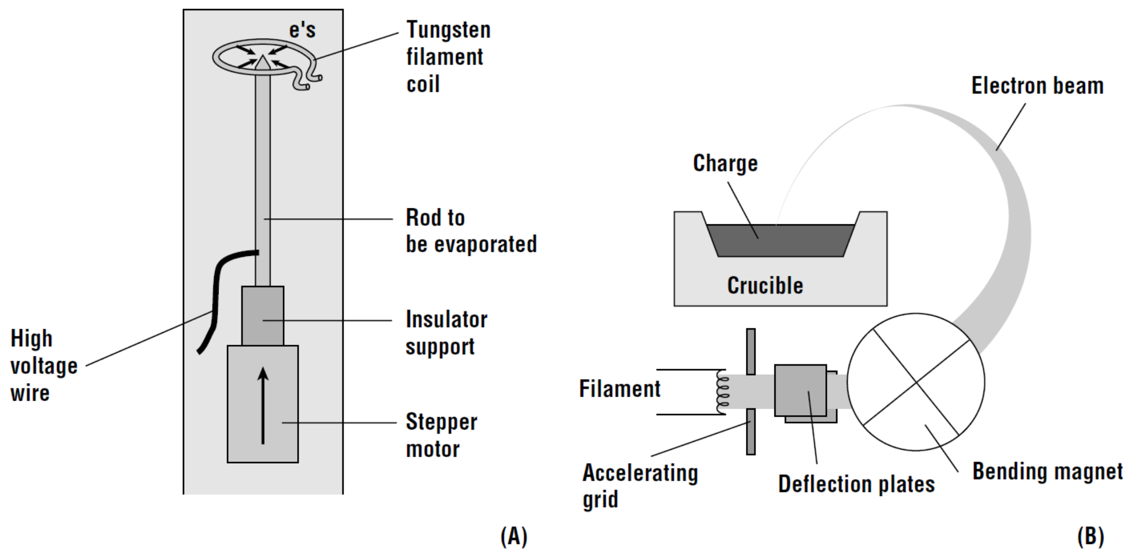


Figure 4.14: A depicts a simple, low flux system with a hot wire electron source. Figure B shows a system where the electron beam can be rastered across the source material surface via the use of a strong magnet [9].

E-beam evaporation is frequently used in GaAs technologies because of its ability to deposit a variety of different materials. For silicon technologies on the other hand, a more serious problem is radiation damage. Highly excited electrons in the evaporant decay back to core levels and the energy is conserved by emitting a characteristic X-ray photon. These generated X-rays damage both the substrate and the dielectric and this makes e-beam evaporation unsuitable for making MOS-structures unless subsequent thermal annealing is enough to remove the damage.

Multiple sources are often placed inside the evaporator, even if only one is to be used during deposition. This allows several different materials to be deposited without needing to open the high vacuum chamber. In a resistive evaporator, multiple source evaporation requires a high current switching box with heating coil for each crucible. Since the electron beam can be easily steered by using an electrostatic potential or varying the magnetic field, this makes e-beam evaporators suitable for using multiple sources in one chamber. Another way is to mount the charges on a wheel and rotate it, in this way moving the source material into the beam [9].

4.1.4. Lithography

Lithography is the process where the geometry of the semiconductor device is defined by transferring a pattern onto the wafer through exposure of ultraviolet light. A mask with the desired pattern is used during exposure and the surface of the wafer is covered with a photoresist. The photoresist most commonly used is called a positive photoresist, which entails that the exposed regions become more soluble in the developer and hence the regions that have been exposed to radiation are removed. A negative photoresist works the opposite way. The regions that have not been illuminated are more soluble in the developer than the parts that have been illuminated, resulting in removal of the regions that have not been exposed to light. The implantation regions, the bonding pads and the contact windows are all defined by the patterns of the mask. However,

the patterns are not permanent after having been defined on the resist; they are simply replicas of the final device features. To make these features permanent they have to be transferred into the semiconductor itself. This is achieved through selective etching where unmasked portions of a layer are removed [16].

In large-scale production of microelectronic devices lithography accounts for about a third of the total cost and it is the most critical, expensive and complicated step in the fabrication process. Usually, in lithography of silicon devices, between 15 and 20 masks will be used, but for some processes as more than 20 different masks are required. While technologies for GaAs have used fewer masks in the past, the number has recently increased for these processes as well. The performance of the technique is often based on how well it produces very fine lines, but even evaluating the technique's performance is not completely straightforward. For a memory manufacturer for instance, tight control on feature size over a huge number (hundreds of billions) of transistors on each wafer and over thousands of wafers is crucially important, whereas for a researcher it might be sufficient if about half of the features fall into an acceptable range on each wafer. This is important to keep in mind during consideration of lithographic performance [9].

Exposure

Lithographic exposure of the wafer is required in order to transfer the pattern to the wafer surface. There are three important parameters to consider concerning the performance of an exposure tool: registration, resolution and throughput. Registration describes how accurately a pattern can be aligned with respect to other patterns that have already been defined on the wafer. Resolution is a measure of how small the minimum device features that can be transferred with high fidelity to the photoresist are. Throughput is simply the number of wafers that can be exposed per hour with any given technique.

The optical exposure methods are divided into two groups: Projection printing and shadow printing. In shadow printing the mask may be in direct contact with the sample (contact printing) or in close proximity to it (proximity printing).

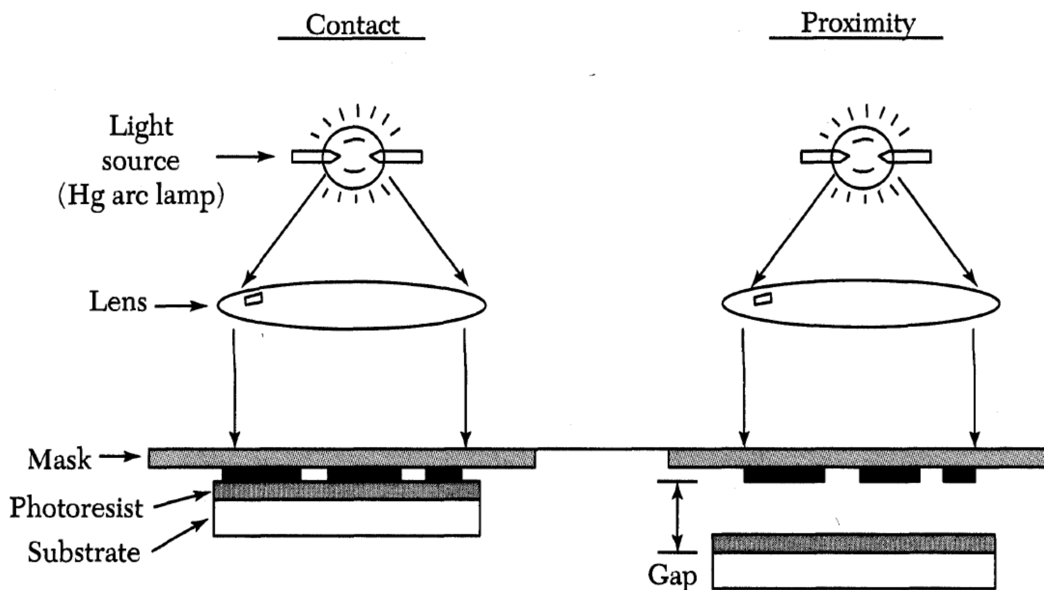


Figure 4.15: Illustration showing the difference between contact and proximity printing [16].

For contact printing, exposure is done with a nearly collimated UV light beam through the mask. A resolution of 1 μm is achieved due to the intimate contact with the mask, but a major drawback of this technique is that dust particles that are embedded into the mask during contact lead to defects in the wafer, in addition to damage to the shadow masks. More defects are added to the wafer after each succeeding exposure. The damage to the mask can be minimized by using the proximity method instead. In this setup, the exposure is performed with a 10-50 μm gap between the mask and the wafer. Though this avoids the defects associated with contact printing, it results in lower resolution. This is because the small gap gives rise to optical diffraction at the feature edges on the mask. Fringes are formed by light passing through an opaque mask feature causing some light to reach the shadow region. This degrades the resolution to around 2-5 μm.

The critical dimension (CD) for shadow printing is given by:

$$CD \cong \sqrt{\lambda g} \tag{4.2}$$

λ is the radiation wavelength and g is the gap between the mask and the sample. It is advantageous to reduce both λ and g, since this leads to a smaller CD. However, as g decreases the probability that a dust particle with diameter > g damages the mask will increase.

The other method, projection printing avoids the mask damage of shadow printing by projecting an image of the patterns onto the wafer from several centimeters away. Exposure of only a small part of the mask at one particular time ensures higher resolution, and by scanning this small area over the wafer, the entire surface is covered.

A projection lithography system has a resolution given by the following equation:

$$l_m = k_1 \frac{\lambda}{NA} \tag{4.3}$$

λ is the wavelength of the exposure radiation, k1 is a process dependent factor and NA is the numerical aperture. NA is given by:

$$NA = n \sin\theta \tag{4.4}$$

Here, n is the refractive index of the image medium which is usually air, and n is therefore equal to one in most cases. θ is the half-angle of the cone of light which converges on a point image of the wafer.

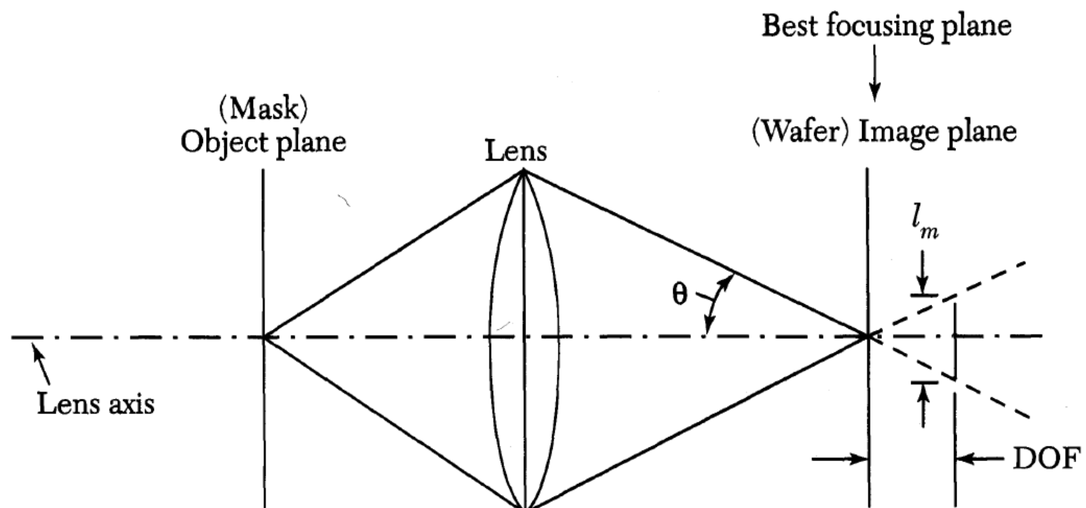


Figure 4.17: Depiction of an image system for optical lithography [16].

The depth of focus (DOF) (which is shown in figure 4.17) can be written as:

$$DOF = \frac{\pm l_m}{2\tan\theta} \approx \frac{\pm l_m}{2\sin\theta} = k_2 \frac{\lambda}{NA^2} \tag{4.5}$$

Here k_2 is another process dependent factor and all the other variables are as previously defined. The equation for resolution implies that l_m can be made smaller (and hence improved) by decreasing the wavelength, increasing the numerical aperture or both. The equation above, on the other hand, implies that the DOF will degrade far more rapidly when the numerical aperture is increased than when the wavelength is decreased. This is the reason that light sources used in optical lithography has moved towards smaller wavelengths as the technology has progressed.

The most common source in exposure tools in lithography is the high-pressure mercury lamp. More advanced tools, like the 248 nm lithographic system which has a KrF excimer laser as the light source, (the 193 nm system which uses an ArF excimer laser and the 157 nm system which employs a F2 excimer laser) have higher resolution and can be used for mass production. The resolutions for these systems are 0.18 pm, 0.10 pm and 0.07 pm respectively [15].

LED lithography

Light emitting diodes (LEDs) have emerged as a popular alternative as light sources in a wide range of applications. LEDs have low noise and high light intensity over a narrow range of wavelengths in the visible region, making them an attractive alternative to conventional lamps. In addition, LEDs have long lifetimes (10 000 h) and low cost compared to other high intensity light sources, for instance lasers. There are a range of high power near UV-LEDs available with maximum output around 365 nm; a suitable wavelength for exposure of commonly used photoresists. Although there are advantages with using LEDs (such as those mentioned above), it also has some drawbacks. The low power and small size of the beam makes exposure of large areas through a mask (as done in conventional lithography) impractical. Instead LEDs are employed without a mask and focused into a very small spot which is scanned across the photoresist, thus forming the desired pattern [17].

4.2. Characterization Techniques

4.2.1. Ellipsometry

Ellipsometry is an optical measurement technique used to determine dielectric properties and thin film thickness. The advantage of optical measurement techniques is that they are usually non-invasive. There is no physical contact with the surface and hence it usually remains undamaged after measurement. The exception would be if the sample surface is sensitive to bleaching, in which case optical measurement may impact the surface negatively. Optical measurement techniques which exploit the reflection or transmission of light include ellipsometry, interferometry and reflectometry.

Although ellipsometry has been known and used for more than century, it only became widely used in more recent times because it requires a certain amount of computer power to calculate results. The technique can be used to measure all properties of an optical system that causes the polarization of the incident light wave to change. Ellipsometry is therefore a versatile measurement technique which can be utilized in several different applications.

An example is measuring the thickness of an oxide layer on a silicon wafer. It is important to know the film thickness and this can be found by using ellipsometry. Ellipsometry has a high accuracy when very thin films are measured, providing accurate measurements in the Ångstrøm region and below. For thicker films, more calculations are necessary and the technique becomes more complex. Ellipsometry can also be applied to determine (among other things) the refractive index, the uniformity of the sample and the roughness of its surface.

Since ellipsometry measures how the polarization changes, it does not depend on absolute intensity given that the absolute intensity is sufficiently high. As a result of this, ellipsometry is both very precise and easily reproducible. Ellipsometry exploits the fact that light with linear polarization obliquely incident on a surface, changes its polarization when reflected. The name ellipsometry stems from the elliptical polarization of the incident light after it has been reflected off the surface. In some cases the incoming light has elliptical polarization to begin with. Figure 4.19 illustrates the basic idea behind the technique.

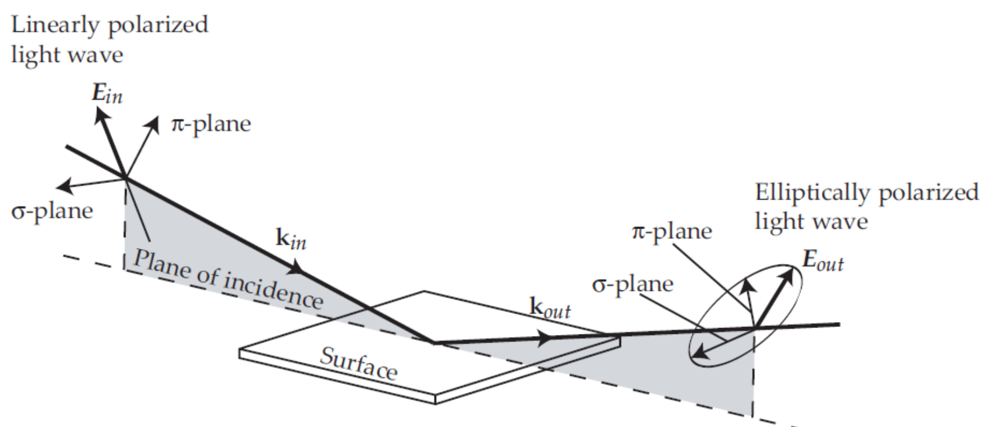


Figure 4.19: Principle behind the use of ellipsometry [18].

By directing a monochromatic, plane light wave obliquely at a surface, the plane of incidence can be defined as the plane perpendicular to the surface which contains the vector pointing in the

direction of the light wave. There are two mutually perpendicular vectors to this wavevector (denoted by $\mathbf{k}_{in}$), one for the electric field **E** and one for the magnetic field **B** of the light wave. The only one shown in figure 4.19 is the **E** vector since this is the one that defines the polarization of the wave. By decomposing **E**, one can get two components that are mutually perpendicular to $\mathbf{k}_{in}$. One of these components is parallel to the plane of incidence, while the other is perpendicular to it. They are called 'Parallel' and 'Senkrecht' (from the German word for perpendicular) and denoted by π and σ, respectively.

As mentioned, the incident light usually has linear polarization and the π and σ components can be seen as oscillating with an amplitude and mutual phase. This makes the endpoint of E move in a straight line in the plane of the two components. After the light has been reflected off the surface its polarization changes from linear to elliptical. The endpoint of E is now caused to move in an ellipse due to the change in the amplitude and mutual phase of the π and σ components. A detector registers the form of the ellipse. The ellipsometric parameters ψ and Δ can then be related to the measured form by using data processing tools. By using the relation

$$\rho = \frac{\rho_\pi}{\rho_\sigma} = \tan\psi \, e^{i\Delta} \tag{4.6}$$

the reflection coefficients ρ_π and ρ_σ can be related to the ellipsometric parameters. Here, ρ_π is the coefficient for the light polarized parallel to the plane of incidence, ρ_σ is for the light polarized perpendicular to the plane and i is the imaginary unit. The complex ratio ρ between the reflection coefficients is the basic equation in ellipsometry. Ψ and Δ are given by the measurement itself while the reflection coefficients depend on the complex refractive index of the material. A common application of ellipsometry is measuring the thickness of a thin oxide layer deposited or grown on top of a substrate (for instance SiO_2 on Si). Figure 4.20 shows the reflection and transmission of an incident light wave on the surface of a thin film. The thickness of the film can be calculated by using ellipsometry if the refractive indices of the film and substrate are known [17].

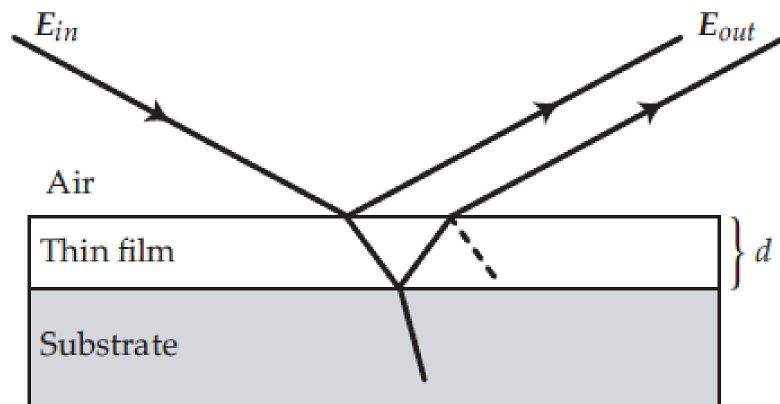


Figure 4.20: Simple illustration of reflection off and transmission through the surface of a thin film on a substrate [18].

4.2.2. X-ray diffraction

X-rays are electromagnetic waves with wavelengths of magnitude ~10^{-9}-10^{-10} m. This is similar to the distance between atoms in a crystalline structure; making x-rays a valuable tool in the study of these structures. When a crystal is exposed to x-ray radiation, the waves will be scattered in all directions, but in certain directions a higher intensity can be observed. This is caused by constructive interference between the scattered waves and since there are specific conditions for this kind of interference, it is possible to draw conclusions about the crystal structure from this information. Figure 4.21 shows how scattering of x-rays in different atomic planes would look like [19].

There are three types of x-ray scattering: photoionization scattering, Compton scattering and Thomson scattering. Photoionization happens when electrons are liberated from bound atomic states by transference of momentum and energy from incoming radiation. In Compton scattering, the energy is transferred to an electron, but unlike in photoionization, the electron is not liberated from its atom in the process. Both Compton scattering and scattering by photoionization are inelastic processes. The third type of scattering is Thomson scattering. In this case the electron oscillates with the same frequency as the incoming radiation and acts as a Hertz dipole. This causes the electron to emit radiation. Thomson scattering is an elastic process, so the momentum and hence the wavelength of the x-rays is unchanged after scattering. The Thomson component of the scattering is the one that is used when studying the structure of a sample with XRD [20].

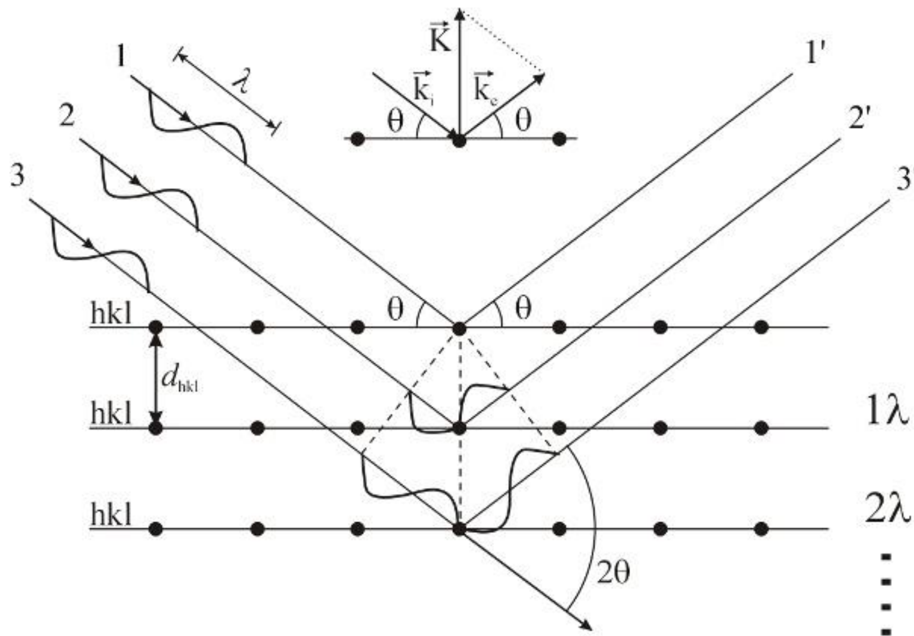


Figure 4.21: X-ray scattering in several atomic planes [19].

From this scattering (figure 4.21) the constructive interference can be derived. Given an x-ray beam with wavelength λ incident on the crystal at an angle θ with the hkl lattice planes and interplanar distance d_{hkl}, constructive interference is observed for x-rays reflected from the lattice planes at a specular angle if the difference in path length for the x-rays is an integer multiple of the wavelength. This is defined by Bragg's law and gives the following relation:

$$n\lambda = 2d_{hkl}\sin\theta \qquad (4.7)$$

Where n is an integer. For diffraction to occur from a set of planes, the normal to these planes has to bisect the angle between the incident and scattered light. If we define a scattering vector $K = k_e - k_i$ as the difference between the wave vectors of the scattering and incident x-rays respectively, constructive interference (i.e. diffraction) of the scattered rays will occur if the Bragg condition is fulfilled and if the scattering vector is parallel to the normal of the hkl-planes (figure 4.21). By observing the interference peaks that are obtained during scanning of crystalline samples, information such as lattice parameters, surface texture and strain can be extracted from the data. The broadness of the peaks will be inversely related to the quality of the crystal layer. If there are two peaks close to each other (where one is slightly higher than the other), the smaller peak is most likely caused by diffraction on the substrate surface [19].

To determine the interplanar distance d_{hkl}, one can perform a q-2q scan. This can be done in several ways depending on the orientation of the set of planes.

If a symmetric q-2q (also called θ-2θ scan) is employed (figure 4.22a), the interplanar distance of the planes parallel to the surface can be found. In this case the angle θ between the incident beam and the sample is varied while the angle between the detector and the incident beam is kept at an angle of 2θ. As a consequence, this type of scan is called a locked coupled scan. The interplanar distance can then be calculated by inserting the θ at which there is a diffraction peak into the equation above.

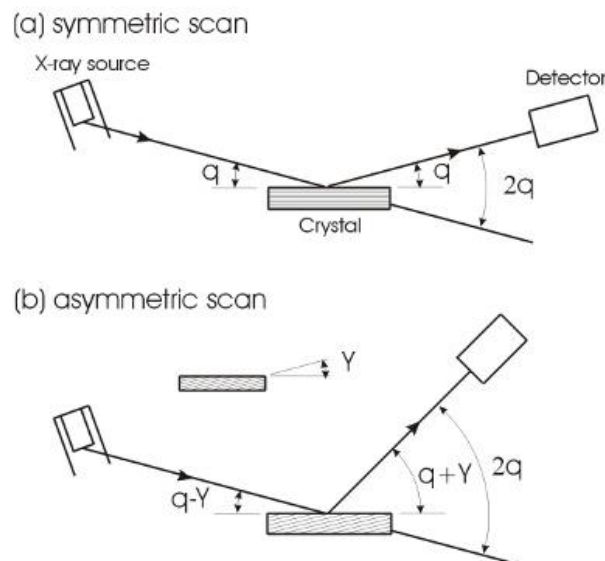


Figure 4.22: Different types of θ-2θ scans. (a) depicts the symmetric and (b) the asymmetric scan [19].

If the set of planes are tilted with respect to the sample surface, the interplanar distance can be determined by doing an asymmetric q-2q scan (figure 4.22b). Like in the symmetric scan, the angle between the incident beam and the detector is 2q in an asymmetric scan. However, the angle between the sample and the incident beam is Ψ. When scanning through q values, the q - Ψ is a fixed offset.

By determining the interplanar distance one is able to identify the different phases in the specimen. When analyzing thin films, these scans are used to find the strain and stress in epitaxial or

implanted layers. Deviations in the interplanar distance will be observed in crystal thin film, structure where stress or strain is present compared to a completely relaxed single crystal structure. This stress may be caused by impurities, lattice mismatch between substrate and the thin film or similar effects. The peak position in a q-2q scan as well as full width at half maximum (FWHM) of the 2q peak contains valuable information about the sample. For a perfect crystal, the width of the interference peak has an inverse proportionality with the thickness of the crystal film. The full width at half maximum is given by:

$$FWHM = \frac{0.9\lambda}{t\cos\theta_B} \tag{4.8}$$

This is the Scherrer formula where FWHM is expressed in radians, λ is the wavelength of the x-rays, θ_B is the Bragg angle of reflection and t is the thickness of the film. In a non-perfect crystal, such as when there long-range stacking faults or other extended defects present, there are different crystalline domains (called crystallites) with slightly different orientations. In this case the 't' in the above equation will be related to the size of these domains (i.e. the size of the crystallite particles) [19].

4.2.3. Capacitance-Voltage characterization

An important part of semiconductor fabrication is the ability to make a reliable gate insulator of high quality. To study these insulators and extract device parameters, capacitance-voltage characterization is used. The structure most commonly characterized with this technique is the metal-oxide-semiconductor (MOS) capacitor, which is basically the same as a metal oxide semiconductor field effect transistor (MOSFET), but without a source and drain. Bulk and interface charges can be calculated from the C-V data, as well as oxide thickness, threshold voltage, flatband voltage and several other important device parameters.

Capacitance is defined as the differential change in charge (Q) divided by the differential change in voltage (V):

$$C \equiv \frac{\Delta Q}{\Delta V} \tag{4.9}$$

This definition can be implemented by applying a small AC voltage to a device, measure the resulting current and derive Q by integrating the current over time. The capacitance can then be calculated from Q and V. C-V measurements are done by using two voltage sources simultaneously, a small AC voltage signal (dV_{ac}) and a DC voltage (V_{dc}) which is swept in time. In other words, the magnitude and frequency of the AC voltage remain fixed, while the magnitude of the DC voltage varies with time. By using different values for the DC voltage, different depths of the material can be sampled during measurement. The small AC signal, on the other hand, provides the bias needed to perform the capacitance measurement at a given depth in the structure [21].

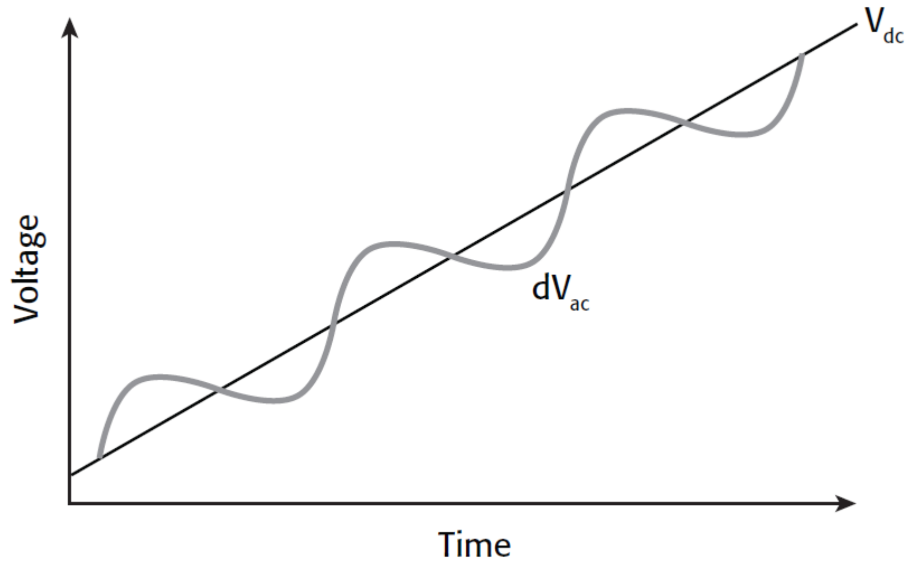


Figure 4.23: The DC and AC voltage of a CV measurement. The AC voltage is kept fixed while the DC voltage is varied with time [21].

The MOS capacitor is made simply by placing an electrically insulating layer between a semiconductor and a metal. The semiconductor and metal correspond to the plates in a parallel-plate capacitor, while the insulating layer is the dielectric. The area of the capacitor is defined by the area of the metal contact. MOS capacitors have the important property that the capacitance changes as a function of the applied DC voltage. This means the capacitor's modes of operation also change when the DC voltage is changed. As different voltages are applied to the gate, the device passes through accumulation, depletion and inversion (figure 4.24).

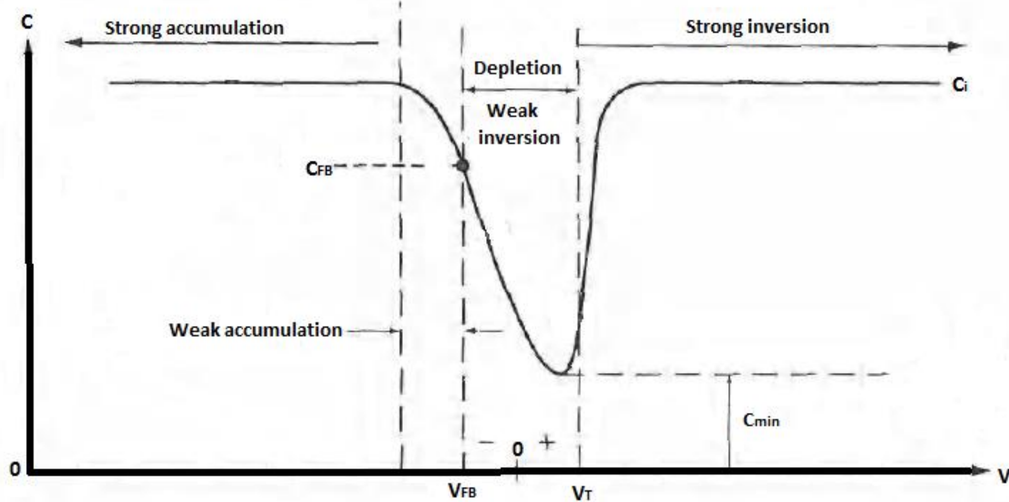


Figure 4.24: CV-curve and the different modes of operation for a MOS-capacitor: Accumulation, depletion and inversion. The dashed line for V > VT corresponds to the capacitance measured at high frequencies. Adapted from [22].

In the following, the three modes of operation will be discussed first for a p-type semiconductor, then briefly for an n-type semiconductor. The same principles apply; the differences simply consist of a reversal in polarity.

Accumulation

By applying a negative bias to the gate, the positive majority carriers in a p-type semiconductor (holes) are drawn towards the gate and accumulate in the semiconductor-oxide interface. The negative charge on the gate induces an equal positive charge in the interface, thus resulting in accumulation in the p-type semiconductor.

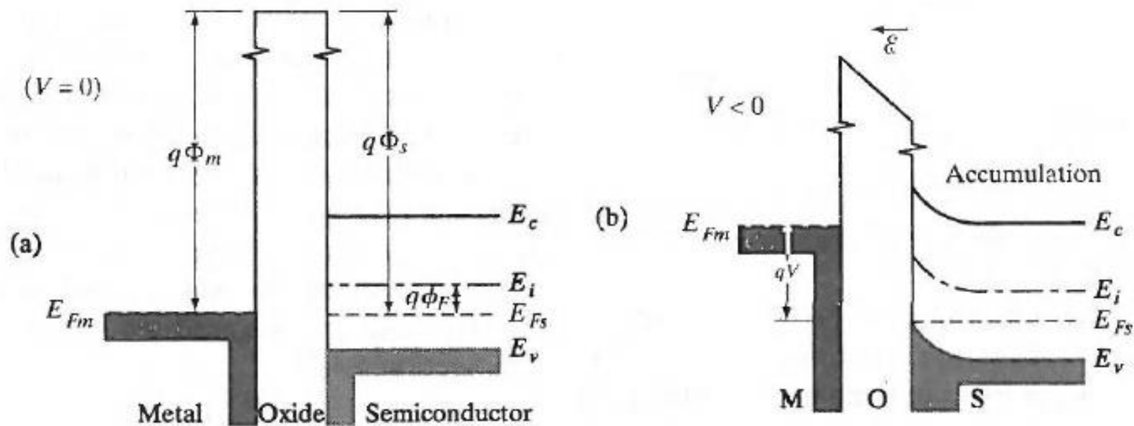


Figure 4.25: Band diagrams showing the MOS-capacitor during equilibrium (a) and accumulation (b). Equilibrium is at zero bias and accumulation happens at negative bias for p-type semiconductor [22].

When doing measurements on a p-type semiconductor, one typically looks at the strong accumulation region. Here, the voltage is negative enough to make the capacitance constant and the C-V curve nearly flat. Measurements in this region are also the ones used to calculate the oxide thickness. However, if the oxide layer is very thin, the C-V curve will not become flat in the accumulation region and the measured oxide capacitance will not be equal to the actual capacitance [21].

Depletion

If a positive bias is applied to the gate in a p-type MOS capacitor, the holes will be repulsed away from the semiconductor-oxide interface. The semiconductor surface will thus be depleted of majority carriers and we have depletion. Since this region no longer contains charge, it acts as an insulator. Therefore, the total capacitance is now the oxide capacitance and this depletion capacitance in series, resulting in a lower measured capacitance (figure 4.24). The width of the depletion region will increase when the voltage is increased, and hence the thickness of the dielectric between the semiconductor and the metal will increase, resulting in a smaller capacitance [20]. Band bending of a MOS-capacitor in depletion is shown to the left in figure 4.26.

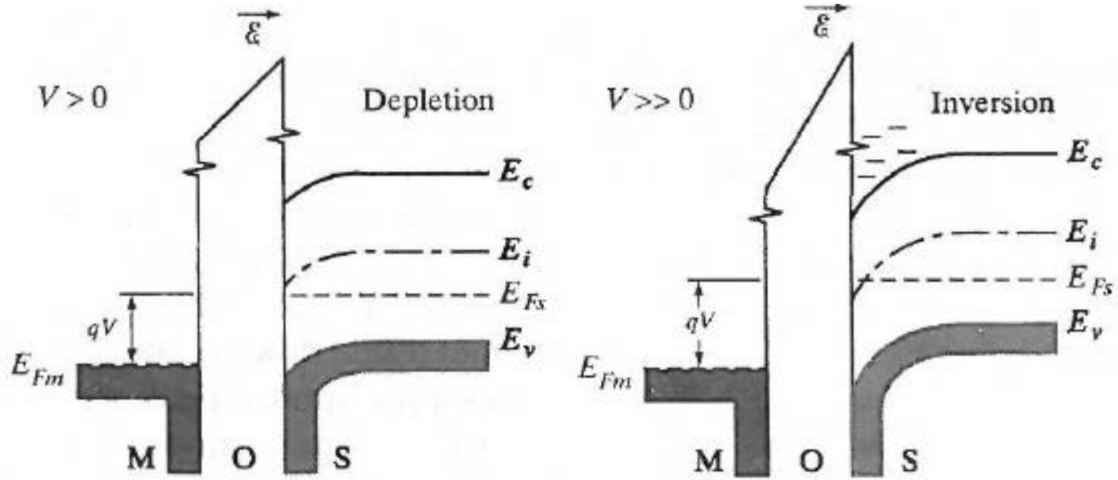


Figure 4.26: Band diagrams for a MOS-capacitor in depletion (left) and inversion (right). Depletion of holes in a p-type semiconductor happens when a positive bias is applied to the gate. If the bias is increased beyond a certain point, electrons will be drawn towards the gate, and inversion is established [22].

Inversion

By applying a higher positive bias, carriers of the opposite polarity (electrons) will be drawn towards the gate. Beyond the threshold voltage, net carrier generation of electrons is achieved in the semiconductor-oxide interface. A layer of electrons (which makes out the channel in a MOSFET) will form and we have inversion (to the right in figure 4.26). When the gate voltage has reached a certain value, increasing it further will not deplete the semiconductor further because nearly all available electrons will be in the inversion layer. As a result, the depletion region will not extend further into the semiconductor. When this maximum depth has been reached, the measured capacitance is the oxide capacitance in series with the maximum depletion capacitance. In this region the slope of the C-V curve is almost flat. To calculate the threshold voltage from C-V measurements, the following equation can be used:

$$V_T = V_{FB} \pm \left[\frac{A}{C_{OX}} \sqrt{4\varepsilon_S q |N\varphi_F|} + 2|\varphi_F|\right] \tag{4.10}$$

V_{FB} is the flatband voltage as before, A is the area of the metal contact, C_{OX} is the oxide capacitance, ε_S is the permittivity of the substrate material, N is the doping concentration and φ_F is the surface potential. The surface potential is given as

$$\varphi_F = \frac{kT}{q} \ln \frac{N}{n_i} \tag{4.11}$$

Where k is Boltzmann's constant, T is the temperature and n_i is the intrinsic carrier concentration of the semiconductor.

For an n-type MOS capacitor the curve is analogous to the one for a p-type capacitor. The differences are that the majority carriers are electrons instead of holes, the curve for the n-type capacitor is the p-type curve mirrored, accumulation happens at a positive gate voltage and inversion occurs at a negative gate voltage [21].

Measurement

Optimal results require that the measurements are done at equilibrium conditions and that one compensates for stray capacitance and series resistance.

After applying a voltage to the MOS capacitor, it will take some time before it is fully charged. Only C-V data obtained after the device has been fully charged should be saved and used for calculations. This is called the equilibrium condition. The steps to reach equilibrium are as follows: 1. Apply a “presoak” voltage before each measurement and hold the sample at this voltage for a sufficiently long time to allow the capacitor to charge up. 2. Use a time delay between each step in the voltage sweep before recording the capacitance. This ensures that the charges are able to move before the device registers the capacitance value. Both the hold and delay times are determined by looking at the capacitance as a function of time and observing how long it takes for the capacitance to settle.

Sweeping from opposite directions may result in slightly different C-V curves, but this can be minimized by adjusting the hold and delay times. One way to find adequate hold and delay times is by generating a series of curves swept from both directions. The curves should look more or less the same when they are swept from inversion to accumulation as they do when swept from accumulation to inversion.

When starting from inversion, the capacitor goes into deep depletion at first, then, after holding the starting voltage fixed for a certain amount of time, the capacitance will increase until it stabilizes to minimum capacitance at equilibrium. This, of course, presupposes that the initial hold time is sufficient to let the capacitor recover from deep depletion. Otherwise, the measured capacitance will be lower than the minimum capacitance at equilibrium. The presoak voltage is usually set to the same value as the first in the voltage sweep to avoid any abrupt voltage change when the sweep starts.

After equilibrium has been reached, a sweep from inversion to accumulation can be done relatively small delay times. As the gate voltage is reduced, the minority carriers are able to recombine quickly. However, a higher capacitance than the equilibrium value may be measured in inversion region if the delay times are too small (the top dotted line in figure 4.27).

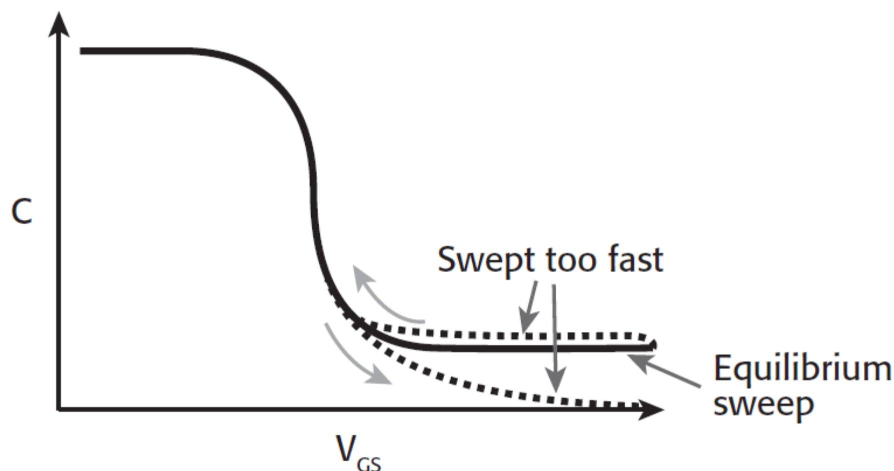


Figure 4.27: The difference between an equilibrium sweep and a sweep performed too quickly [21].

The effects of hold and delay times are more subtle when the sweep is performed from accumulation to inversion than in the opposite direction. Nonetheless, if the sweep is done too quickly, the minority carriers are unable to form an inversion layer, and on the high frequency C-V curve, the capacitor will not reach equilibrium. Instead, it becomes deeply depleted and the

measured capacitance will be significantly smaller than the equilibrium value (bottom dotted line in figure 4.27). It is faster and more controllable to generate a curve by sweeping from inversion to accumulation than vice versa.

In some cases it is necessary to compensate for series resistance after measurement. The series resistance comes either from the substrate or the backside of the wafer. For wafers manufactured in large scale fabrication units, the substrate resistance is usually quite small and can mostly be neglected. However, when using the backside of the sample as an electrical contact, there may be significant resistance because of oxide formation and this may result in a distorted C-V curve. Thus, the measured capacitance may end up being lower than it is supposed to if compensation for series resistance is not done [21].

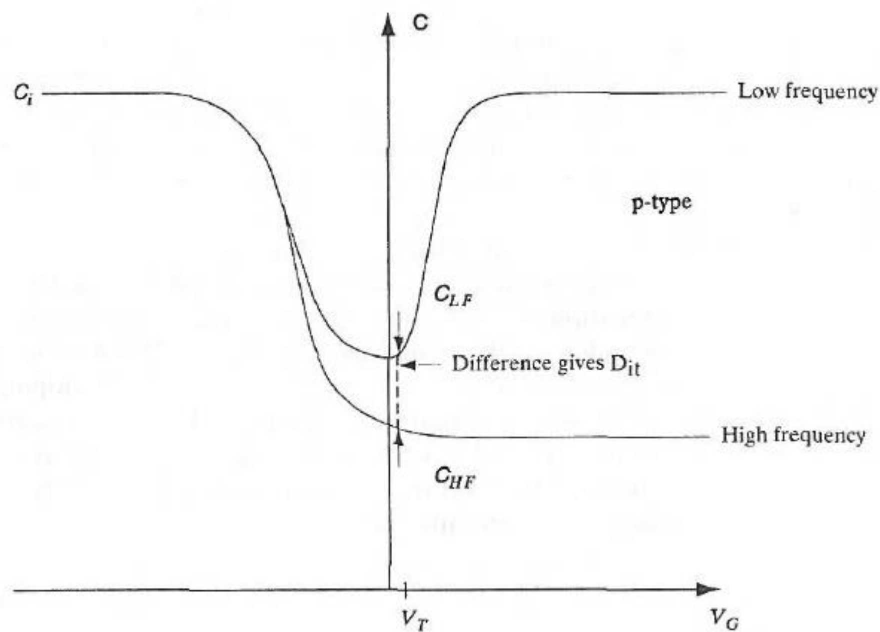


Figure 4.28: The graphs show the difference between low frequency and high frequency CV measurements [22].

In insulator-semiconductor interfaces there are often charges which give rise to interface states. Stored charge results in capacitance and these interface states results in a capacitance in parallel with the depletion capacitance, both of which are in series with the insulator capacitance. At low frequencies (1-1000 Hz) the fast interface states can keep up with variations in gate bias, but at very high frequencies (~1 MHz) they cannot. This means that the fast interface states contribute to the capacitance measured at low frequencies (C_{LF}), but not the one measured at high frequencies (C_{HF}). The shift in CV-curves measured at high and low frequencies are used to determine the density of interface charges (D_{it}) [22].

4.2.4. Current-Voltage characterization

The current-voltage characteristics can be used to calculate important transistor parameters such as field effect mobility, on-off current ratio and threshold voltage. There are two types of I-V characteristics of transistors, namely output characteristics and transfer characteristics. In the case of output characteristics, a voltage is applied between source and gate (V_{GS}) while the voltage between source and drain (V_{DS}) is varied. This voltage sweep is done at different gate voltages to

determine whether the device behaves like a transistor [3]. To obtain the transfer characteristics I_{DS} is measured as a function of V_{GS} while V_{DS} is kept at a fixed value. The transistor parameters mentioned above are calculated from the transfer characteristics.

For current to flow through the channel in a MOSFET, inversion of carriers has to be achieved. This happens when a sufficiently high voltage is applied to the gate. For instance, in an n-channel MOSFET (where the substrate is p-type) when a positive bias is applied to the gate, the carriers at the surface of the semiconductor will be repelled and this leads to a depletion of holes in this region. If the positive bias is increased further, the electrons in the semiconductor will be drawn to the surface and a layer of charges will form a channel just beneath the gate. This is inversion and the layer is called an inversion layer. The minimum voltage necessary to achieve strong inversion is called the threshold voltage. More specifically, the threshold voltage is defined as the voltage value at which the surface layer is as much n-type as the substrate is p-type. At first, after the conducting channel has been established, the source to drain current curves are almost linear, but as the drain bias increases, the voltage across the oxide near the drain will decrease and the induced charge will become smaller in this region. At sufficiently high voltages there will no longer be inversion near the drain end of the channel and the channel is said to be pinched off. At this point the current saturates and remains essentially constant even if the drain voltage is further increased. A shift in the curves is expected when the gate voltage is changed (figure 4.29).

The threshold voltage is given by:

$$V_T = V_{FB} - Q_d/C_i + 2\phi_F \tag{4.12}$$

Where V_{FB} is the flatband voltage, Q_d is the charge in the depletion region, C_i is the oxide capacitance and ϕ_F is the surface potential. The flatband voltage is the voltage necessary to compensate for band bending at the interface:

$$V_{FB} = \Phi_{ms} - Q_i/C_i \tag{4.13}$$

Where Φ_{ms} is metal-semiconductor work function difference and Q_i is the effective positive charge at the interface. From the equation for threshold voltage, in order for inversion of charges and thus channel formation to happen, first, the flatband condition has to be achieved, then the charge in the depletion region has to be accommodated for, and finally the inverted region is induced. The source to drain current is given by the equation:

$$I_{DS} = \mu_{ns}\frac{W}{L}C_i\left[(V_{GS} - V_T)V_{DS} - \frac{1}{2}{V_{DS}}^2\right] \tag{4.14}$$

μ_{ns} is the surface electron mobility (which is different from that of the bulk material), W is the channel width and L is the channel length [22].

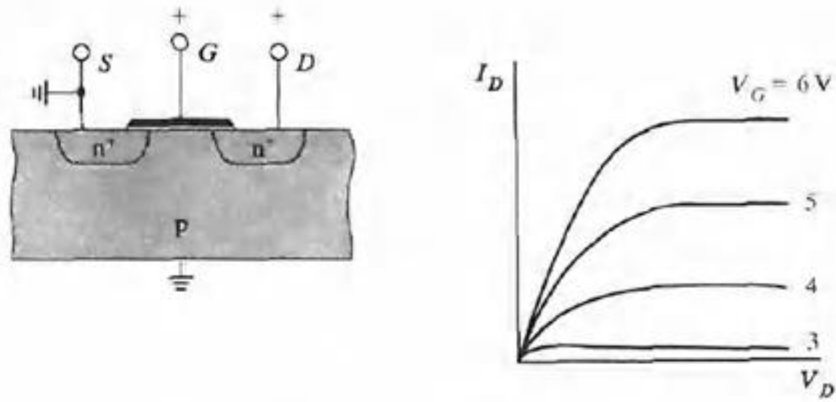


Figure 4.29: The figure shows the cross-section (left) and output characteristics (right) of an n-channel transistor. The source to drain current is shown as a function of source to drain voltage for different values of gate voltage. A device exhibits transistor behavior if there is a shift in the curves for different gate voltages such as shown in the figure [22].

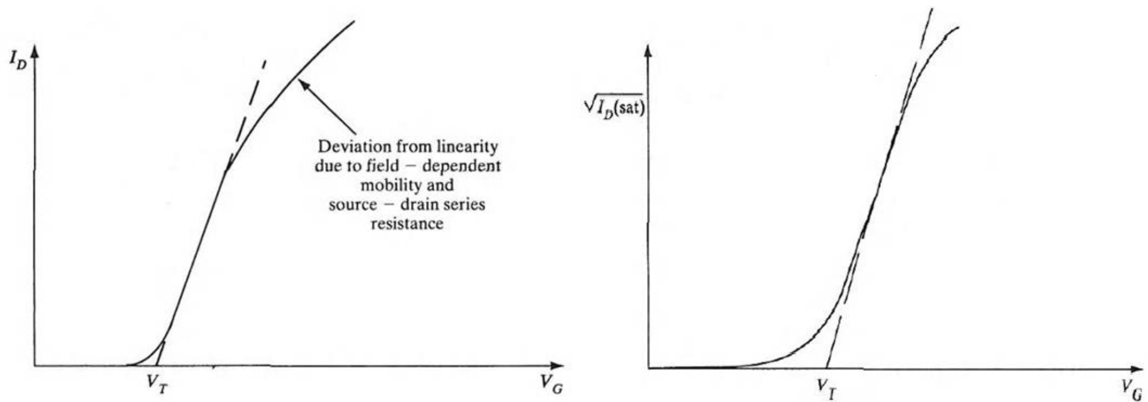


Figure 4.30: Transfer characteristics when looking at the linear (left) and saturation region (right). The top graph shows the drain current as a function of gate-to-source potential while the bottom graph shows the square root of the source to drain current as a function of the same voltage. The straight line intercepting the x-axis gives the threshold voltage in either case [22].

As mentioned earlier, the parameters used to characterize the performance of a transistor are calculated from the transfer characteristics. From looking at equation 4.14, the I_{DS}-V_{GS} curve is expected to be a (somewhat) straight line for transistors in the linear region. By extrapolating this line to the abscissa the linear region threshold voltage is obtained. In reality I_{DS} is linear only at small voltages, at higher values it increases sub-linearly. As can be seen in figure 4.30, I_{DS} shows a quadratic dependence on V_{GS} and a linear behavior is obtained by plotting the square root of I_{DS}. The threshold voltage is here determined by drawing a straight line from this plot. V_T is at the point where this line intercepts the x-axis (figure 4.30) [22].

The field effect mobility (μ_{FE}) is the mobility inferred from a measurement using a field effect transistor. High field effect mobility is desired because it determines the maximum frequency at which the transistor can be operated [23]. μ_{FE} is also extracted from the transfer characteristics and depends on the slope of the I_{DS}-V_{GS} curve. μ_{FE} is determined by looking at the I_{DS}-V_{GS} plot in either the linear (for small V_{DS}) or saturation region (for large V_{DS}) and using equation (4.14) and substituting for μ_{FE}:

$$I_{DS} = \mu_{FE} \frac{W}{L} C_i \left[(V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right] \quad (4.15)$$

This equation is from the approximate equation for a MOSFET in the linear region. Here, W is the gate width of the transistor, L is the gate length, V_{DS} is the drain voltage and C_i is the capacitance of the insulating layer. $C_i = \varepsilon_0 * \varepsilon_i / t_i$ where ε_0 is the permittivity of free space, ε_i is the permittivity of the insulator and t_i is the insulator thickness [3]. The field effect mobility is calculated from the following expression (obtained from the expression for I_{DS} above):

$$\mu_{FE} = m_{lin} \frac{L}{W} \frac{1}{V_{DS}} \frac{1}{C_i} \quad (4.16)$$

Where m_{lin} is the slope of the linear fit to the I_{DS}-V_{GS} curve [24, 25].

The on/off current ratio is simply the ratio of the maximum I_{DS} to the minimum I_{DS} as a function of V_{GS} and needs to be large in order to make the transistor work as an on/off switch. The maximum I_{DS} generally depends on the semiconductor material and on how effective the capacitive injection of the field effect is, whereas the minimum I_{DS} is usually given by gate leakage current (I_G) or the noise level of the measurement equipment [1].

5. Experimental

5.1. Synthesis and characterization of metal-oxide-semiconductor structure

An insulating layer (either SiO_2 or Si_3N_4) was deposited with plasma-enhanced chemical vapour deposition (PECVD) on wafers of <100> silicon with a resistivity of 3 Ωcm. Before deposition the wafers were cut with laser into squares about 3cm x 3cm in size. After this they were cleaned by using the RCA process in order to remove organic contaminations, any developed oxide layer or ionic contaminations. At first, the wafers were submerged in a solution of NH_4, H_2O_2 and water with a ratio of 1:1:5 holding a temperature of 75 ^oC for 10 minutes. Subsequent etching with dilute HF was done to remove the oxide layer. A solution of 1 part HF and 50 parts water was used and the samples stayed in the acid bath for 15-20 seconds. Finally, the wafers were cleaned in a solution of HCl, H_2O_2 and water with a ratio of 1:1:5 maintained at a temperature of about 75 ^oC for 10 minutes. The samples were then rinsed with water and dried with nitrogen before loading into the reaction chamber of the PECVD reactor. Depositions of silicon nitride and silicon oxide were done at different temperatures, pressures and power to explore the influence of the process parameters on the properties of the insulating layer. As a starting point, temperature, power and pressure was fixed at 300 ^oC, 30 W and 800 mTorr respectively for SiO_2 growth and 300 ^oC, 30 W and 650 mTorr, respectively for Si_3N_4, as recommended as the optimized conditions for the PECVD chamber from the manufacturer. The temperature was varied between 260 and 340 ^oC in steps of 20, the power between 20 and 40 W in steps of five and the pressure was varied from 700 to 900 mTorr for SiO_2 and 550 to 750 mTorr for Si_3N_4, in steps of 50 for both, keeping all other process parameters as constant. After deposition the samples were measured with an Ellipsometer to determine the thickness of the layer and its refractive index. The samples were also characterized by XRD. Figure 5.1 shows a typically XRD spectra of SiO_2 and Si_3N_4 deposited on Si(100). No diffraction peaks can be observed for SiO_2 or Si_3N_4, meaning the films are amorphous in nature. All the samples, show similar spectra, except that the intensity at 2theta = ~ 33 degrees, varies for Si_3N_4/Si(100) depending on the process parameters. It has been identified as the surface damage in Si wafer.

To be able to use the same samples later on when making transistors, they were cut into pieces of 1cm x 1cm. The next step in making the MOS structure to characterize the electrical properties of the insulating layer, was deposition of the metal, in this case aluminum. By using shadow masks of silicon with holes of different sizes (diameters 2, 1.5, 0.8 and 0.5 mm), contacts were deposited on top of the insulating layer. The shadow masks were fabricated by using a laser cutter on silicon wafers. To ensure smooth holes the masks were etched in a mixture of 25 parts CH_3COOH_3, 16 parts HNO_3 and 2 parts HF. Certain tolerance limit was provided for the hole size during laser cutting, in order to achieve the desired size after etching process. A layer of about 100 nm Al was deposited on all samples. The MOS structure was then characterized with capacitance-voltage measurement. Two types of C-V measurements were done, one at single fixed frequency and another at six different frequencies. This was to determine the concentration of fixed charges in the insulating layer from the shift in the C-V curve between higher and lower frequency.

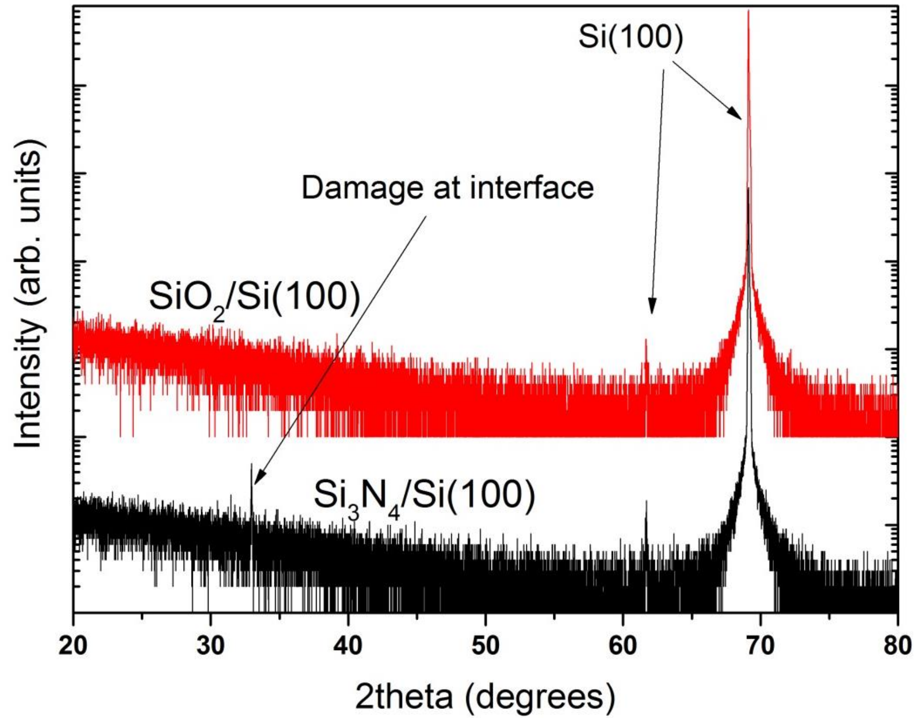


Figure 5.1: Typically XRD spectra of SiO_2 and Si_3N_4 deposited on Si(100) by PECVD.

5.2. Synthesis and characterization of bottom gate ZnO thin film transistor

ZnO films were deposited $SiO_2(Si_3N_4)$/Si(100) by MOCVD operating in a vector flow epitaxy mode, so that the group II and VI precursors are fed over the substrate surface separately, over a rotating susceptor platen (see section 4.1.2). In short, the reactor is equipped with radial/tangential injectors for introducing group II/VI species, respectively and corresponding tangential exhausts orthogonal to the group VI injector. The platen rotation directs gases across the substrates and out through separate exhausts. As a result, an advantage of alternative dosing of the substrates with group II / VI precursors and their full consumption prevents pre-reactions in the chamber. In addition to keeping the reactants separate, the reactor runs at nearly atmospheric pressure to encourage the efficient use of precursors by maximizing the reactant partial pressures, which simplifies the operation of the system. Substrates were cleaned using acetone and ethanol in an ultrasonic bath. Prior to inserting into the chamber, substrates were washed with deionized water and dried in N_2. Afterwards, DEZn, N_2 gas and t-BuOH were used as the zinc source, carrier gas and oxidizing agent, respectively. The bubblers containing DEZn and t-BuOH were usually kept at 10 and 30 ^{o}C, respectively, while the bubbler pressures were always maintained at 900 Torr. As mentioned, different process parameters like growth temperature, reactor pressure will influence the quality of as grown ZnO (if the precursors are fixed). Other parameters like, rotation rate, Zn/O molar ratio and total carrier gas will also influence the quality of ZnO. As shown in figure 5.2, the quality of the ZnO on sapphire substrates, can be varied from epitaxial film to preferential growth (columnar growth) to nanorods to polycrystalline films. From our earlier experience, optimized growth conditions for high quality epitaxial films were used. However, one has to note

that quality of the film will differ depending on the substrate used.

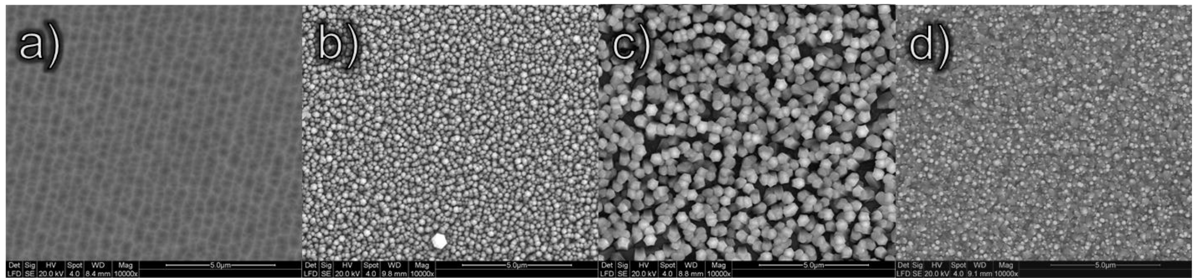


Figure 5.2: Quality of ZnO grown on c-plane sapphire substrates (top view) to be (a) epitaxial, (b) columnar preferential growth (c) nanorods and (d) polycrystalline, by varying the growth conditions.

ZnO was deposited with MOCVD on top of the insulating layer yielding a semiconductor-oxide-semiconductor structure. (Initially, two different thicknesses of ZnO (75 and 120 nm) were deposited, but since the measured difference in TFT characteristics between these two thicknesses were negligible, this has been ignored for the rest of the thesis). The growth temperature for the ZnO films was maintained at 370 ^{o}C. Hall measurements revealed a carrier concentration of ~$5*10^{17}$ cm^{-3} in the ZnO samples. The deposited ZnO films were characterized by XRD. Figure 5.3 shows the XRD spectra of ZnO deposited in SiO_2/Si(100) and Si_3N_4/Si(100) substrates. Diffraction peaks corresponding to (0002) crystal orientation of ZnO can be observed for both the samples. Additionally, no other characteristics ZnO diffraction peaks can be observed, indicating that the growth is either preferential along (0002) ZnO or epitaxial in nature. The broadness in 2theta peak could be attributed to thin ZnO layer (~ 75 nm).

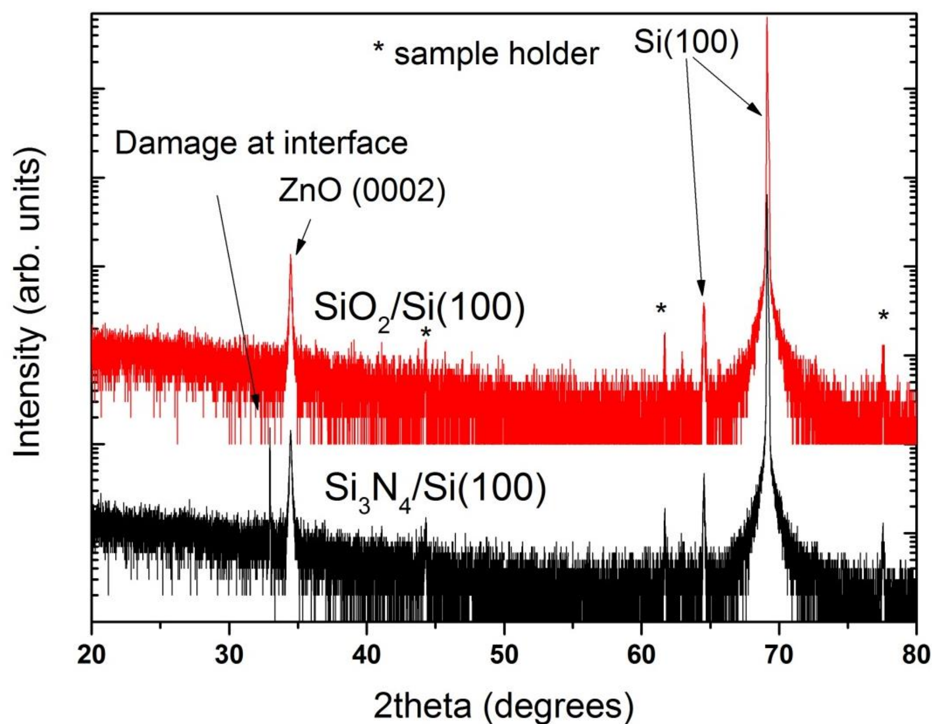


Figure 5.3: Typically XRD spectra of ZnO deposited on SiO_2/Si(100) and Si_3N_4/Si(100) substrates by MOCVD.

To form the geometry of the transistors, maskless LED lithography was employed. First a positive photoresist was spun on at 3500 rpm for 60 seconds, then the sample was baked at 120 ^{o}C for 60 seconds after which it was exposed to the LED beam in a Heidelberg maskless aligner system.

The pattern was drawn in the layout manager before exposure. Transistors with gate length of 25 µm and widths of 75, 100, 150 and 200 µm were made. In addition, there were also transistors with gate length of 50 µm and gate widths of 150, 200, 300 and 400 µm, making up a total of 8 transistors per sample. Pads of 1mm x 1mm were made in contact to the source and drain of each transistor in order to make IV-characterization more practical. Figure 5.4 shows the pattern.

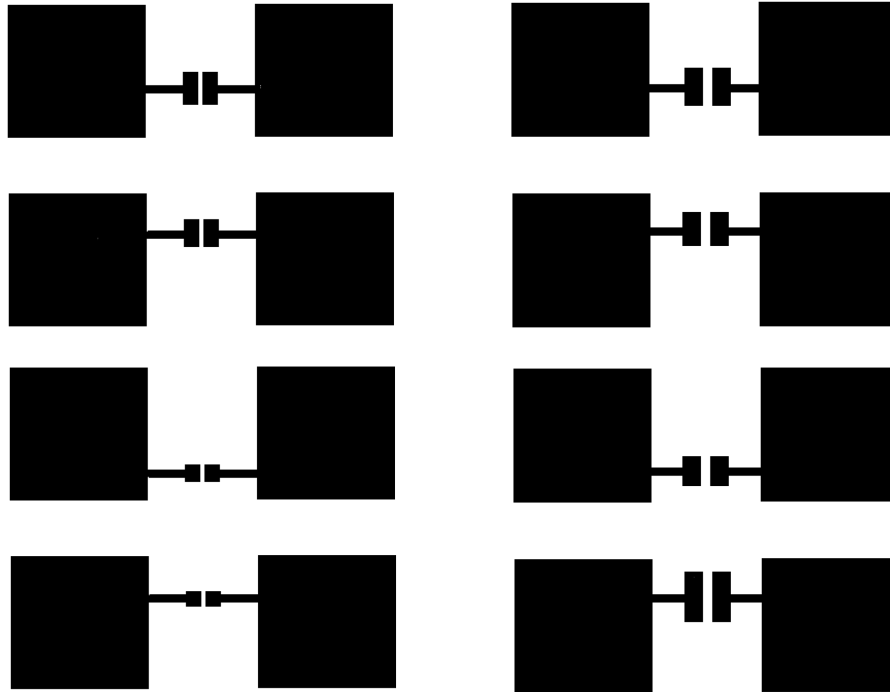


Figure 5.4: Illustration depicting the pattern. The figure shows the eight bottom gate TFTs made on ZnO. This is not the actual pattern, just an approximate schematic. To the left are transistors with gate length 25 µm and to the right are transistors with gate length 50 µm.

After exposure, the samples were immersed in a developer solution (consisting of 2 parts water and 1 part standard developer) for 60 seconds. Subsequently, they were rinsed in water for another 60 seconds and the structures examined in an optical microscope. If the structures developed were satisfactory, wafers will be transferred for the next process step, if not, the photoresist was washed off with acetone and the lithography process will be repeated. When the geometry of the devices had been defined, a layer of metal was deposited to make contacts to the source and drain. About 100 nm of gold (Au) was deposited with thermal evaporation. As mentioned earlier, Au forms ohmic contact to ZnO without any surface treatment. Lift-off was performed by rinsing the samples in acetone after deposition, thus removing the gold from the sample except on the parts that had been exposed during lithography. Transistors were made on samples with SiO_2 and Si_3N_4 deposited at different temperatures.

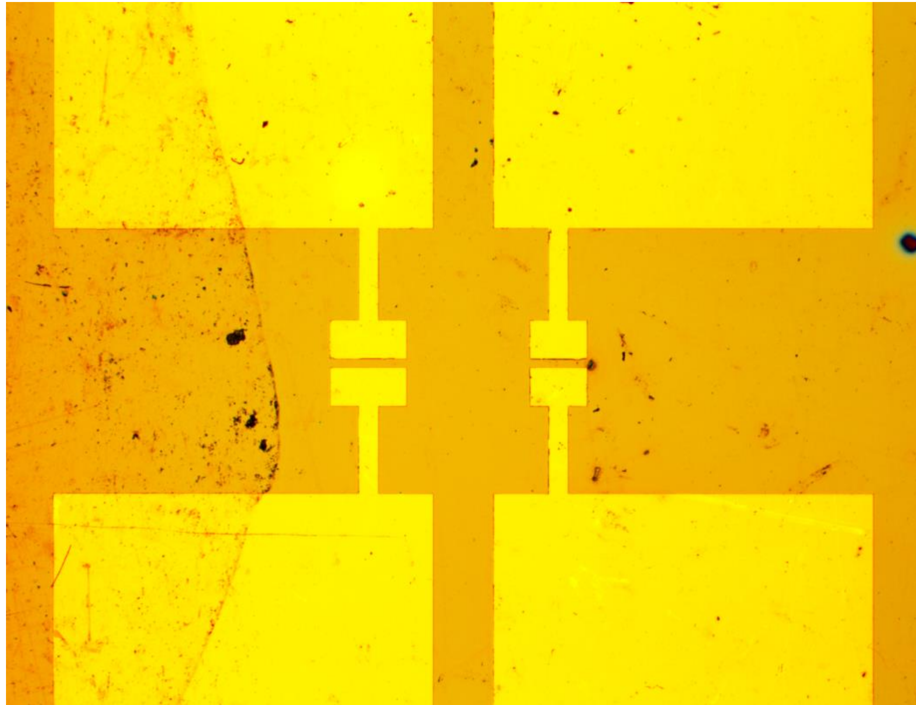


Figure 5.5: Picture taken with optical microscope of the bottom gate TFTs. The transistors in the figure have gate length 25 µm and gate width 200 µm (to the left) and 150 µm (to the right).

The fabricated transistors were then subjected to I-V characterization. To ensure connection between the backside of the sample and the measurement device, the samples were scratched with a diamond pen and a layer of Gallium Indium eutectic was put on the backside surface. The low connections of both the voltage source and the measuring device were connected to the source, while the high of the measuring device was connected to the drain and the high from the voltage source was connected to the backside of the sample, which functioned as the gate. This defined the gate potential between the gate and the source (V_{GS}). The current between source and drain (I_{DS}) was measured as a function of source drain voltage (V_{DS}). By measuring for several different gate voltages and sweeping the source drain voltage in the range of -10 to 10 V, the output characteristics of the devices were produced. To obtain the transfer characteristics V_{DS} was kept at fixed values while varying V_{GS}. The gate was swept in the range of -2 to 20 V with fixed drain voltages at -4, -2, 0, 2 and 4 V.

5.3. Synthesis and characterization of top gate ZnMgO/ZnO thin film transistor

A $\simeq$ 75 nm layer of ZnMgO was deposited employing MOCVD on top of a $\simeq$700 nm layer of ZnO grown on different sapphire (Al_2O_3) substrate (c-plane and r-plane). In addition to DEZn and t-BuOH, methyl-bis-cyclopentadienyl (M-Cp_2Mg) was used as the Mg source for $Zn_{1-x}Mg_xO$ layer using the optimized growth conditions. It has to be noted that, ZnMgO/ZnO structures were fabricated on c-Al_2O_3 and r-Al_2O_3 substrates at the same time, the quality of the films will be slightly different as the optimized conditions were for c-Al_2O_3 substrates. The Mg content in the film was estimated to be 8 % from our earlier hetero-epitaxy growth on c-Al_2O_3 with repeatability, however there will be $\pm$ 0.5% in Mg content due to different lattice mismatch at ZnMgO growth

interface. To determine crystalline properties of the samples, XRD was performed. Figure 5.6 shows the XRD 2theta scans of ZnMgO/ZnO on c-Al_2O_3 and r-Al_2O_3. Clearly, XRD indicates that growth of ZnMgO on c-Al_2O_3 is along polar- (0002) orientation, while it is non-polar- (11-20) growth on r-Al_2O_3. Additionally, no other orientations or phase separation can be observed from XRD.

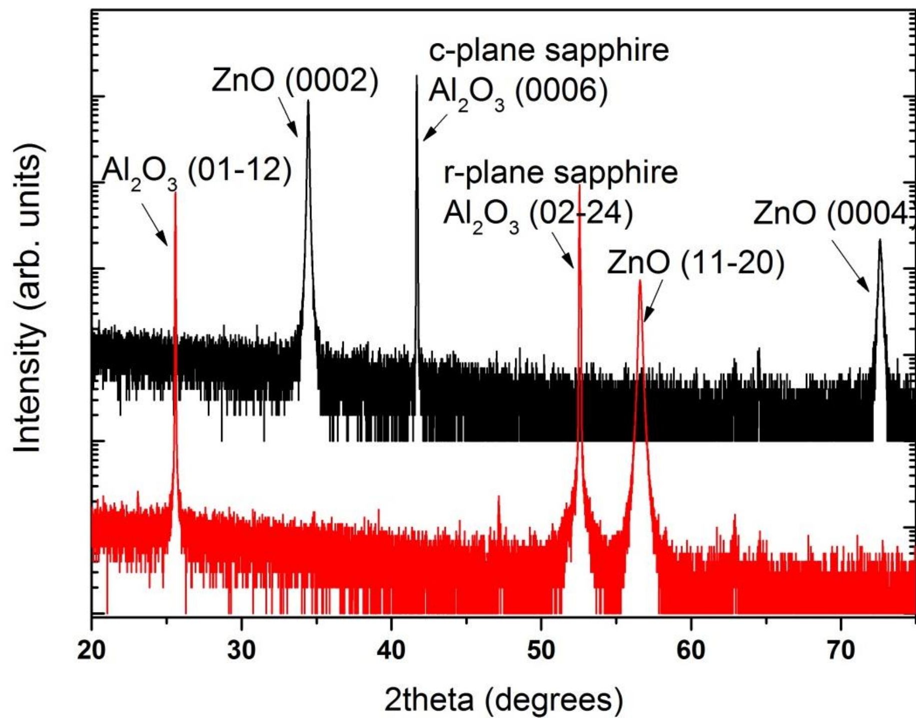


Figure 5.6: XRD spectra of ZnMgO fabricated on ZnO/c-Al_2O_3 and ZnO/r-Al_2O_3 by MOCVD

After this, the samples were split into two parts by using a diamond pen and SiO_2 and Si_3N_4 was deposited on top of the ZnMgO samples with PECVD. Depositions were made on four samples: SiO_2/ZnMgO grown on r-Al_2O_3 and c-Al_2O_3, and Si_3N_4/ZnMgO grown on r-Al_2O_3 and c-Al_2O_3. Lithography was performed to define the first part of the transistor structure.

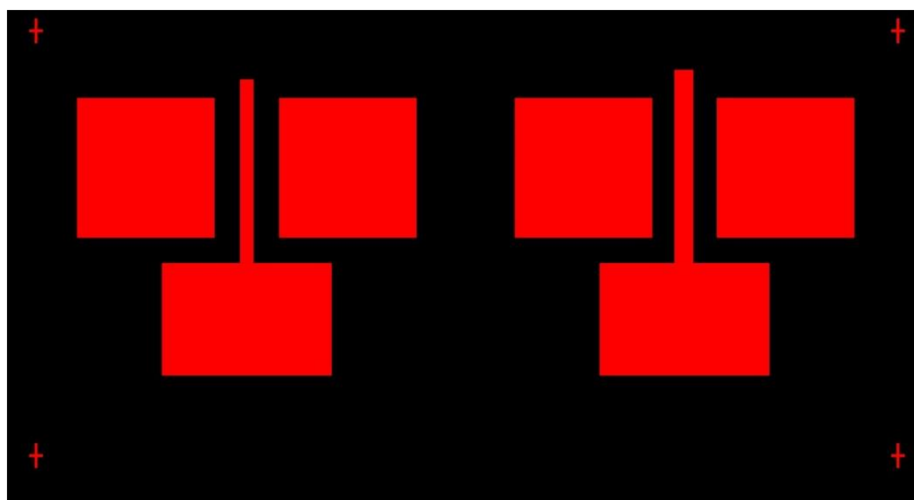


Figure 5.7: First layer of the ZnMgO/ZnO TFT taken from the layouteditor. This layer was etched into the sample before alignment was performed.

Photoresist was spun on the sample at 3500 rpm for 60 seconds which was then baked at 120 °C for another 60 seconds. The exposure was done with maskless LED beam lithography around the structure rather than on the structure itself. This was to make sure that when the following etching is performed, the oxide is left intact where the structure is (the red part in figure 5.7) and the sample is etched around it instead. When exposure had been performed the sample was immersed in development solution for 60 seconds. After this, the sample was etched with buffered oxide etchant for a total of 60 seconds and then rinsed with deionized (DI) water. When etching had been completed, the photoresist was removed with acetone before another layer of photoresist was spun on using a rotation speed of 3500 rpm for 60 seconds and another baking at 120 °C. Alignment was performed to define the rest of the structure, and then, as previously, developed in 60 seconds before rinsing with (DI) water and drying with N_2.

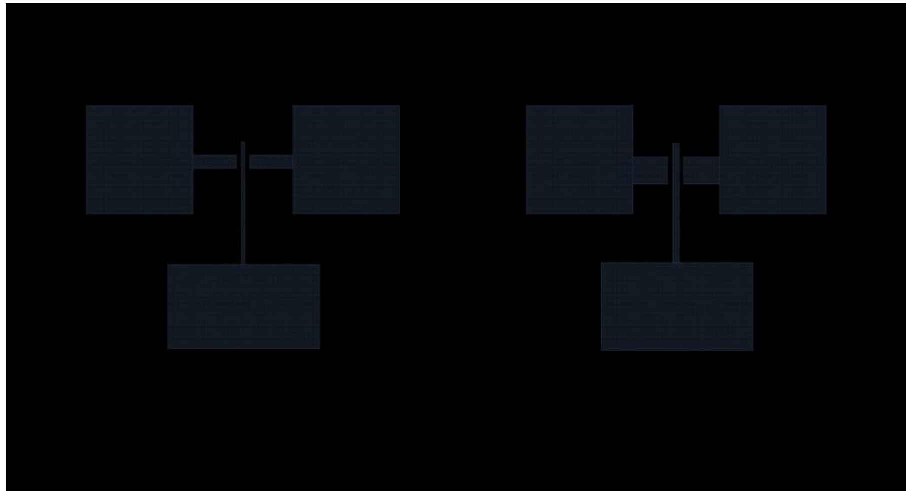


Figure 5.8: Second lithography performed on the ZnMgO/ZnO samples. This layer was aligned and exposed on top of the previous layer. Gold was then deposited on top. The transistor on the left had a gate length of 25 µm and a gate width of 100 µm. The transistor on the right had a gate length of 50 µm and a gate width of 200 µm. Pattern taken from layouteditor.

When the second lithography step had been finalized, the samples were placed in a thermal evaporator for gold deposition to make the gate, source and drain and contacts pads for all of these. Sequentially, a layer of 100 nm gold was deposited on the samples. As mentioned earlier, ZnO surface exhibits high resistive conductivity after the H_2O_2 treatment at 100 ^{o}C, suggesting that the treatment promotes a compensation effect. This enhances the rectifying behaviour of the Au contacts to ZnO. Because of this, the most probable active region in this transistor type is the low resistive 2DEG at the ZnMgO/ZnO interface. To make sure that the gold remains on the structure, the samples were baked for 1 minute at 110 ^{o}C. Finally, the gold was removed from the sample surface in a lift-off process by using acetone.

Figure 5.9 shows the structures taken with an optical microscope after processing had been concluded.

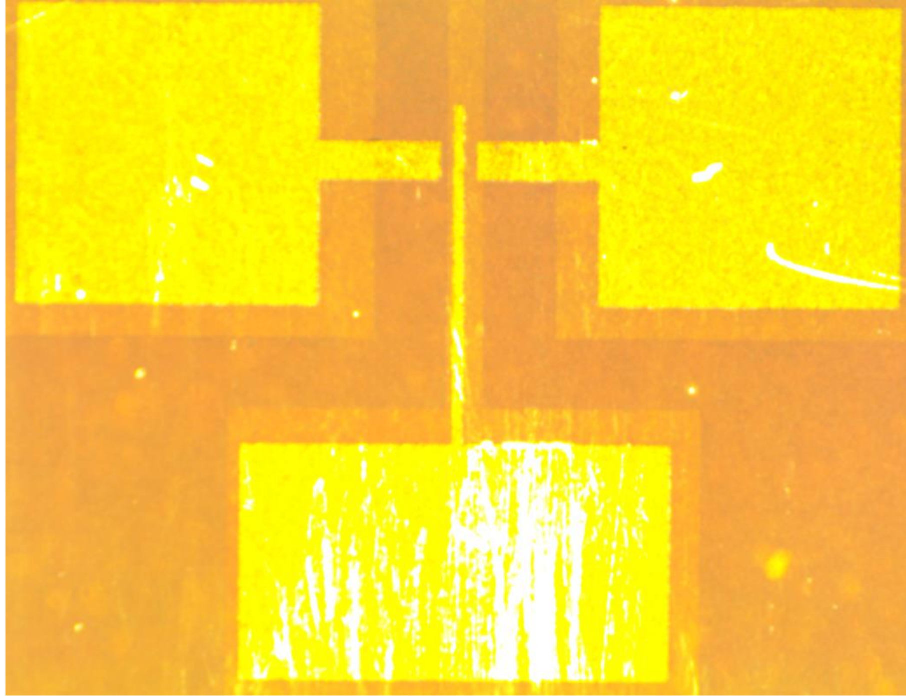


Figure 5.9: Picture taken of the ZnMgO/ZnO TFT after processing. This is the transistor with gate length 25 µm and gate width 100 µm (the left one in the two previous figures).

After transistor fabrication, the samples were measured by current-voltage characterization. Both output and transfer characteristics were obtained in order to extract the TFT performance parameters.

6. Results and Discussion

6.1. Ellipsometry measurements

The samples were measured with a Rudolph Ellipsometer to obtain the thicknesses of the deposited SiO_2 and Si_3N_4 layers and their refractive indices. This provided a way of checking how close the refractive index of the material was to the theoretical value and also to calculate the film thickness and consequently, the deposition rate. The ellipsometry measurements were performed with a wavelength of 632 nm.

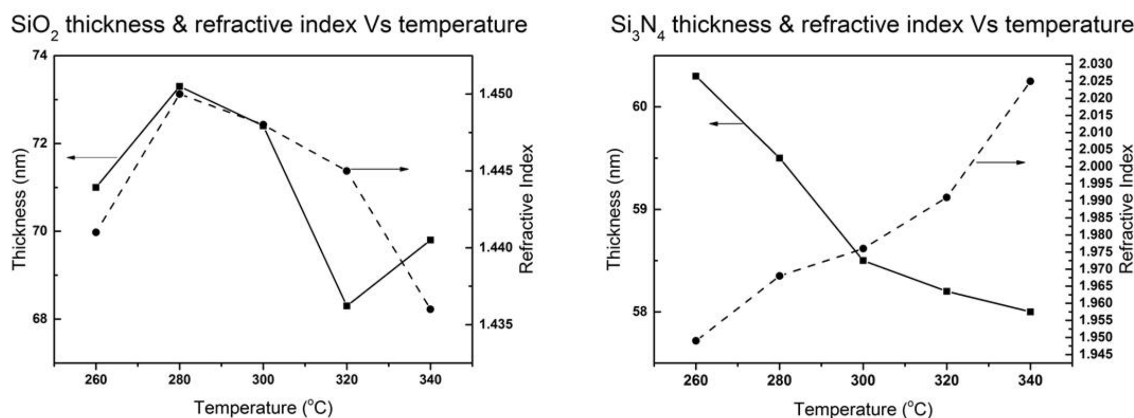
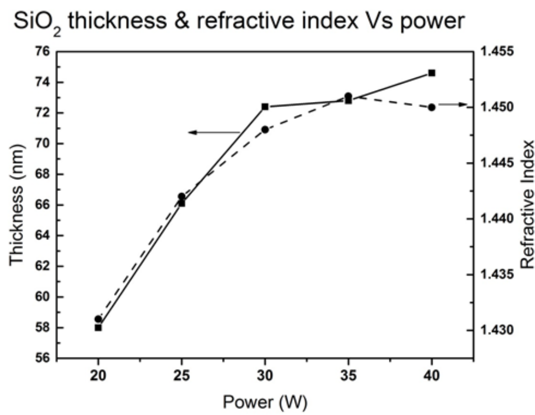


Figure 6.1: The measured thickness and refractive index of SiO_2 and Si_3N_4 as a function of deposition temperature.

The deposition time for all the depositions was 2 minutes and the measured thickness typically varied from 73 to 68 nm. The repeatability of the layer thickness measurements at different places varied between $\pm$2 nm. It can be deduced that growth temperature has only less influence on the growth rate of SiO_2 layer.

The theoretical refractive index of SiO_2 is 1.457 [26]. For all temperatures except 340 ^{o}C the measured values are somewhat close to the theoretical one (within 1% deviation), with the measured values for SiO_2 deposited at 280 and 300 ^{o}C being closest to the ideal.

Highest growth rate was for the lowest temperature. Deposition time was 7 min and the measured thickness was 58.5 nm, so the given rate for deposition of Si_3N_4 at 300 ^{o}C was 8.36 nm/ min. In literature the refractive index for Si_3N_4 is given as 2.0107 [27]. The samples with nitrides deposited at 320 and 340 ^{o}C have indices closest to this value.



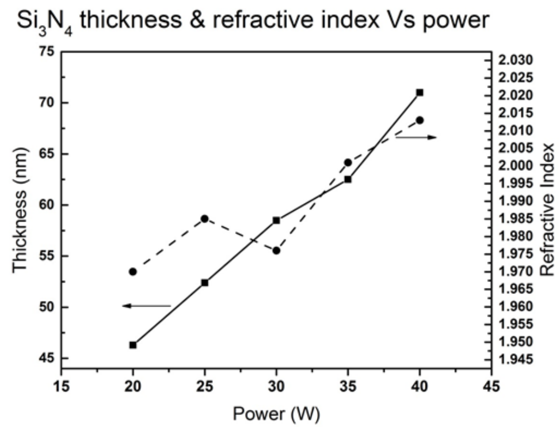
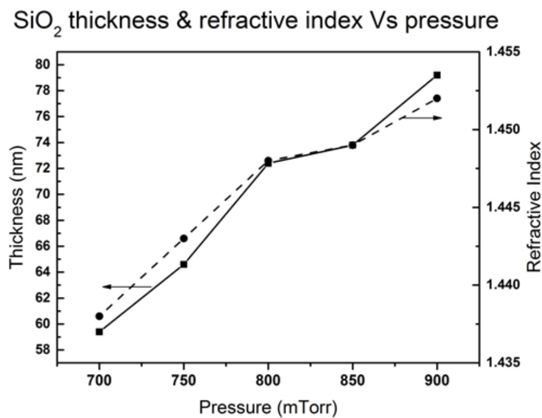


Figure 6.2: Thickness and refractive index of SiO_2 and Si_3N_4 as a function of RF power.

Increasing RF power results in higher growth rate. However, a high rate does not necessarily give the best quality layer. The oxide layers deposited at 30, 35 and 40 W have refractive indices close to the ideal values. The layer deposited at 20 W exhibits further away from ideal value.

The thickness of Si_3N_4 increases linearly as a function of RF power. Refractive indices close to the ideal occurred for depositions with 35 and 40 W. Further analysis might help to determine the optimal RF power.



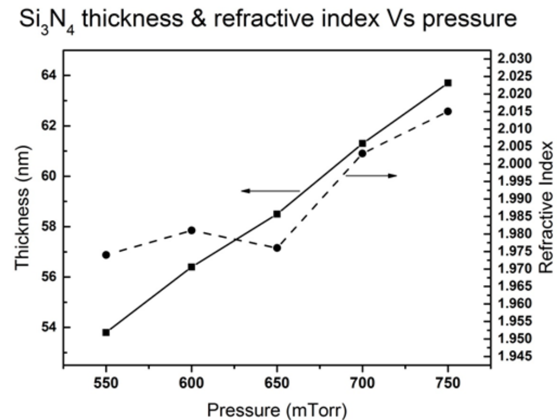


Figure 6.3: Thickness and refractive index of SiO_2 and Si_3N_4 as a function of reactor pressure given in millitorr (mTorr).

The growth rate increases with reactor pressure. The rate seems to depend on RF power and reactor pressure to a similar degree, from figure 6.2 and 6.3 it seems that reactor pressure is a slightly more decisive factor, when RF power steps of 5 W are compared with pressure steps of 50 mTorr. SiO_2 deposited with a reactor pressure of 900 mTorr has the refractive index closest to the ideal one. Analysis of C-V results in the following chapter will determine whether this is the optimal reactor pressure or not.

The curve for reactor pressure follows similar trend as for power series, but with smaller slope. In addition, the growth rate is more strongly dependent on RF power than it is on reactor pressure. However, high reactor pressure results in Si_3N_4 layers with refractive index close to the theoretical value.

6.2. C-V characterization of MOS structure

Non-ideal effects in MOS capacitors included fixed charge near the interface, trapped charge in bulk oxide and interface trap charges. All three types of charge can be identified by performing a capacitance-voltage measurement. The samples were characterized at six frequencies, but only the three highest (1 MHz, 250 000 Hz and 80 000 Hz) were deemed fit for analysis of the fixed charges in the insulating layer. The measurements done at low frequencies demonstrated enhanced capacitance. Unlike the ideal curve (shown in section 4.2.3) which will first increase then reach a constant value, the measured results showed graphs that increased to a much higher value than expected at lower capacitance before dropping (figure 6.4). Similar results have been obtained in [28] where the capacitance was shown to depend on the measurement frequency to a large degree, especially at low frequencies. This observation is attributed to the interface charges, which can follow the frequency scan at very low frequencies. The following equation shows how the oxide capacitance depends on the measurement frequency ω. G_m and C_m are conductance and capacitance measured in the strong accumulation region and dox is the insulator thickness [28].

$$C_{OX} = \frac{\varepsilon_i \varepsilon_0 A}{d_{OX}} = C_m \left(1 + \frac{{G_m}^2}{\omega^2 {C_m}^2}\right) \tag{6.1}$$

The reason is that the ions will be fixed at high frequencies, but will respond to the lower frequencies and move during measurement. For the ions to be stabilized it would take delay and hold times during measurements that were far longer than what was practical to perform. A possible remedy to this issue was to anneal the samples in an atmosphere of hydrogen. However, because the samples were to be used as transistors this was not a viable option. The hydrogen would diffuse into ZnO and degrade its properties. Since low frequency measurements are influenced by the interface trap charges at Si/SiO_2, it is irrelevant for the ZnO TFT characteristics in 'staggered configuration' during later part of the thesis, as interface defects at gate material will have no influence on the device performance and hence it is not considered for further analysis.

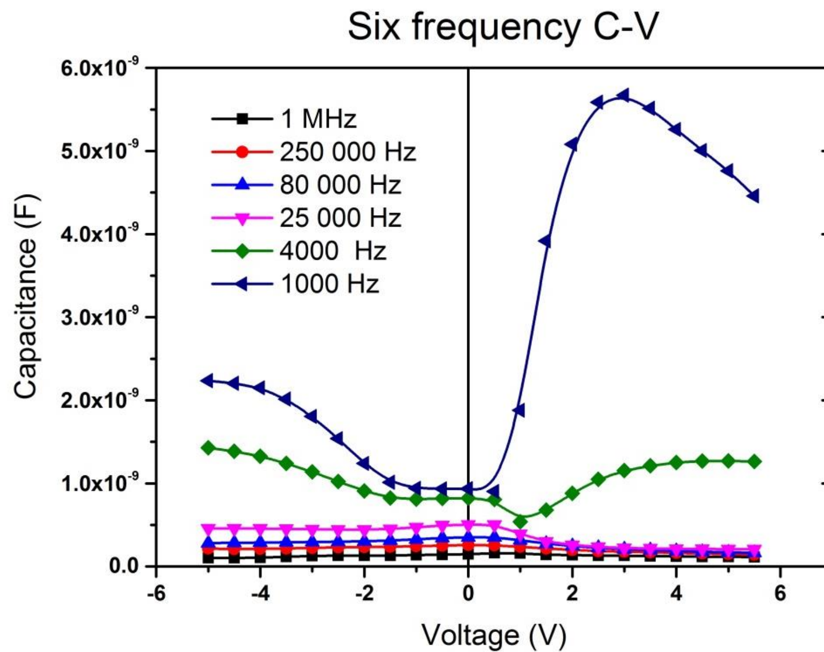


Figure 6.4: C-V curves at six different frequencies measured for MOS structure with SiO_2 deposited at 25 W.

The reason that PECVD was used in the first place is that thermal oxidation would result in higher concentration of fixed charges for highly doped p-type substrate such as the one used in this project. For silicon with low carrier concentrations, thermal oxidation would work well, but for these wafer (with $N_a \approx 10^{15}$ cm^{-3}) the dopants produce trapped charges in the insulator resulting in high gate leakage current and generally poor quality. PECVD, on the other hand, is supposed to give pure SiO_2, with less fixed charges inside the dielectric layer. However, these layers had high concentration of interface trap defects. A possible explanation for this effect could be due to the surface damage incurred by the Si wafer during the deposition process. This is also supported by the XRD results, where prominent damage is observed in Si wafer during Si_3N_4 deposition.

To ensure repeatability all the samples were measured at contacts with four different diameters: 2, 1.5, 0.8 and 0.5 mm. Since it would be impractical to include all the measurements that were done, a selection of the relevant data is included in the following sections. The best insulator, most preferably is the one that has a low capacitance and which has a curve that most closely resembles the ideal curve shown in section 4.2.3.

SiO_2

Temperature series

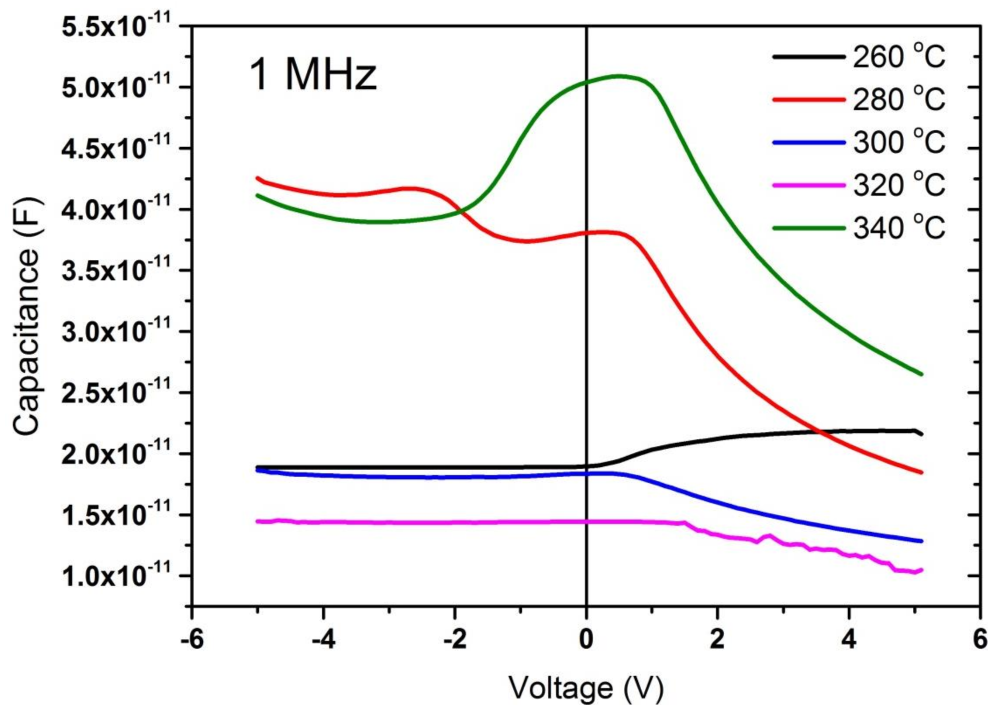


Figure 6.5: C-V curves for samples with SiO_2 deposited at different temperatures measured at a frequency of 1 MHz at contact with diameter 0.5 mm.

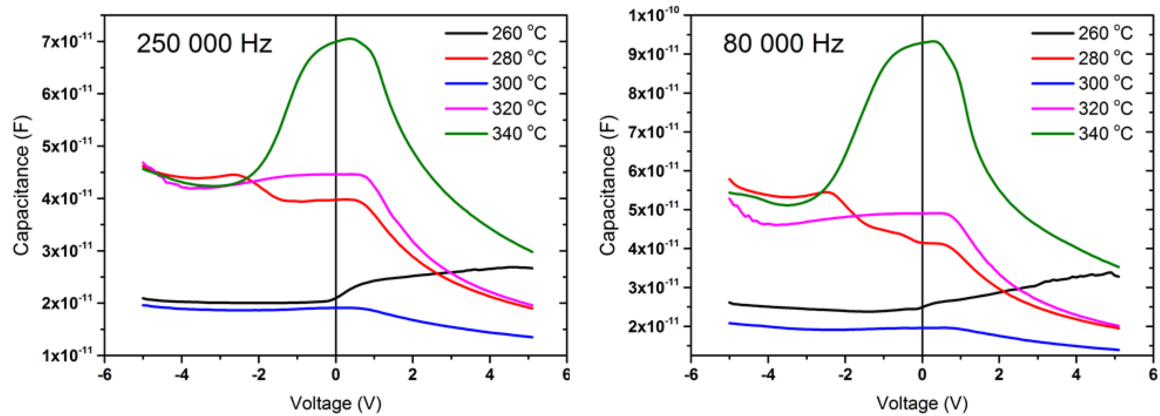


Figure 6.6: C-V curves for samples with SiO_2 deposited at different temperatures measured at a frequencies 250 000 (left) and 80 000 Hz (right). These measurements are performed on contacts with diameter 1.5 mm.

The C-V curves for SiO_2 deposited at 260 °C behaves in the opposite way of that of the curves for the other samples; it increases in the right hand side of the plot where the other curves all decreases (albeit a small decline for curves measured at samples with SiO_2 deposited at 300 and 320 °C). This behavior indicates that there are a lot of fixed and interface charges in the oxide. The curve for the sample deposited at 300° C shows low capacitance due to few fixed oxide charges compared to samples deposited at the other temperatures. If trapped/fixed charge is present inside the insulator/near the interface, it will screen a part of the applied field and thereby reduce the depletion region and result in higher capacitance. Importantly, the fixed charges will shift the flat band capacitance to the left. From looking at C-V-measurements and the results obtained from ellipsometry 300 °C was found to be the optimal temperature for deposition of SiO_2 with PECVD.

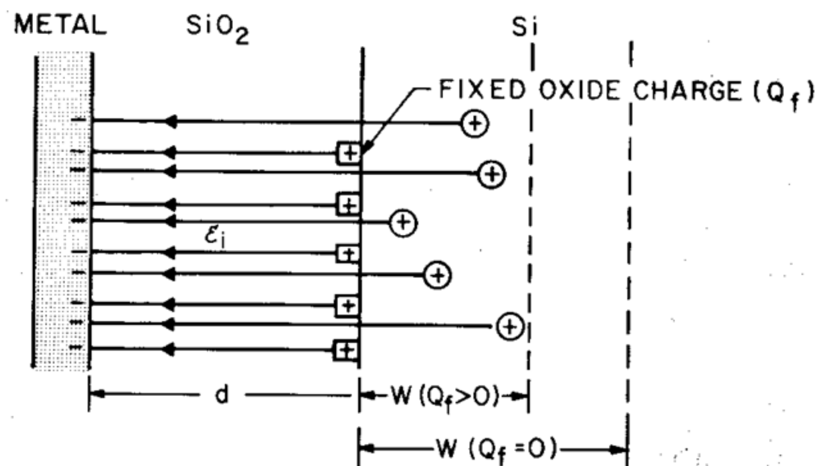


Figure 6.7: Conceptual representation on the influence of near interface fixed charges (Q_f) on the depletion width for p-type silicon.

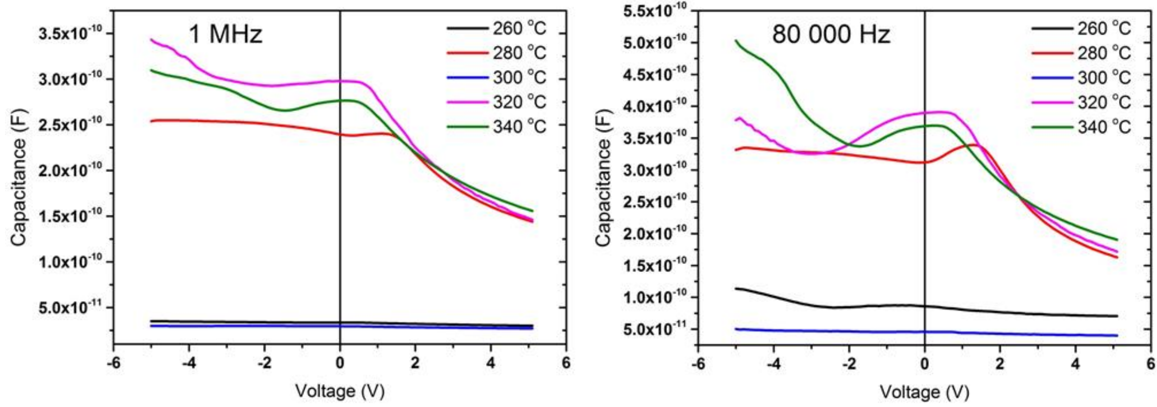


Figure 6.8: C-V curves for samples with SiO_2 deposited with different temperatures, measured at frequency 1 MHz (left) and 80 000 Hz (right) on contact with diameter of 1.5 mm.

All these measurements show some of the same trend and indicate that the optimal temperature for PECVD deposition is 300 °C.

The theoretical flatband voltage was calculated as -1.14 V. Threshold voltages for the MOS structure were found by using dielectric constants calculated from the C-V measurements taken at 1 MHz. V_T for oxides deposited at different temperatures was determined by using equation 4.10 and are presented in table 6.1. The column to the left is calculated from measurements on contacts with diameter 0.5 mm; the column to the right is calculated from measurements done on contacts with diameter 1.5 mm. There was only a small variation in threshold voltage between samples with oxides deposited at different temperatures.

T (°C)	V_T (V) 0.5 mm	V_T (V) 1.5 mm
260	-0.477	-0.199
280	-0.481	-0.444
300	-0.481	-0.451
320	-0.475	-0.452
340	-0.481	-0.450

Table 6.1: Threshold voltages calculated from C-V measurements performed with 1 MHz of MOS structures with contact diameters 0.5 and 1.5 mm and SiO_2 deposited at different temperatures.

Power series

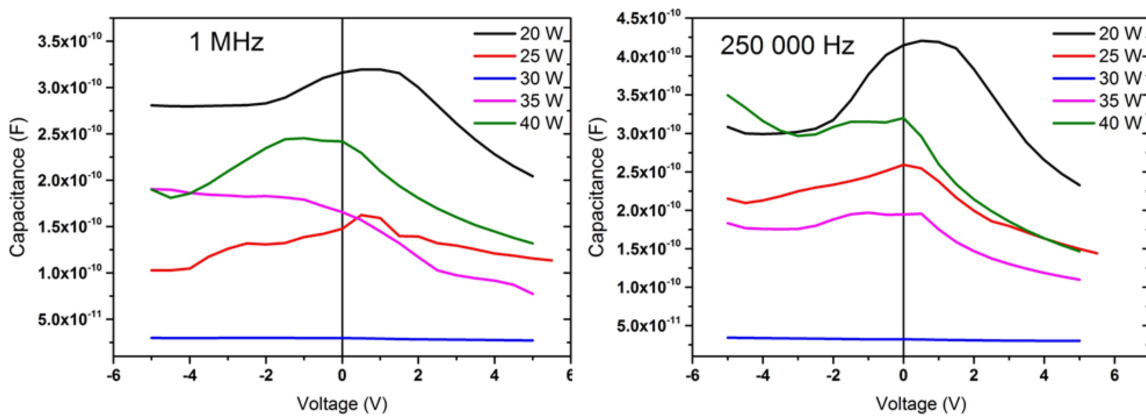


Figure 6.9: C-V curves for samples with SiO_2 deposited with different power values, measured at frequency 1 MHz (left) and 250 000 Hz (right) on contact with diameter 1.5 mm.

From these measurements it seems that depositing with an RF power of 30 W gives the best quality oxide layer.

Pressure series

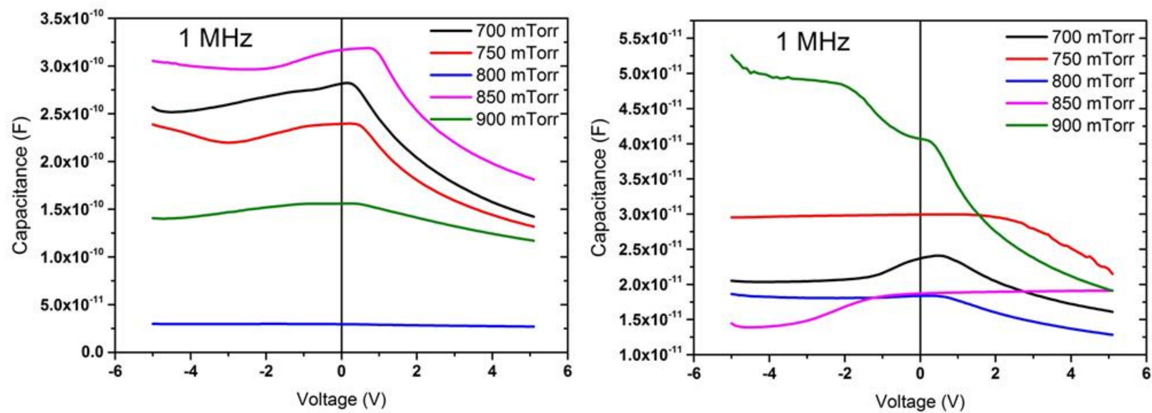


Figure 6.10: CV curves for samples with SiO_2 deposited with different pressure values, measurement frequency 1 MHz and contact diameters of 1.5 mm (left) and 0.5 mm (right).

Measurements performed on contacts with diameters 0.5 and 1.5 mm indicate that the best reactor pressure for PECVD deposition of SiO_2 is 800 mTorr.

Si_3N_4

Temperature series

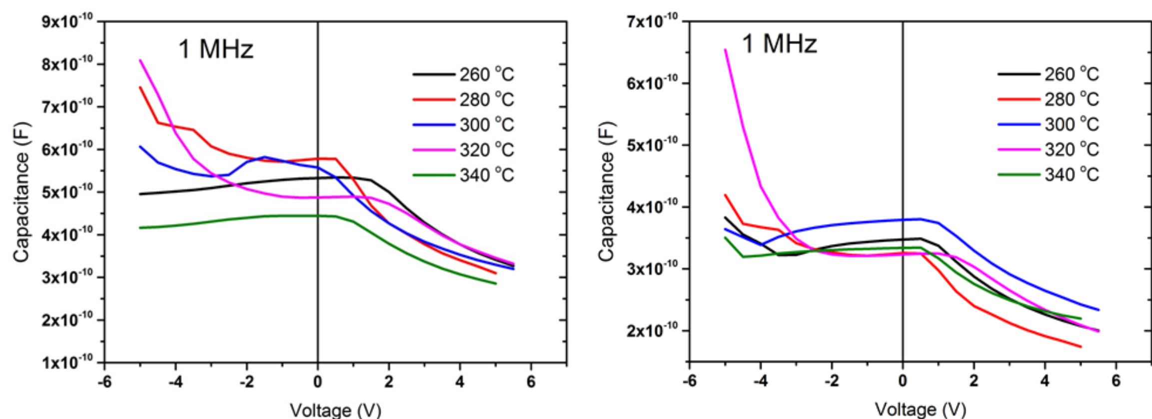


Figure 6.11: Temperature series for Si_3N_4 measured with a frequency of 1 MHz on contacts with diameters 2 and 1.5 mm.

For Si_3N_4 it was more difficult to determine from C-V measurements which temperature gave the best insulator. As can be observed in figure 6.11 the curves are almost on top of each other, thus not giving a clear picture as to which one is preferable to the others.

From C-V measurements done with 1 MHz the threshold voltages for MOS structures with Si_3N_4 deposited at different temperatures were calculated.

T (°C)	V_T (V) 0.5 mm	V_T (V) 1.5 mm
260	-0.481	-0.455
280	-0.480	-0.457
300	-0.481	-0.455

320	-0.482	-0.462
340	-0.482	-0.453

Table 6.2: Threshold voltages calculated from C-V measurements performed with 1 MHz of MOS structures with contact diameters 0.5 and 1.5 mm and Si_3N_4 deposited at different temperatures.

Power series

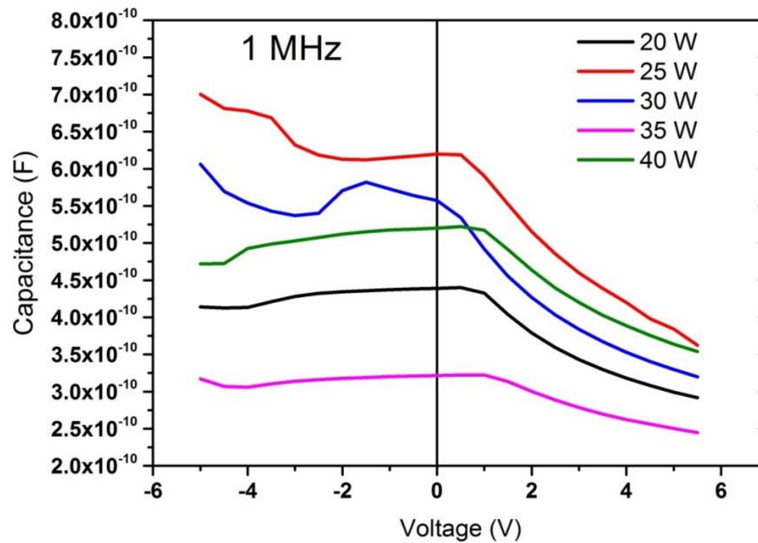


Figure 6.12: Measurement of Si_3N_4 with variation in RF power performed on contact with diameter 2 mm and measured at 1 MHz.

From analysis of these and other C-V measurements there is indication that either 20 or 35 W was the optimal RF power. However, it is difficult to say for certain given the variation in the results. In addition, since these two values are so far apart it seems more sensible not to draw any firm conclusions from the measurement of this power series.

Pressure series

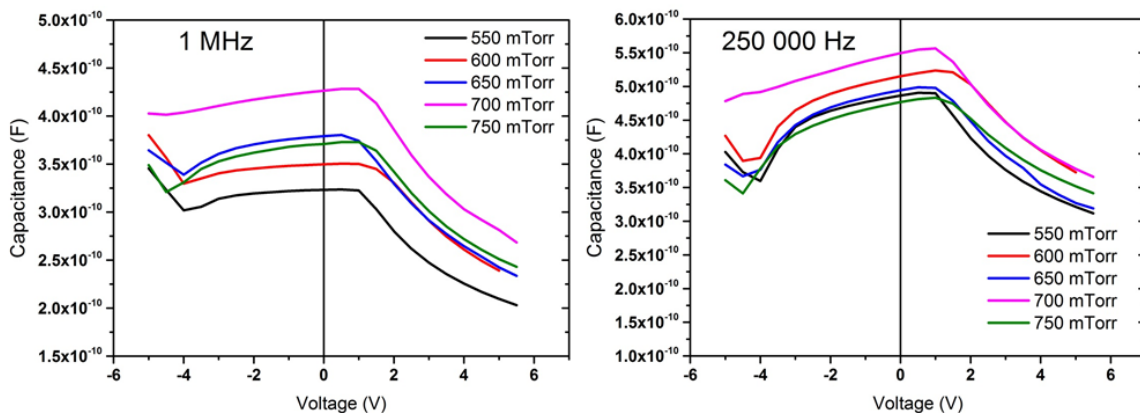


Figure 6.13: C-V measurements of samples with Si_3N_4 deposited at different reactor pressure. These data were obtained from measurements on a contact with diameter 1.5 mm and frequencies 1 MHz (left) and 250 000 Hz (right).

Also for variation in pressure it is difficult to determine which value results in the best Si_3N_4 layer.

Dielectric constant

The dielectric constant was calculated for all contacts on samples with both SiO_2 and Si_3N_4. A few graphs showing measurements done with different samples are presented in the following section. One should also note that, SiO_2 deposited at 300 °C (~10^{-11} F) has one order less capacitance values compared to Si_3N_4 (~10^{-10} F) layers. This implies that, the fixed charge density in Si_3N_4 layers is higher compared to SiO_2 layers. The fixed charge density was not calculated, as the ZnO TFT fabrication was done at 370 °C, temperature higher than insulator growth temperature, also near interface fixed charge will be altered during ZnO growth. The theoretical values for the dielectric constants of SiO_2 and Si_3N_4 are 3.9 and 7.5 respectively [29]. As can be seen in the figure 6.14, SiO_2 deposited at 300 and 320 °C shows the smallest variation in dielectric constants when comparing measurements done at different frequencies. Since the mobile charges will move at low frequencies, but not at high, this indicates lower concentration of these charges in oxides deposited at 300 and 320 °C than other temperatures.

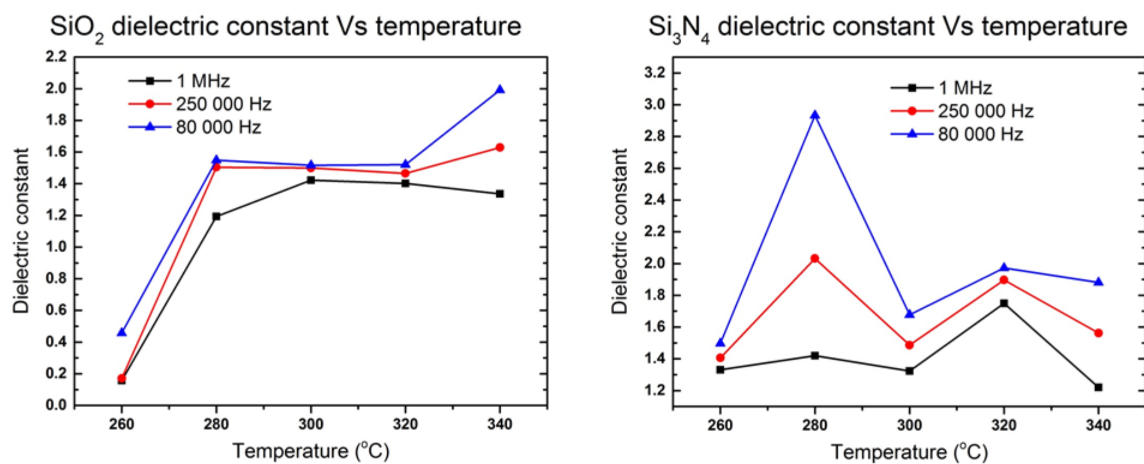


Figure 6.14: Dielectric constant as a function of deposition temperature for SiO_2 (left) and Si_3N_4 (right). Calculated from measurements performed on contacts with diameter 1.5 mm.

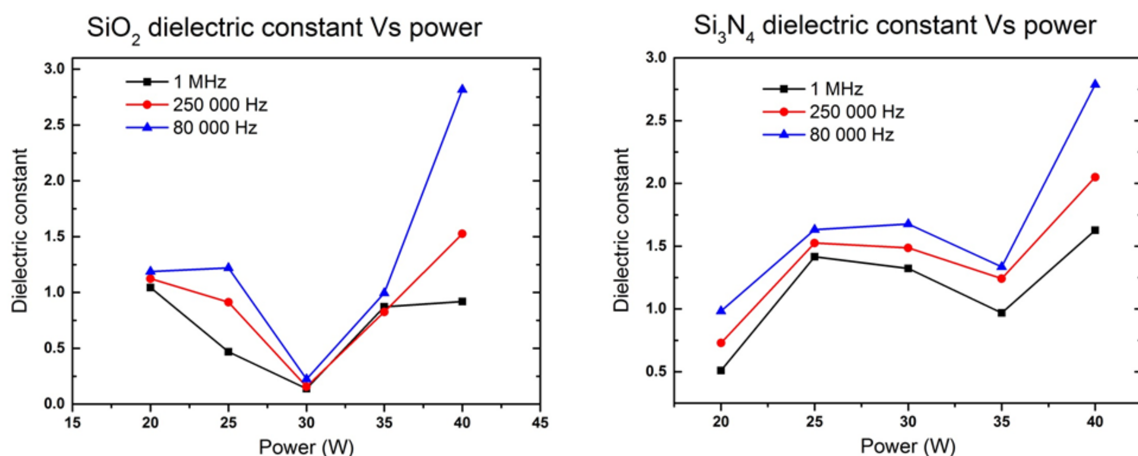


Figure 6.15: Dielectric constant as a function of RF power for SiO_2 (left) and Si_3N_4 (right). Calculated from measurements performed on contacts with diameter 1.5 mm.

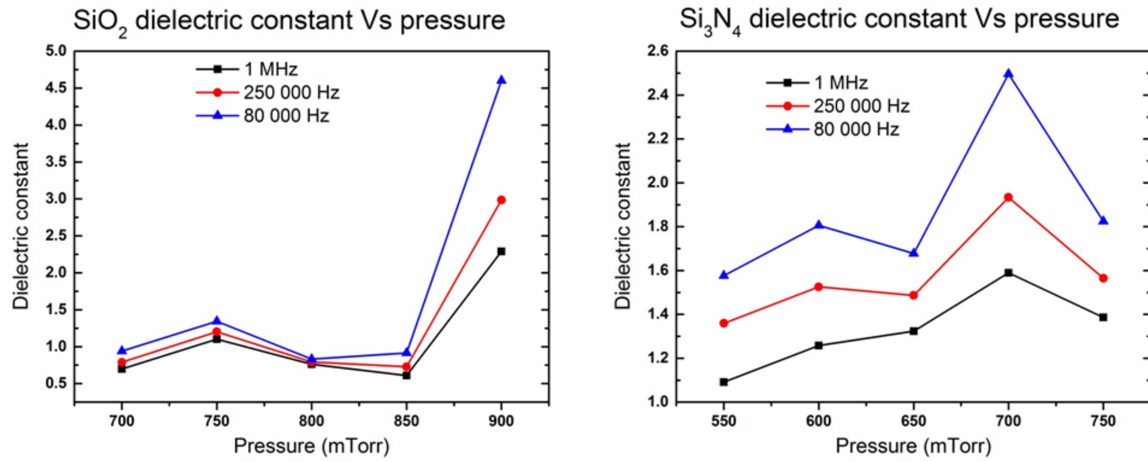


Figure 6.16: Dielectric constant as a function of reactor pressure for SiO_2 (left) calculated from measurements performed on contact with diameter 0.5 mm and Si_3N_4 (right) calculated from measurements performed on contact with diameter 1.5 mm.

6.3. I-V characterization of ZnO bottom gate TFT

I-V measurements were performed on all transistors made on samples with SiO_2 and Si_3N_4 deposited at five different temperatures. Output characteristics (I_{DS} vs. V_{DS}) and transfer characteristics (I_{DS} vs. V_{GS}) were obtained for all transistors (for presentation, I have flipped the I_{DS}-V_{GS} graphs by changing from negative to positive currents). The following section includes a selection of the most important results found in these measurements. Transistor parameters such as threshold voltage, field effect mobility and on/off current ratio are presented.

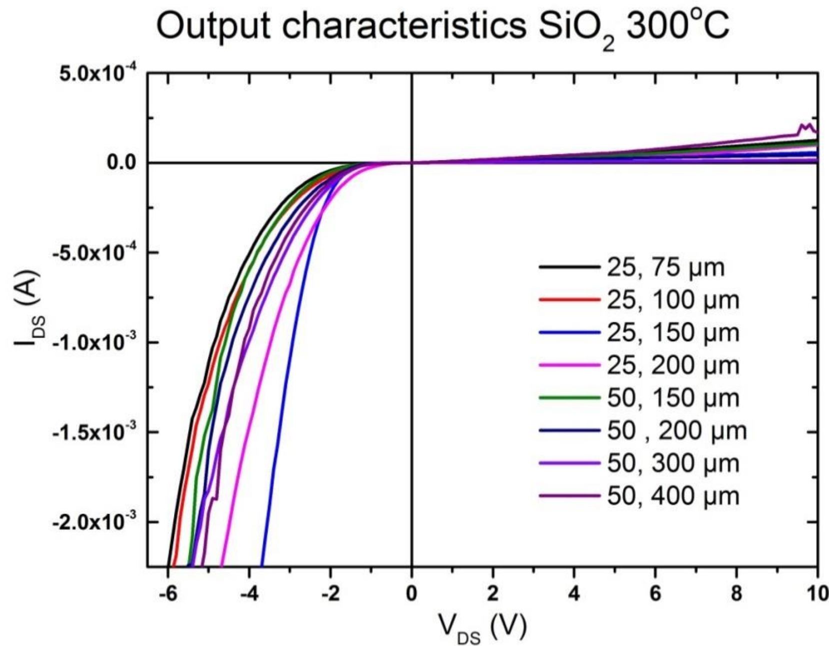


Figure 6.17: Output characteristics of ZnO TFT on Si with SiO_2 as gate insulator. The curves are for transistors with gate length 25 µm and gate widths 75, 100, 150 and 200 µm, and gate length 50 µm and gate widths 150, 200, 300 and 400 µm. V_{GS} = 0 V for all the curves in the figure.

Some shift can be observed for output characteristics for transistors with different gate lengths and gate widths. However, the gate dimensions does not seem to be a particularly important factor for the shape of the I_{DS}-V_{DS} curves for either SiO_2 (figure 6.17) or Si_3N_4 (figure 6.18). One possible explanation could be because of the staggered configuration, where the active region is far away from the insulator/ZnO interface, which is merely a conducting layer with ohmic contacts. The conducting layer is mostly affected by the depletion of the carriers by applying a bias to the gate.

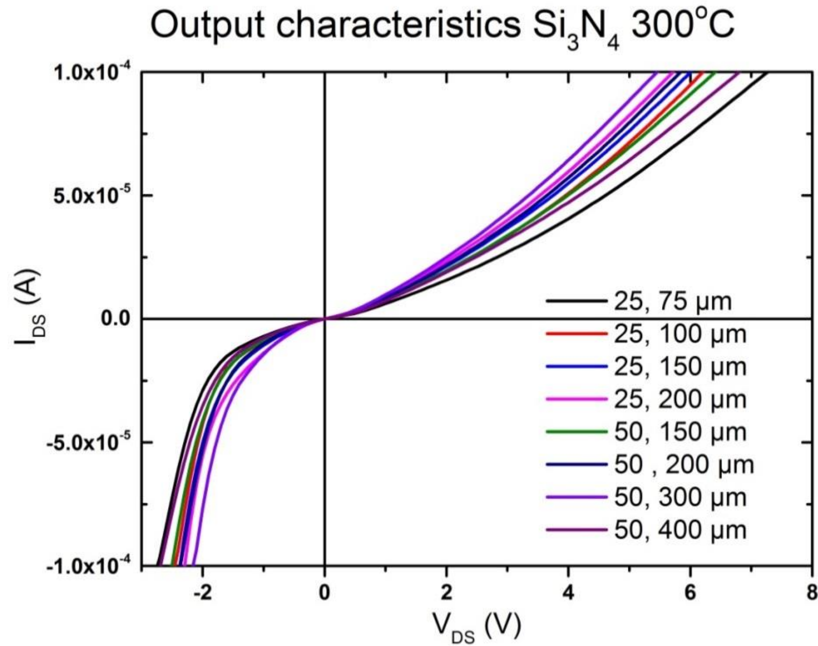


Figure 6.18: Output characteristics of ZnO TFT on Si with Si_3N_4 as gate insulator. The curves are for transistors with gate length 25 µm and gate widths ranging from 75, 100, 150 and 200 µm, and gate length 50 with gate widths 150, 200, 300 and 400 µm. $V_{GS} = 0$.

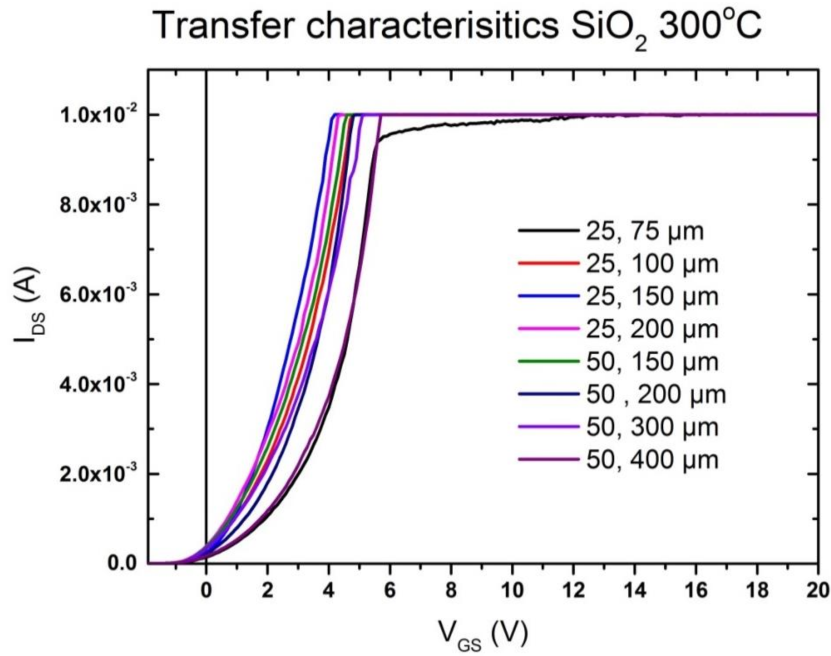


Figure 6.19: Transfer characteristics measured with V_{DS} = 2 V for transistors with SiO_2 deposited at 300 °C. Gate length 25 µm with gate widths 75, 100, 150 and 200 µm, and gate length 50 µm with gate widths 150, 200, 300 and 400 µm.

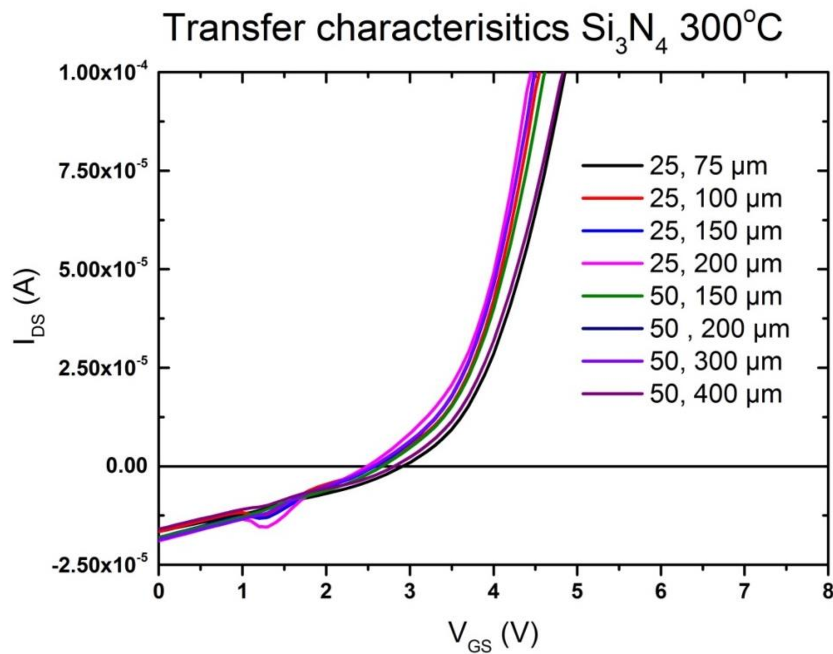


Figure 6.20: Transfer characteristics for different gate lengths and gate widths for transistors on sample with Si_3N_4 deposited at 300 °C.

Only small differences can be observed in transfer characteristics for transistors with different gate lengths and gate widths (figure 6.19 and 6.20). I-V characteristics of the transistor with gate length 25 um and width 75 um, tend to show saturation current, when $V_{GS} > 5$ V. However, this is not observed for all other gate lengths and gate widths due to measurement limitations. Compliance of the measurement device was set to 10 mA, which is why the curves flatten out abruptly in figure 6.19. For other measurements it could be observed that the curves were somewhat flat in this region (like the transistor with gate length 25 and gate width 75 in figure

6.19). The main problem would be when calculating the on/off current ratio since the maximum current could not be observed because it was higher than the compliance of the measurement device. However, since other curves (for the same transistors) did not exceed 10 mA, these could be used to calculate the on/off current ratio for most transistors to evaluate the device performance. With regards to the field effect mobility, the only important factor is the slope of the I_{DS}-V_{GS} curve, and measurement limitations have no influence on the calculated values.

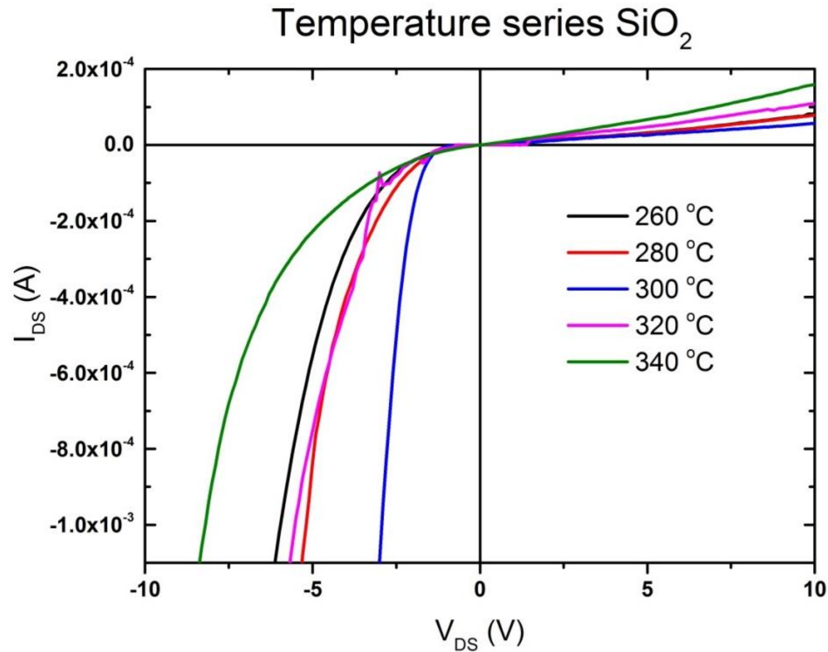


Figure 6.21: Comparison of output characteristics for transistors with gate length 25 µm, gate width 150 µm and SiO_2 deposited at temperatures ranging from 260 to 340 °C. Gate bias is 0 V.

Saturation was not reached for any of the transistors. All parameters are thus calculated in the linear region.

SiO_2 deposition temperature (°C)	V_T (V)	μ_{FE} ($cm^2V^{-1}s^{-1}$)	On/off current ratio
260	4.8	4260.8	$3.29*10^3$
280	4.2	2005.1	$1.88*10^3$
300	4	5453.9	$2.37*10^4$
320	4.73	4999.4	$2.97*10^3$
340	7	2651.2	$1.01*10^4$

Table 6.3: Threshold voltage, field effect mobility and on/off current ratio for TFTs with gate length 25 µm, gate width 150 µm and SiO_2 deposited at different temperatures.

Gate length, gate width (µm)	V_T (V)	μ_{FE} ($cm^2\ V^{-1}s^{-1}$)	On/off current ratio
50, 400	4.57	2386.1	$1.6*10^3$
50, 300	4.25	5453.9	$9.65*10^5$
50, 200	4.69	8862.5	$4.05*10^4$
50, 150	4.59	15452.6	$1.61*10^4$
25, 200	4	5113.0	$5.11*10^4$
25, 150	4	5453.9	$2.37*10^4$
25, 100	4.23	8862.5	$7.78*10^3$
25, 75	4.2	4544.9	$1.73*10^4$

Table 6.4: Threshold voltage, field effect mobility, and on/off current ratio calculated for the 8 different transistors on the sample with SiO_2 deposited at 300 °C, the optimal temperature. The parameters were calculated with a fixed drain voltage of -2 V.

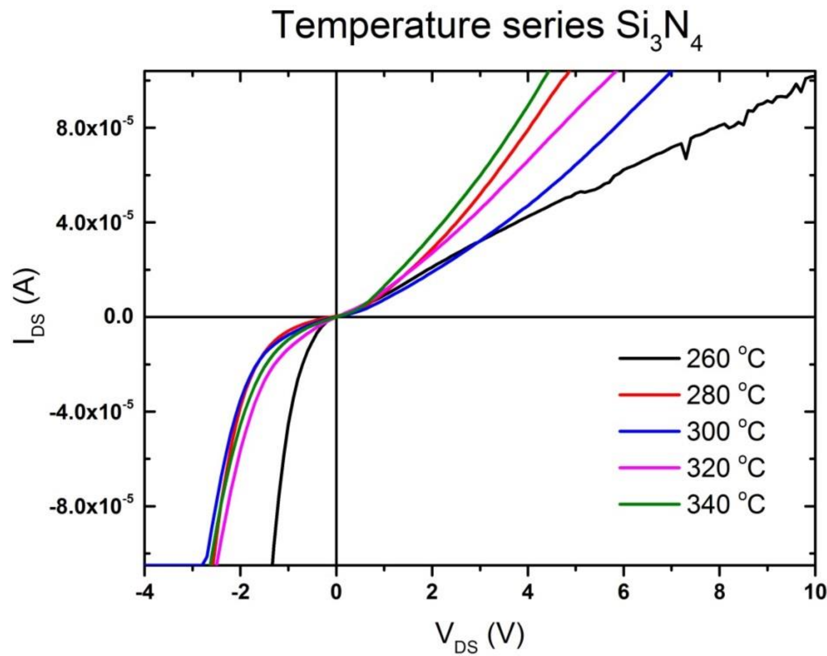


Figure 6.22: Output characteristics for the temperature series for Si_3N_4. Measured on transistors with gate length 50 µm and gate width 400 µm. V_{GS} = 0 V.

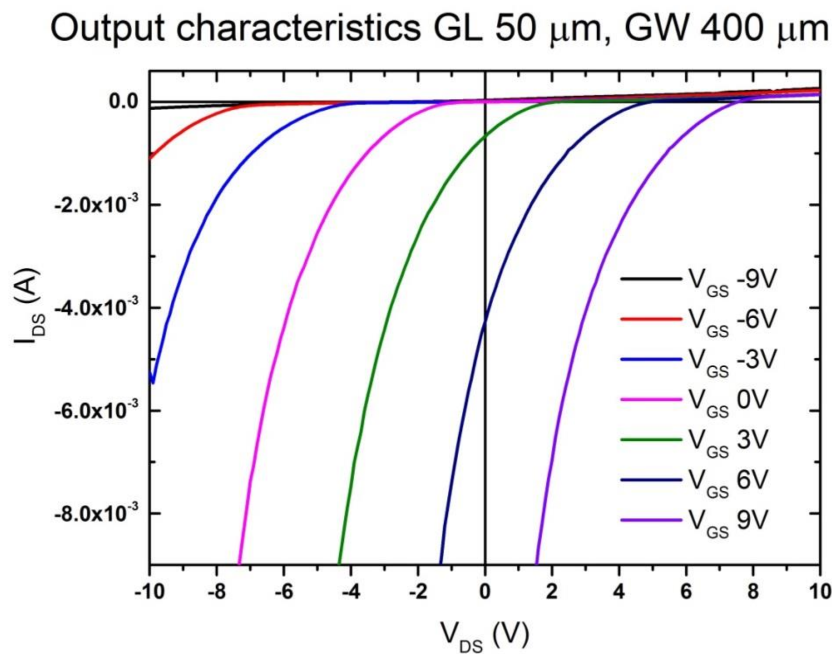


Figure 6.23: Output characteristics of bottom gate TFT with gate length 50 µm, gate width 400 µm and SiO_2 deposited at 300 °C.

In the output characteristics (see figure 6.23) a clear shift in the curves can be observed at different gate voltages. In the first approxiamtion, considering metal/oxide/n-semiconductor, applying positive bias to the metal will cause reduction of depletion region; will cause

accumulation, when the applied bias is high enough. The reduction of depletion region indicated that the active layer region is widened. As a consequence, with increase in V_{GS}, the forward diode characteristics of the gate region should shift towards right, which is observed in figure 6.23.

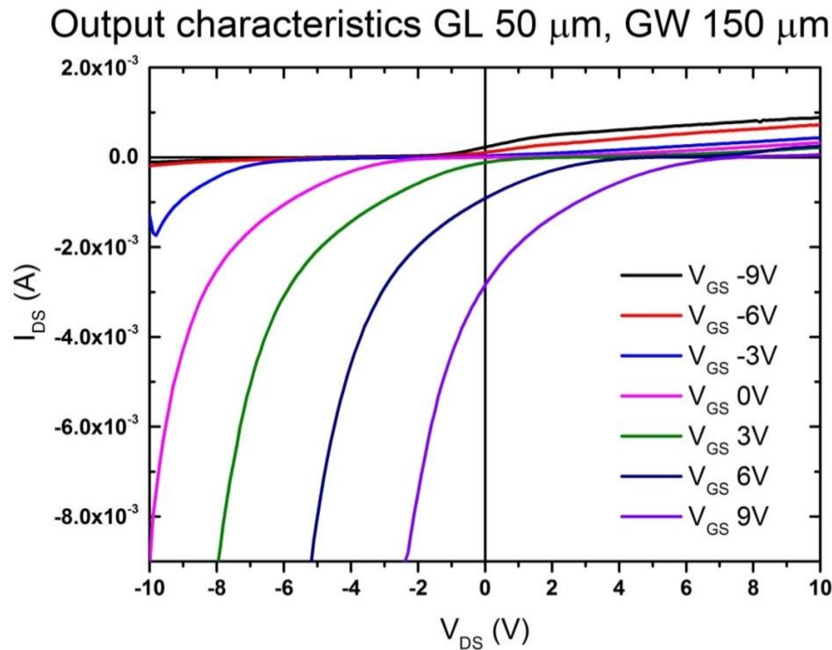


Figure 6.24: Output characteristics of bottom gate TFT with gate length 50 µm, gate width 150 µm and Si_3N_4 deposited at 340 °C as gate insulator.

As in the case of SiO_2 a clear shift at different gate voltages can be observed in figure 6.24. The shape of the curves becomes more linear with higher gate bias. Current flows more freely, implying that a channel is formed. At positive biases (and partly at zero bias) the curves resemble diode characteristics indicating that the channel was depleted for these gate voltages. The difference between this plot and the one for SiO_2 (figure 6.23) is that there is a higher current for transistors with Si_3N_4 when applying the same voltages to the gate. In SiO_2 the fixed charges are few, whereas in Si_3N_4 the fixed charges near the interface is higher due to effective surface passivation. When disparate situation is considered for figure 6.16, fixed charges at the interface to n-type semiconductor, say ZnO in this case, will cause thin layer of electrons accumulating near the interface, causing inverse band bending. This accumulation due to fixed charges at the interface will compensate for the applied field; meaning the depletion layer will be reduced only at higher bias than for SiO_2. As a result, the widening of the active region in ZnO layer will occur at relatively high bias. In other words, the diode characteristic of ZnO layer will shift towards left for similar gate bias. Similar I-V characteristics were obtained for other transistors on the same sample and transistors made on samples with different oxide layers.

Gate length, gate width (µm)	V_T (V)	μ_{FE} ($cm^2 V^{-1}s^{-1}$)	On/off current ratio
50, 400	4	1573	$5.73*10^3$
50, 300	4.4	1748	$1.57*10^4$
50, 200	5	3146	$6.51*10^3$
50, 150	4.2	4544	$1.38*10^4$
25, 200	5	524	$2.84*10^3$
25, 150	4.8	1748	$5.67*10^3$

25, 100	5	2097	$6.68*10^3$
25, 75	5	4195	$5.65*10^4$

Table 6.5: Performance parameters for all transistors made on the sample with Si_3N_4 deposited at 280 °C as dielectric.

The table above shows transistors parameters obtained from the transfer characteristics of all transistors on the sample with Si_3N_4 deposited at 280 °C. Calculations was done for several samples to compare the transistor performance and the conclusion was that the transistors with Si_3N_4 deposited at 280 °C gave the best performance. The sample with Si_3N_4 deposited at 260 °C had a few transistors with good performance (like the one in table), but for others the mobility was comparatively low (around 20 cm^2/vs). The samples with Si_3N_4 deposited at 340 °C had some transistors with high mobility, but these transistors also had relatively high threshold voltages (6-8 V).

Parameters for the temperature series of Si_3N_4 for transistor with gate length 50 µm and gate width 150 µm are listed in table 6.6.

Si_3N_4 deposition temperature (°C)	V_T (V)	μ_{FE} ($cm^2 V^{-1}s^{-1}$)	On/off current ratio
260	3.75	5593.70	$3.78*10^3$
280	4.17	4544.88	$1.38*10^4$
300	3.33	645.85	$2.63*10^3$
320	5	2597.08	$7.34*10^3$
340	6.33	3718.54	$4.9*10^4$

Table 6.6: Performance parameters for TFTs with Si_3N_4 deposited at different temperatures.

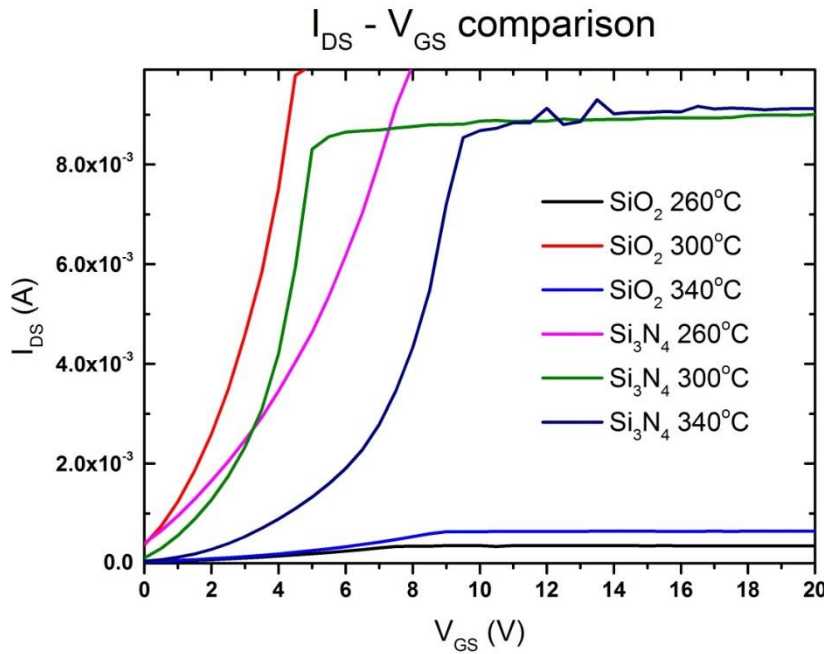


Figure 6.25: Comparison of transfer characteristics for TFTs with SiO_2 and Si_3N_4 as dielectric deposited at three different temperatures. These curves were measured on transistors with gate length 50 µm and gate width 150 µm. V_{DS} = -2 V.

The reason that the mobility of these transistors was so high is because of the structure. The defects in the dielectric/semiconductor interface do not affect the active surface region where the

mobility is measured. If a conventional ‘coplanar’ structure had been used with the same gate dielectric, the mobility would likely have been much lower. Even so, when comparing the mobility to that of bottom gate transistors in literature [3, 30] it is very high. This is attributed to the high quality of the ZnO active channel layer grown with MOCVD. Comparing table 6.4 and 6.5, it can be observed that transistors with SiO_2 as gate insulator seem to have generally higher performance than those with Si_3N_4 as gate insulator. As mentioned, the fixed charges in Si_3N_4 causes opposite band bending of that of the charges in SiO_2, and this is likely to be responsible for this difference in performance.

6.4. I-V characterization of ZnMgO/ZnO top gate TFT

The top gate TFTs made on ZnMgO were also characterized. In the following section the output characteristics and transfer characteristics of transistors with gate lengths 25 and 50 µm, SiO_2 or Si_3N_4 as gate dielectrics fabricated on r- and c-sapphire as substrates are presented.

Output characteristics of ZnMgO/ZnO top gate transistor

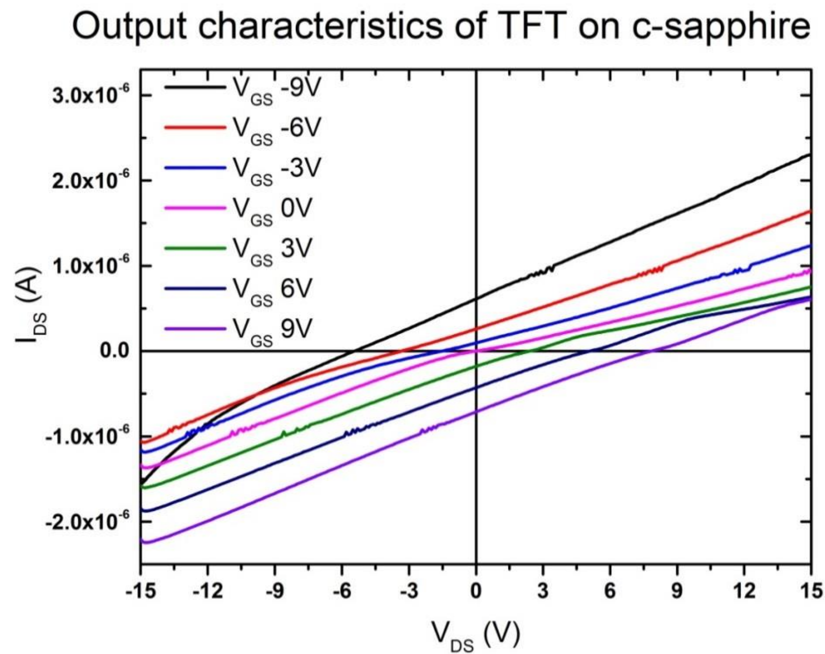


Figure 6.26: Output characteristics of ZnMgO/ZnO TFT with SiO_2 as gate insulator, gate length 25 µm and c-sapphire. V_{GS} vas varied from -9 to 9 V and V_{DS} was swept from -15 to 15 V.

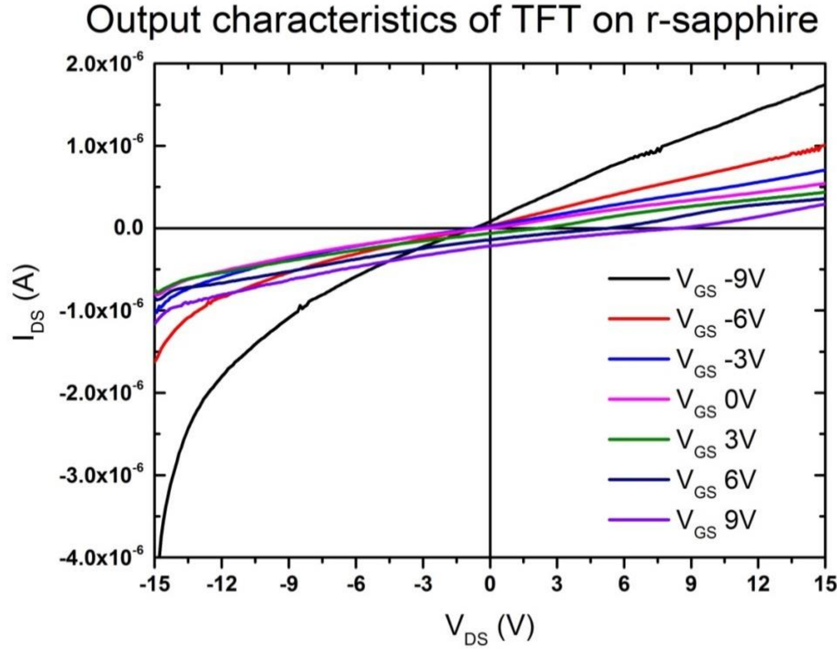


Figure 6.27: Output characteristics of ZnMgO/ZnO TFT with SiO_2 as gate insulator, gate length 25 µm and r-sapphire as substrate.

The transistors with gate length 25 µm on c- and r- sapphire show different output characteristics. For the c-sapphire the conduction is basically linear with applied bias indicating ohmic and also it shifts downwards from negative to positive bias. As mentioned earlier in section 2.3, when ZnMgO/ZnO is grown along Zn-polar (O-polar), positive (negative) polarization charges are located at the interface. This will compensate by accumulating electrons (holes) at the interface. Increasing Mg content in ZnO will increase the band gap in ZnMgO, increasing both valence band and conduction band compared to ZnO, forming barrier for electrons or holes at the interface - thereby the formation of a 2-dimensional electron gas (2-DEG) at the ZnMgO/ ZnO interface for Zn-polar and 2-dimensional hole gas (2-DHG) for O-polar. When the gate bias is varied, the resulting band bending will modulate the 2-DEG or 2-DHG channel. For example, when the bias is sufficient to reach flat-band potential, this 2-DEG will disappear. As a consequence, the device will behave like a conventional TFT in coplanar configuration.

Considering ZnO/ZnMgO Zn-polar interface for the current samples under study, applying a positive bias to the gate will compensate the negative fixed charges at the interface, reducing band bending at the interface and electron density. On the contrary, a negative bias will increase band bending at the interface and electron density. A similar behavior is observed in figure 6.26, where I_{DS} increases with V_{GS} for a constant V_{DS}. The transistor on the r-sapphire substrate, on the other hand, does not show this kind of conduction. This type shows more of a diode-like characteristic similar to the one exhibited by the bottom gate TFT previously analyzed in this thesis. A 2-DEG will only be formed for ZnO grown on c-sapphire as the hetero-structures are polar in nature. Hence, the measurements are as expected in this regard. And, as in the case of the bottom gate TFT, no drain current saturation was observed for any of the top gate TFTs.

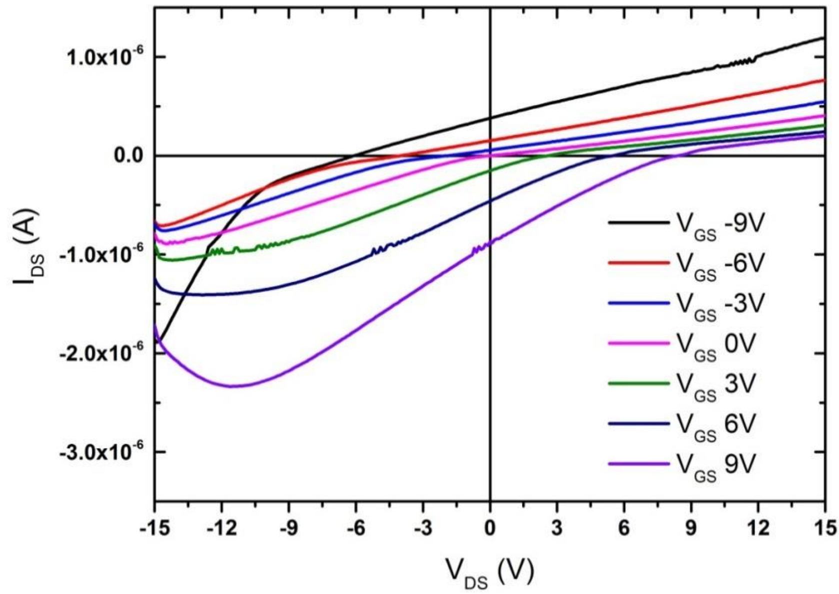


Figure 6.28: Output characteristics of ZnMgO/ZnO TFT with SiO_2 as gate insulator, gate length 50 µm and c-sapphire as substrate.

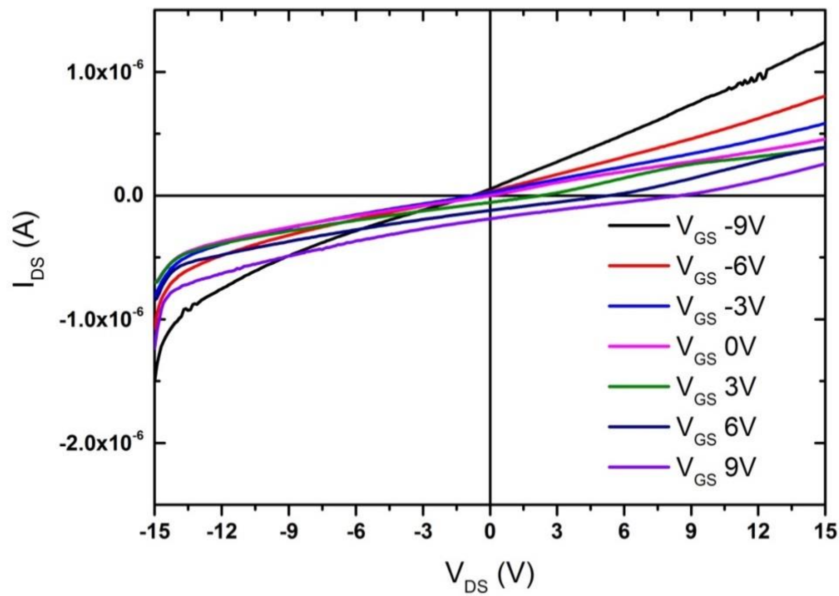


Figure 6.29: Output characteristics of ZnMgO/ZnO TFT with SiO_2 as gate insulator, gate length 50 µm and r-sapphire as substrate.

Transistors with gate length 50 µm also exhibit different behavior for the different substrates. The one on r-sapphire looks similar to the one with gate length 25 µm. Although the curves for the transistor with gate length 50 µm on c-sapphire (figure 6.28) looks a bit different from the same one with gate length 25 µm (figure 6.26), they show more conduction (in the negative region) than either of the two transistors on r-sapphire (figure 6.27 and 6.29). This could be attributed to

the field distribution across the channel region. Increase in the channel width, will reduce the field across and form a very narrow channel region near the source.

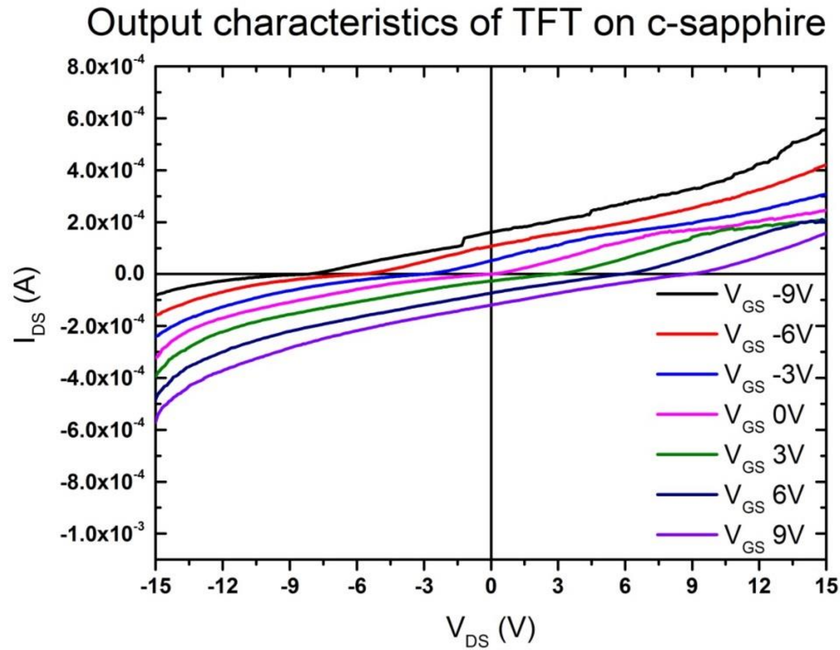


Figure 6.30: Output characteristics of ZnMgO/ZnO TFT with Si_3N_4 as gate insulator, gate length 25 µm and c-sapphire as substrate.

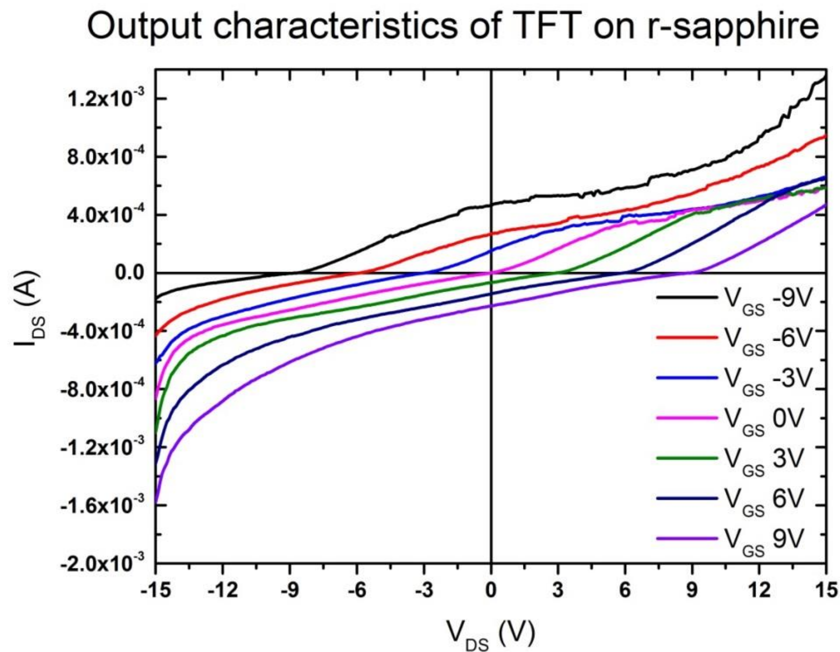


Figure 6.31: Output characteristics of ZnMgO/ZnO TFT with Si_3N_4 as gate insulator, gate length 25 µm and r-sapphire as substrate.

The characteristics for the transistors with Si_3N_4 as gate insulator, gate length 25 µ grown on the two different substrates are more difficult to distinguish. However, the one grown on c-sapphire (figure 6.30) seems to show slightly more ohmic conduction than the same transistor on r-sapphire (figure 6.31). As mentioned earlier, the fixed charges at the ZnMgO/Si_3N_4 will form

accumulation of electrons near the interface, again forming a 2-DEG. For the structures on c-sapphire, 2-DEG is expected to form both at ZnMgO/ZnO interface and ZnMgO/Si_3N_4 interface. On the other hand, single 2-DEG will form at ZnMgO/Si_3N_4 interface for TFTs on r-sapphire. Hence both the TFTs have similar characteristics (refer figure 6.30 and 6.31). However, the observation of increased conductivity on r-sapphire is unclear.

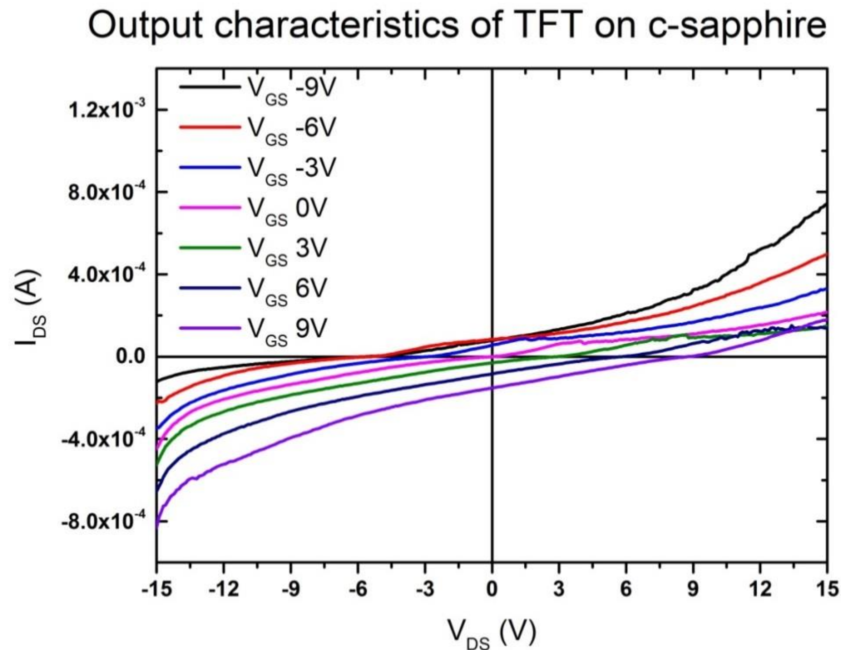


Figure 6.32: Output characteristics of ZnMgO/ZnO TFT with Si_3N_4 as gate insulator, gate length 50 µm and c-sapphire as substrate.

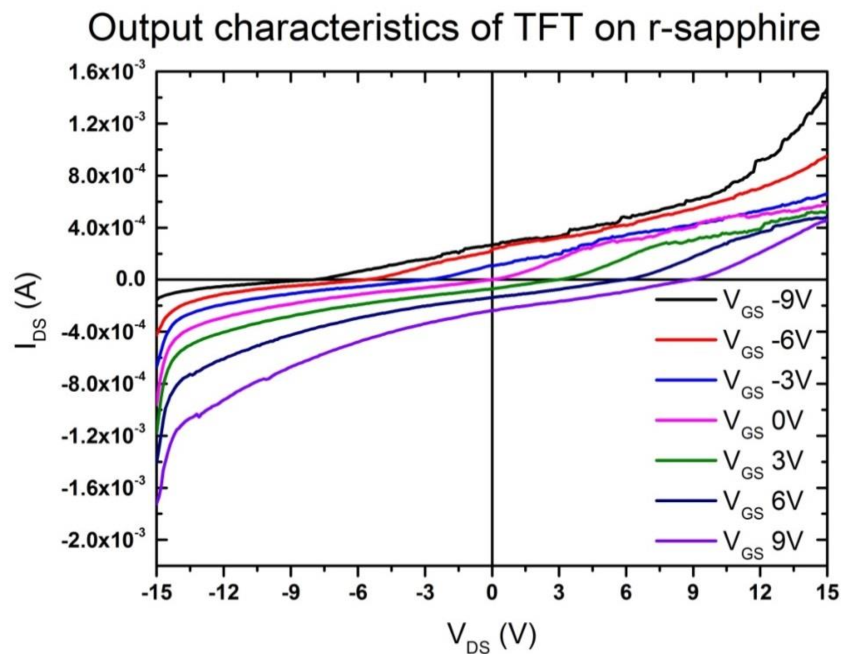


Figure 6.33: Output characteristics of ZnMgO/ZnO TFT with Si_3N_4 as gate insulator, gate length 50 µm and r-sapphire as substrate.

The transistors with gate length 50 with Si_3N_4 as gate insulator (figure 6.32 and figure 6.33) look similar to their respective counterparts with 25 μm gate length. The I-V characteristics of the transistor on c- sapphire look slightly more ohmic also in this case and thus more similar to the I-V characteristics obtained for the transistors with SiO_2 as gate insulator.

Transfer characteristics of ZnMgO/ZnO top gate TFT

By extrapolating the linear region of the graph, the threshold voltage was calculated for drain voltage -2, 0 and 2 V. The field effect mobility was calculated for V_{DS} equal to -2 and 2 V, and the on/off current ratio was calculated for V_{DS} equal to -2, 0 and 2 V. Presented here are the values calculated for V_{DS} = 2 V. A way to get an idea of the mobility of these transistors is to look at the steepness of the I_{DS}-V_{GS} curves; the steeper the curve, the higher the mobility.

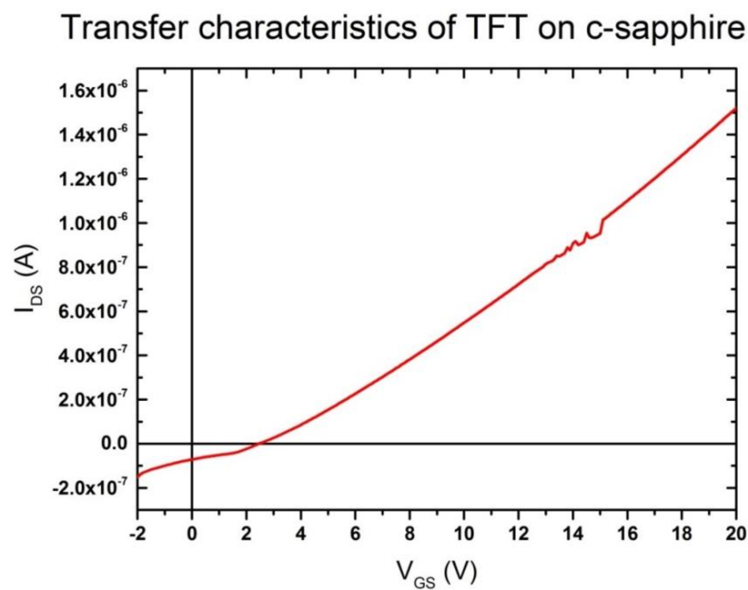


Figure 6.34: Transfer characteristics of ZnMgO/ZnO TFT with SiO_2 as gate insulator and gate length 25 μm on c-sapphire. V_{DS} = -2V.

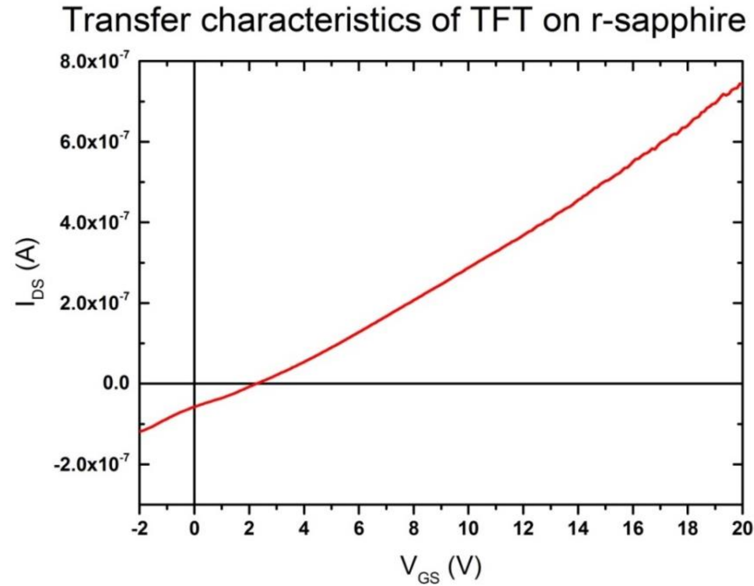


Figure 6.35: Transfer characteristics of ZnMgO/ZnO TFT with SiO_2 as gate insulator and gate length 25 µm on r-sapphire. V_{DS} = -2 V.

V_T, μ_{FE} and on/off current ratio was calculated from the transfer characteristics. The values were 2.5 V, 0.682 cm^2 $V^{-1}s^{-1}$ and $7.42*10^2$ respectively for transistor on c-sapphire with gate length 25 µm and SiO_2 as gate dielectric (figure 6.34). For the same transistor on r-sapphire (figure 6.35) the parameters were: Threshold voltage of 2.5 V, μ_{FE} 0.341 cm^2 $V^{-1}s^{-1}$and an on/off current ratio of $7.89*10^2$. Since the values for the mobility measured in the two transistors (on r- and c-sapphire) with gate length 25 and with SiO_2 were lower than expected, measurements were performed a second time. This time the gate voltage was swept from 0 to 50 V with drain voltages equal to -2 and 2 V. The mobilities obtained were 37.1 cm^2 $V^{-1}s^{-1}$ for the transistor on c-sapphire and 5.9 cm^2 $V^{-1}s^{-1}$ for the transistor on r-sapphire. Both these values were calculated from the measurements done with V_{DS} = 2 V, but similar values were obtained for V_{DS} = -2 V. The other transistors were also measured with V_{GS} swept from 0 to 50 V, but the differences in these calculated values were much less significant.

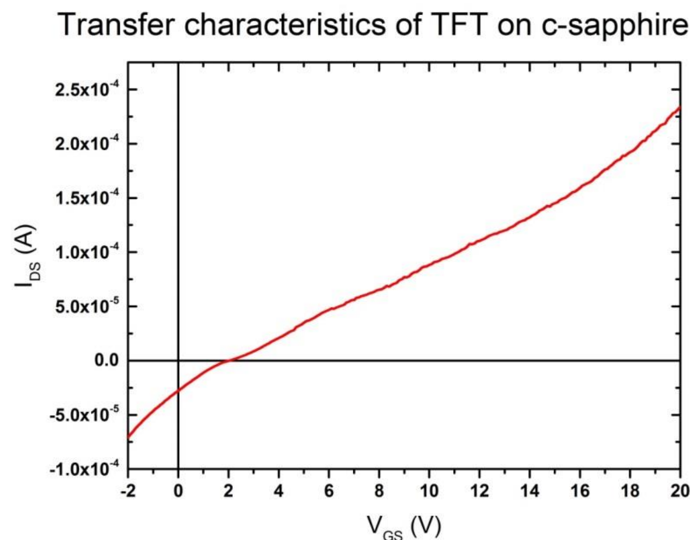


Figure 6.36: Transfer characteristics of ZnMgO/ZnO TFT with Si_3N_4 as gate insulator and gate length 25 µm on c-sapphire. V_{DS} = -2V.

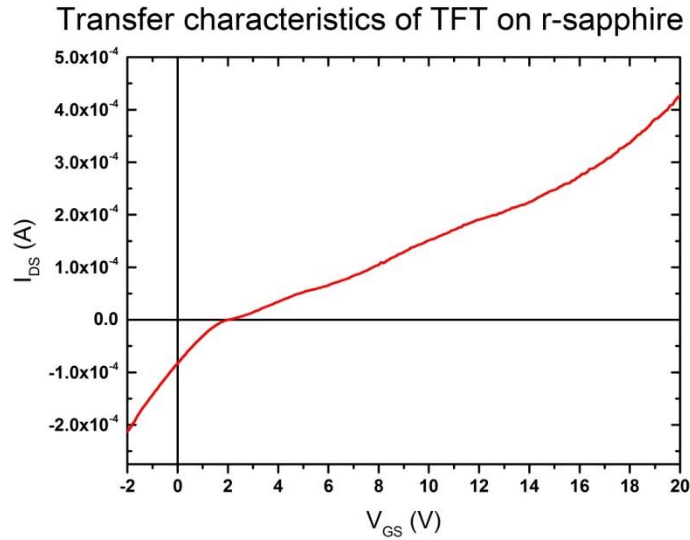


Figure 6.37: Transfer characteristics of ZnMgO/ZnO TFT with Si_3N_4 as gate insulator and gate length 25 µm on r-sapphire. V_{DS} = -2 V.

For the transistor fabricated on c-sapphire with gate length 25 µm and Si_3N_4 as gate dielectric (figure 6.36) V_T, μ_{FE} and on/off current ratio was 2 V, 86.98 cm^2 $V^{-1}s^{-1}$ and $1.34*10^3$ respectively. For the same TFT on r-sapphire (figure 6.37) V_T was 2 V, μ_{FE} was 131 cm^2 $V^{-1}s^{-1}$ and on/off current ratio was $4.29*10^3$. Here the mobility was higher for the transistor on r-sapphire than the one on c-sapphire. It can be mentioned, however, that in the second measurements performed with V_{GS} from 0 to 50 V, the mobilities for the two TFTs were basically equal.

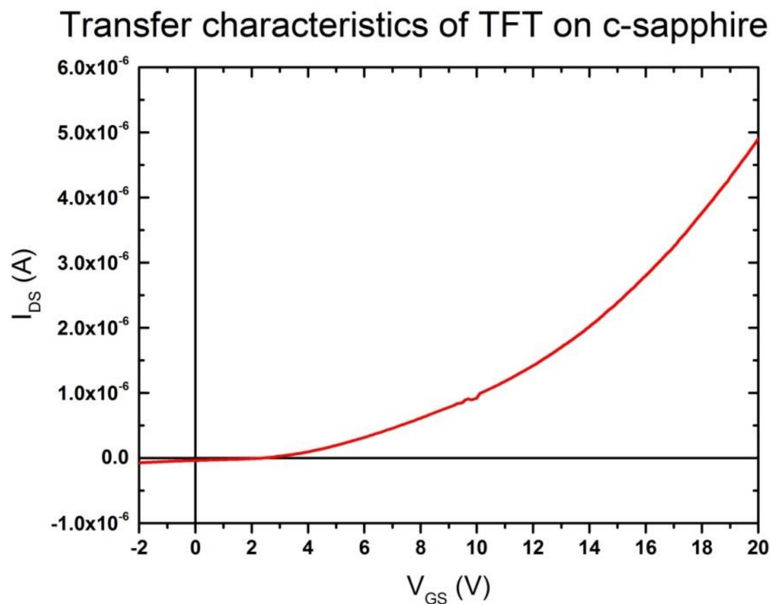


Figure 6.38: Transfer characteristics of ZnMgO/ZnO TFT with SiO_2 as gate insulator and gate length 50 µm on c-sapphire. V_{DS} = -2 V.

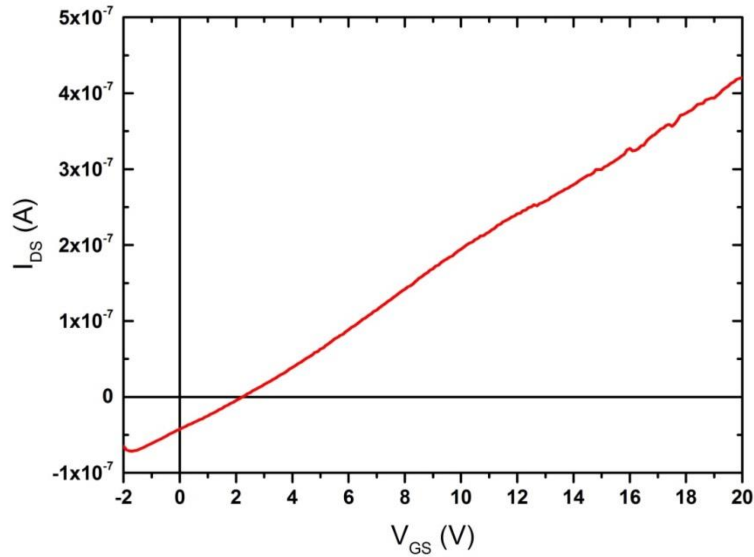


Figure 6.39: Transfer characteristics of ZnMgO/ZnO TFT with SiO_2 as gate insulator and gate length 50 µm on r-sapphire. V_{DS} = 2 V.

By comparing the characteristics in figure 6.38 to the corresponding plot for the transistor on r-sapphire substrate (figure 6.39) a clear difference in slope can be observed. The slope of the curve in figure 6.38 is significantly higher than the slope of the curves in figure 6.39. As a consequence the calculated field effect mobility is higher for the transistor on c-sapphire than the same one on r-sapphire. The threshold voltage was 3.5 V, the field effect mobility was 4.09 cm^2/Vs and the on/off current ratio was $2.94*10^3$ for the TFT c-sapphire. V_T, μ_{FE} and on/off current ratio was calculated to be 2.3 V, 0.273 cm^2/Vs and $8.95*10^3$ respectively for the corresponding on r-sapphire.

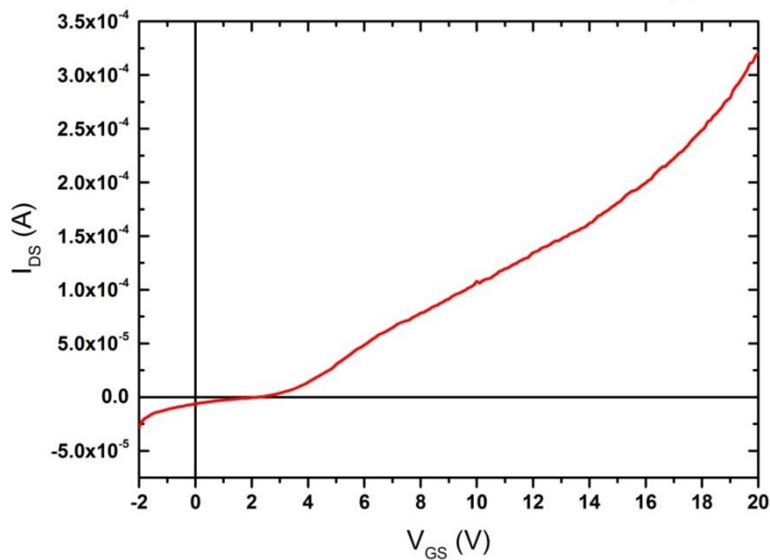


Figure 6.40: Transfer characteristics of ZnMgO/ZnO TFT with Si_3N_4 as gate insulator and gate length 50 µm on c-sapphire. V_{DS} = -2 V.

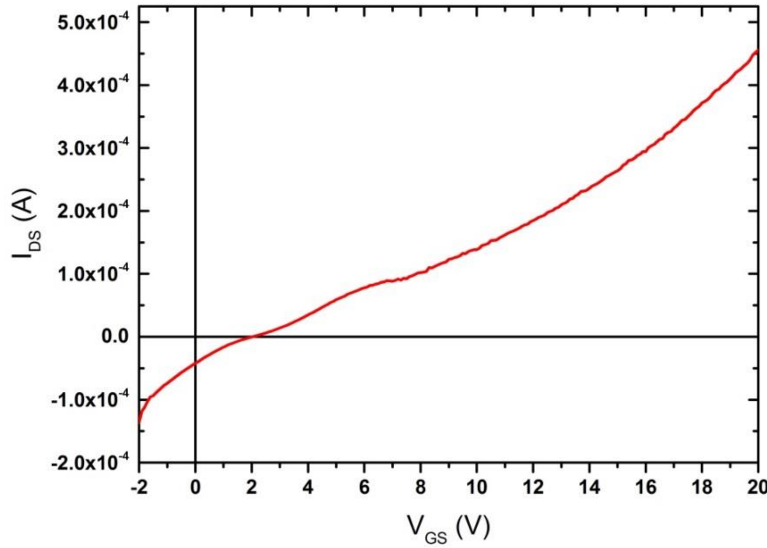


Figure 6.41: Transfer characteristics of ZnMgO/ZnO TFT with Si_3N_4 as gate insulator and gate length 50 µm on r-sapphire. V_{DS} = -2 V.

For the transistor with gate length 50 µm and gate insulator Si_3N_4 fabricated on c-sapphire the threshold voltage, field effect mobility and on/off current ratio was 3 V, 173.95 cm^2 V^{-1} s^{-1} and $3.33*10^3$ respectively. The same transistor on r-sapphire had threshold voltage, field effect mobility and on/off current ratio of 4 V, 131 cm^2/Vs and $1.58*10^3$ respectively.

Generally, the mobilities and the on/off current ratios were comparable to that achieved in [11], whereas the threshold voltages differed. Here threshold voltages between 2 and 4 V were calculated, while Sasa et al. observed a threshold voltage of -7.2 V. Comparing TFTs with SiO2 and Si_3N_4 as dielectric layer, the current I_{DS} is higher irrespective of structures on c- and r-sapphire. This could be attributed to additional 2-DEG at ZnMgO/Si3N4 interface. The lower mobility of 2-DEG at ZnMgO/ZnO interface could be due to the strain effect (lattice mismatch) as a result of coherent growth of ZnMgO layer on ZnO, whereas this effect is less prominent for amorphous Si_3N_4.

7. Conclusion

Thin film transistors of ZnO have been investigated. By varying deposition parameters for PECVD and studying the deposited dielectrics with C-V characterization and Ellipsometry, the optimal temperature, RF power and reactor pressure have been found for SiO_2. These were 300 ^oC, 30 W and 800 mTorr respectively. For most of the MOS-structures, the measured C-V characteristics measured at low frequencies deviated from ideal/theoretical MOS-characteristics demonstrating enhanced capacitance. This effect is attributed to the fact that interface surface states can follow the ac signal at low frequencies and give rise to excessive capacitance, as observed in the measurements. However, the trap charges at the Si/SiO_2 interface will have no influence on the performance of the ZnO TFTs, but fixed charges will influence by screening the applied potential. XRD showed no diffraction peaks for SiO_2 or Si_3N_4, meaning that the films are amorphous in nature. Variation in intensity at 2theta = ~ 33 degrees was observed for different process parameters and identified as surface damage on Si wafer caused by Si_3N_4 deposition, a possible explanation for the abnormality in the related C-V measurements. XRD on ZnO indicated that the growth was preferential along (0002) ZnO. ZnMgO/ZnO films were also analyzed with XRD and indicate that the growth of ZnMgO on c-sapphire is along the polar (0002) orientation, whereas for r-sapphire it is along the non-polar (11-20) orientation.

Two types of TFTs were fabricated. The first type was a ZnO bottom gate TFT made on a substrate of silicon. The second type was a hetero-structure ZnMgO/ZnO top gate TFT made on r- and c-sapphire made with the purpose of demonstrating 2-dimensional electron gas (2-DEG). Patterning of the TFTs was done with LED maskless lithography on positive photoresist. Both transistors were characterized with IV measurements and their device parameters were extracted from these measurements. Compared to bottom gate TFTs existing in literature, the fabricated transistors exhibited very high mobilities (2000-5500 cm^2/Vs), similar values for the current on/off ratio (10^3-10^5) and slightly higher threshold voltages (3-5 V). Generally, the TFTs with SiO_2 as gate dielectric showed better characteristics than the ones with Si_3N_4 as gate dielectric.

I-V characteristics of the hetero-structure TFTs with SiO_2 as dielectric layer indicate the formation of a 2-DEG at the ZnMgO/ZnO interface in the transistors made on c-sapphire. On the other hand, the TFTs with Si_3N_4 as dielectric layer has 2-DEG at ZnMgO/Si_3N_4 layer irrespective of structures on c- and r- sapphire. For the ZnMgO/ZnO TFTs mobilities ranged from 0.3 to 170 cm^2/Vs. In comparison between transistors on c- and r-sapphire as substrate, those on c-sapphire had higher mobility. This is likely caused by the formation of a 2-DEG, which happens in polar ZnO grown on c-sapphire, and not on non-polar ZnO grown on r-sapphire.

ZnMgO/ZnO transistors with Si_3N_4 had generally higher mobilities than the corresponding for SiO_2, due to formation of additional 2-DEG Si_3N_4 as dielectric. Threshold voltages for these hetero-structure TFTs were 2-4 V and on/off current ratios were of the order 10^3-10^4. Based on the fabricated device characteristics, ZnO based device technologies utilizing 2-DEG may be possible in the future.

8. Further Work

It has been demonstrated that ZnO synthesized by MOCVD exhibited superior transistor characteristics. The device performance can be further enhanced by lowering the contact resistance by employing transparent conducting oxides (TCOs) like Indium tin oxide (ITO), ZnO doped with aluminum, etc. towards fully transparent device. When ZnMgO is grown over ZnO O-polar, the negative charge at the interface will induce 2-dimentional hole gas (2-DHG) at the interface forming a p-channel. In addition, the relative contribution of bulk and interface traps in the dielectric and dielectric/ZnO interface, respectively, is also not well understood in the present work.

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