Signal processing using CMOS-MEMS integrated resonators

Ph.D. Thesis

Jan Erik Ramstad

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Abstract

A central part of the ubiquitous computing world of today is Wireless Sensor Networks (WSN), consisting of node-based components in a mesh that detects the environment around it. The sensing and radio part of the WSN node are typically off-chip components which are needed in order to realize the required performance. This thesis sets forth to investigate how to use MicroElectroMechanical Systems (MEMS) resonators as signal processing units, directly integrated in Complementary Metal-Oxide Semiconductor (CMOS) technology. By integrating MEMS resonators directly with CMOS, one can omit some of the typical off-chip devices and thus enable more compact and cost-efficient WSN nodes.

CMOS-MEMS resonator structures have been made by etching CMOS dies after being processed, thus defining structures from the metal layers offered in the CMOS process. Post-processing of CMOS dies was possible through a service known as Application Specific MEMS Process Service (ASIMPS) where Carnegie Mellon University (CMU) has etched and released the MEMS structures. This post-CMOS process was further developed by making MEMS out of two different 90 nm CMOS processes. Five different CMOS runs were performed, three at UiO and two at CMU in 0.35 μm, 0.25 μm and 90 nm CMOS processes from both Taiwan Semiconductor Manufacturing Company (TSMC) and ST Microelectronics (STM).

Different resonator topologies have been modeled, simulated and measured. A set of basic resonators were combined in order to make more advanced multi-port MEMS resonators, enabling down-mixing of high-frequency signals to an intermediate-frequency. Composite resonators have been connected at selected nodal points in order to obtain higher order filtering characteristics. Higher-order MEMS filters were made in different ways and compared. Soft frequency tunable MEMS resonators and multi-mode features of composite MEMS resonators were investigated.

Composite MEMS resonators and CMOS amplifiers have been combined to convert the resonator current to a voltage, enabling voltage-to-voltage filters and mixer-filters. High gain, low-noise Trans-Impedance Amplifiers (TIAs) was made and different Trans-Impedance Amplifier (TIA) topologies were evaluated. The various combinations of MEMS and CMOS resulted in unique filtering capabilities with an increased Q-factor and low-noise performance.

ACKNOWLEDGEMENTS

During my thesis I have been able to work with a diverse set of competent scientists, researchers and professors that all have been very helpful to me during my PhD. First and foremost I would like to thank my supervisor Oddvar Søråsen who has been there for me for many years here at UiO. Without his support, advices and guidance I would not have been where I am today. My two co-supervisors Tor Fjeldly from UNiK and Geir Uri Jensen from SINTEF have been valuable resources with regular half-year meetings and they have given me the opportunity to use certain facilities and measurement equipment at MiNaLab.

Through a scholarship from the Fulbright Foundation, I was able to do a visiting research scholar stay at Carnegie Mellon University in Pittsburgh, USA. That stay has been incredibly valuable and insightful for me, and I am grateful that my two mentors professor Gary K. Fedder and professor Tamal Mukherjee gave me the opportunity to do research at their university. I learned a lot by working in the project named “Self-Healing MEMS” at CMU with PhD students Andrew Phelps, Chih-Ming Sun, Gokce Keskin and Jonathan Rotner.

The Nanoelectronics group at Institute of Informatics deserves a great deal of credit for being an open and including group. During my PhD, my research group evolved into a more social atmosphere, so a special thanks goes out to my senior engineer Olav Stanly Kyrvestad for his social and academic contributions. I’ve shared office with Jørgen Michaelsen during most of the time spent working on my PhD thesis where we have done collaborative research and we’ve had many scientifically related and non-related discussions together.

Finally I would like to thank my family and friends who have been very supportive during my thesis and have been a great aid and listening to me talk about my thesis!

PREFACE

This PhD evolved from my undergraduate studies at Vestfold University College and through working part time at SensoNor. From there I discovered that the typical method of utilizing MEMS sensors was to make the MEMS using a custom process and bonding a separate ASIC die to connect the two worlds together. This subject fascinated me, and it became obvious to me that there was a clear interest of attempting to tightly integrate MEMS with advanced signal processing through a more common platform.

My path then lead me to do my graduate studies at University of Oslo where I was attracted to the world of CMOS and the nanoscale transistors. Doing my Master Thesis at UiO significantly increased my interest for further research on this topic. Thus by engaging in a PhD position at UiO, my work on combining MEMS and CMOS had started.

The job atmosphere at my Nanoelectronics group was diverse, interesting and complementary. Indulging in physics, mathematics, informatics, mechanics and electronics made my work environment both challenging and inspiring. Through a scholarship from the Fulbright Foundation I was able to do research at an American university in Pittsburgh, Pennsylvania. My destination was Carnegie Mellon University with a renowned expertise in this particular research field. My stay there proved to be very valuable for my PhD thesis. After my stay at Carnegie Mellon University I had started the final path of my PhD in a new building: "Ole Johan Dahls hus". With it came an entirely new environment and a refreshing end of my PhD.

This PhD thesis supplies the reader with new knowledge about how to combine CMOS and MEMS and to learn how one can use vibrating micromechanical structures in combination with on-chip amplifiers to signal process intermediate and high-frequency signals.

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Chapter 1

Introduction

> ”*To make future wireless sensor devices smaller, smarter and more autonomous, fully integrated and multifunctional nodes will be required. It is challenging to design on-chip RF front-end devices, and today's solutions typically use discrete, off-chip components to meet the RF performance requirements (external inductors, crystals, SAW and ceramic filters). It has been shown that micromachined components (RF MEMS) can beneficially replace a great number of those bulky off-chip components with even better performance, smaller size and lower power consumption.*”
>
> J. E. Ramstad et al.
>
> In *Proceedings of DTIP 2009*

THE ongoing trend known as "More Than Moore" focuses more on total system integration rather than just reducing the Complementary Metal-Oxide Semiconductor (CMOS) transistor size [1]. Including typical off-chip components on the same die provides a common platform for different technologies. MicroElectroMechanical Systems (MEMS) has traditionally been a technology that has a separate production method compared to CMOS. MEMS devices are typically coarse-grain in size compared to the nanoscale CMOS transistors. Different MEMS oscillators and sensors are used extensively in many commercial and industrial products, therefore there is a driving force of finding a common platform for combining these two technologies. In short, combining MEMS directly with CMOS allows for much more compact devices with less parasitics, lower power consumption and larger Q-factors. For Wireless Sensor Networks (WSNs), the sensing devices and radio transmitting devices are components which could be directly integrated on-chip with the CMOS circuitry.

A tight integration of MEMS with CMOS can result in a reduction of space by including typical off-chip components on the same chip. This compact integration will also result in reduced power consumption, less parasitics and a reduced component price. A somewhat different sensor and transceiver technology with slightly lower overall performance may turn out to be adequate enough for certain application areas. As a consequence of "More Than Moore", it is believed that a new trend will develop within this CMOS industry where the most cost effective integration method with sufficient performance will become popular. My work will demonstrate one of many methods of integrating CMOS with MEMS to demonstrate tight and compact technology integration. Another aspect of this thesis is to evaluate a different method of processing signals than what is commonly done. This is done by utilizing micromechanical beams in different ways used as filters, mixer-filters or oscillators.

This thesis investigates methods of how to combine electronics and micromechanical parts in order to process signals in the context of WSN applications. The combination of MEMS directly in CMOS has certain advantages and disadvantages as will be described later on in this thesis. The combination method has been performed in various CMOS processes of 0.35 μm, 0.25 μm and 90 nm technology nodes. The newer CMOS processes have certain advantages such as lower power consumption but will also have certain drawbacks, and a comparison between the processes will be shown. The combination of CMOS and MEMS creates a foundation to make resonators and filters where the signal processing is performed in the mechanical domain.

On-chip amplifiers combined with these micromechanical resonators can give filters with a large Q-factor compared to typical off-chip components used today. The embedded CMOS circuitry is used to enhance filter characteristics through controlled impedance levels and self-adjusting bias levels. The combination of CMOS and MEMS results in a voltage-to-voltage conversion with low noise levels. Electrically or mechanically connected resonators combined with on-chip amplifiers results in filters and mixer-filters which may be used in front-end transceivers. The filter characteristics of these CMOS-MEMS integrated filters will be shown with suggestions for improvements and further research.

A part of this thesis has been performed at Carnegie Mellon University in Pittsburgh, Pennsylvania USA. An exchange stay from 2009–2010 has proved to be very valuable for this thesis. The project that I participated at CMU was known as "Self-Healing MEMS Resonators" which was sponsored by DARPA. Design, simulation and results from system implementations of that project will be shown later in this thesis. The integration of CMOS and MEMS in this thesis has been possible through the Application Specific MEMS Process Service (ASIMPS) and through the contact and connections with CMU [2, 3]. The CMOS-MEMS integration method is known as post-CMOS or CMOS-MEMS and will be further explained in this thesis. The ASIMPS allows fabless customers to do prototyping on CMOS-MEMS integrated designs at an acceptable price. The outline of this thesis is shown in the next section.

1.1 Thesis outline

This thesis is built up using the following disposition:

Chapter 2 : Expanding circuit design with MEMS - Examples of application areas where MEMS resonators can be used to expand CMOS circuit design are described. The method of how to combine CMOS and MEMS is explained with examples, and tentative design rules for CMOS-MEMS are derived.

Chapter 3 : Resonator modeling - Mechanical beams with different boundary conditions are modeled. The method of how to use the mechanical beams as electrical signal processing elements is explained and low-level system performance parameters, damping mechanisms and non-linear effects are explained.

Chapter 4 : Composite resonator structures - Beams with different boundary conditions are combined to create more complex, composite resonators, allowing resonators with multiple ports and multiple modes. Theory and analytical equations are shown to create a base foundation for these composite resonators. Theory and examples of how to couple composite resonators to create higher order filters are shown.

Chapter 5 : CMOS-MEMS implementations - Actual implementations of CMOS and MEMS integrated together are demonstrated with schematics, layout and SEM photos. These implementations are in various CMOS technologies. Analytical results, simulation results and measurements from these CMOS-MEMS implementations are presented.

Chapter 6 : High-level tradeoff parameters - By investigating the most promising CMOS-MEMS filter in this work, high-level system parameters are derived and compared with other research results. The purpose of this chapter is to show important higher level filter performance parameters, using the low-level parameters defined in the previous chapters. The chapter ends with suggestions of how to improve filter design by using refined high-level and low-level parameters.

1.2 Contributions and publications

The list below shows the papers produced in this thesis and Table 1.1 shows the different CMOS runs that were performed during this PhD thesis.

[4] O. Soeraasen and J. E. Ramstad. From MEMS Devices to Smart Integrated Systems. In *Journal of Microsystem Technologies*, vol. 14, no. 7, pages 895–901, Springer 2008.

[5] J. E. Ramstad, K. G. Kjelgaard, B. E. Nordboe and O. Soeraasen. RF MEMS front-end resonator, filters, varactors and a switch using a CMOS-MEMS process. In *Proceedings of DTIP 2009, Symposium on Design, Test, Integration and Packaging of MEMS/MOEMS*, pages 170–175, IEEE 2009.

[6] J. E. Ramstad and O. Soeraasen. Higher order FFSFR coupled micromechanical mixer-filters integrated in CMOS. In *the 28th Proceedings of Norchip*, pages 1–4, IEEE 2010.

[7] J. A. Michaelsen, J. E. Ramstad, D. T. Wisland and O. Soeraasen. Low-power Sensor Interfacing and MEMS for Wireless Sensor Networks. A book chapter in *Wireless Sensor Networks*, pages 373–395, InTech 2011.

[8] J. E. Ramstad, J. A. Michaelsen, O. Soeraasen and D. T. Wisland. Implementing MEMS resonators in 90 nm CMOS. In *Proceedings of DTIP 2011, Symposium on Design, Test, Integration and Packaging of MEMS/MOEMS*, pages 463–470, IEEE 2011.

[9] J. E. Ramstad and O. Soeraasen. Modeling and design of higher order, multi-mode, multi-port MEMS resonators in 90 nm CMOS. In *Proceedings of the Eurosensors XXV Conference*, pages 1–4, Elsevier 2011.

	Process	**Application**	**Loc.**
Nov. 2008	STM 0.25 μm	45° coupled base resonators as filters	UiO
July 2009	STM 90 nm	Tuneable MEMS VCO for A/D converter	UiO
Oct. 2009	TSMC 0.35 μm	FFSFR mech. conn. mixer-filters w/diff. amp	CMU
March 2010	TSMC 0.35 μm	El. summed FFSFR mixer-filter w/ CS TIA	CMU
Oct. 2010	TSMC 90 nm	PPTF, CCSFR and FFSFR mixer-filters w/TIA	UiO

Table 1.1: CMOS runs during the PhD thesis

In publications [5] and [7], co-authors have contributed with details on varactors, switches and FDSMs respectively. The author of this thesis has a large contribution to most of the papers and publications produced in this thesis. The acronyms in Table 1.1 are explained later on in this thesis. Three out of the five tapeouts have been performed at UiO while two tapeouts have been performed during the stay at CMU in 2009–2010. As can be seen in Table 1.1, 0.35 μm, 0.25 μm and 90 nm CMOS processes have been used. An evaluation of these processes is done in chapter 2, and the system implementations are shown in chapter 5.

Chapter 2

Expanding circuit design with MEMS

Advanced signal processing can be complemented with other technology platforms in order to enhance system capabilities and performance. A CMOS LC tank with mixer and an LNA for front-end transceiver systems can be made with CMOS inductors and varactors which unfortunately provide low Q-factors for the filter part of the system. Circuit design can be expanded by using a different technology platform for the filter part, as well as including the filter as a part of the mixer, making it a mixer-filter. On-chip filters or mixer-filters with a large Q-factor will put less stringent requirements on the amplifier design and may alleviate the need for a separate mixer, allowing mixing high frequency signals down to an intermediate frequency and perform filtering at the same time.

This chapter will show application areas for integration of CMOS with MEMS including some examples of compact integration to illustrate the possibilities of expanding circuit design with MEMS. The chosen CMOS-MEMS integration method is described, pros and cons of different technology nodes will be highlighted and tentative CMOS-MEMS design rules are developed.

2.1 MEMS and their applications

Using MEMS to complement CMOS circuit design can be done in different ways. Using on-chip micromechanical filters, oscillators or sensor components is a popular research field. The research in my work puts these MEMS resonators combined with CMOS in a context of Wireless Sensor Networks. These micromechanical signal processing elements or sensor elements can be tightly integrated with CMOS.

Table 2.1 shows a list of various research facilities, institutes and universities which perform research on MEMS sensors or front-end transceiver components, all integrated with CMOS with different methods. As can be seen, research is being done in France, Finland, Spain, Canada, USA and Taiwan. Using inductors, varactors or micromechanical resonators for front-end signal processing is shown to be a popular research topic.

Parameter	Research area
U. of Barcelona [10, 11, 12]	Resonators, oscillators and mixer-filters
U. of California, Berkeley[13, 14]	Resonator amplifiers, mixer-filter, oscillators, switches
Carnegie Mellon U.[15]	Biological sensors, gyroscopes, filters, inductors, varactors
U. of Florida [16]	Accelerometers, gyroscopes
Georgia Institute of Tech.[17]	Bulk Acoustic Wave (BAW) resonators
National Chung-Hsing University[18]	Sensors and resonator filters
National Tsing Hua University [19]	Sensors, resonators and oscillators
U. of Waterloo [20]	Inductors, resonators
VTT [21]	Filters, resonators, transmission lines

Table 2.1: Research areas

Fig. 2.1 shows a simple transceiver architecture [22]. The various processing elements shown in Fig. 2.1 can potentially be done with different on-chip micromechanical components. Typically off-chip components that perform filtering and mixing tasks may offer better specifications such as lower Insertion Loss (IL), higher filter Q-factor or lower power consumption. The idea of using MEMS resonators as filtering components is to alleviate typical off-chip components for some of these tasks by utilizing on-chip electronics combined with MEMS. The end result of doing this to obtain almost the same results with more flexibility by using the integrated electronics to tune and control the filter frequency.

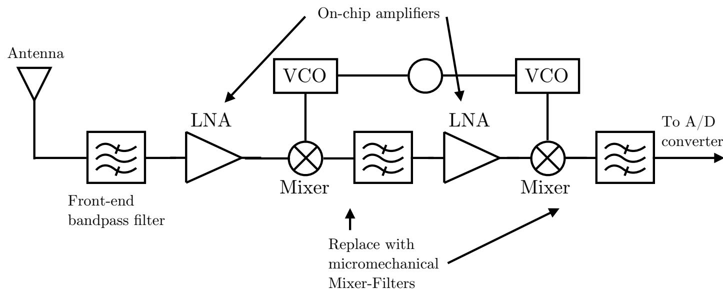


Figure 2.1: Simple transceiver architecture

Fig. 2.2 shows typical implementations of filters, oscillators and mixer-filters. An LC tank can be done either on-chip or off-chip, but it only has two terminals, and for CMOS LC tanks the Q-factor is low. An LC tank can offer a narrow or a large bandwidth, depending on the desired usage. A crystal is a component which is typically made of a Quartz material which offers a very large Q-factor, low phase-noise and therefore a very clearly defined resonance frequency. The crystal may also be used to tune the resonance frequency through a third terminal using a polarization voltage on the resonator. Quartz are typically one-port devices, therefore tuning the frequency with a polarization voltage may become difficult. For the same reason Quartz crystals typically offer significant feedthrough from the input to the output of the device which must be compensated. Finally, a mixer can be implemented by using transistors, thus mixing two signals ω_1 and ω_2 down

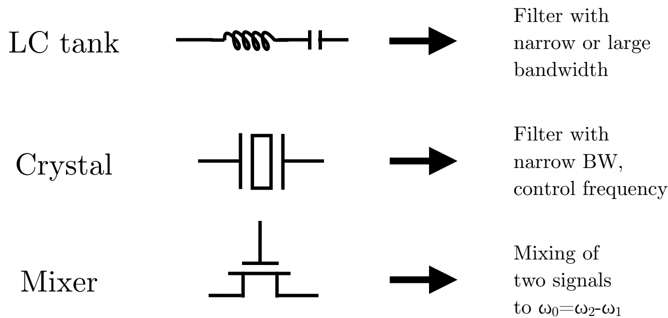


Figure 2.2: Examples of typical filter, oscillator and mixer realizations

to a frequency defined as $\omega_0 = \omega_2 - \omega_1$. Using transistors to mix down frequency is a typical method of mixing two signals, although RF frequency capable transistors must be used. Even though RF transistors are specially implemented from the foundry they will also have feedthrough from the input to the output.

By using more complex MEMS resonator architectures, it is possible to include more terminals, reduce feedthrough from the various terminals and to include on-chip electronics to automatically adjust desired parameters. CMOS-MEMS implemented resonators can offer more complex signal processing capabilities by combining the MEMS resonators with CMOS circuitry as well as reducing cost and size. In addition to this, less off-chip engineering will be required, and external impedance matching is not required because everything is done on-chip. This is true for frequencies that are sufficiently low, i.e. lower than the typical 2.4 GHz consumer frequency. Any impedance matching of MEMS resonators must be adjusted to match the following amplifier or any electronics thereafter.

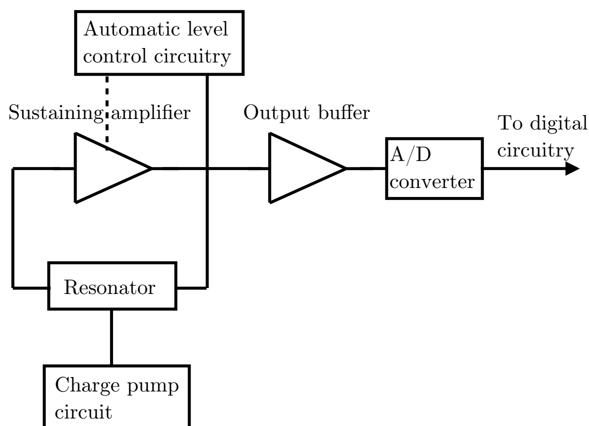


Figure 2.3: Voltage-Controllable Oscillator with MEMS resonator and self-adapting electronics

One example of using MEMS and CMOS together to complement each other is shown in Fig. 2.3. It shows the realization of using the MEMS resonator in a feedback circuit including a sustaining amplifier to make an oscillator circuit. Since the MEMS resonator is a passive element, it requires an amplifier to initiate and sustain oscillation. An Automatic Level Control (ALC) circuit is included to adjust biasing levels at the input and output of the sustaining amplifier. If large voltage levels are required for the MEMS resonator, a charge pump is also implemented. The output of the oscillating circuit goes to an output buffer and a following A/D conversion step. This type of circuit can also be used as a Voltage Controlled Oscillator (VCO) circuit, adjusting the resonance frequency by increasing a polarization voltage.

Oscillator circuits or VCO circuits both place stringent requirements on the passive element which dictates the resonance frequency as well as any parasitics from the amplifier. CMOS-MEMS implemented resonators have a low Q-factor compared to state-of-the-art Quartz or MEMS oscillator implementations [15]. However, by utilizing a clever and complex resonator architecture, feedthrough can be substantially reduced. The resulting phase noise of such CMOS-MEMS implemented oscillator circuits may not be as good as other implementations, however the resulting performance may be "adequate" through the usage of CMOS circuitry.

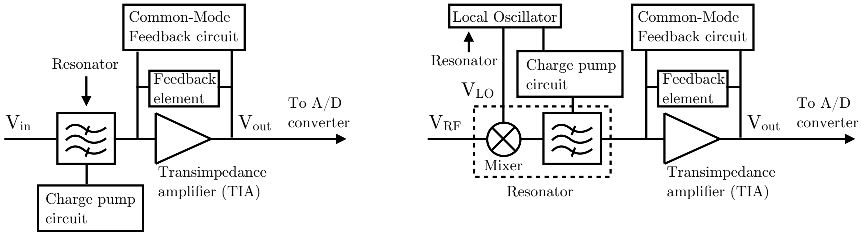


Figure 2.4: Examples of CMOS-MEMS filters and mixer-filters

The left part of Fig. 2.4 shows CMOS-MEMS implemented resonator used as a filter. A charge pump circuit can be implemented on-chip to increase the polarization voltage, thus the total filter will comply with voltage levels required from the CMOS foundry design rules. Following the output of the resonator filter is a Trans-Impedance Amplifier (TIA) with a feedback element and a Common-Mode Feedback (CMFB) circuit. The CMFB ensures correct voltage levels of the input and output of the amplifier. The feedback element can consist of a resistor, capacitor or transistor and converts the motional current out from the resonator to a voltage at the output of the amplifier.

The right part of Fig. 2.4 demonstrates a RF signal mixed with an LO signal down to an Intermediate Frequency (IF). This IF signal is at the same frequency as the MEMS resonator and is further filtered through the resonator. Using multiple terminals on a resonator, it is possible to both downmix a signal and filter at the same time, using the one and same device to both tasks [23]. The LO frequency is generated from a Local Oscillator (LO) which can also be implemented as a

CMOS-MEMS resonator. The downmixed filtered current is then converted into an output voltage V_{out} by the same output circuitry.

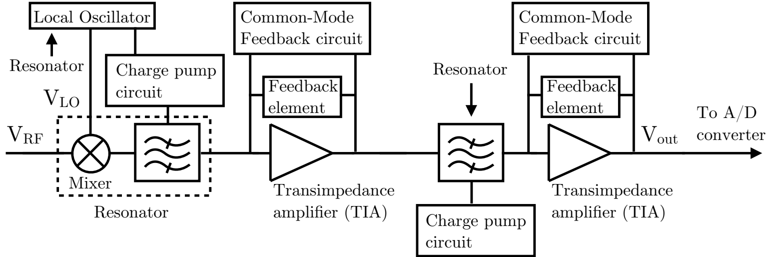


Figure 2.5: Augmenting CMOS with MEMS resonator filters and mixer-filters

By combining both parts that were shown in Fig. 2.4, it is possible to achieve a total on-chip CMOS-MEMS mixer-filter and CMOS-MEMS filter with appropriate electronics. An example of this is seen in Fig. 2.5. At the receiver part of a transceiver system, mixing down an RF to IF is performed and then followed by low-noise amplifiers and an additional filtering step. All of this can be implemented using CMOS-MEMS resonator filters, mixer-filters and oscillators. The output from this system is then led to an Analog-to-Digital (A/D) converter. The system implementation of Fig. 2.5 is less dependent on impedance levels and voltage levels as they can be controlled internally. Even if the CMOS-MEMS resonators were to have large impedance values, this could be compensated for by using the on-chip circuitry to achieve a 1:1 conversion gain and still consuming little power.

Pros of CMOS-MEMS	**Cons of CMOS-MEMS**
Integrate filters or sensors on-chip	Possible small electrode area
Reduced parasitics	Material composition limited
More routing capabilities	Comply to CMOS foundry rules
Compatible with CMOS technologies	Possible lower Q-factor
Can reduce bill of materials (BOM)	Packaging challenges

Table 2.2: Pros and cons of CMOS-MEMS integration

A summary of pros and cons of implementing MEMS components directly in CMOS is shown in Table 2.2. These advantages and disadvantages of making MEMS directly in CMOS will be further pointed out throughout this chapter. It should be mentioned that the final advantage of using CMOS-MEMS devices is that even though it has some drawbacks, it may turn out that this implementation method may offer sufficient performance at a cheap price.

This work will investigate one of several methods of combining CMOS and MEMS which is shown in section 2.2.

2.2 Integrating MEMS with CMOS

All methods of integrating MEMS with CMOS will face different types of challenges. A common denominator for these integration methods is that in order for compact integration to take place, the MEMS process must adapt to the CMOS process line as foundries typically do not want to change their existing process line infrastructure too much. All integration methods must take into consideration the fabrication temperature, photolithography mask complexity, internal stress, acceptable materials, the possibility of creating good interconnections and using acceptable packaging methods [24, 25, 26].

The different integration methods are illustrated in Fig. 2.6. A MEMS first method is more difficult to implement as the CMOS foundries are reluctant to accepting "dirty" silicon wafers which have been processed in beforehand. An example of MEMS first are processes that use Deep Reactive Ion Etching (DRIE) etches deep into the silicon to make microstructures from Silicon On Insulator (SOI). These SOI processes can offer lateral moving micromechanical resonators with a large electrode area and high Q-factor [27].

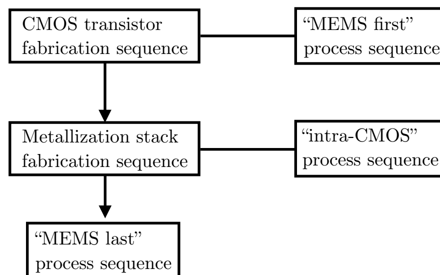


Figure 2.6: Process integration methods

An intra-MEMS process consists of integrating the MEMS part after the transistor fabrication part has been performed (deposition of polysilicon) but before the metallization sequence takes place. For polysilicon microstructures, this method makes it possible to anneal the polysilicon at high temperatures to get a good stress profile. This type of integration method is relatively complex as it disrupts the normal CMOS process flow, maybe requiring fabrication at different foundries.

The last integration method in Fig. 2.6 is the post-CMOS method which implements microstructures after the metallization fabrication sequence has been performed. This is known as "MEMS last" or post-CMOS. Because the polysilicon and interconnects have already been made, the thermal budget is critical. The deposition temperature for the structural material must be lower than this thermal budget in order to not alter the characteristics of the transistors and the interconnects.

There are two different types of post-CMOS implementation methods. The first one is based on depositing materials on top of the top metal layer to make microstructures. The second method is based on using the embedded metal layers

to make microstructures.

An example of the first post-CMOS method is by depositing AlN on top of Pt to make Bulk Acoustic Wave (BAW) resonators. The deposition temperatures during fabrication comply with the acceptable temperatures allowed by the foundry. This method does not damage CMOS interconnects or the CMOS transistors after fabrication.

There is a lot of research going on in the area of integrating MEMS and CMOS. My work does not go into the depth of describing the different integration methods and refers to the literature [24, 25, 26] for in depth details.

My work is based on a post-CMOS process where the already existing metal-dielectric stack from the CMOS is used to make micromechanical structures. This post-CMOS process has been made possible through a service known as Application Specific MEMS Process Service (ASIMPS), offered both in Europe and in USA [2, 3]. The process steps of this post-CMOS process are shown in Fig. 2.7.

Fig 2.7(a) shows the die immediately after being produced at the respective CMOS foundry. The yellow metal layer is typically set to be the top metal layer from the CMOS process and is used to protect the CMOS circuitry from becoming etched during processing. The green metal layer is the top structural layer and is used to define the MEMS structures.

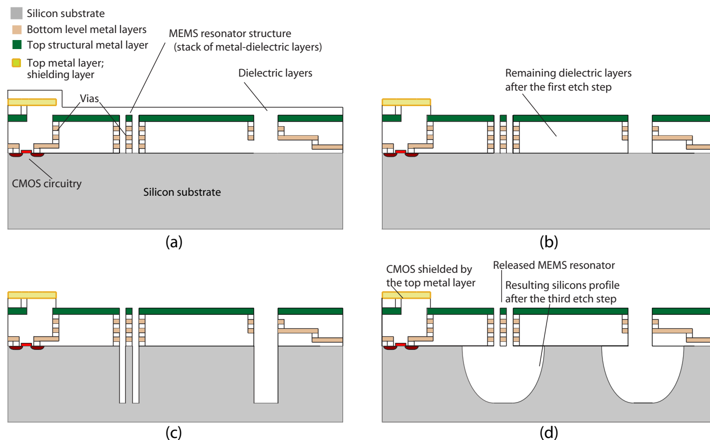


Figure 2.7: General CMOS-MEMS process etch steps

In Fig. 2.7(b) the openings without the green metal layer allows for etching trenches down towards the silicon substrate by using an anisotropic etch step sequence. An optional DRIE etch step is shown in Fig. 2.7(c) etching about 35 μm into the silicon substrate. The last step is shown in Fig. 2.7(d) where an isotropic etch releases the MEMS structures, creating circular trenches which cut in under the openings. This process step is tentative and can be modified in many ways. However, for this thesis, Fig. 2.7 shows the general dry etch steps that have been used in this thesis through ASIMPS.

The process flow in Fig. 2.7(b) is based on Table 2.3. Etching the dielectric where there are narrow gaps is the biggest challenge of this process due to chemical reactions during the RIE etch. More details of this etch process is found in [28].

Parameter	**Value**
Gas flow [sccm]	20 CHF_3 20 CF_4 95 O_2
Pressure [mT]	100
Power [W]	65
DC bias [V]	270
Time [min]	$\sim$ 120

Table 2.3: Typical dielectric etch parameters

The reason for the dielectric step in Fig. 2.7(b) being the most difficult etch step is because of the fluorocarbon (C_xF_y) reactions during the dielectric etch [28]. CHF_3, CF_4 and O_2 in Table 2.3 contributes to this unwanted fluorocarbon reaction. In general, there are four unknown factors to the dielectric etch:

- Type of etch equipment used for the dielectric etch
- The type of dielectric material in the CMOS process
- The thickness of the dielectric layer(s)
- Type of metal layer, i.e. aluminum or copper

It is also possible to take the gap between two structures into account as an unknown factor. However, due to these uncertain factors – it is not possible to clearly define the gap between two structures. As will be described in chapter 3.5, a method of changing the gap after the etching has been performed is used in order to achieve a controlled gap. This means that it is possible to tune the process to get an adequately small gap size and then later on control the actual gap. The etch equipment may be different for the different processing steps, i.e. Plasma-Therm 790 parallel-plate RIE system for the dielectric etch and Surface Technology Systems (STS) for the deep silicon RIE etch [28]. Steps (c) and (d) in Fig.2.7 are less challenging than the dielectric etch, although they may also contribute to determine post-CMOS design rules.

This thesis is will not go into the very depth of topic of post-CMOS processing as it is possible to write a PhD thesis on that topic alone [28]. It should be mentioned that the materials offered in a CMOS process have changed throughout the years, going from aluminum to a newer dual Damascene copper process. This means that the etch process must be modified slightly in order to accommodate for this copper composite material. The challenge of etching the dielectric layer remains the most difficult etch step, which is why this thesis relies on using a gap reduction technique after processing.

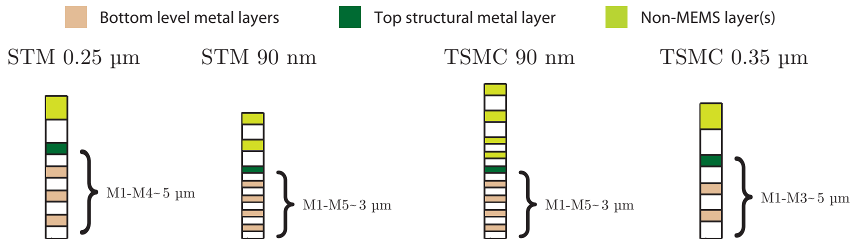


Figure 2.8: Cross section of the selected CMOS processes

This work has implemented MEMS resonators in four different CMOS processes, all through ASIMPS. Design rules for the official CMOS-MEMS process are offered by ASIMPS and are not shown here due to copyright rules. This thesis has attempted to implement CMOS-MEMS structures in more modern and fine-pitch CMOS processes (sub 100 nm CMOS processes): An unofficial development of the ASIMPS in two 90 nm CMOS processes has been attempted. This section will describe and show the possibilities that open up when migrating from coarse-grain (large transistor sizes) CMOS to fine-pitch CMOS. Fig. 2.8 shows a cross section of various CMOS processes that are used in this thesis. These CMOS processes offer different structural thicknesses and a different amount of metal layers.

Table 2.4 shows extracted parameters for 4 different CMOS processes encountered in this thesis. The STM 0.25 μm process became obsolete in 2009, and the STM 90nm became phased out to a newer STM 65nm process in 2010. One STM 0.25 μm run was done in November 2008. Two TSMC 0.35 μm runs were done while doing an exchange stay at CMU (2009-2010) and one TSMC 90nm run was done in October 2010. All implementations were performed using the ASIMPS service offered by CMU. Creating MEMS devices from two different foundries (ST Microelectronics and TSMC) as well as implementing MEMS designs in both coarse-grain (0.25 to 0.35 μm) and fine-pitch CMOS (90 nm or smaller) has provided insightful information about CMOS-MEMS implementations. It should be mentioned that 0.35 μm CMOS are stable and old processes which will still be around for a while, however they too will be phased out sometime in the future which was an important reason for investigating CMOS-MEMS implementations in 90nm CMOS.

	STM 0.25 μm	**STM 90 nm**	**TSMC 90 nm**	**TSMC 0.35 μm**
# of metal layers	5	7	9	4
Stack thickness [μm]	$\sim$5μm	$\sim$3μm	$\sim$3μm	$\sim$5μm
Top stack layer	M4	M5	M5	M3
Bottom stack layers	M1-M3	M1-M4	M1-M4	M1-M2
Shield layer(s)	M5	M6-M7	M6-M9	M4
Material features	1P5M aluminum w/M1 as tungsten	1P7M copper w/ Dual Damascene interconnect	1P9M copper w/ Dual Damascene interconnect	1P4M aluminum
$\sqrt{E/\rho}$ ratio $\left[\sqrt{\frac{Pa}{kg/m^3}}\right]$	6470	4115	4115	5435

Table 2.4: Extracted parameters for the selected CMOS processes

In this work, the microstructure which is a metal-dielectric composite is known as "the stack". The 0.25 and 0.35 μm processes define roughly 5 μm thick MEMS structures while the two 90 nm processes defines a stack of about 3 μm thick. The two 90 nm processes were implemented as a variant of the standard ASIMPS service with extended etching time during dielectric etch in order to be able to etch narrow gaps and be able to etch away all the dielectric and get to the silicon level. With this in mind, both 90 nm processes were designed with a smaller thickness. Also, the lower-pitch processes have a different thickness composition compared to the coarse-grain processes as shown in Fig. 2.8.

Fig. 2.8 shows that the coarse-grain processes define a 5 μm thick stack using 3 or 4 metal layers, while for the 90 nm processes, 5 metal layers must be used to achieve only 3 μm thick structures. The TSMC 90 nm run, which was performed after the STM 90 nm run, was designed to have the same amount of metal layers (5) to define MEMS structures. This was done even though the process had two extra metal layers (M6 and M7) which in turn could have resulted in roughly 4.2 μm thick structures. Certain beams tend to bend upwards after being released, this effect is known as curling. The underlying mechanisms and equations behind the curling phenomenon are explained in chapter 3.5. By making the stacks homogenous (that is, metal and dielectric are roughly equally thick), will reduce the amount of curling. Table 2.4 shows that the coarse-grain processes will have a higher E/ρ (Young's modulus E divided by material density ρ will define the resonance frequency, see chapter 3.1) ratio compared to the fine-pitch copper processes while the coarse-grain processes will allow for thicker structures instead and a larger electrode area. The fine-pitch CMOS processes, however, allows for more intricate routing capabilities as they have more bottom level metal layers.

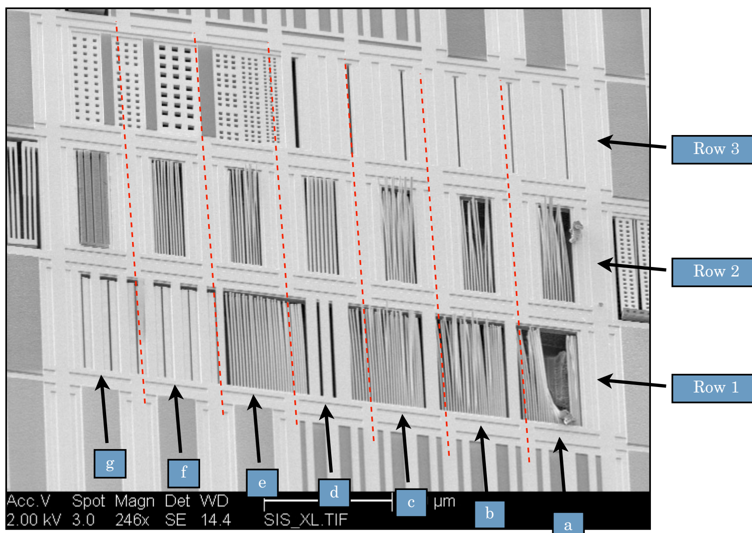


Figure 2.9: An optical test island

	a	b	c	d	e	f	g
Row 1	W=0.6	W=0.8	W=1.0	W=1.2	W=1.2	W=20	W=20
Row 2	M4M1	M5M4	M7M6	M5 (poly)	M5 (poly VW)	M5 (w/o active)	Alucap
Row 3	SA	SA	SA	SA	VH	VH	VH

Table 2.5: Optical test island table

An implemented optical test island with various structures are demonstrated in Fig. 2.9. These test structures were implemented in a STM 90 nm process in the first attempt to make MEMS in fine-pitch CMOS. Table 2.5 shows the implemented optical test island where all dimensions are given in μm. Row 1 consists of cantilever beams with varying width (W). Row 1 f and g consists of 20 μm wide beams. Row 2 consists of varying the amount of metal layers internally. Some of these structures include polysilicon beneath (2d and 2e) where 2e has Varied Width (VW) of the polysilicon layer. 2f consists of all metal layers up to metal 5 (M5) but without something called the Active layer (see p. 17–18) to see possible excessive out-of-plane curling. 2g consists of the aluminum cap layer from foundry, typically used for bond pads. The third row consists of rather wide beams of 40 μm to see if they were released (SA=Semi-Anchored). Row 3e to 3g consists of holes with varying dimensions (VH=Vary Holes).

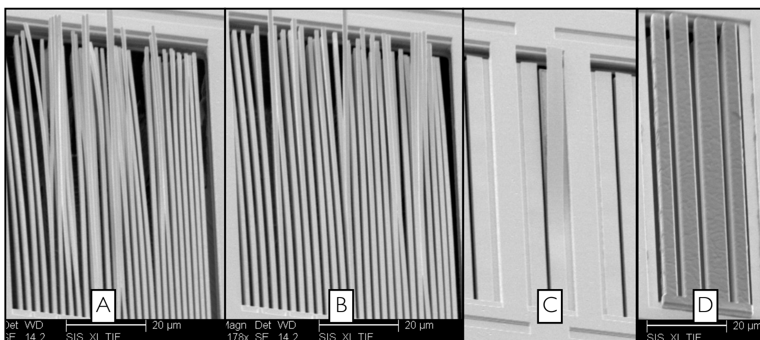


Figure 2.10: Delaminated and curling structures

Examples of delaminated and curling structures are seen in Fig. 2.10. In B, the far left three beams are homogenous consisting of metal 1 up to metal 5, while the other beams have a varying amount of metal layers embedded. A rather wide M5 part of a 20 μm wide beam started to delaminate (detach itself from the underlying structure) in C. D shows a rough aluminum surface, showing that it reacts more with the etch recipe than the copper does.

The cross section of a STM 90 nm released beam with metal layers can be seen in Fig. 2.11. From Fig. 2.11 it can be seen that metal layers M1-M5 have roughly equal thickness of the dielectric and metal layer while M6 and M7 have roughly twice the thickness. Table 2.6 shows the various thicknesses for both coarse-grain and fine-pitch CMOS processes. Exact thicknesses are not stated due to copyrights. However, the thicknesses in Table 2.6 give a general idea of possible stack thickness that can be made from metal-dielectric stacks.

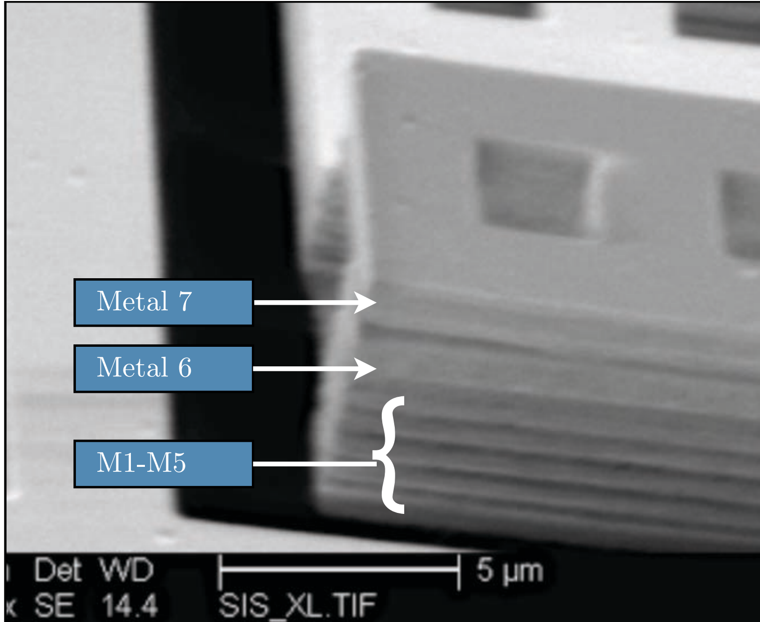


Figure 2.11: SEM showing cross section of STM 90 nm metal layers

Dim. in nm	Coarse-grain CMOS	Fine-pitch CMOS
Metal 7		800
Via6 (M7-M6)		800
Metal 6		800
Via5 (M6-M5)		800
Metal 5	1200	300
Via4 (M5-M4)	1200	300
Metal 4	650	300
Via3 (M4-M3)	650	300
Metal 3	650	300
Via2 (M3-M2)	650	300
Metal 2	650	300
Via1 (M2-M1)	650	300
Metal 1	650	300
Via (M1-Silicon)	650	300
Total thickness	∼ 7600	∼ 6200

Table 2.6: General thicknesses for coarse-grain and fine-pitch CMOS processes

Released cantilever beams for process characterization are shown in Fig. 2.12. The curling and delamination effects shown in Fig. 2.10 and 2.12 can occur due to several reasons. The delamination effect consists of beams becoming detached from the underlying material, starting to curl out-of-plane even before the silicon release etch. This delamination effect occurs due to the processing temperatures and the geometry of the device as seen in Fig. 2.12.

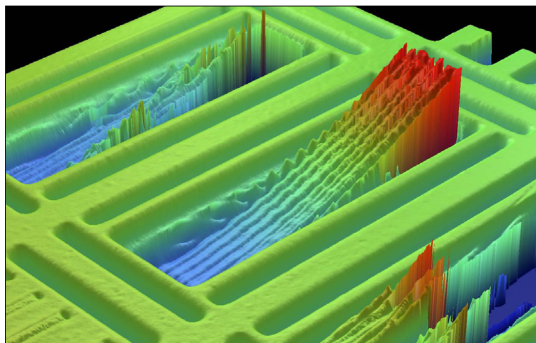


Figure 2.12: Wyco measurement of cantilever beams

A stack which is as homogenous as possible will reduce the internal stress in the mechanical structure. If the internal stress is too large, the free parts of a released beam may bend upwards or downwards. One method of reducing the amount of internal stress is to include a layer offered from the CMOS process which is known as the Active layer. The Active layer is used to define transistors as areas with this layer will contain a small dielectric deposited at lower temperatures. This will result in a reduced internal stress and therefore a reduced amount of curling [28].

The implementation of Active layers can be seen in Fig. 2.13. The light green area defines the Active layer. The red layer is polysilicon. CMOS foundry rules do not allow the Active layer to cross the polysilicon unless polysilicon and the Active layer both overlap each other (something which is not possible for the structure which is to be released). Therefore structures with polysilicon beneath are partially covered by the Active layer. The CMOS rules state that there must be a small separation from the Active layer to the polysilicon layer. Also, if the polysilicon is too close to the edge of the structure, it may become etched.

Fig. 2.14 shows Wyco measurement of long thin simply clamped beams. Fig. 2.14(a) shows beams consisting of M1-M7 (thick blue line) and M1-M5 including polysilicon beneath. It is clear that the M1-M7 beam has more curling, starting to bend 4.5 μm at 60 μm from the anchor. It was not possible to measure the whole 100 μm long beam due to resolution limitations. This clearly shows that a more homogenous beam will curl less. Fig. 2.14(b) shows a M1-M5 beam with and without the Active layer. The thin green line is without the Active layer, showing that the curling is roughly 700 nm for a 100 μm long beam compared to roughly 300 nm curling for the beam with the Active layer.

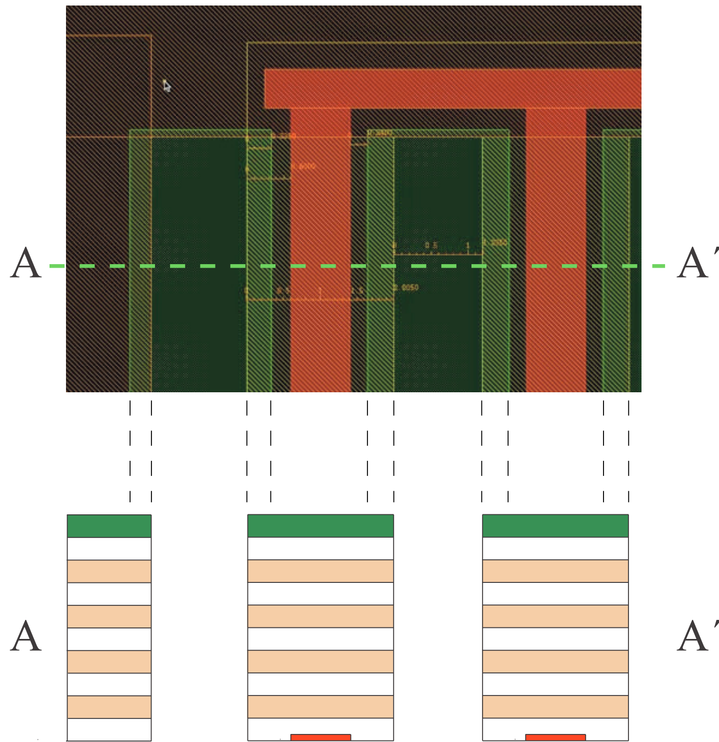
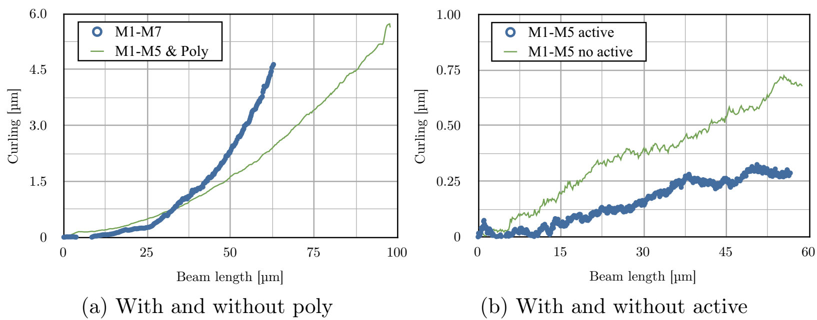


Figure 2.13: Layout rules for Active and Poly layers



(a) With and without poly

(b) With and without active

Figure 2.14: Results from Wyco measurements

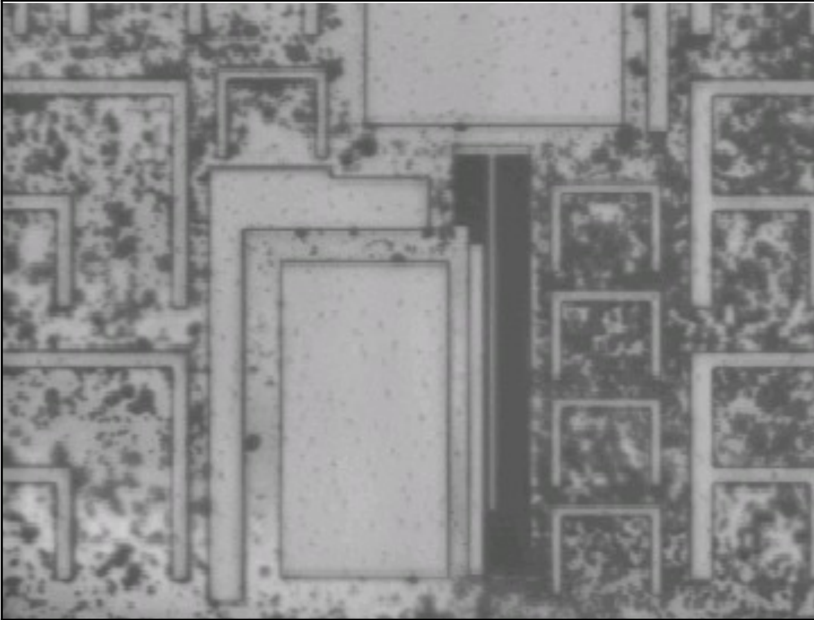


Figure 2.15: Corroded copper surface from a 2007 0.25 μm BiCMOS tapeout

As seen in Fig. 2.15, corrosion of the surface material may occur when exposed to the environment for a too long time. If the die package is not sufficiently sealed, moisture from the environment will cause corrosion of the surface material. CMOS processes based on aluminum tend to corrode less. By cleaning with Ar or rinsing with IPA (Isopropynol Alcohol), it is possible to reduce this corrosion effect for copper composite materials [28]. Curling, delamination, corrosion, materials for the microstructures and possible Q-factor are challenges for this post-CMOS method.

	Dim. [μm]	Rule name	Comment
Minimum width	1	W1	Delamination
Maximum width	10	W2	CMOS rule
Max length fixed-free	< 60	L1	Delamination
Max length fixed-fixed	< 100	L2	Curling
Max stack thickness	5	H1	Preliminary
Gap spacing	1.2	S1	Guarantees release
Poly from metal edge	0.6	S2	Prone to etch
Active cover edge	0.3	A1	Reduce curling
Active sep poly	0.1	A2	CMOS rule

Table 2.7: Tentative fine-pitch CMOS-MEMS design rules

Table 2.7 illustrates the developed rules for 90 nm CMOS designs. These design rules are tentative and are slightly adjusted compared to the coarse-grain CMOS-

MEMS implementations. For example, to avoid delamination of structures, the width should be 1 μm or larger. However, if a beam is sufficiently short and fixed at two ends, the width may be designed to be less than 1 μm. The CMOS foundry places maximum widths for the structures, although by clever design it is possible to create larger widths. Due to curling and delaminated structures, a maximum length has been set for fixed-free and fixed-fixed structures. The maximum thickness is given by the selected CMOS process and the gap size has been limited to 1.2 μm where self-adjusting gaps after release will create an even smaller gap as explained in chapter 3.5.

Pros of fine-pitch	**Cons of fine-pitch**
Less parasitics	Excessive curling may occur
Lower V_{DD} and power consumption	Small stack thickness
Intricate routing capabilities	Stringent CMOS design rules
In line with newer CMOS technology	Delamination effects

Table 2.8: Pros and cons of fine-pitch CMOS-MEMS

As can be seen in Table 2.8, a comparison of coarse-grain and fine-pitch CMOS-MEMS has been demonstrated. It should be noted that the stack thickness can be roughly 5 μm thick by including two more metal layers, making the total stack thickness comparable to coarse-grain CMOS-MEMS. The reason why this was not done was to keep the resonator thickness as homogenous as possible in order to reduce delamination and curling effects. Fine-pitch CMOS has even less parasitics compared to coarse-grain CMOS, and the power consumption is much less due to a lower V_{DD}. The foundry design rules for 90 and 65 nm CMOS are much more stringent and demanding compared to the 0.25 and 0.35 μm CMOS processes, requiring more of the designer to be able to implement the wanted micromechanical structures. However, through the usage of Verilog-A code it is possible to make semi-automated layout design which will satisfy the foundry rules. With clever layout design and resonator architecture, fine-pitch CMOS can offer even better results than coarse-grain CMOS-MEMS.

This chapter has gone through some examples of utilizing MEMS with CMOS circuitry and described various methods of how to combine CMOS and MEMS. The chosen implementation method has been explained with examples of tentative derived design rules for fine-pitch CMOS-MEMS designs. With the implementation method being explained, the functionality and description of the resonator is described in chapter 3.

Chapter 3

Resonator modeling

VIBRATING beams inhibits behavior of self resonating modes which produces distinct frequencies with maximum throughput, thus making it possible to use resonating beams as signal processing elements. These self resonating modes are due to a dynamic behavior of external forces which in turn generates a spring effect from the beam; a force generated internally in the beam which counteracts the external force. This spring effect results in a movement of the beam at distinct frequencies. It is possible to register this self resonating dynamic behavior of a beam if the surrounding ambient does not produce a damping which is greater than the internal spring force from the beam. A beam at a self-resonating mode will vibrate back and forth until an external or internal damping mechanism limits this vibration. Modeling of the resonator and its self resonating modes is necessary in order to build more complex MEMS resonator filters. This chapter will describe how beams can have different modes and show the model for an electromechanical equivalent description. Finally this chapter will go through some damping mechanisms, non-linear effects and a method of increasing resonator throughput by using a gap reduction technique.

3.1 Mechanical beam model

By using the Euler-Bernoulli beam theory [29, 30], it is possible to find a static spring stiffness and a dynamic resonating frequency. The Euler-Bernoulli beam theory is valid for beams with a length to width ratio of 10 or more and assumes that translational and angular shear forces are small compared to the bending deformation.

$$EI\frac{d^4z}{dx^4} + \rho A\frac{d^2z}{dt^2} = 0 \tag{3.1}$$

The dynamic beam behavior is described in eq. 3.1. E is the Young's Modulus, I is the area moment of inertia, ρ is beam density and A is the cross section area. $z(x,t)$ is the amount of bending of the beam depending on the position x throughout the beam length where the time part of z is disregarded in this analysis:

$$z(x) = C_1 sin(\beta x) + C_2 cos(\beta x) + C_3 sinh(\beta x) + C_4 cosh(\beta x) \tag{3.2}$$

The trial solution in eq. 3.2 is used to find solutions for the radial frequency of the beam that have different boundary conditions. The mode number β_N (where $\beta_N = \beta x$) in eq. 3.2 is related to the radial frequency of the beam:

$$\omega_0^2 = \frac{EI}{\rho A}\beta_N^4 \tag{3.3}$$

$$f_{0,nom} = \kappa \frac{\beta_N^2}{4\pi\sqrt{3}}\sqrt{\frac{E}{\rho}}\frac{W}{L^2} \tag{3.4}$$

The radial frequency is related to the resonance frequency by $\omega_0 = 2\pi f_{0,nom}$. Eq. 3.4 is a rearranged version of eq. 3.3 where a scaling factor κ has been introduced to model a possible frequency shift due to topological variations of the resonator [31]. W is the resonator width and L is the resonator length. Eq. 3.4 is very important in this work as it is used to model different resonator types which will have different resonance frequencies depending on the mode number β_N.

Fig. 3.1 shows two different boundary conditions. The derivative of $z(x)$ up to three times results in the momentum M ($z'(x) = M$), the angle θ ($z''(x) = \theta$) or the shear force V ($z'''(x) = V$). The clamped condition has a boundary axis which is fixed and it has zero displacement and bending because that part can not move. The clamped condition has a momentum and shear forces. The right side of Fig. 3.1 is the pinned condition where the boundary axis is not fixed, but the circular dot in the middle is fixed, making it a fixed point. The pinned condition will not experience displacement nor momentum, but it will have a bending angle and shear forces.

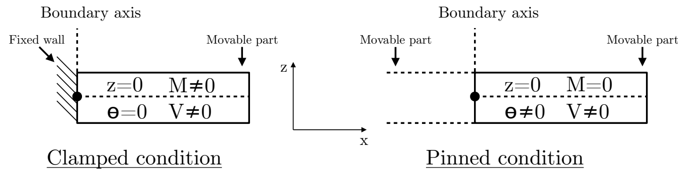


Figure 3.1: Two beam boundary conditions

For beams connected at one or two ends in various ways, the two boundary conditions of Fig. 3.1 can then be used in eq. 3.2. The general characteristic equation for beam bending can be solved by using boundary conditions that are known.

In this work, there are five different beam boundary conditions which are used as can be seen in Fig. 3.2. A Clamped-Clamped (CC) condition means that both ends will not have any angle, but the Pinned-Pinned (PP) condition shows that there will be an angle at the point where it is fixed. The Clamped-Free (CF) condition in this work is referred to as a cantilever beam. The Clamped-Pinned (CP) condition is another important beam type used in this thesis.

A final important bending condition for the beams is the Free-Free (FF) condition. This mode can in one sense be seen upon as a Pinned-Pinned mode with

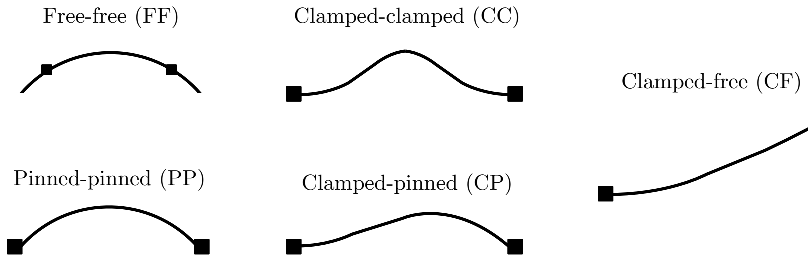


Figure 3.2: The 5 different boundary conditions

additional beams attached to its end. However, the fixed points are located at strategically $\lambda/4$ and $3\lambda/4$ positions on the beam. This will make the free ends bend in an opposite direction as the middle part of the beam, making it vibrate back and forth as one vibrating beam. The Free-Free beam can lead to certain advantages as will be explained in chapter 3.3.

Boundary condition	β_1	β_2	β_3
Clamped-Free (CF)	1.875105	4.694091	7.854757
Clamped-Pinned (CP)	3.92660231	7.06858275	10.21017612
Pinned-Pinned (PP)	π	2π	3π
Clamped-Clamped (CC)	4.73004074	7.85320462	10.9956079
Free-Free (FF)	4.73004074	7.85320462	10.9956079

Table 3.1: 3 mode numbers for various beam clamping conditions

Finding the mode numbers for the beams presented in Fig. 3.2 is possible by using the same general beam bending movement (eq. 3.2). The mode numbers for all five beam types are shown in Table 3.1. The details on finding these mode numbers are more thoroughly explained in chapter **A** in the appendix. These five beam conditions, their mode numbers and equation 3.4 are important as they are used extensively in this work. Not all of these five beam conditions are to be used as resonators, but anchoring beams and coupling beams will be used which have mode numbers different from the actual resonator.

All of these beam types will, regardless of boundary type, have a certain static mass given by:

$$m_{static} = \rho LWH \tag{3.5}$$

where H is the thickness of the beam. A vibrating beam, however, will not have a constant mass throughout the beam length due to the fact that kinetic energy must be constant:

$$E_k = \frac{1}{2}mv^2 = \frac{1}{2}\rho A \int_0^L v^2\left(x'\right)dx' \tag{3.6}$$

Because the velocity of the beam will vary depending on the location x throughout the beam length, the mass must also vary in order for the kinetic energy to

remain constant. By integrating the length L from the start of the beam to the end of the beam and dividing that by a non-integrated E_k term, it is possible to obtain the effective mass:

$$m_{eff}(x) = \frac{E_k}{\frac{1}{2}v(x)^2} = \frac{\frac{1}{2}\rho A \int_0^L v\left(x'\right)^2 dx'}{\frac{1}{2}v(x)^2}$$

where the velocity is defined as

$$v^2(x) = -\omega^2 x^2_{mode}(x)$$

and where x_{mode} is a description of the deflection of the beam relative to x, and ω is the angular velocity. As an example of this, eq. 3.7 describes the beam shape of a cantilever beam

$$x_{mode}(x) = z \cdot \gamma(sin\beta x - sinh\beta x + \alpha(cosh\beta x - cos\beta x)) \tag{3.7}$$

where $\gamma = 0.367$, $\beta = \frac{1.875}{L}$ and $\alpha = 1.362$ [26]. z is the maximum deflection that the beam experiences which will be due to electrostatic forces as described in section 3.2. For the cantilever beam, a maximum amplitude occurs for $x = L$. By inserting the x_{mode} equation and the velocity equation in the general effective mass equation yields:

$$m_{eff}(x) = \frac{\rho W H \int_0^L \left[x_{mode}(x')\right]^2 dx'}{\left[x_{mode}(x)\right]^2} \tag{3.8}$$

The modeling of resonators with effective mass is shown in eq. 3.8 where the dynamic behavior of the beam is taken into consideration. The effective mass will be larger towards any anchored ends and have its minimum at parts of the beam which is displaced the most. For the cantilever beam, the lowest effective mass is experienced at the tip of the cantilever which is lower than the calculated static mass (m_{static}). The Free-Free, Pinned-Pinned and Clamped-Clamped beam types follow the same type of analysis to find the effective mass, each with its own x_{mode}. Most resonators used in this work has the lowest effective mass at the middle of the beam due to pinned or clamped conditions at the start and at the end of the beam. A special case occurs for the CC and FF boundary condition where their mode number (and resonance frequency) are the same, but their beam mode shape is different resulting in a slightly different effective mass.

The stiffness of the beam can be obtained through a static analysis similar to the dynamic analysis which was performed earlier in this section. However, due to the fact that effective mass is not constant throughout the beam length means that the mechanical spring stiffness, k_m, must also vary throughout the beam length:

$$\omega_0 = \sqrt{\frac{k_m}{m_{eff}}} \rightarrow k_m(x) = \omega_0^2 m_{eff}(x) \tag{3.9}$$

ω_0 is obtained from eq. 3.3 or eq. 3.4 where β_N depends on the type of beam boundary condition. As with m_{eff}, k_m will have its minimum value where maximum beam displacement occurs and k_m will be rather large towards its anchoring points.

3.2 Electromechanical resonator description

The previous section described the vibrating beam as a pure mechanical device. To make the beam vibrate back and forth at various frequencies is possible by using electromagnetic, piezoelectric, magnetostrictive, electrostrictive or thermal actuation [32]. This work will use the electrostatic actuation principle due to relatively good coupling efficiency, speed and its simplicity. If the beam experiences an external force, the net force the on the beam must be zero at all times and is given by

$$F_{net} = F_{el} + F_{mech} = -\frac{\varepsilon_0 A_e V^2}{2g^2} + k(g_0 - g) = 0 \tag{3.10}$$

where $z = g_0 - g$. The total net force is the sum of the electrostatic force F_{el} and the mechanical force F_{mech}. The electrostatic force has an opposite sign compared to the mechanical force. The mechanical force F_{mech} is given by Hooke's law $F = kz$. This mechanical term opposes the electrical force which initiates displacement of the beam. The electrostatic force equation originates from potential energy equation:

$$E_p = \frac{CV^2}{2} \rightarrow F_{el} = -\frac{dE_p}{dg} = -\frac{V^2}{2}\frac{dC}{dg} \tag{3.11}$$

where $C = \frac{\varepsilon_0 A_e}{g}$. The solution in eq. 3.10 becomes unstable for a small change of the net force divided by a small change of the gap less than zero ($dF_{net}/dg < 0$). This unstable area is not used for resonators but typically applied for mechanical switches which cause the beam to collapse onto the electrode. The resonator must therefore have a voltage lower than the pull-in voltage which is defined as

$$V_{pi} = \sqrt{\frac{8kg_0}{27\varepsilon_0 A_e}} \tag{3.12}$$

The pull-in voltage becomes low for a small spring stiffness, low initial gap (g_0) or large electrode area (A_e). The resonator must be operated at voltage levels lower than V_{pi}. It should be mentioned that the analysis provided here is based on a linear Hooke's law and the parallel-plate theory, assuming that the displacement of the beam is the same throughout the beam length, something which is not necessarily the case for the different beams in this thesis. If the beam displacement is only a fraction compared to the beam length, these simple equations can be used. However, Finite Element Method (FEM) simulations must still be performed to compare with analytical calculations. If the analytical equations are too coarse-grain compared to the simulation results, expanding the resonator equations with non-linear capacitive or stiffness terms will make the results more comparable with FEM simulations. Non-linear resonator behavior is explained in section 3.4. The effective spring stiffness of the resonator is defined as k and is given by:

$$k = k_m - k_e \tag{3.13}$$

where k_e the electrical spring stiffness. The effective beam stiffness is obtained by subtracting the electrical spring stiffness from the mechanical spring stiffness [31].

Large voltage values can cause a noticeable reduction of k as k_e becomes large enough. This effect is known as spring softening due to reduction of the effective spring stiffness k in $\omega_0^2 = \frac{k}{m_{eff}}$. This softening of the spring stiffness may result in a non-linear behavior of the beam. It is possible for the beam to also experience a stiffening effect. Both of these effects are more described in section 3.4.

Beams that are stimulated with a sinusoidal electrostatic force has a counteracting mechanical force which opposes the electrostatic force which causes the beam to move back and forth; the beam starts oscillating. For an ideal case without any damping, the beam would vibrate back and forth infinitely. However, the real world will provide damping to these mechanical systems. Any vibrating beam with damping mechanisms will follow

$$F_{el} = m_{eff}\frac{d^2z}{dt^2} + b\frac{dz}{dt} + kz \tag{3.14}$$

where F_{el} is the electrostatic force which initiates oscillation and b is a damping term. Eq. 3.14 shows the physical behavior for a beam opposing the electrostatic force. By using LaPlace and rearranging, this relationship can be rewritten as a function of displacement $z(j\omega)$

$$z(j\omega) = \frac{F_{el}(j\omega)}{k}\frac{1}{1 + \frac{j\omega}{Q\omega_0} - (\frac{\omega}{\omega_0})^2} \tag{3.15}$$

Eq. 3.15 shows the resonator displacement response as a function of frequency. If $\omega = \omega_0$ then the $\frac{F_{el}(j\omega)}{k}$ term becomes amplified by Q, thus enhancing the resonator displacement by the resonator Q-factor. For really large Q-factors, the displacement may become rather large:

$$z(\omega = \omega_0) = \frac{F_{el}Q}{k} \tag{3.16}$$

The resonator displacement at the first resonance mode of the beam is given in eq. 3.16. The electrostatic force F_{el} was previously stated in 3.11 but is now redefined as:

$$F_{el} = V_{ac}\frac{\varepsilon_0 A_e V_P}{g^2} \tag{3.17}$$

The V^2 in eq. 3.11 has now been replaced by V_{ac} and V_P. It turns out that $V^2 = V_{ac}^2 sin^2(\omega_0 t)$ will cause the resonator to oscillate at $sin(2\omega_0 t)$ in addition to $sin(\omega_0 t)$. By using a DC polarization voltage (V_P), the resonator will resonate at the desired frequency. For this to be possible, V_P must be orders of magnitude larger than V_{ac}. V_P will act as an amplifying term for the resonator, allowing an increase in resonator throughput.

Eq. 3.14 stated that an oscillating behavior is stimulated from the electrical force F_{el}. A simple schematic of a mechanical oscillating system and its electrical equivalent is shown in Fig. 3.3. The left part of Fig. 3.3 shows F_{el} attracting a beam

mass m which has a damping factor b and coupling to an anchored wall through the beam stiffness k. The right part of Fig. 3.3 shows the electrical equivalent of the mechanical model. Analyzing the electrical schematic results in a transfer function which is comparable with the mechanical transfer function. From this comparison it can be seen that the mass is proportional to the inductor (L), the spring stiffness k is inversely proportional to the capacitor ($1/C$) and the damping b is proportional to the resistor (R).

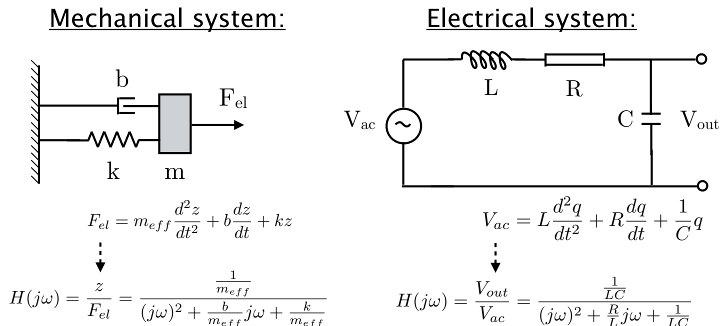


Figure 3.3: Schematic comparison of a mechanical and electrical system

The LCR schematic of Fig. 3.3 is a direct conversion schematic of mechanical components to electrical ones. A more accurate schematic for the resonator is developed which takes into account a transformation between the mechanical and electrical domain. Eq. 3.17 showed that F_{el} will increase linearly with V_{ac} due to V_P. From eq. 3.17 it is now possible to define this linearized relationship:

$$F_{el} = \eta V_{ac} \; where \; \eta = V_P \frac{dC}{dz} = V_P \frac{\varepsilon_0 A_e}{g^2} \tag{3.18}$$

Eq. 3.18 shows an important parameter, the electromechanical coupling coefficient η. The η is valid for small perturbations of the beam and represents the winding ratio of the schematic equivalent of the resonator. Explained in a simple manner, the η describes the winding ratio of a transformer, converting the electrical signal to a mechanical signal. As the vibrating beam is a mechanical device, this part of the resonator schematic is really just a mechanical response induced by an electrostatic force. Going from the resonator to an output electrode, the output from the resonator goes through a transformer with winding ratio which represents going from the mechanical energy domain to the electrical energy domain again.

The equivalent schematic of the resonator with transformers is shown in Fig. 3.4. The resonator is described by l_z, c_z and r_z that are assigned in lower case to specify that these are component values in the mechanical domain. Looking at the resonator from the outside of this two-port schematic, the l_z, c_z and r_z are turned into L_z, C_z and R_z by removing the transformers and including η. The upper case LCR values then represents the electrical values as seen in or out of this "black box" which represents the resonator.

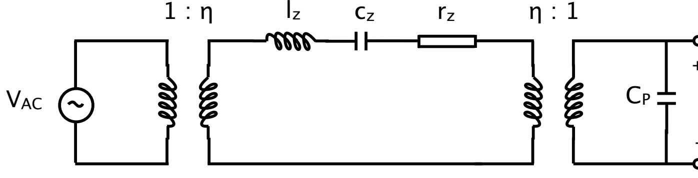


Figure 3.4: Simple electromechanical resonator schematic

$$L_z = \frac{m_{eff}}{\eta^2} \tag{3.19}$$

$$C_z = \frac{\eta^2}{k} \tag{3.20}$$

$$R_z = \frac{\sqrt{k m_{eff}}}{Q\eta^2} \tag{3.21}$$

Eq. 3.19-3.21 shows that L_z, C_z and R_z are converted into electrical component equivalents in the electrical domain through the usage of η. R_z can be represented in an alternative way:

$$R_z = \frac{kg^4}{\omega_0 Q \varepsilon_0^2 A_e^2 V_P^2} \tag{3.22}$$

Eq. 3.22 shows the resonator motional impedance [31]. This is one of the most important equations when describing the performance of a resonator. This value should typically be around 50 Ω, thus matching any previous or following circuitry.

Achieving a very low R_z is possible by a low electrostatic gap g, a large electrode area A_e, a large polarization voltage V_P or a large resonator Q-factor. There is a lot of ongoing research on various methods of how to achieve a very low R_z value by different means. This could for example be tuning the process thus allowing a small gap or a large electrode area, applying a large V_P or make the MEMS resonator using a material which inhibits a very low intrinsic loss and therefore resulting in a large Q-factor. The latter example is possible by making the MEMS resonator out of a material such as diamond [33].

This work does not focus on trying to fine tune the process to achieve a very low R_z value. However, what is of focus in this work is the investigation of expanding CMOS by using MEMS to simplify signal processing. This does not mean that R_z can be designed to be huge, however it is possible to allow it to have a value in the few tenths to hundred of kΩ (in contrast to sub kΩ in other research literature). This is possible by having control of the following on-chip amplifier accompanying the resonator. More details on total filter description of CMOS-MEMS resonators with important performance parameters are described more throughout this thesis.

$$i_o = V_P \frac{dC}{dt} = V_P \frac{dC}{dz}\frac{dz}{dt} = \frac{\omega_0 Q \varepsilon_0^2 A_e^2}{kg^4} V_P^2 V_{ac} \tag{3.23}$$

Eq. 3.23 shows the resonator output motional current which arises from a time varying capacitance (dC/dt) multiplied by the polarization voltage across the gap at the output of the resonator. This term can be split into dC/dz times dz/dt where the time varying part can be replaced by $z\omega_0$. Alternatively, eq. 3.23 can be obtained by from eq. 3.22 and assuming that L_z and C_z are of equal value during resonance, thus canceling each other. The i_o for micromechanical resonators is typically on the orders of a few nA up to a few hundred nA.

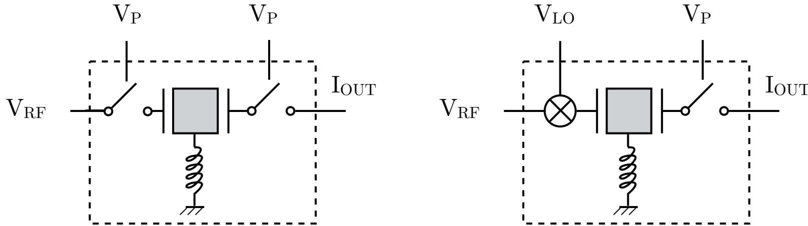


Figure 3.5: Filter and mixer-filter resonator symbol

Fig. 3.5 shows the symbol of the micromechanical component as a schematic symbol. The left part shows the symbol of a 2-port MEMS resonator filter with a spring-mass-dashpot attached to it. Internal routing of the resonator may allow different terminals inside the resonator itself, thus allowing two V_P terminals. These may be connected together or can be two different voltages, depending on the desired usage of the device. By referring to Fig. 3.4, the left V_P is the left transformer and the right V_P is the right transformer.

In the right part of Fig. 3.5, the resonator is connected as a mixer-filter. It is almost the same symbol, except that one of the V_P terminals has been replaced by a mixer symbol and a V_{LO} terminal. This allows the possible mixing of $V_{RF}cos(\omega_{RF}t)$ with $V_{LO}cos(\omega_{LO}t)$. The internal routing of the resonators gives the flexibility of both doing mixing and filtering of a signal at the same time, which in transceiver architectures are typically done with two different components. Eq. 3.24 and 3.25 describes the down-mixing functionality of frequency and electrostatic forces due to the mixing of the V^2 term from eq. 3.10 [34]:

$$\omega_{IF} = \omega_0 = \omega_{RF} - \omega_{LO} \tag{3.24}$$

$$F_{el,mixer-filter} = V_{RF}\frac{\varepsilon_0 A_e V_{LO}}{2g^2}cos\left([\omega_{RF} - \omega_{LO}]t\right) \tag{3.25}$$

Both symbols of Fig. 3.5 results in a filtered motional current out from the resonator. This current needs to be converted to a voltage for further signal processing. The conversion through the resonator filter (or mixer-filter) is a voltage-to-current conversion. As will be discussed in chapter 5.3, this current can be converted back to a voltage with a unity gain conversion (i.e. 1 V in, the output is a filtered 1 V signal out).

3.3 Damping mechanisms and the Q-factor

Vibrating beams that are to be used as filtering components inhibits a dynamical oscillating behavior. Because of the complex transfer function of the system, for certain frequency modes, the system will be located between being able to oscillate and be damped due to imaginary and real parts in the transfer function. This can be represented as a graph with an imaginary axis being the oscillation and a real axis being the damping as seen in Fig. 3.6.

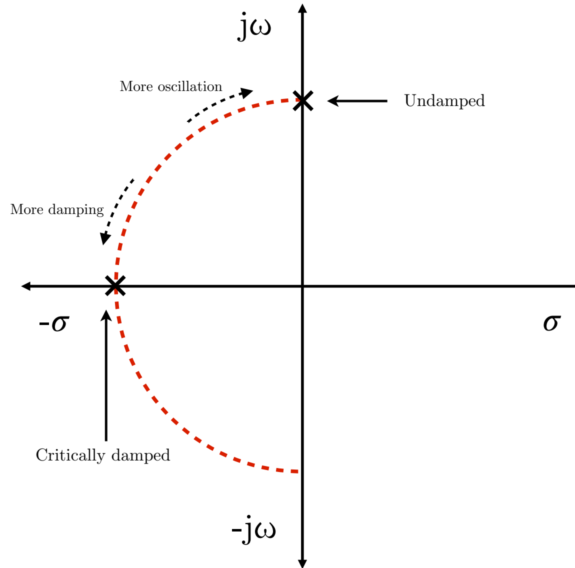


Figure 3.6: Examples of a critically damped or undamped micromechanical system

In reality these vibrating beams will have a damping factor which will cause a stable system to reside in the left half of the complex plane. For Q-factors larger than $1/\sqrt{2}$ allows for oscillation of micromechanical beams [35]. The Q-factor is an important parameter which defines the gain of the system. The transfer function for the resonator is shown below:

$$H(j\omega) = \frac{\frac{1}{LC}}{\frac{1}{LC} + \frac{R}{L}j\omega + (j\omega)^2} = \frac{\omega_0^2}{\omega_0^2 + \frac{\omega_0}{Q}j\omega + (j\omega)^2} \tag{3.26}$$

The left part of eq. 3.26 describes the resonator as an electromechanical LCR transfer function with $\omega_0 = 1/\sqrt{LC}$. The R/L can be shown to be equal to b/m_{eff} as was described earlier. The right part of eq. 3.26 shows that the system is only related to ω_0 and the Q-factor. The resistive part R_z creates the damping part, while the L_z and C_z creates the oscillating part for the transfer function. Eq. 3.21 shows that R_z is inversely proportional to the Q-factor.

It is desirable to have a low R_z value in order to match previous or following signal processing parts and because narrow filter bandwidth may be desirable. In the end, tweaking the geometry to achieve a low R_z will at some point reach a limit, which is why it is important to focus on achieving a large Q-factor for these micromechanical systems. It should be mentioned that for frequencies above the GHz range, the Q-factor must be on the order of hundreds of thousands in order to achieve sufficient performance. This work relates to frequencies below the GHz area for WSN nodes, something which will place a less stringent requirement on the Q-factor.

Estimating and calculating the Q-factor for these micromechanical filter systems is a difficult task, it could be possible to write a thesis on that topic itself. Trying to precisely define the Q-factor becomes out of scope for this thesis, so the main damping mechanisms will be explained here and crude estimations of the Q-factor for CMOS-MEMS resonators. The usual definition of the Q-factor is:

$$Q = 2\pi \frac{W}{\Delta W} \tag{3.27}$$

Eq. 3.27 defines Q as energy stored (W) over energy dissipated per cycle (ΔW), specified in radians. In short, micromechanical systems have various damping terms. Finding the loss mechanisms and the energy stored is a difficult task. Instead, it is typical to define damping terms that are inverse Q-factor:

$$\frac{1}{Q} = \frac{1}{Q_{Air}} + \frac{1}{Q_{TED}} + \frac{1}{Q_{Surface}} + \frac{1}{Q_{Anchor}} \tag{3.28}$$

Eq. 3.28 describes the total inverse Q-factor as a sum of four inverse Q-factor (damping) terms: Air, Thermoelastic damping (TED), Surface damping and damping through anchoring parts [36, 37, 38]. There may be more terms which contribute to damping, however these are the most important ones. The largest $1/Q_{term}$ will be the dominating part which in turn will contribute to most damping.

The first term is Q_{Air} which is damping due to energy loss through the surrounding environment. The surroundings may be air or vacuum depending on the conditions and is given by

$$Q_{Air} = \frac{k}{\omega_0 b_{sq}} \tag{3.29}$$

where b_{sq} is a damping factor obtained from rectangular parallel-plate geometry calculated using Reynolds gas-film (squeeze film) equation:

$$b_{sq} = \frac{3}{2\pi} \mu \frac{A_e}{g^2} \tag{3.30}$$

where $\mu = 1.78 \cdot 10^5$ for air and is a coefficient which describes the viscosity of the surroundings and depends on pressure and the mean free path of the gas molecules. Notice that eq. 3.29 was obtained from eq. 3.21 where the Q in that equation is the total Q-factor of the system while eq. 3.29 is used to just find the Q_{Air} term.

The second term is due to movement of beams which may cause a generation of thermal energy which causes damping:

$$Q_{TED} = \frac{E\alpha_T^2 T_0}{C_P}\frac{\omega\tau}{1+\omega\tau} \tag{3.31}$$

where τ is defined as

$$\tau = \frac{C_P W^2}{C_T \pi^2} \tag{3.32}$$

C_P is the specific heat at constant pressure of the material, α_T is the Thermal Coefficient of Expansion (TCE), T_0 is the environmental temperature, C_T is the thermal conductivity of the beam and ω is the angular frequency of the resonator.

The third damping term is $1/Q_{Surface}$ that is a result of energy loss mechanisms of surface loss:

$$Q_{Surface} = \frac{WH}{3W+H}\frac{E}{2E_{ds}\delta} \tag{3.33}$$

where δ is the characterized thickness of the surface layer and E_{ds} is a constant which is related to surface stress.

Finally, the $1/Q_{Anchor}$ defines the damping and loss of energy due to energy being pumped into the anchoring parts of the resonator:

$$Q_{Anchor} = 2\pi\frac{E_{k,tot}}{E_{loss}} \tag{3.34}$$

The stored flexural energy is defined as $E_{k,tot}$ which varies for each resonant mode and is expressed as:

$$E_{k,tot} = \frac{1}{2}m_{eff}v^2 = \frac{1}{2}\rho HWL\omega_0 Z \tag{3.35}$$

where ω_0 is the resonance frequency at that mode and Z is the maximum vibrational amplitude. E_{loss} is the loss of energy which is dissipated per cycle of vibration through the anchor or support parts into the substrate. For a Clamped-Clamped beam, this is calculated as:

$$E_{loss} = \frac{1.3441+\nu}{EH(1-\nu)}\Gamma_0^2 \tag{3.36}$$

ν is the Poisson ratio for the support beam, Γ_0 is the vibrating shear force of the support. It is evident from eq. 3.34-3.36 that a large geometry, high operating frequency and beam displacement is desirable in order for low loss in the supporting beam of the resonator. As will be shown in chapter 4, it is possible to alleviate some of this anchor loss by designing special support beams with certain dimensions.

As a summary, the $1/Q_{Air}$ term is more or less dependent on a low A_e or large g something which contradicts resonator design methodology. μ is fixed as it depends on the environment conditions. Q_{air} can be kept large by designing for high k while retaining a low mass. The Q_{TED} is a factor which will depend greatly on the type of material and its heat capacity and the thermal coefficient of expansion. In general, as micromechanical resonators scale down the Q_{TED} will decrease, especially for

beams with small widths. The $Q_{Surface}$ is also difficult to design to be large as it also depends on the material parameters. It should be mentioned that the Q-factor could be loaded and reduced in the same manner as the spring stiffness of the resonator [39]. Eq. 3.37 and eq. 3.38 describes this effect:

$$f_0 = f_{0,nom}\sqrt{1 - \frac{k_e}{k_m}} \tag{3.37}$$

$$Q = Q_{nom}\sqrt{1 - \frac{k_e}{k_m}} \tag{3.38}$$

As a conclusion to this section, it should be noted that Q-factor estimations are difficult and time consuming. It requires a good knowledge of the materials involved and the anchoring methods of the resonator. Analytical calculations alone can not provide sufficient estimations without the use of FEM tools. CMOS-MEMS implemented resonators have shown to provide Q-factors between 1000 and 2000 in vacuum conditions and up to 50 in air [28, 40]. The Q-factor estimations in this thesis assume both a Q-factor of 1000 and 2000 in vacuum. For all micromechanical systems there will be a variation of the Q-factor, both with respect to design properties, material properties and environmental conditions which will cause the Q-factor to fluctuate from device to device. It is possible to utilize on-chip CMOS circuitry to adjust for lack of gain (low Q-factor) by using amplifiers to achieve a 1:1 conversion factor of the total resonator filter system.

3.4 Non-linearity effects

The displacement z from micromechanical resonators will result in a filtered output current i_o. Both the displacement and current can contain non-linear terms from mechanical or electrical contributions. The electrical contributions are from capacitive effects while mechanical terms can be from strain and deformations, for example causing length elongation of the beam. The mechanical spring stiffness may contain non-linear terms:

$$k_{m,tot} = k_m\left(1 + k_{m1}z + k_{m2}z^2\right) \tag{3.39}$$

The mechanical spring stiffness k_m is the first term and is a linear term. k_{m1} and k_{m2} are higher order terms which are given by

$$k_{m1} = \frac{E_1}{L}, k_{m2} = \frac{E_2}{L^2} \tag{3.40}$$

The E_1 and E_2 in eq. 3.40 are non-linear Young's modulus terms and depends on the type of beam material [41]. In this work, mechanical non-linearity is typically not dominant due to the resonator architectures used. Pure Clamped-Clamped beam resonators with large deflections and with a large E will experience more mechanical non-linearity.

Capacitive non-linearities will cause k_e to be non-linear. Typically eq. 3.16 is sufficient to describe resonator displacement. However, when the resonator has a low mechanical stiffness k_m and is at the same time operated with a large V_P value, the linear k_e model may become inaccurate [42, 43]. The electrical stiffness k_e with non-linear terms is modeled as:

$$k_{e,tot} = k_e \left(1 + k_{e1}z + k_{e2}z^2 + ...k_{en}z^n\right) \tag{3.41}$$

Eq. 3.41 shows that the electrical spring stiffness consists of higher order terms that all are related to the displacement z. The k_e term is the first term and is linear. k_{e1} and k_{e2} are square and cubic electrical spring coefficients respectively.

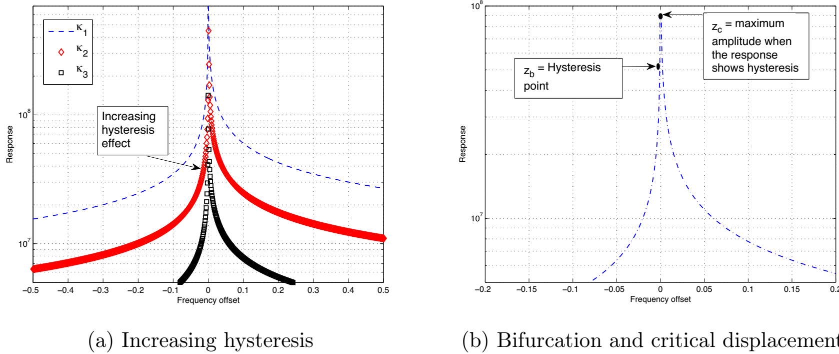
$$k_e = \frac{V_P^2 C}{g^2}, k_{e1} = \frac{3}{2g}, k_{e2} = \frac{2}{g^2} \tag{3.42}$$

The k_e terms contribute to reducing or increasing the frequency depending on which term that dominates. When operating the resonator with high vibration amplitudes, the square and cubic spring stiffness terms will become more dominant. Because the amplitude-frequency curve no longer becomes a single valued function, the oscillation may become chaotic once the amplitude is larger than a critical value known as z_c. The maximum usable vibration value is extracted from the largest value that appears before a bifurcation (hysteresis of the curve). The bifurcation amplitude and critical amplitude are respectively [42]:

$$z_b = \frac{1}{\sqrt{\sqrt{3}Q|\kappa|}}, z_c = \frac{2}{\sqrt{3\sqrt{3}Q|\kappa|}} \tag{3.43}$$

where

$$\kappa = \frac{3k_{e2}k_e}{8k} - \frac{5k_{e1}^2 k_e^2}{12k^2} \tag{3.44}$$



(a) Increasing hysteresis (b) Bifurcation and critical displacement

Figure 3.7: Non-linear resonator behavior and possible hysteresis effect

Fig. 3.7(a) is an example of how κ will affect the response from the resonator. κ_1 is the lowest value and κ_3 is the largest value. In this example, κ is negative and contributes to a reduction of the resonance frequency as well as tilting the curve to the left. κ_1 is the lowest value and shows less tilting of the curve. When the negative value of κ is too large (see κ_3), the curve enters a state of hysteresis. At the point when the hysteresis starts, the bifurcation amplitude z_b is reached (see Fig. 3.7(b). For any curve with a hysteresis, the maximum usable amplitude of vibration is z_c as shown in Fig. 3.7(b). z_c is always larger than z_b and ultimately sets the limit for the maximum vibration amplitude as well as it sets the maximum output current out from the resonator. κ is a factor which will contribute to a modified resonance frequency due to the spring stiffness non-linearities. The new resonance frequency is therefore expressed as

$$\omega_{0(effective)} = \omega_0 \left(1 + \kappa z^2\right) \tag{3.45}$$

Equation 3.44 and eq. 3.45 shows that the κ will either increase (the resonator becomes more stiff) the operational resonance frequency or decrease the resonance frequency. The resonator used here will have a negative κ, thus the capacitive non-linearities will contribute to reduce the electrical spring stiffness. Because κ contributes to "soften" and tilt the output response, V_P should be reduced. By using equation 3.43 and 3.44, an expression for the maximum output current possible from the resonator can be developed:

$$i_o^{max} = \eta \omega_0 z_c \tag{3.46}$$

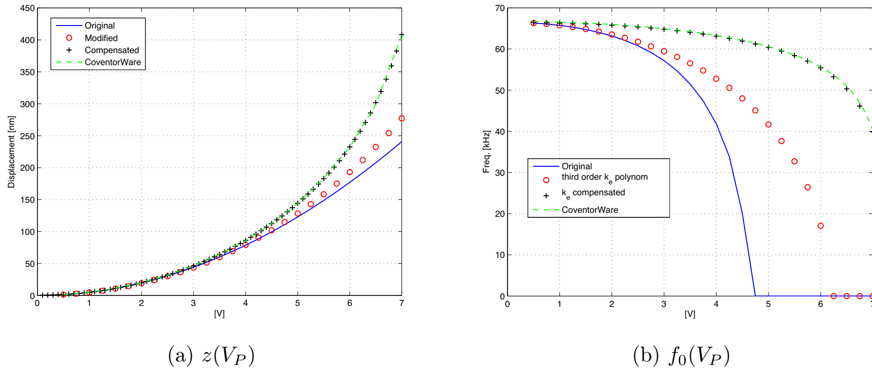
i_o^{max} sets the limit for how much current that can be detected at the output electrode before bifurcation (the hysteresis). It is also possible to define the maximum energy stored in the resonator by using z_c in a similar manner

$$E_{stored}^{max} = \frac{1}{2} k z_c^2 \tag{3.47}$$

where k is the linear spring constant ($k = k_m - k_e$). The maximum energy stored also decides the energy dissipation out from the resonator which is

$$P_{dissipated} = R_z i_o^2 = \frac{\omega_0 E_{stored}^{max}}{Q} = \frac{\omega_0 k z_c^2}{2Q} \tag{3.48}$$

Fig. 3.8 is an example of a resonator with a low k where V_P is increased. The result is an increase in the displacement and a reduction of the resonance frequency. The displacement equation is relatively inaccurate for a very soft beam and a large electrostatic coupling (i.e. small gap and/or large electrode area). By taking into account non-linear capacitive contributions as well as possible mechanical beam stiffening terms, the displacement is adjusted as seen in Fig. 3.8(a) (the green line). In Fig. 3.8(b), the resonance frequency is more rapidly reduced for an increased V_P compared to the FEM simulation. The FEM simulator is more accurate and takes these non-linear terms into consideration. A compensated term has been included here as well to get close to the results from the FEM simulator.



(a) $z(V_P)$ (b) $f_0(V_P)$

Figure 3.8: Analytical and FEM simulation comparison of z and f_0

As can be seen in Fig. 3.9, the initial sweep of V_P hardly increases the displacement of the resonator. Beyond a certain voltage, the displacement starts to increase rapidly. Critical displacement is defined in eq. 3.43 and when the resonator displacement crosses this value, the resonator enters a highly non-linear domain and chaotic behavior occurs. The importance of investigating z_b, z_c and κ is to find the maximum motional current (eq. 3.46) and the power handling capability of the resonator (eq. 3.48). For all resonator filters and oscillators, this chaotic behavior must be avoided, thus z_c sets the limit of the vibration amplitude.

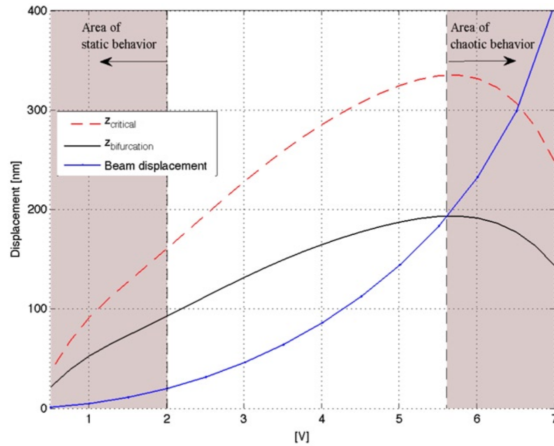


Figure 3.9: Displacement as a function of V_P showing critical displacement

3.5 Gap reduction technique

As mentioned earlier, a low gap between the electrode and the resonator or a large electrode area results in an increased electrostatic coupling and therefore a reduced R_z. The thickness of a post-CMOS resonator depends on the amount of metal layers and the thickness of the metal layers provided from the CMOS process. The thickness of a metal-dielectric stack is about 3 to 5 μm, thus limiting A_e. As this work does not focus on tuning a CMOS-MEMS process, a method on gap reduction after processing has been implemented. The method is based on utilizing built in stress differences internally in electrode beams. These electrodes are known as Self-Assembly (SA) beams which will move laterally after being released, creating a narrow gap. The SA beam is demonstrated in Fig. 3.10 with before etch (left side) and the released SA beam after etch (right side).

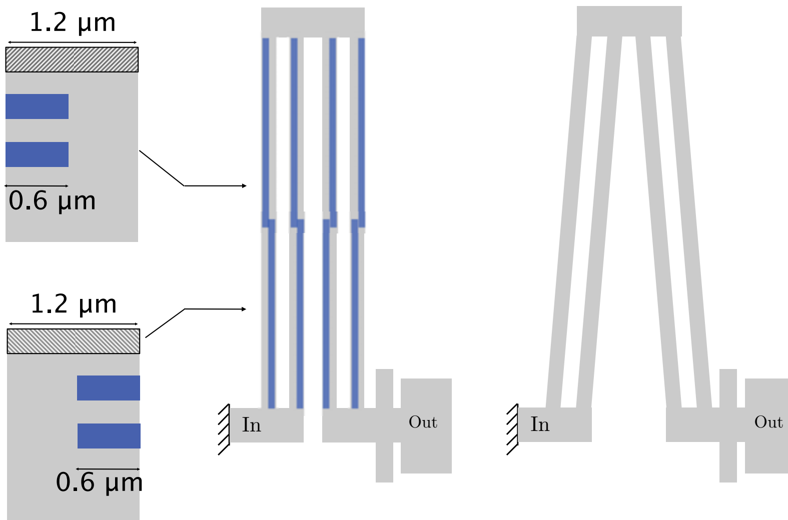


Figure 3.10: The Self-Assembly principle

As can be seen in Fig. 3.10, long thin beams are anchored at one end and free to move in the other end. For one half of the beam, half the beam width has more metal layers on one side. A top metal layer acts as a mask and makes it possible to have more dielectric on the other side. The second half of the beam is the exact opposite where the metal and the dielectric has switched sides.

This structure is a bimorph beam with two different materials. The dielectric and metal layers will have different Thermal Coefficient of Expansion (TCE) which will cause an induced stress force between the metal and the dielectric. During the post-CMOS processing, the beam will move laterally due to this built in stress after being etched and released. In order to not physically touch the resonator, the electrode must somehow be stopped. By implementing limit stops as demonstrated

in Fig. 3.11, it is possible to create small gaps that are in the order of 200–300 nm. The stoppers touching each other are internally routed in a way which does not create any short circuit. The resulting gap will depend on any sidewall deposition on the electrode and the limit stops, so the gap is typically 10–50 nm larger than intended. In this work, it turned out that the fine-pitch 90 nm CMOS-MEMS implementations had much less sidewall polymer depositions than the coarse-grain 0.25 and 0.35 μm processes.

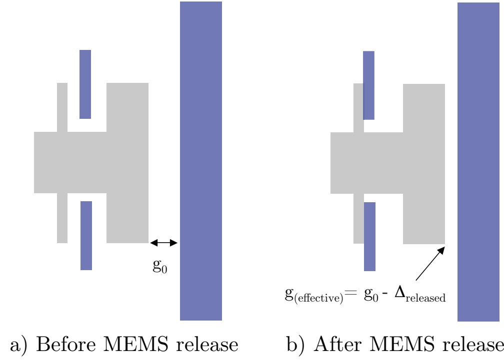


Figure 3.11: Limit stops

The governing equations of these self-assembly beams are based on the bimorph theory [44, 45, 46]. Two materials with a different TCE but equal lateral width will cause the beam to curl laterally according to eq. 3.49:

$$\frac{1}{\rho} = \frac{24(\alpha_2 - \alpha_1)(T - T_0)}{W_{SA}(14 + n + \frac{1}{n})} \tag{3.49}$$

As seen from eq. 3.49, the curvature depends on the difference between the TCE $(\alpha_2 - \alpha_1)$ between the two materials. A small beam width (W_{SA}) will result in more curvature as well. The temperature T and the characteristic temperature T_0 will also affect the curling [46]. From eq. 3.49 it is evident that an increase in temperature will increase the curvature.

$$n = \frac{E_2}{E_1} \tag{3.50}$$

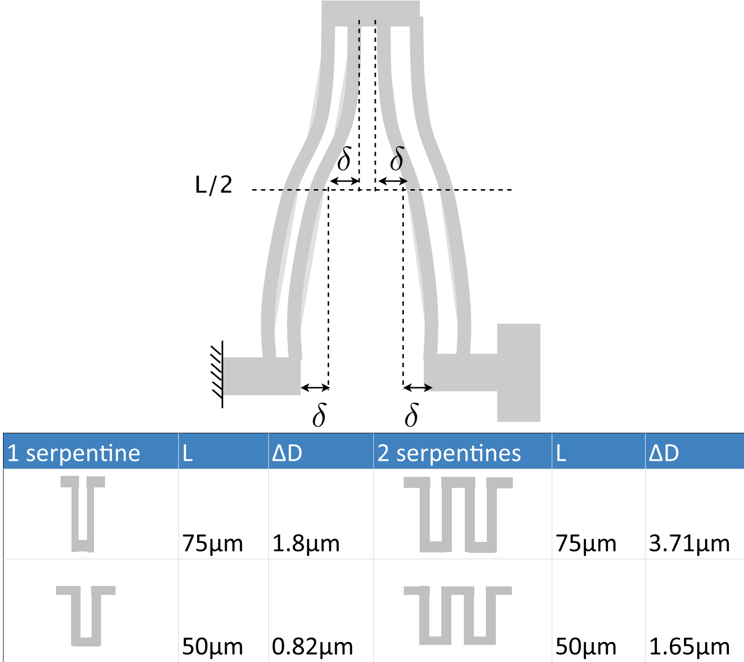
n given in eq. 3.50 is the difference of Young's Modulus between the two materials. δ is the half beam deflection and ΔD is the total deflection of the entire Self-Assembly composite structure. As seen in eq. 3.51, the midway beam deflection depends on the beam length and the curvature. From eq. 3.51 it is evident that a large curvature or long beam length will result in an increased δ.

$$\delta = \frac{(\frac{L}{2})^2}{2\rho} \tag{3.51}$$

The SA electrode can be regarded as four beams where eq. 3.51 indicates the displacement of one of these four beams. The total displacement ΔD is shown to be four times δ:

$$\Delta D = \Sigma_{i=1}^{4} \delta_i = 4\delta \tag{3.52}$$

Fig 3.12 demonstrates the relationships between δ and ΔD more clearly where it is seen that the SA beam can be regarded as four half-beam deflections:



1 serpentine	L	ΔD	2 serpentines	L	ΔD
	75µm	1.8µm		75µm	3.71µm
	50µm	0.82µm		50µm	1.65µm

Figure 3.12: SA half beam displacement and calculations of beam displacement

The bottom part of Fig. 3.12 is an estimation of how much the SA electrode will move after release. These estimations are relatively similar for all of the technology nodes in this work. The calculations in Fig. 3.12 are based on a TSMC 0.35 μm process. In this work, SA electrodes were placed close to each other, which required smaller beam lengths in order to not overlap other structures. This required that the SA electrodes were designed with a smaller length.

As seen in eq. 3.51, a reduction of the length will drastically reduce the displacement of the SA electrode. By making the SA electrodes as 2 serpentine beams it is possible to achieve the required displacement. As an example of this, for a desired gap of 300 nm requires a designed gap of 1.8 μm and a SA displacement of 1.5 μm. According to Fig. 3.12, 75 μm long beams with one serpentine or 50 μm long beams with two serpentines will move 1.8 and 1.65 μm respectively, which is more than the required 1.5 μm.

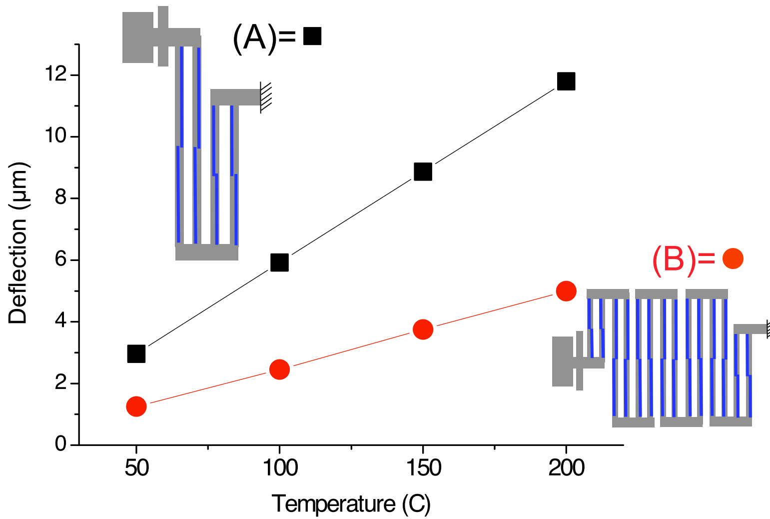


Figure 3.13: Calculating Self-Assembly displacement as a function of temperature

The lateral deflection of these SA electrodes will also depend on the temperature according to eq. 3.49. As the temperature is increased, the displacement will increase significantly as seen in Fig. 3.13. SA electrode A is a modified SA electrode with slightly shorter length to the anchoring point compared to the movable end in order to fit in more complex layouts as will be shown later in this thesis. SA electrode B has multiple serpentines and is less dependent on the temperature. Both SA designs will meet a limit stop, thus the displacement will not increase for an increased temperature. However, for excess temperatures, out-of-plane curling may cause the beam to no longer to touch the limit stops, resulting in a lateral and out-of-plane displacement at the same time. Research on reducing those effects should be further investigated.

A Wyco measurement of a double-jointed SA electrode is shown in Fig. 3.14. It can be seen from Fig. 3.14 that the lateral displacement is much larger than the out-of-plane curling which is hardly visible. Out-of-plane curling was explained in chapter 2.2 with a suggestion for reducing curling seen in Fig. 2.14. Another method of reducing this out-of-plane curling effect can be done by using temperature compensated structures [47, 48].

It is possible to make the SA move laterally after release by including polysilicon (heating) resistors at the bottom of the beams. From this polyresistor loop, an increased current will induce motion of the SA electrode due to the different TCE as explained earlier. This work has not focused on implementing poly-heaters to move the SA electrodes after release, but for certain applications this can be used as a feature to lock electrodes to create more controlled gaps between structures [49]. Be aware that too large currents may cause material meltdown as can be seen in Fig. 3.15.

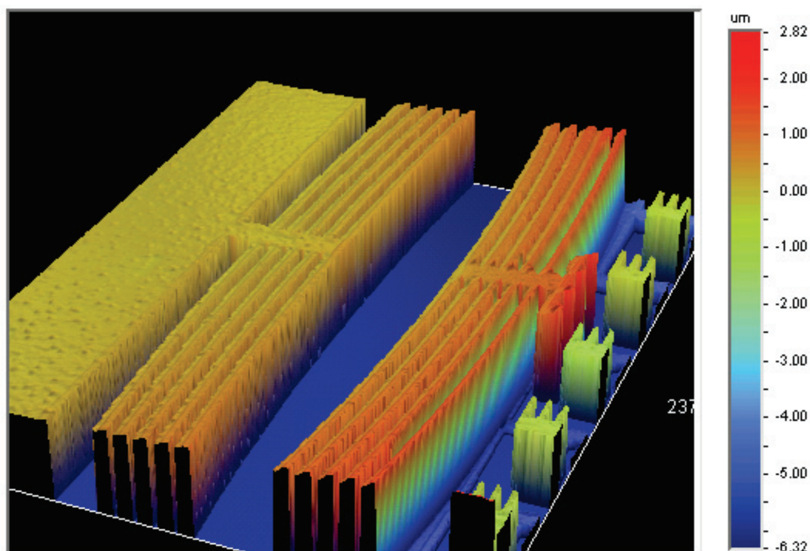


Figure 3.14: Wyco measurement of an SA electrode

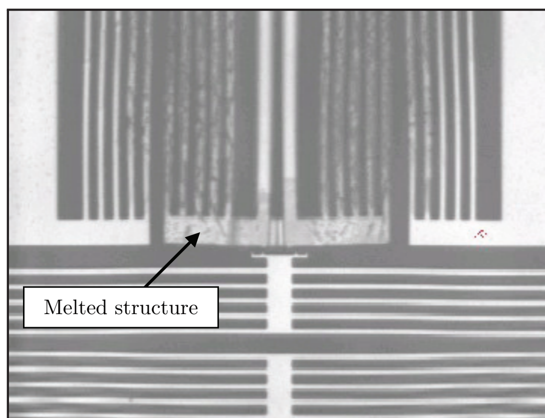


Figure 3.15: Melted Self-Assembly electrodes

Chapter 4

Composite resonator structures

COMBINATIONS of basic beam topologies can lead to more complex resonator architectures with multiple ports, increased internal routing possibilities, reduced feedthrough and a more symmetric design. These beam combinations leads to a resonator architecture called composite resonators.

This chapter will describe a method of connecting basic resonator topologies such as the cantilever, Clamped-Clamped, Clamped-Pinned and Pinned-Pinned and Free-Free beam types to make more advanced multi-terminal resonators. These combinations have lead to various Square-Frame Resonator (SFR) architectures. Some of the SFR architectures are symmetrical devices with similarities to the Wine-Glass resonators [50]. The composite resonators are of a flexural type and move laterally above the surface.

The final part of this chapter will show various methods of coupling multiple resonators together for improved filter design. The chosen coupling method for this thesis is investigated and described in detail. The coupled resonator filters and the standalone resonators all inhibit multiple operational modes and the output from these devices is a filtered motional current to be used for further signal processing. The composite resonators vibrate in different modes which depends on the beam boundary conditions which are explained in chapter 3.1 and appendix **A**.

4.1 Composite resonator modeling

The Square-Frame Resonator (SFR) is a symmetrical composite resonator made by using basic resonator topologies. Chapter 3.1 explained these basic beam bending modes. The Clamped-Clamped (CC), Pinned-Pinned (PP), Clamped-Pinned (CP) and Free-Free (FF) beam types are all used in this section to describe the SFR behavior. The main advantage of the SFR is its symmetrical behavior with clearly defined input and output ports. This leads to reduced capacitive feedthrough from the input to the output of the device. The architecture also offers multiple electrodes and more intricate and flexible internal routing capabilities.

4.1.1 Square-Frame Resonators

The Square Frame Resonators in this work has been made in two versions. The FFSFR (Free-Free Square-Frame Resonator), which is based on the Free-Free and Clamped-Pinned beam types. The Free-Free beam type constitutes the resonator and the Clamped-Pinned beam types are used as anchoring parts.

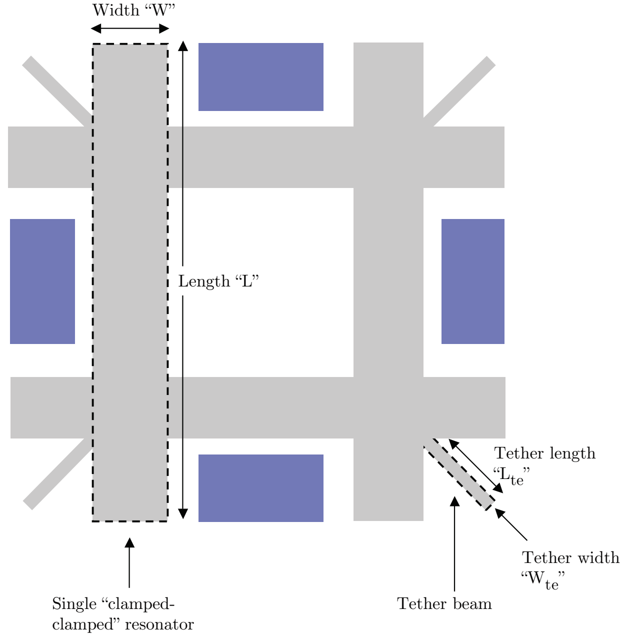


Figure 4.1: Free-Free Square-Frame Resonator top view

Fig. 4.1 is a top view of four laterally movable Free-Free resonators connected together, creating a square-frame composite resonator. The grey part is the resonator and the blue parts are the input and output electrodes. The Free-Free part has a width W and a length L and the tether (anchor) beams have a width W_{te} and a length L_{te}. The four 45° anchor beams are clamped at one end and attached to the Free-Free beams at the other end. Connecting these four Free-Free beams together at strategical nodal points will make this device resonate as if it was only one Free-Free beam. This is, of course, if the nodal points are exactly at the desired locations.

In reality, these nodal points are not exactly where they should be which will cause a slight change of the resonance frequency of the resonator. Ideally these nodal points should be exactly located at $\frac{L}{4}$ and $\frac{3L}{4}$ positions of the beam. As can be seen in chapter 3.1 and appendix **A**, the FF-beam and CC-beam have the same resonant mode β_N. By designing the tether beams using a $\lambda/4$ design methodology, it is possible to derive an equation for the tether beam length L_{te} [51].

$$L_{te}^2 = \frac{1}{4}\left(\frac{\beta_{te}}{\beta_N}\right)^2 \frac{W_{te}}{W} L^2 \tag{4.1}$$

where β_{te} is the tether beam mode which consists of a Clamped-Pinned beam bending type. These tether beams will have a torsional bending, and during operation these tether beams will not (ideally) contribute to translational movement. That means that the energy loss through these anchoring points is minimized as these beams will behave like acoustic transmission lines. The tether beam will present virtually no impedance to the resonator through this quarter-wavelength of the resonator operating frequency. Seen from the anchoring points, there is infinite acoustic impedance which is transformed to zero impedance at the resonator nodal attachment points. As a consequence of this, the resonator (ideally) does not see the supports and operates as if it is levitated above the surface. At these frequencies and with the materials of the resonator (metal-dielectric stack), the damping mechanisms are primarily due to intrinsic losses and not due to losses through the anchoring points. The acoustic network model of the tether beam is shown in Fig. 4.2 where k_{te} is the tether spring stiffness.

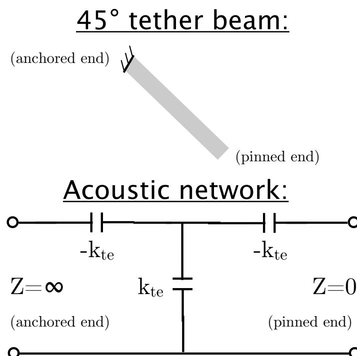


Figure 4.2: The tether beam and its acoustic network schematic

Q-factors of 1000–1400 for CMOS-MEMS resonators up to 10 MHz has been demonstrated [23, 38, 49]. Those research results show that the Q-factor has been primarily limited by Thermoelastic Damping (TED) and surface loss and not anchor losses. Another factor to take into consideration is the width of the resonating beams. For widths that are small enough, thermoelastic damping starts to limit maximum achievable Q-factor.

Fig. 4.3 shows the total FFSFR composite including self-assembly electrode structures and internal routing of the device. Due to the single-resonator being built up by several Free-Free resonators, the FFSFR can be implemented with various routing schemes inside the resonator. This allows the FFSFR to become a four-terminal, two-port device. The west and east sides of the resonator are stimulated while the north and south sides of the resonator act as two variable capacitors thus creating two resonator currents which can be summed in one node.

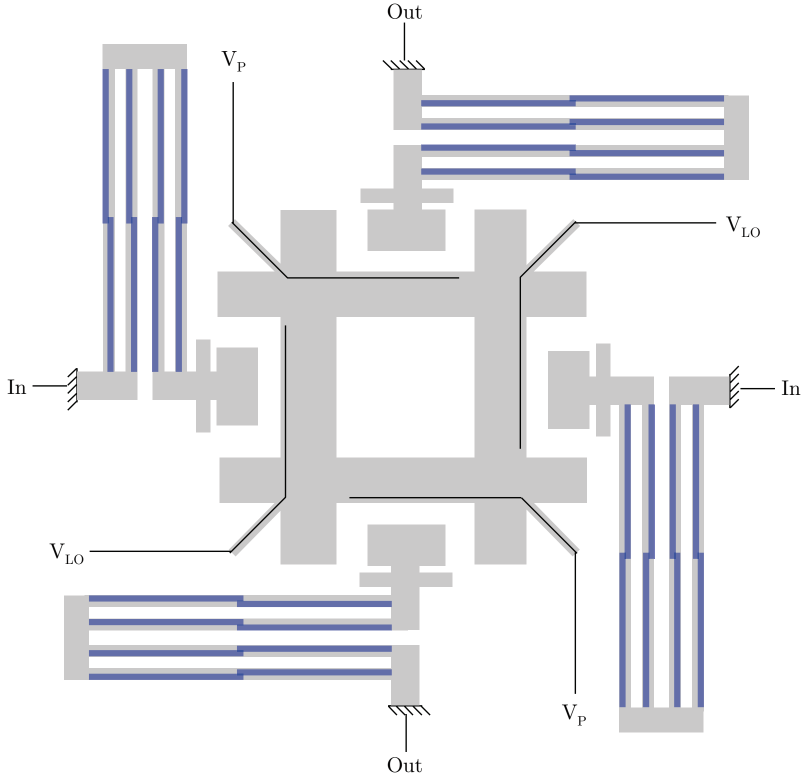


Figure 4.3: FFSFR with Self-Assembly electrodes and internal routing

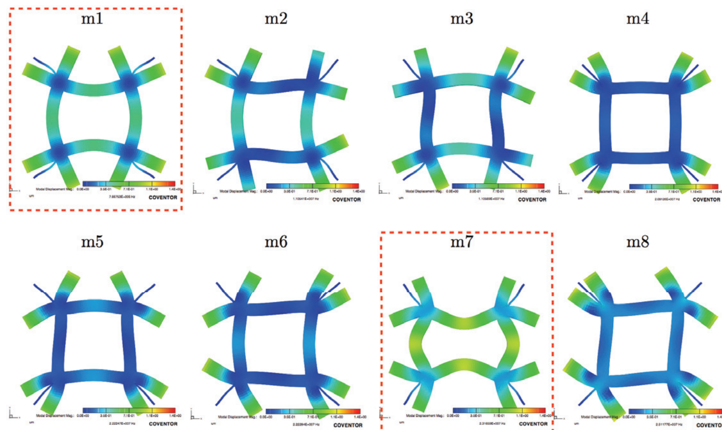


Figure 4.4: First 8 modes of an FFSFR

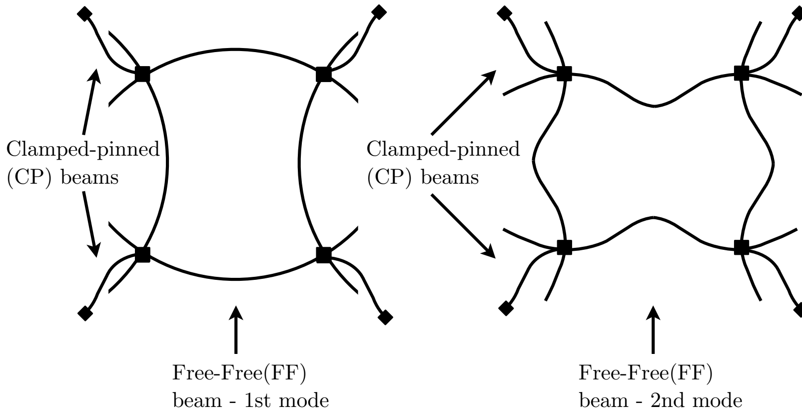
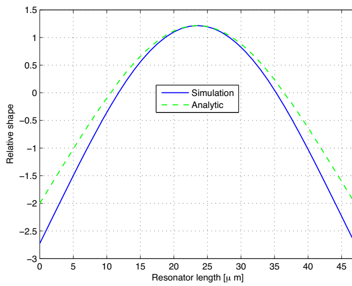
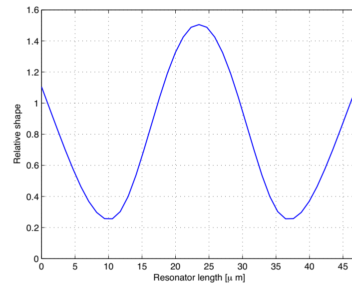


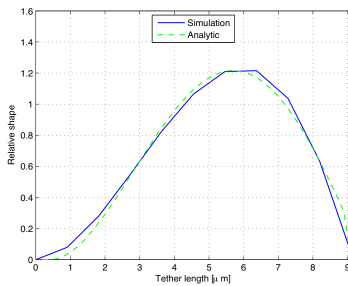
Figure 4.5: Schematic overview of the two first modes of the FFSFR



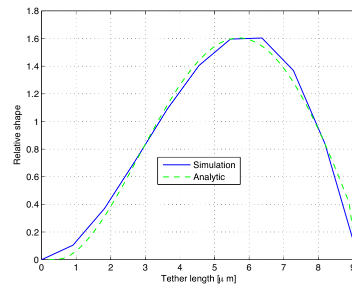
(a) M1 FFSFR



(b) M2 FFSFR



(c) M1 tether



(d) M2 tether

Figure 4.6: Mode shapes M1 and M2 for the FFSFR and its tether beams

The first 8 modes of the FFSFR are shown in Fig. 4.4. The first and seventh mode (m1 and m7) are the only modes that are excited electrically. The first and seventh mode in Fig. 4.4 are referred to as the first and second detectable (and operative) mode of the FFSFR, designated as M1 and M2. A schematic view of the two first modes of the FFSFR is shown in Fig. 4.5. Simulated and analytic mode shapes for the FFSFR and its associated tether beams are shown in Fig. 4.6. These mode shapes show the relative displacement of the resonator and its tether beams as a function of the length. For the tether beam, the left side is the anchor and the right side is the pinned end, similar to Fig. 4.2.

The second SFR type, the Clamped-Clamped Square-Frame Resonator (CCSFR) is shown in Fig. 4.7. Four Clamped-Clamped resonators are connected together at the anchoring points, creating a square-frame composite resonator with tether beams to the anchoring ("clamped") locations.

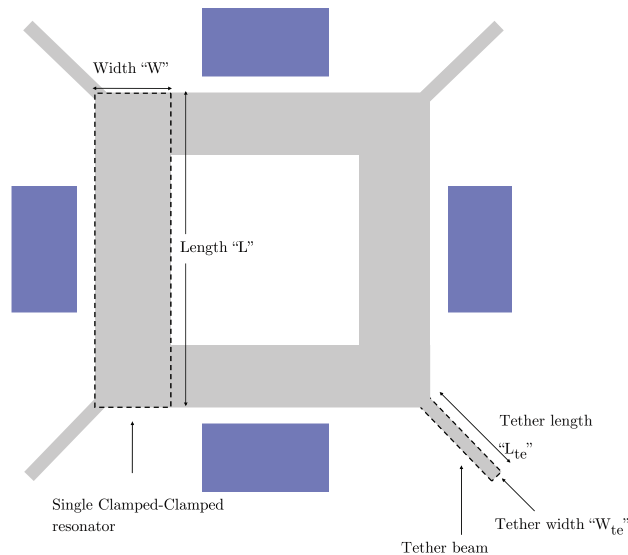


Figure 4.7: Clamped-Clamped Square-Frame Resonator top view

As seen in Fig. 4.8, the CCSFR has two operative modes where the first mode follows a Pinned-Pinned boundary condition and the second mode follows a Clamped-Clamped boundary condition. This is a special case where one and the same composite resonator can lead to two different modes for the same physical structure. The CCSFR is, of course, designed to operate at both of its two modes due to a specified length of the tether beams which operate at the $\lambda/4$ of the resonance frequency for a Clamped-Clamped beam case. The CCSFR is optimally designed for the second mode, and the Pinned-Pinned mode (which is the first mode) is still stimulated with almost the desired resonator stiffness. The simulated and analytical mode shapes for the CCSFR and its attached tether beams are shown in Fig. 4.9.

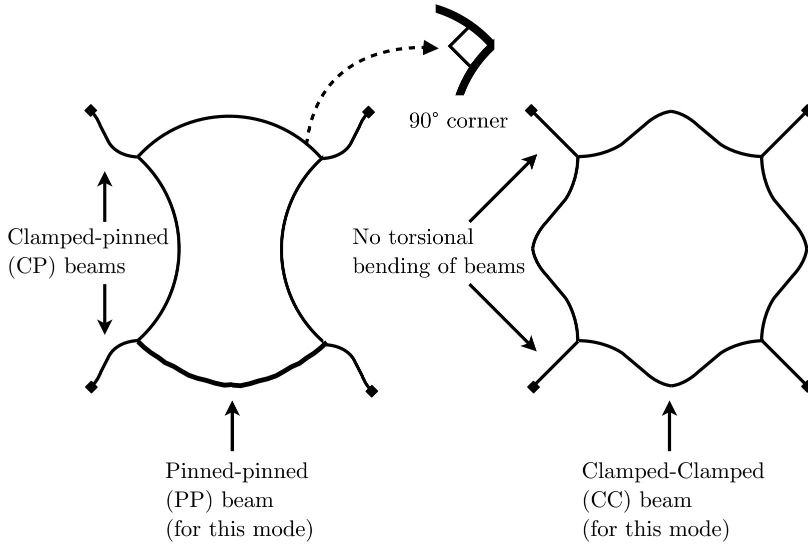
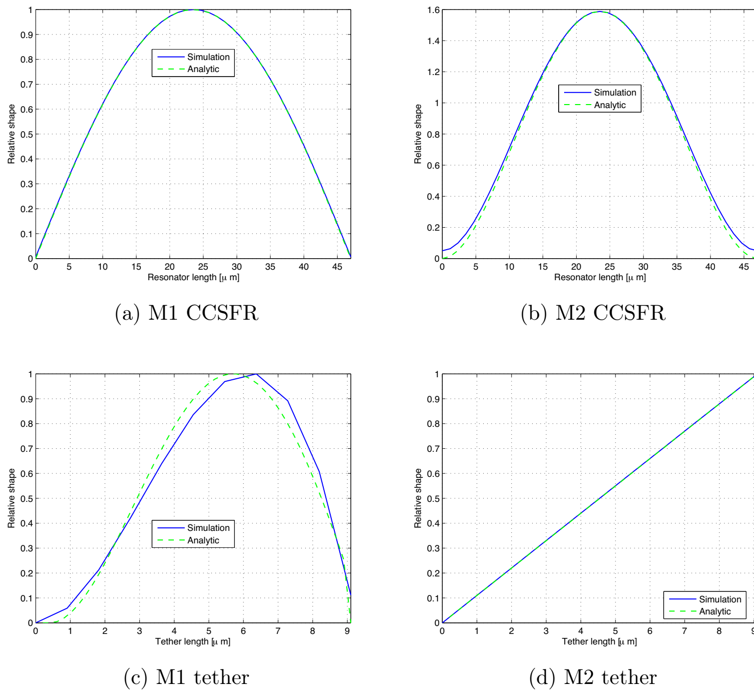


Figure 4.8: Schematic overview of the two first modes of the CCSFR



(a) M1 CCSFR

(b) M2 CCSFR

(c) M1 tether

(d) M2 tether

Figure 4.9: Mode shapes M1 and M2 for the CCSFR and its tether beams

4.1.2 The Parallel-Plate Tuning Fork

The other composite resonator type is the Parallel-Plate Tuning Fork (PPTF). Unlike the FFSFR and CCSFR, the PPTF is not driven from two sides but will resonate back and forth with one input and one output terminal. The PPTF has its input and output clearly separated in a similar fashion as the other SFRs. The operational mode of the PPTF will depend on the spring stiffness as the device will resonate at two distinct frequencies.

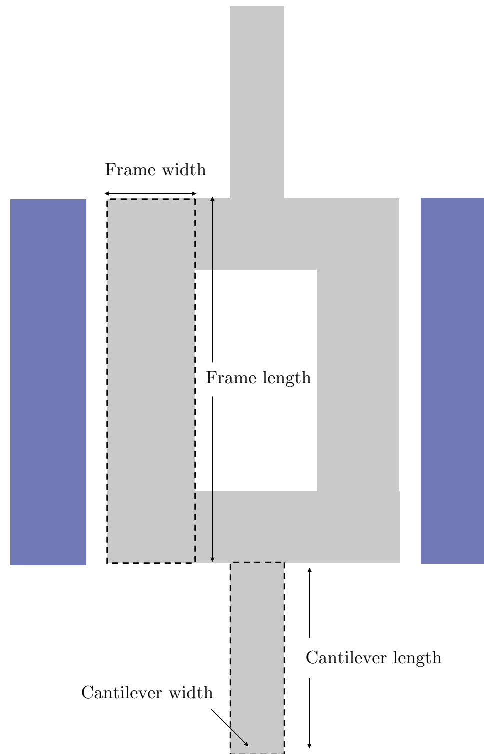


Figure 4.10: Parallel-Plate Tuning Fork overview

A top view of the PPTF is shown in Fig. 4.10. The blue rectangles are the input (left) and output (right) electrodes. For the first mode (M1), the PPTF operates as a large “Clamped-Clamped” resonator where the two cantilever beams make up the “CC-beam” the and the square frame in the middle results in an extra mass. The second mode (M2) of the PPTF can be regarded as a proper tuning fork behavior where the “Frame width” and “Frame length” will dictate the resonance frequency. These two frequency modes are clearly spaced apart and it is possible to route the device internally to have two internal terminals of the PPTF (i.e. V_{LO} on the input side and V_P at the output side). A schematic view of M1 and M2 for the PPTF is seen in Fig. 4.11.

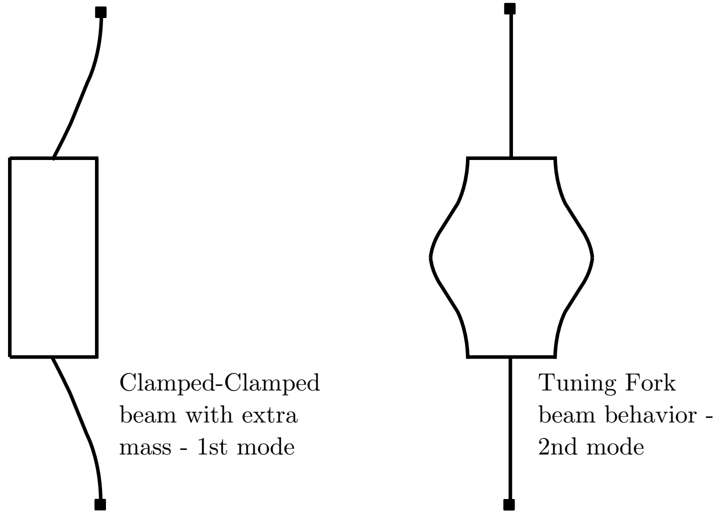


Figure 4.11: Schematic overview of the two first modes of the PPTF

The following list is a summary of the operation of the three different composite resonators, each operated with two modes M1 and M2.

- FFSFR - M1: Normal 1st mode Free-Free, $\beta_N = 4.73004074$
- FFSFR - M2: Normal 2nd mode Free-Free, $\beta_N = 7.85320462$
- CCSFR - M1: Pinned Pinned mode, $\beta_N = \pi$
- CCSFR - M2: Clamped-Clamped mode, $\beta_N = 4.73004074$
- PPTF - M1: Clamped-Clamped mode + square frame mass, $\beta_N = 4.73004074$
- PPTF - M2: Tuning fork mode, $\beta_N = 4.73004074$

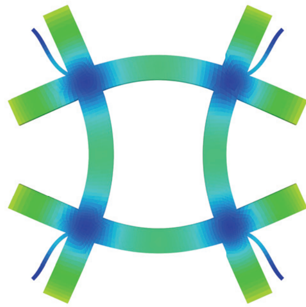
The FFSFR and CCSFR both follow the normal resonance frequency equation:

$$f_{0,nom} = \kappa \frac{\beta_N^2}{4\pi\sqrt{3}} \sqrt{\frac{E}{\rho}} \frac{W}{L^2}$$

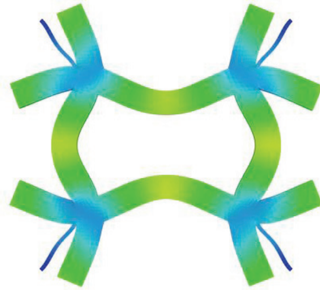
M1 of the PPTF, however, follows a slightly different resonance equation:

$$f_0 = \frac{1}{2\pi} \sqrt{\frac{k_{CC}}{m_{CC} + m_{square}}} \tag{4.2}$$

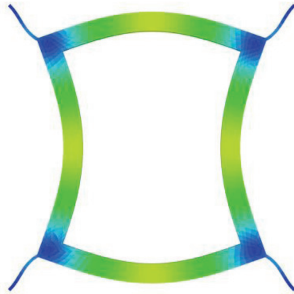
The k_{CC} and m_{CC} are based on geometry of the long and thin anchoring beams. m_{square} is the mass of the square-frame in the middle. M2 of the PPTF follows the normal resonance frequency equation with the length and width of the beams in the middle dictating the frequency. FEM (Finite Element Method) simulations of two mode shapes for these three composite resonator types are shown in Fig. 4.12.



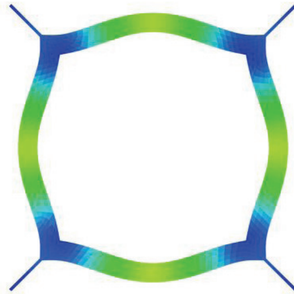
(a) M1 FFSFR



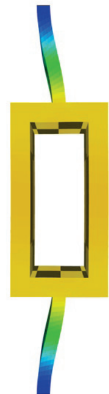
(b) M2 FFSFR



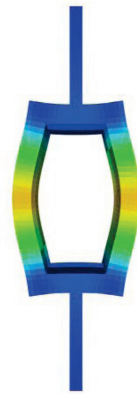
(c) M1 CCSFR



(d) M2 CCSFR



(e) M1 PPTF



(f) M2 PPTF

Figure 4.12: FEM simulated mode shapes M1 and M2 for the FFSFR, CCSFR and PPTF

4.1.3 Electromechanical equivalent circuit

The composite resonators presented in section 4.1 follows an electromechanical equivalent representation, similar to the one presented in Fig. 3.4 (chapter 3.2). The FFSFR and CCSFR have two input and two output terminals, thus the schematic representation is split into two branches:

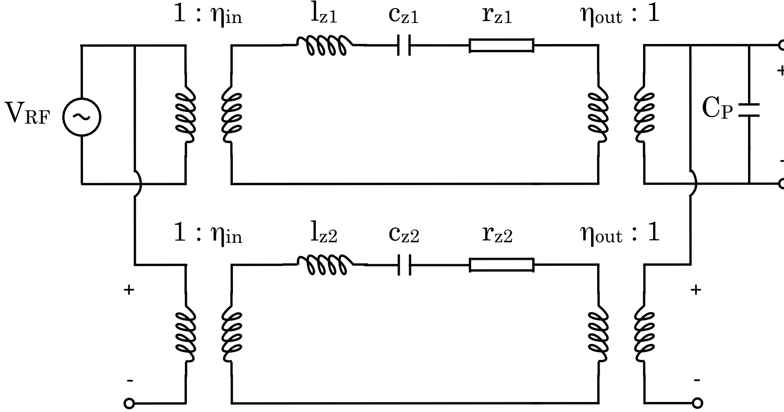


Figure 4.13: Electromechanical schematic for an SFR

C_P is parasitic capacitance from the resonator and the routing. There are two branches with transformers as shown in Fig. 4.13. The branches are represented with two transformers to define the two terminals. l_{zn}, c_{zn} and r_{zn} are without transformers. The lcr and the electromechanical coupling coefficients are given by

$$l_{zn} = m_{eff} \tag{4.3}$$

$$c_{zn} = \frac{1}{k} \tag{4.4}$$

$$r_{zn} = \frac{k}{\omega_0 Q} \tag{4.5}$$

$$\eta_{in} = V_{LO}\frac{dC_{in}}{dz} \tag{4.6}$$

$$\eta_{out} = V_P\frac{dC_{out}}{dz} \tag{4.7}$$

As seen in Fig. 4.13, the transformer is clearly split into η_{in} and η_{out} to designate the different ports of the resonator. The η_{in} can be connected to a Local Oscillator (LO) signal for a mixer-filter or a DC voltage (V_P') for filtering. Using the input and output transformers with lcr equations above results in

$$L_{zn} = \frac{m_{eff}}{\eta_{in}\eta_{out}} \tag{4.8}$$

$$C_{zn} = \frac{\eta_{in}\eta_{out}}{k} \tag{4.9}$$

$$R_{zn} = \frac{k}{\omega_0 Q \eta_{in}\eta_{out}} \tag{4.10}$$

where n depends on the branch. The SFR has the same filtering characteristics as earlier. Slight differences in k and m_{eff} as well as the input and output terminals may lead to a change in resonance frequency and resonator motional current. Variations in these parameters can be utilized as an advantage as will be explained later. The PPTF composite resonator has only one branch as it is a one-terminal, two-port device and follows the same electromechanical schematic in Fig. 3.4

4.2 Coupling techniques

This section will go through two different coupling techniques: Coupling resonators electrically or mechanically. The first method will present examples and results from my exchange stay at Carnegie Mellon University, Pittsburgh 2009–2010.[1]

4.2.1 Electrical summation

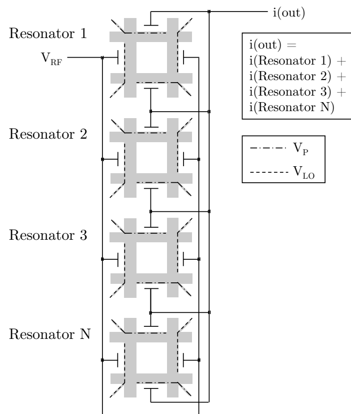


Figure 4.14: Schematic of identically summed resonators

The principle of electrical summing of resonators is shown in Fig. 4.14. This is an array of ideally identical resonators which will add multiple currents to a common node where the currents are summed together. This requires that the

[1]Figures and graphs in section 4.2.1 are reproduced by permission from Gary Fedder, CMU

resonators are at exactly the same frequency. A variation of kHz in f_0 for resonators in the MHz area results in a larger bandwidth and not an increase of the throughput. This observation leads to the natural expansion of this electrical summing principle: A matrix of resonators to sum currents at various frequencies. With a matrix of identical resonators, it is also possible to select the resonators with the exact same resonance frequency to sum currents to get an increased throughput. The filter order, however, remains the same – in this case a second order FFSFR filter array.

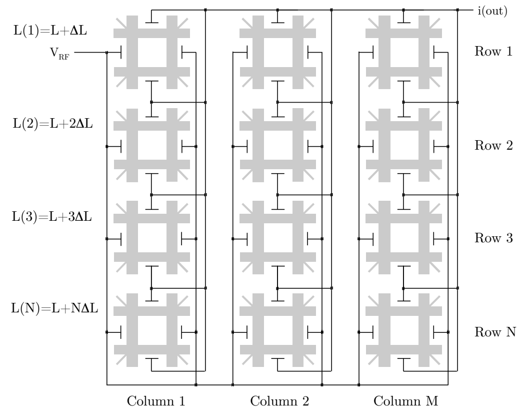


Figure 4.15: Resonator array with intended length shift for an increased bandwidth

The principle of summing the resonators can be expanded to make a larger filter bandwidth, or even better; a controllable bandwidth! This can be seen in Fig. 4.15 where the columns are identical while the rows consists of resonators with varied lengths. This will make it possible to pick and choose resonators to control both the bandwidth and the total gain of the filter. A proposed system schematic for electrical summing is seen in Fig. 4.16.

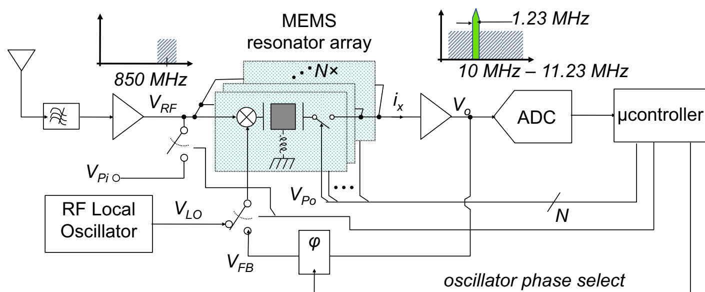


Figure 4.16: Proposed system schematic for the Self-Healing MEMS project at CMU

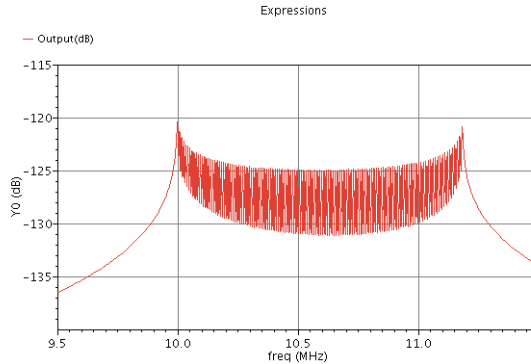
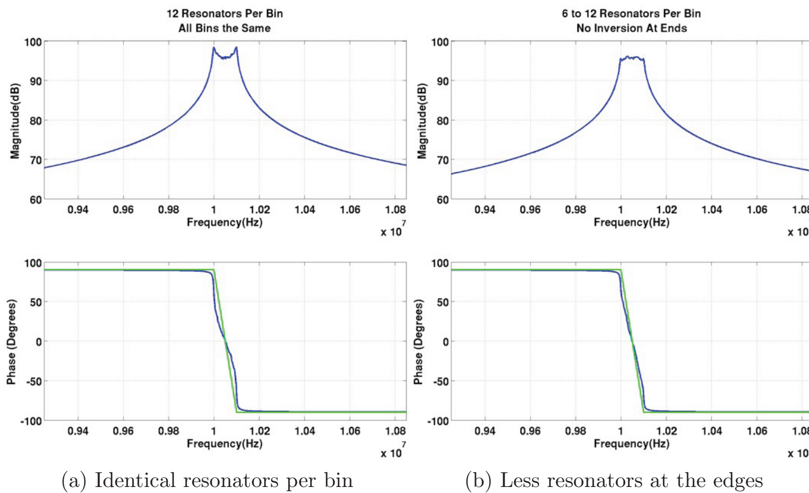


Figure 4.17: Filter response from a 128 resonator FFSFR array

Results from a summed filter is shown in Fig. 4.17. These are NODAS simulations (Verilog-A beam models at Carnegie Mellon University) which shows an array of 128 resonators with a slight shift in beam lengths in order to vary the resonance frequency and therefore to create a 1 MHz bandwidth going from 10 MHz to 11.23 MHz. As can be seen from this, there is a drop in the middle of the passband and more gain at the filter ends.



(a) Identical resonators per bin (b) Less resonators at the edges

Figure 4.18: Improved filter band with varied amount of resonators per bin

The filter output drop was investigated and it was found that the cause was that the filter total 180 degree phase shift was not completely linear towards the middle of the passband. By adding more resonators in the middle compared to the edges, the phase shift for these becomes stronger as can be seen in Fig. 4.18.

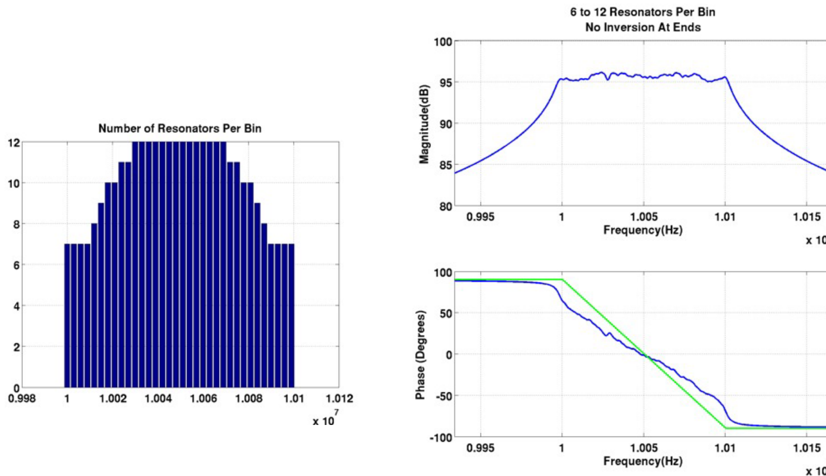


Figure 4.19: Zoom of ideal matlab filter with adjusted resonators per bin

A closeup of the filter with the number of resonators per frequency bin (bin being a set of identical resonators for that particular frequency) is seen in Fig. 4.19. From this it can be seen that the phase shift is becoming more linear throughout the total bandwidth of the filter where the green line is the complete theoretical linear phase shift.

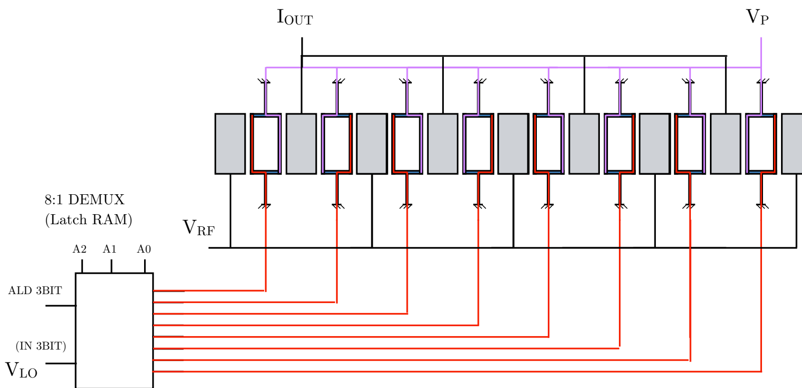


Figure 4.20: Using a DEMUX to couple in and out electrically summed resonators

Another example of electrically summed resonators is seen in Fig. 4.20. This example uses a multiplexer to select which PPTF resonators to use in an array. The resonators share a common V_P and the 8:1 DEMUX selects which resonators receives the V_{LO}. The multiplexer must be designed to be able to handle the V_{LO} which is a high-frequency signal. For filters, V_{LO} can be replaced by a V_P' which is lower than V_P in order to comply with transistors voltages.

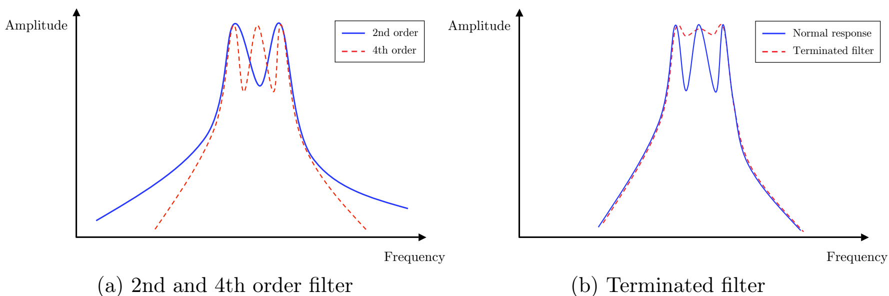
	Average [MHz]	Standard deviation [kHz]
Mismatch	10.0002	20.411
Process	10.0151	348.344
Process & mismatch	10.0097	364.287

Table 4.1: Simulated mismatch and process variation example of a 10 MHz resonator

As can be seen in Table 4.1, a statistical simulation on a 10 MHz FFSFR has been performed. The resonator has been implemented in Verilog-A code, taking into consideration possible deviations in the geometry and the undercut etch both locally and a globally. These models make it possible to perform Monte Carlo simulations of the CMOS-MEMS resonators. It can be seen that the process mismatch contributes to the most variation, showing that the center frequency of the resonator varies greatly. However, it should be mentioned that this variation depends on the complexity of the resonator geometry. As can be seen from this example of electrical summing, the process variations can be utilized as an advantage to make filters with controlled bandwidth and throughput.

4.2.2 Mechanical summation

The other coupling technique is by mechanically coupling (sum) resonators together. Depending on how the resonators are coupled together, this can increase the order of the filter as shown in Fig. 4.21a). Mechanically coupled resonators will also have a statistical spread, as was mentioned in section 4.2.1. By designing the resonator to have a slightly larger resonance frequency than desired, it is then possible to use V_P to reduce the frequency of the resonator to the desired level. By doing this, it is possible to circumvent the statistical variation of the resonance frequency and to control a higher order filter with an adjustable bandwidth.



(a) 2nd and 4th order filter

(b) Terminated filter

Figure 4.21: Filter responses and filter termination

The 2nd and 4th order filter in Fig. 4.21(a) are of an unterminated type. That is, there is a ripple within the passband which is larger than 0.5–1 dB. In Fig. 4.21(b) a 4th order filter with and without termination is demonstrated. By

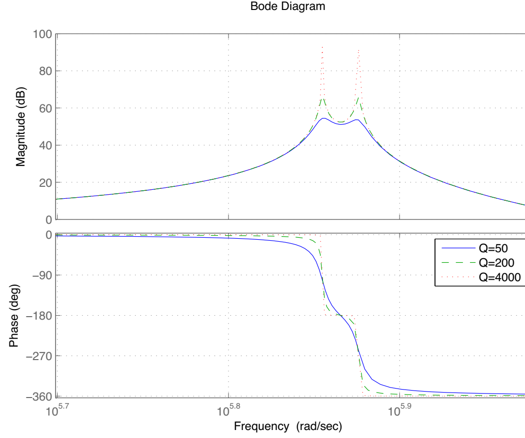


Figure 4.22: Filter and phase response of a mechanical 4th order filter

including resistors at the input and output stage of the filter, it is possible to attenuate and reduce the ripple [22]. Depending on the filter type (i.e. Chebyshev, Butterworth) and the filter specifications, the total Insertion Loss (IL) of the filter should be as low as possible.

As was seen for the electrically summed resonators, there is a correlation between the Q-factor and the phase, this is demonstrated in Fig. 4.22 where the Q-factor is increased from 50 to 2000. If the Q-factor of the individual resonator is large enough, the need for terminating the filter becomes more obvious. A 4th order filter will have two resonant modes which will create a larger bandwidth than the individual resonators:

$$BW = f_2 - f_1 \tag{4.11}$$

$$Q_{filter} = \frac{f_c}{BW} \tag{4.12}$$

Eq. 4.11 and 4.12 above describes the filter relationships. f_1 and f_2 are two distinct modes which creates a filter bandwidth by subtraction. It is important to point out that the f_1 is a frequency which is -3dB prior to the first mode M_1 and f_2 is a frequency is the -3dB past the second mode M_2. The center frequency f_c of the filter is defined as the frequency between the two modes M_1 and M_2.

$$f_1 = \frac{1}{2\pi}\sqrt{\frac{k}{m_{eff}}}, f_2 = \frac{1}{2\pi}\sqrt{\frac{k + k_c}{m_{eff}}} \tag{4.13}$$

The two frequencies f_1 and f_2 are described analytically in eq. 4.13. f_1 is simply the stiffness divided the effective mass of the resonator. The second frequency f_2 leads to an increased total spring stiffness of the total resonating device. The coupling beam is considered as an ideal mass-less component, thus only introducing additional spring stiffness.

4.3 Mechanically coupled composite resonators

The description of mechanically coupled resonators in section 4.2.2 was in a simplified sense. By coupling two resonators together, the acoustic network of the resonators is expanded with an acoustic network for the coupling beam. Depending on the chosen dimensions for the coupling beam, the acoustic network for the coupling beam becomes a T-network with capacitors or a T-network with inductors and a capacitor as shown in Fig. 4.23:

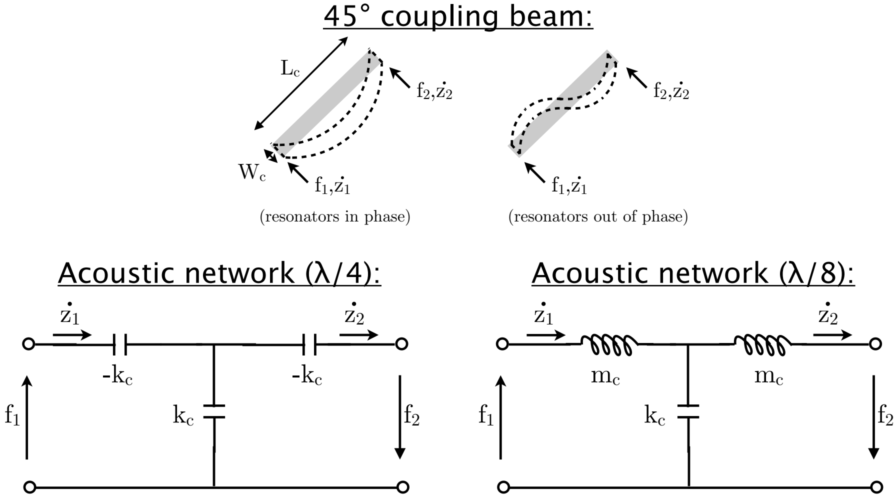


Figure 4.23: The coupling beam and its acoustic network schematic

The bottom left part of Fig. 4.23 shows that if the coupling beam is designed to be four times the operational frequency of the resonators, it will follow a $\lambda/4$ operational mode. This is possible by choosing the width W_c and the length L_c of the coupling beam so that $f_c = 4f_0$. Similarly, if the coupling beam is designed to be eight times f_0 of the resonators, it follows a $\lambda/8$ mode. The SFRs in this work are designed for $\lambda/4$ while the PPTF is designed for $\lambda/8$. This section will go into the depth of mechanically coupling the SFR and PPTF resonators together in order to make higher order filters.

The top part of Fig. 4.23 shows the two phases which occurs for the coupling beam when two resonators are connected together. The in-phase mode results in a two nodal locations for the coupling beam while the out-of-phase mode results in three nodal locations. By analyzing the acoustic network of the coupling beam for resonators that vibrate in phase it is possible to find the mechanical impedance Z_c of the coupling beam [52, 53]. Z_c is given by the force (effort) divided by the velocity (flow):

$$Z_c = \frac{f_1}{\dot{z}_1} = -\frac{EI_c\alpha^3 H_6}{j\omega L_c^3 H_3} \tag{4.14}$$

I_c is the area moment of inertia and L_c is the length of the coupling beam. α, I_c, H_3 and H_6 are given by

$$\alpha = L_c(\frac{\rho W_c H_c \omega^2}{EI_c})^{0.25} \tag{4.15}$$

$$I_c = \frac{H_c W_c^3}{12} \tag{4.16}$$

$$H_3 = cosh(\alpha)cos(\alpha) - 1 \tag{4.17}$$

$$H_6 = sinh(\alpha)cos(\alpha) + cosh(\alpha)sin(\alpha) \tag{4.18}$$

The mechanical coupling beam stiffness when the resonators are vibrating in phase is given by

$$k_{c1} = -\frac{EI_c\alpha^3 H_6}{L_c^3 H_3} \tag{4.19}$$

Likewise, the mechanical impedance for the coupling beams when two coupled resonators are out of phase is given by

$$Z_c = \frac{f_2}{z_2} = -\frac{EI_c\alpha^3 H_7}{j\omega L_c^3 H_3} \tag{4.20}$$

where H_7 is given by

$$H_7 = sin(\alpha) + sinh(\alpha) \tag{4.21}$$

For the case of two resonators vibrating out of phase the mechanical spring stiffness of the coupling beam is given by

$$k_{c2} = -\frac{EI_c\alpha^3 H_7}{L_c^3 H_3} \tag{4.22}$$

From these two cases it is possible to derive the spring stiffness of the coupling beam, depending on the desired usage. By setting $H_6 = 0$ and solving for L_c it is possible to find the values for k_{c1} and k_{c2}. A quarter-wavelength of the operating frequency results in the following coupling beam stiffnesses

$$k_{c1} = 0 \tag{4.23}$$

$$k_{c2} = \frac{EI_c\alpha^3(sin(\alpha) + sinh(\alpha))}{L_c^3(cos(\alpha)cosh(\alpha) - 1)} \tag{4.24}$$

From this analysis, k_{c1} for the first mode does not contribute to a change in the filter frequency while k_{c2} effectively adds to the original f_0 for one resonator. This analysis is valid for the FFSFR and CCSFR. As was done with the tether beam, a $\lambda/4$ dimensioning of the coupling beam leads to an equation defining the length of the coupling beam as seen in eq. 4.25. In eq. 4.25, the β_c defines the mode of operation for the coupling beam and varies depending on beam bending of the composite resonator.

$$L_c^2 = \frac{1}{4}\left(\frac{\beta_c}{\beta_N}\right)^2 \frac{W_c}{W} L^2 \tag{4.25}$$

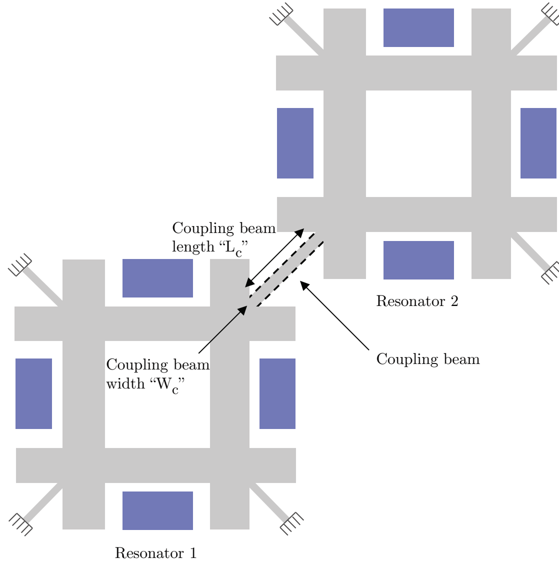


Figure 4.24: A 4th order FFSFR filter with a coupling beam

Two FFSFRs connected together with a coupling beam are demonstrated in Fig. 4.24. Fig. 4.25 shows an electromechanical schematic for Square-Framed resonators which is the same for both the FFSFR and the CCSFR. The $\lambda/4$ coupling beam is included with transformers as given in eq. 4.26. η_{cij} is the electromechanical coupling coefficient for the coupling beam and depends on resonator i and terminal j. η_{cij} is related to the coupling beam stiffness k_c divided by the stiffness k:

$$\eta_{cij} = \sqrt{\frac{k_c}{k}} \tag{4.26}$$

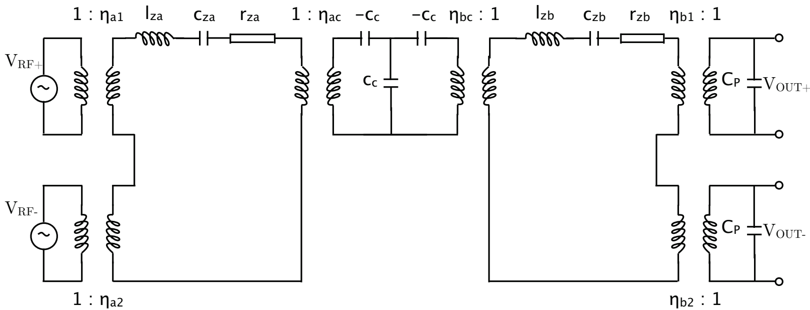


Figure 4.25: Electromechanical schematic for two SFRs connected as a higher order filter

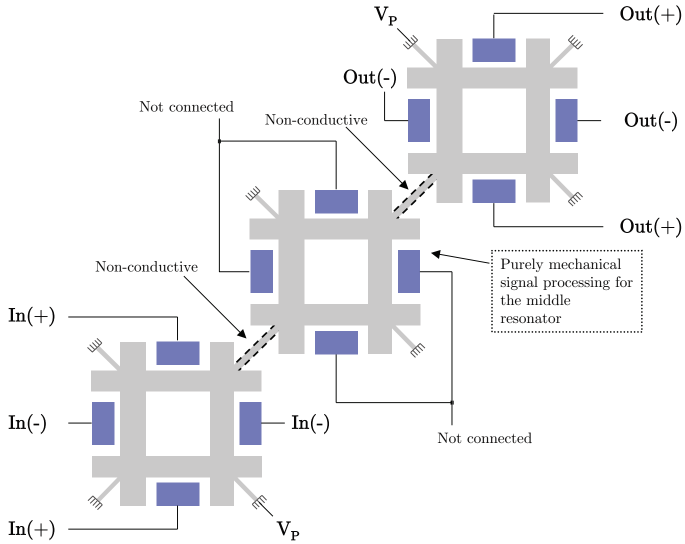


Figure 4.26: A 6th order FFSFR filter with coupling beams

Fig. 4.26 shows an example of three FFSFRs connected together with two coupling beams. The resonator in the middle does not have its electrode terminals connected, thus only the input and output resonators perform stimulation and detection of signals. Terminals for the differential drive are shown in Fig. 4.26.

FEM simulations of two mechanically connected FFSFRs are shown in Fig. 4.27. These plots are exaggerated in order to illustrate bending behavior where M1 is out of phase and M2 is in-phase. Fig. 4.28 shows the modal analysis for three mechanically coupled FFSFRs. For M1, the input and output resonator are in-phase while the middle resonator is out-of-phase. For M2, the input and output resonator are out-of-phase. Finally M3 shows that all three resonators are in-phase.

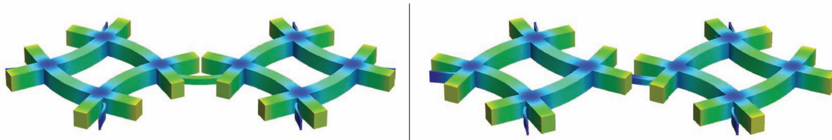


Figure 4.27: 2-FFSFR and its two modes

Figure 4.28: 3-FFSFR and its three modes

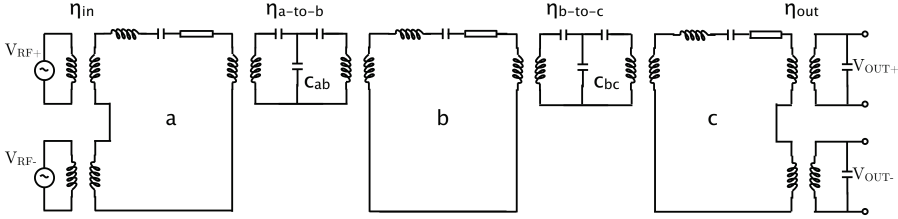
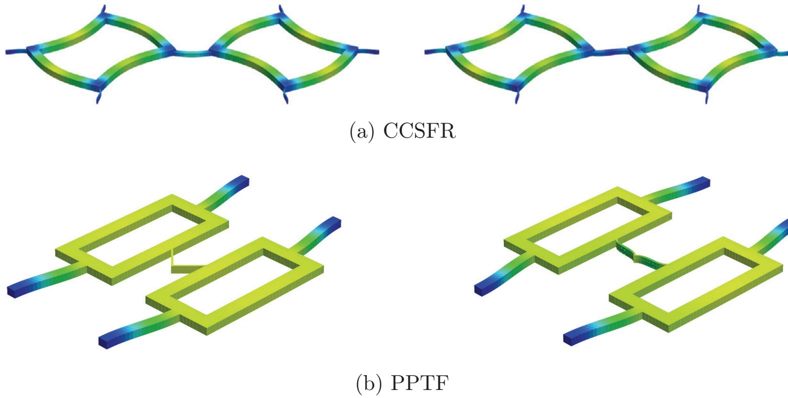


Figure 4.29: Electromechanical schematic for three SFRs connected as a 6th order filter

A filter schematic of a 6th order FFSFR or CCSFR is shown in Fig. 4.29. The electromechanical schematic in Fig. 4.29 and Fig. 4.25 has merged the lcr from the two terminals into one common lcr for simplicity.

FEM simulations for two mechanically coupled resonators for the CCSFR and the PPTF are demonstrated in Fig. 4.30. Fig. 4.31 shows an electromechanical schematic for two PPTF resonators connected together with a coupling beam. A top view of all three composite resonator types is shown in Fig. 4.32 where dark colors are parts that do not move while light parts have maximum displacement.



(a) CCSFR

(b) PPTF

Figure 4.30: M1 and M2 for mechanically coupled CCSFR and PPTF

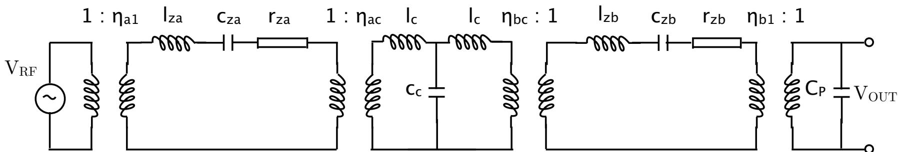
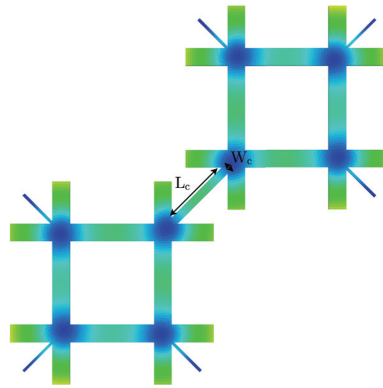
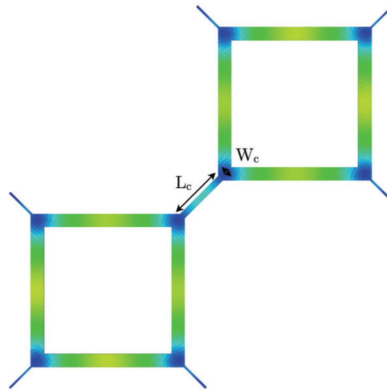


Figure 4.31: Electromechanical schematic for two PPTF connected as a higher order filter

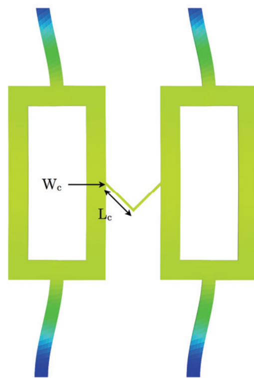
The V-shaped coupling beam of the PPTF follows a special design case of $\lambda/8$. This means that the mass of the coupling beam must be taken into consideration.



(a) FFSFR



(b) CCSFR



(c) PPTF

Figure 4.32: Top view of mechanically coupled FFSFR, CCSFR and PPTF

The coupling beam stiffness is inversely proportional to c_c while the coupling beam mass is proportional to l_c in the acoustic T-network. Eq. 4.27 defines this relationship where the mass is multiplied by 2 due to the two 45 degree beams connected together creating a V-shape [52]:

$$c_c = \frac{1}{k_c} = \frac{2}{EH_c}\left(\frac{L_c}{W_c}\right)^3 \tag{4.27}$$

$$l_c = m_c = 2\rho H_c W_c L_c \tag{4.28}$$

With the electromechanical equivalents for the FFSFR, CCSFR and PPTF described, the remaining component which needs to be described is the termination resistor R_{Qi}. As was shown in Fig. 4.21b), the introduction of termination resistors will reduce the ripple in the passband. Eq. 4.29 shows termination resistor R_{Qi} being related to the motional impedance R_z, the resonator Q-factor, the filter Q-factor, a filter mode constant q_i and the number of terminals n. It is obvious from this equation that designing for a low R_z is important. Trying to reduce R_z will at some point reach a limit due to process constraints or non-linearities. R_{Qi} can be decreased by increasing the number of terminals instead of trying to reduce R_z.

$$R_{Qi} = \frac{R_z}{2n}\left(\frac{Q}{q_i Q_{filter}} - 1\right) \tag{4.29}$$

As can be seen from the figures presented in this section, the composite resonators present certain layout challenges with regard to feedthrough between terminals, including space requirements in order to use self-assembly beams to make small gaps. These layout considerations are discussed in section 4.4.

4.4 CMOS-MEMS layout considerations

There are important aspects to take into considerations when making MEMS resonators. For instance, the feedthrough between the input and output of the resonator should be as low as possible. Due to the complexity of the FFSFR and CCSFR, there are parts where routing of one signal crosses the other. In addition to this, any parasitics from the output of the resonator will add to any following amplifier. Designing for low feedthrough and small parasitic capacitance is of importance.

An example of how to reduce the parasitic capacitance is shown in Fig. 4.33. This example is taken from a 90 nm CMOS process where a signal layer has almost equal distance between the silicon and any top metal layer (which protects against the etch). The top metal layer will be grounded, as is the silicon beneath. This is because CMOS foundry rules does not allow floating layers (except dummy layers). Having the signal layer equally spaced to ground will reduce the total capacitance added to the signal layer.

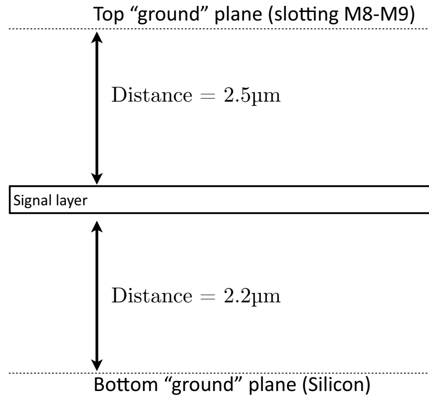


Figure 4.33: Schematic of how to to position a signal layer to reduce parasitics

Fig. 4.34 shows the input signal (V_{RF}) as a vertical line which at some point crosses another line which is the motional current (I_{out}) out from the resonator. Feedthrough between input and output of a resonator is very critical for the filter performance. For most of the path, both signals are routed in the middle signal layer. Closer to the crossing point one of the signals is routed to a different level so the input and output signal layers do not short-circuit each other. In addition to that, a grounded metal layer is placed between the two signals. This leads to a drastic reduction of input to output capacitance, which is extremely important for the filter characteristics.

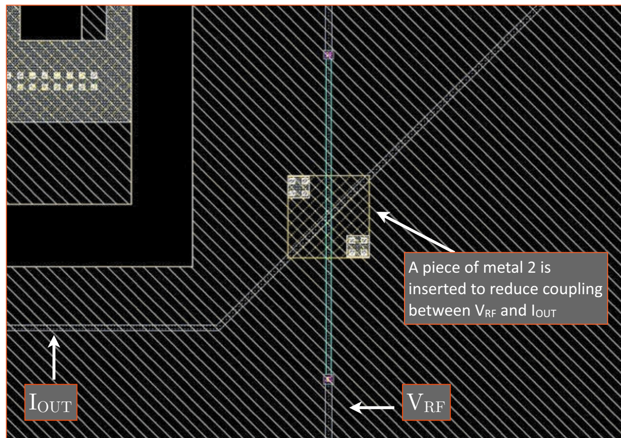


Figure 4.34: Layout overview showing a piece of metal to protect from feedthrough

Capacitive feedthrough is shown in eq. 4.30 [54]. From this it is evident that if C_F is large, there will be a substantial current leakage proportional to the frequency through the device. It is possible to reduce feedthrough by the addition of feedback

compensation circuitry [55]. By reducing the capacitive feedthrough, the signal only passes the filter and does not pass through C_F.

$$i_{feedthrough} = V_{ac}\omega C_F \tag{4.30}$$

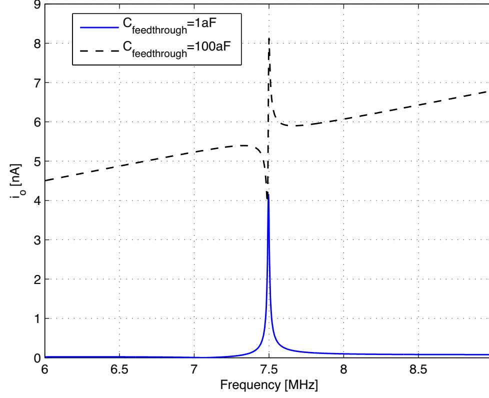


Figure 4.35: Simulation of an FFSFR with and without feedthrough

This feedthrough effect is more clearly demonstrated in Fig. 4.35. The feedthrough will cause a major impact on the output response of the filter. A capacitive feedthrough of 100 aF is enough to make the output voltage increase linearly with frequency because of the coupling capacitor. Feedthrough capacitances calculated in this thesis have been limited to tenths of aF after introducing these types of layout "shields" as shown in Fig. 4.34. Parasitic capacitance to ground is also important: The routing capacitance, C_P, from the output of the resonator to the amplifier is simulated and calculated to be about 10 fF:

$$\begin{aligned}
C_{P(route,SA-to-SA)} &= 2(\varepsilon_0\varepsilon_r 0.1\mu 325\mu/2.135\mu) = 2.7fF \\
C_{P(route,SA-to-amp)} &= 2(\varepsilon_0\varepsilon_r 0.1\mu 175\mu/2.135\mu) = 730aF \\
C_{P(SA,air-to-sidewall)} &= 2(\varepsilon_0 0.1\mu 220\mu/1.5\mu) = 1fF \\
C_{P(amplifier)} &= 5fF \\
C_{P(total)} &\approx 10fF
\end{aligned}$$

This is an example where the layout has been implemented from one of the chip tapeouts. The SA-to-SA parasitics consist of the routing from two self-assembly beams until they join the same electrical path. The SA-to-amp parts are the remaining routing from that point to where the amplifier is located. The air-to-sidewall parts are capacitances which occurs from the sidewalls in the open etched areas and the $C_{P(amplifier)}$ is the assumed input capacitance from the gate-source capacitance of the input transistor of the amplifier. Cadence simulations have been performed as well, and the capacitance has been calculated to be close to the

theoretical values. However, Cadence does not "understand" the part of the MEMS structure which is released and which may lead to different parasitics than what Cadence can calculate. Therefore a crude manual estimation is performed, leading to an assumed worst case parasitics of 15–25 fF. This means that the amplifier must be able to drive at least 15–25 fF of input capacitance. Layout of dimensions and internal routing of a Self-Assembly beam is demonstrated in Fig. 4.36 and Fig. 4.37.

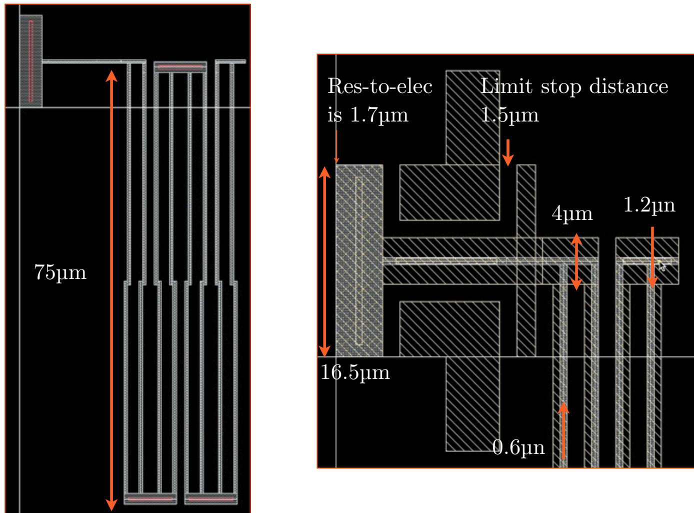


Figure 4.36: SA electrode layout

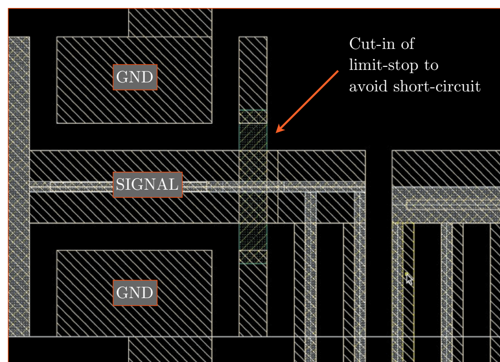


Figure 4.37: SA layout, showing the details of the limit stops

Since the SA electrodes move after being etched and released, a cut-in of the sidewall has been made. This causes the SA structure to not hit the sidewall and only hits the limit stops instead as seen in Fig. 4.38. Another detail of the SA

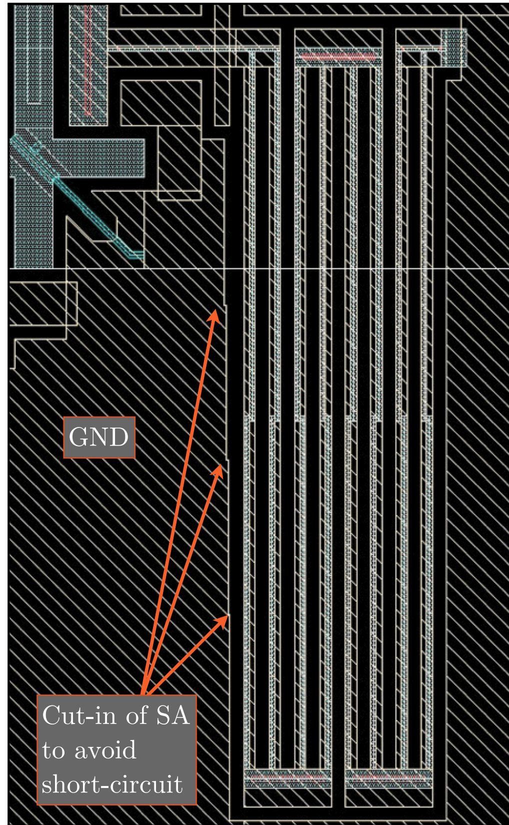


Figure 4.38: Sidewall cut-in to avoid short-circuit

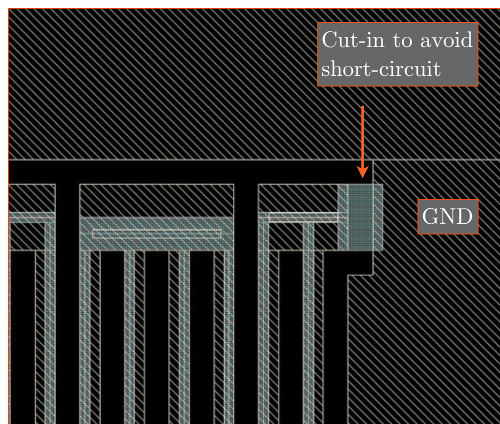


Figure 4.39: Details of the anchoring of the SA electrode

electrode is seen in Fig. 4.39. All of the metal layers are used to route the signal internally in the SA electrode, therefore a cut-in "metal bridge" is used to not short-circuit the signal with the large grounded metal plane.

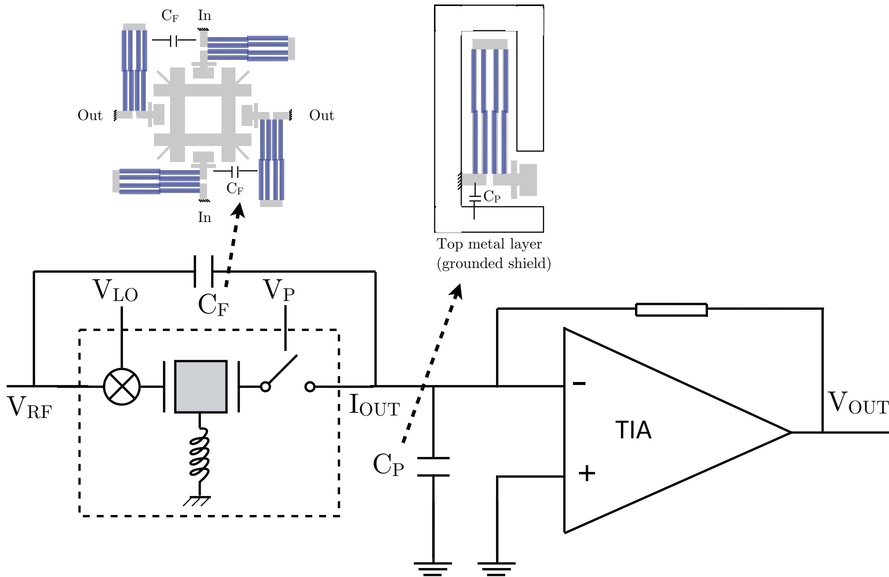


Figure 4.40: Feedthrough and ground parasitics example

The examples from the layout considerations for CMOS-MEMS resonators are demonstrated by showing the layout with the schematic as seen in Fig. 4.40. The input to output feedthrough capacitance C_F is related to the FFSFR layout including self-assembly electrodes. From the layout it can be seen that the south and west SA electrodes create a feedthrough from input to output, as does the north and east SA electrodes. As was explained with Fig. 4.34, a grounded metal layer between the signals can be included to significantly reduce the feedthrough parasitics. The C_P in Fig. 4.40 shows that the sidewall along the SA electrode adds parasitics to ground. By putting the signal layer as a sandwich between a top layer (which is used the mask against the etch) and the bottom layer (silicon level), the signal-to-ground parasitic C_P can be greatly reduced as shown in Fig. 4.33.

It is important to have a clever layout methodology for CMOS-MEMS resonators in order to have low parasitics to ground (C_P) and as low input-to-output capacitive feedthrough (C_F) as possible. This chapter showed the modeling of composite resonators. When coupling resonators together some considerations must be done for the layout of these devices. These devices can now be put into a larger context and chapter 5 shows CMOS-MEMS implementations done in this PhD thesis.

Chapter 5

CMOS-MEMS implementations

Basic CMOS-MEMS resonators and composite resonator types can be interfaced to amplifiers in various CMOS processes. The filtering capabilities of each resonator and composite resonator type will have certain advantages which can be utilized in different forms in combination with CMOS circuitry.

This chapter shows implemented CMOS-MEMS designs such as soft tunable resonators used as VCOs, low-noise amplifier designs and composite resonators as filters and mixer-filters with associated circuitry for voltage-to-voltage conversion. The results from these implementations are evaluated and discussed.

5.1 Simulation techniques

Modeling and simulation of MEMS resonators are challenging and critical for CMOS-MEMS design. Electrical engineers with the knowledge of CMOS circuit design are typically not familiar with mechanical beam models where knowledge of physics and mechanics is important. By including filtering components on-chip, there is less need for off-chip engineering and instead an increased need for understanding of the mechanical domain of the resonators. For CMOS-MEMS to be successful, proper resonator models which can be directly used in regular CMOS CAD (Computer Aided Design) software are important.

FEM tools are typically used to design and model MEMS devices as they are based on detailed node-to-node simulation techniques; a beam is meshed with a large density of nodes. Using FEM tools to design and analyze MEMS structures is important, however it is a very time consuming design methodology. Alternative semi-FEM tools have appeared in order to simplify simulation time and to be able to simulate (co-simulate) this in CMOS CAD. SUGAR from University of California, Berkeley [56] uses Matlab algorithms of three-dimensional mechanical structures and electrical circuits. Another example is NODAS from Carnegie Mellon University, Pittsburgh, which is based on a Verilog-A code [57]. This Verilog-A code is also based on three-dimensional mechanical beam models, and the Verilog-A code can very easily be used with CAD software.

As these nodal simulation tools become more readily available and integrated with CMOS CAD software from Mentor Graphics or Cadence, it becomes easier for designers to make MEMS structures combined with CMOS circuitry and to perform co-simulation of CMOS and MEMS. It should be mentioned that Coventor has an official add-on software for Cadence with the name "MEMS+" which is based on Verilog-A code similar to the one used at CMU [58].

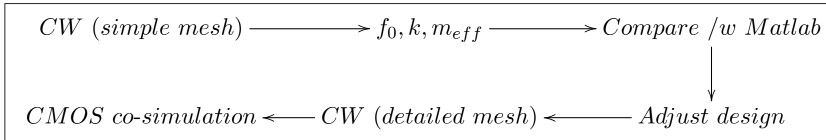


Figure 5.1: CoventorWare and analytic (Matlab) design methodology flow chart

A proposed design methodology using CoventorWare (CW) is shown in Fig. 5.1. Some of the simulation results in this thesis are based on NODAS Verilog-A simulations performed during an exchange stay at CMU. However, most simulations are based on a combination of CoventorWare and Matlab as shown in Fig. 5.1. Pure analytical equations become too coarse-grain. The results from CW and Matlab have then been ported to Cadence by using LCR equivalents and transformers as was shown in chapter 3 and 4. This has been done because CoventorWare is not able to model the beam as an electromechanical LCR equivalent which then can be directly used for simulation together with CMOS circuitry. Using results from CW and Matlab in Cadence has enabled co-simulation of CMOS and MEMS in order to get more realistic simulation results.

5.2 Tuneable MEMS VCO for A/D converter

This section describes an implementation of soft tuneable resonators combined with A/D (Analog-to-Digital) circuitry in a 90 nm STM CMOS process. The reason for this implementation was two-folded: It served as a purpose to investigate the possibility of going from coarse-grain CMOS processes to fine-pitch CMOS processes as well as expanding A/D design methodology with MEMS. The result from this implementation gave the possibility of implementing MEMS in a different 90 nm process later on. The work in this section is a result of a cooperation with PhD student Jørgen Andreas Michaelsen resulting in a tapeout, a book chapter [7] and a publication [8].

5.2.1 System idea

A Frequency $\Delta\Sigma$ Modulator (FDSM) based converter is used to convert frequency modulated (FM) signals to a quantized and discrete bitstream. Quantization

noise is shaped away from the signal band as a part of the FDSM. As a result, a Frequency-to-Digital (F/D) conversion takes place. The input FM signal is $x_{fm}(t) = cos[\theta(t)]$ where the $\theta(t)$ is given by

$$\theta(t) = 2\pi \int_0^t f_c + f_d x(\tau) d\tau \tag{5.1}$$

f_d is the maximum deviation from the carrier and f_c is the carrier frequency. The relationship between x_{fm} and the digital output y is shown in Fig. 5.2:

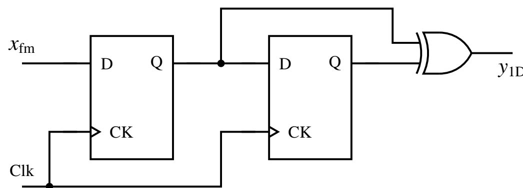


Figure 5.2: First order, single-bit FDSM using two DFFs and an XOR port

The time varying FM signal x_{fm} is converted to a digital bit signal as shown in Fig. 5.2 by using two Digital Flip-Flops (DFF) and an XOR port. The result is a digital bitstream y[n]. This is a simple implementation for a first order FDSM where the resolution for the converter is given by

$$SQNR_{dB} = 20log_{10}\left(\frac{\sqrt{2}f_d}{f_s}\right) - 10log_{10}\left(\frac{\pi^2}{36}\left(\frac{2f_b}{f_s}\right)^3\right) \tag{5.2}$$

where f_s is the output bitrate and f_b is the bandwidth of the input signal. f_s/f_c is assumed to be orders of magnitude larger than 1.

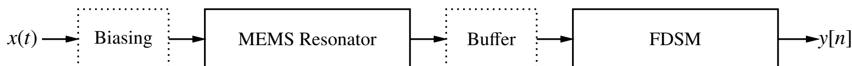


Figure 5.3: MEMS resonator and FDSM schematic

A schematic overview of the MEMS resonator and FDSM is seen in Fig. 5.3. The biasing of the resonator is from a DC voltage, V_P, which can be used to tune the resonance frequency of the resonator. This frequency tuning of $x(t)$ is detected as a bitstream $y[n]$ from the FDSM. By placing the resonator in a feedback loop with an amplifier and using V_P to control the frequency, this results in a Voltage Controlled Oscillator (VCO) circuit.

This thesis does not focus on the design of the FDSM, but concentrates on the resonator and analog amplifier design. More details about the FDSM are given in [7]. Combining a MEMS VCO and an FDSM circuit demonstrates the feasibility and possibilities that can be achieved when combining CMOS and MEMS. In order to create a self-oscillating loop with the MEMS resonator, a sustaining amplifier is required as described in section 5.2.2.

5.2.2 Sustaining amplifier design

The configuration of the resonator in a feedback loop including a sustaining amplifier is shown in Fig. 5.4. From the feedback loop, one path goes to a buffer and then to the FDSM. The clock for the FDSM is V_{CLK} while the terminal which tunes the frequency of the resonator is V_P.

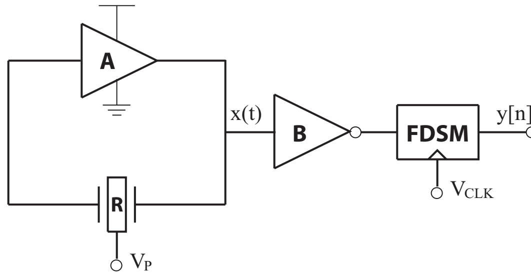


Figure 5.4: MEMS and amplifier creating an oscillator loop

The sustaining amplifier with its bias circuitry is shown in fig. 5.5. A diode connected nMOS transistor from the cascode current mirror configuration sets a fixed voltage on the gate of the nMOS transistor between V_O and V_I, causing the transistor to act as a high-impedance resistor. The input V_I is routed to the source of this feedback transistor as well as to the gate of an nMOS transistor (bottom right transistor in Fig. 5.5) which acts as a Common-Source (CS) amplifier. The current mirror provides a bias current I_d which controls the gain of the CS transistor through the transconductance g_m. The motional current from the resonator is converted to a voltage at the output of the node V_O.

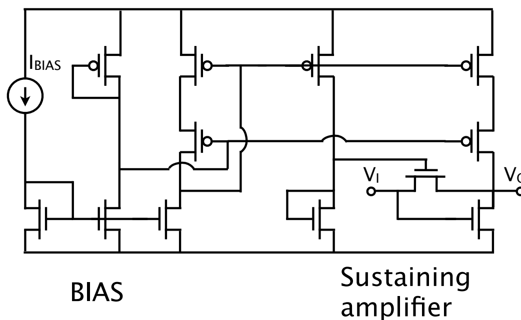


Figure 5.5: Pierce amplifier and belonging bias circuitry

In order to initiate and sustain oscillation, the feedback loop must have zero degree (or n multiple of 360 degrees) phase shift from the start to the end of the loop. In addition to this, the loop gain must be larger than one. The amplifier is designed to have a transimpedance gain Z_{TIA} (gain given in Ω). Z_{TIA} must be

larger than R_z which is the impedance representing the resonator during resonance. The gain of the amplifier should not be too large or else the oscillator will start oscillating with a damping factor which eventually turns it off again [59]. The transistor dimensions in Table 5.1 show that the feedback transistor is small and that the mirror and the CS transistor has a large W/L (transistor width over transistor length) ratio in order to achieve a large g_m.

	nMOS	pMOS
Width top left transistor [μm]	-	0.75
Length top left transistor [nm]	-	600
Width feedback transistor [nm]	150	-
Length feedback transistor [nm]	800	-
Width all other transistors [μm]	3.0	3.0
Length all other transistors [nm]	600	600

Table 5.1: STM 90 nm Pierce Oscillator circuit dimensions

The are two main challenges for CMOS-MEMS oscillators: Having a sufficiently large Q-factor and a small frequency drift. For oscillator applications it is possible to reverse the polarity of V_P in order to reduce frequency drift over time [60]. For CMOS-MEMS resonators with a sufficiently large Q-factor, it would be possible to add compensation circuitry which would reverse the polarity of V_P, making the frequency stable over time and giving low phase noise at the same time. The challenge, however, is to achieve adequate phase noise as the Q-factor for CMOS-MEMS resonators (with metal-dielectric stack) is limited to values between 1000 and 2000.

5.2.3 Results from soft-tuneable resonator implementations

Resonators implemented in the STM 90 nm process are designed to have a relatively low mechanical spring stiffness k_r so that the electrical spring stiffness k_e will reduce the effective spring stiffness k. It should be noted that non-linear terms become more dominant for this type of soft beam design, which was explained in chapter 3.4. This limits the maximum motional current of the resonator. Instead of showing this limit with respect to current, eq. 3.46 has been rearranged to demonstrate the minimum achievable motional impedance

$$R_z^{min} = \frac{V_I}{\eta \omega_0 z_c} \tag{5.3}$$

where V_I is the input voltage shown in Fig. 5.5. This equation demonstrates that η and z_c can only have a certain value before the resonator output produces a non-linear response, resulting in poor oscillator performance. This sets a design goal for how much gain the sustaining amplifier requires. If R_z is too large, the circuit may never start oscillating. Unfortunately, for the resonators presented here, the k was too small compared to k_e, resulting in pull-in conditions of the

beams instead. However, measurement results as well as results from analytical modeling and simulations will be shown in this section.

In order to understand the stability of the resonance frequency, the phase-noise of the system can be evaluated. Leeson's equation models the phase-noise-to-carrier ratio in an ideal oscillator:

$$\mathcal{L}(\Delta f) = 10log\left[\frac{k_B T}{\pi E_{stored}^{max}}\frac{Q}{f_0}\left(1+\left(\frac{f_0}{2Q\Delta f}\right)^2\right)\right] \tag{5.4}$$

where k_B is Boltzmann's constant, T is the absolute temperature, Δf is the frequency offset and E_{stored}^{max} is the maximum energy stored (eq. 3.47). It is common to relate eq. 5.4 to the power dissipated by the resonator (eq. 3.48), as well as adding a buffer noise source from the following amplifier after the resonator[41]:

$$\mathcal{L}(\Delta\omega) = \frac{2k_B T}{P_{dissipated}}\left(\frac{\omega_0}{2Q\Delta\omega}\right)^2 + \frac{P_N^{buffer}}{2P_{dissipated}} \tag{5.5}$$

P_N^{buffer} is buffer noise from an amplifier source. This value can be set to -155 $dBm/\sqrt{Hz}$ (or $v_n = 4\ nV/\sqrt{Hz}$ for a 50 Ω system). The phase noise is given by an offset in radial frequency ω. Investigating eq. 5.4 and 5.5, better energy storage capacity or less power dissipation will improve the phase noise of the oscillator. 1/f flicker noise arising from $1/\Delta\omega^2$ will limit the performance of these systems

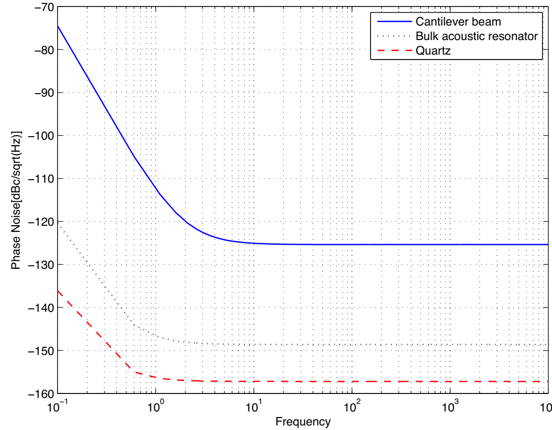


Figure 5.6: Theoretical comparison of Phase Noise for different resonator types

As can be seen in Fig. 5.6, the phase noise of the CMOS-MEMS cantilever beam is not as good as the phase noise of Quartz or SOI Bulk-Acoustic resonators. This shows that the phase noise for the cantilever beam is not good enough, mostly due to the low energy storage capacity but also due to the low electrostatic coupling.

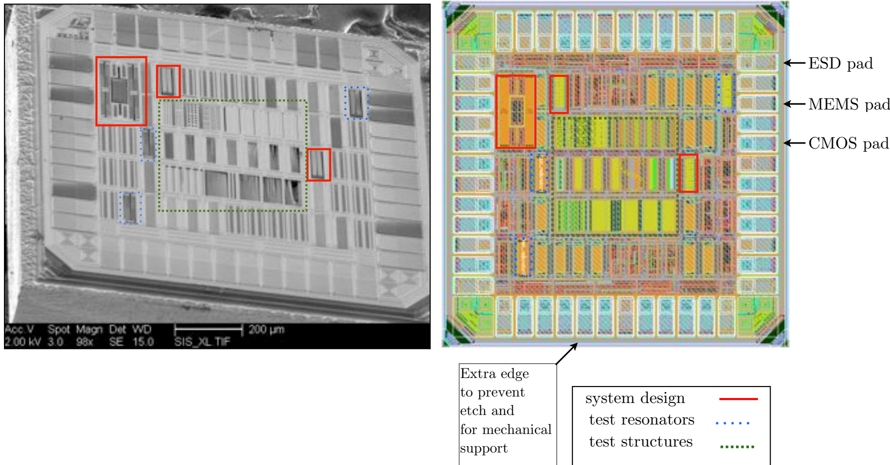


Figure 5.7: SEM and layout of implemented chip

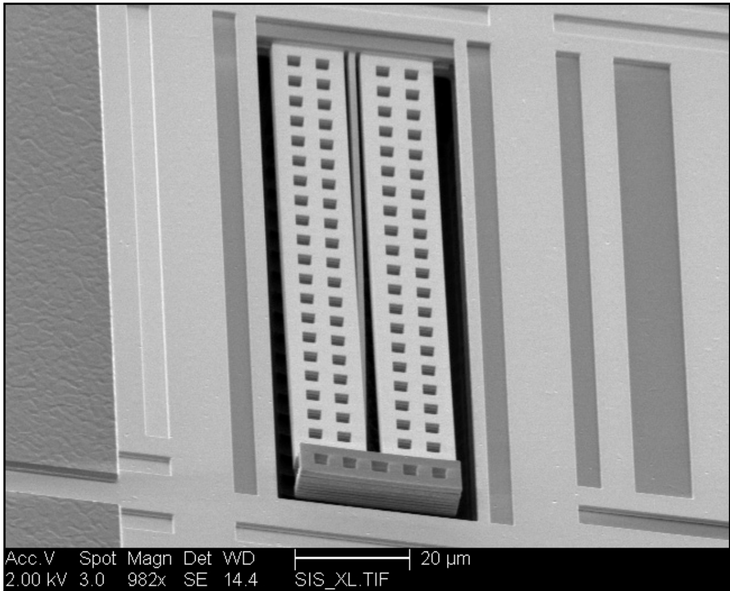


Figure 5.8: Cantilever beam with static electrode

The right part of Fig. 5.7 is a layout view of the implemented chip while the left part of Fig. 5.7 shows a SEM of the CMOS-MEMS processed chip. As can be seen in the figure, various resonators have been implemented as cantilevers, a CC-resonator and a PPTF. Input/output pads have been specially designed with ESD protection as well as bare MEMS pads for V_P voltages. The die and the pads complied with the CMOS foundry rules, albeit it took a long time to make the layout for this chip due to manual filling of dummy metal layers.

A SEM of a soft cantilever beam is seen in Fig. 5.8. An input and output electrode with holes surround the resonator. The cantilever beam does not curl with the same extent as the electrode frame surrounding the beam. The frame is mechanically connected, but the input and output part of the electrode is separated. Unfortunately, the beam is too much misaligned from its electrodes and the resulting output current is too low to be properly detected by the amplifier.

Another soft resonator implemented in this STM 90 nm tapeout is a CC resonator. The CC resonator including an SA electrode is seen in Fig. 5.9. This particular CC resonator is a 1-port beam, thus requiring decoupling of the V_P at the output. A narrow gap between the resonator and the electrode is seen at the left part of Fig. 5.9.

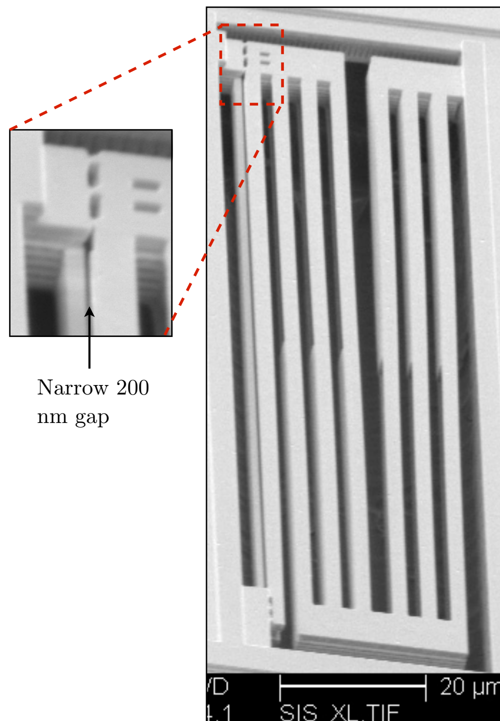


Figure 5.9: Clamped-Clamped resonator with self-assembly electrode

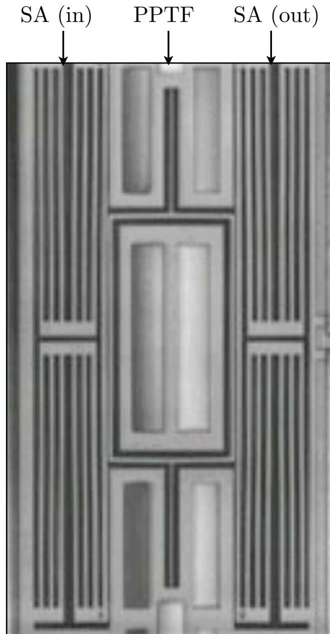


Figure 5.10: Overview of a STM 90 nm PPTF

The third resonator type implemented is a PPTF as seen in Fig. 5.10. The PPTF has input electrodes on the left side and output electrodes on the right side. These electrodes consist of double-jointed SA electrodes in order to achieve a large electrode area and design symmetry with less curling (both out-of-plane and lateral curling). Fig. 5.11 shows a zoom in of the PPTF in order to see the narrow gap between the SA electrode and the movable resonator. Table 5.2 shows the implemented designs and their respective dimensions. The cantilever resonator was designed as two versions with different gap sizes. The dimension labels for the PPTF in Table 5.2 are displayed in Fig. 4.10 on page 50. The thickness is roughly 3 μm for the metal-dielectric stack.

	Cantilever	**CC-beam**	**PPTF**
Resonator length [μm]	100	100	L_{FRAME}=100 $L_{CANTILEVER}$=50
Resonator width [μm]	1	1	W_{FRAME}=2 $W_{CANTILEVER}$=1
Resonator thickness [μm]	3	3	3
Electrode length [μm]	100	100	100
Electrode gap [nm]	1200/1000	200	200

Table 5.2: STM 90 nm resonator dimensions

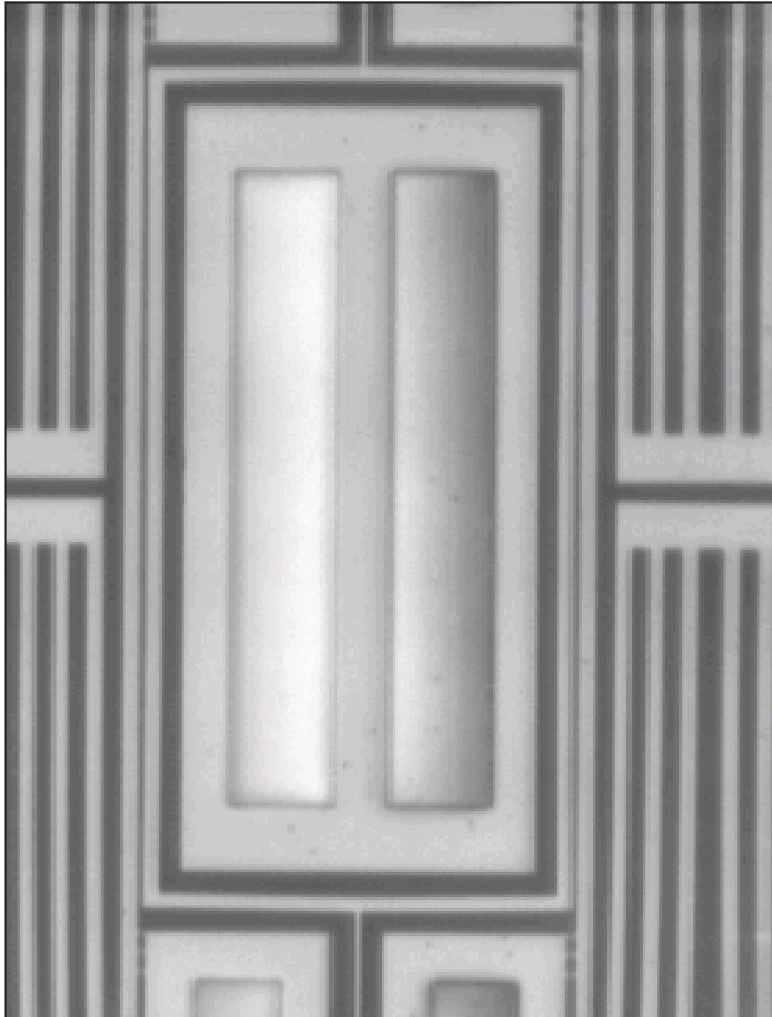
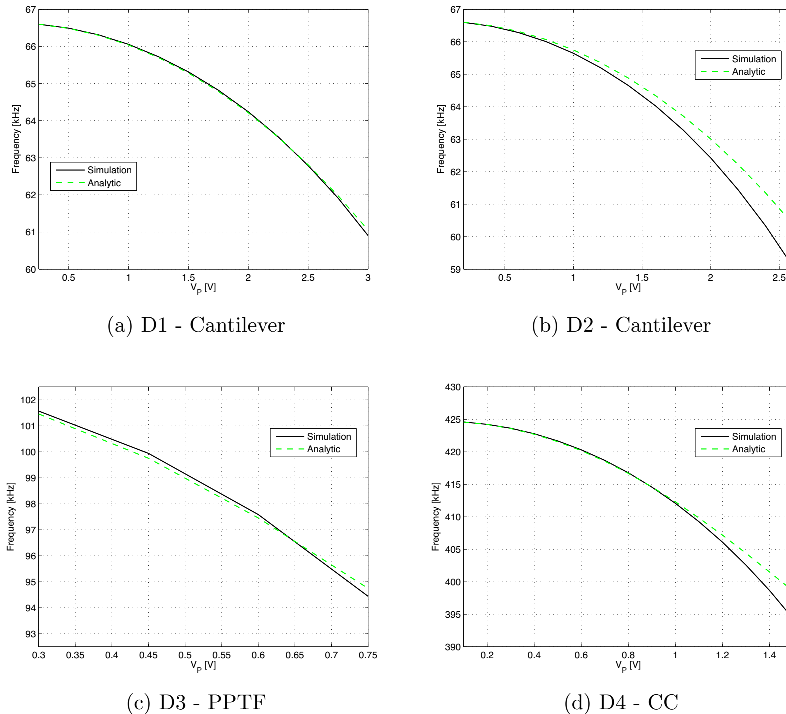


Figure 5.11: A zoom of the PPTF to see the narrow electrode gaps

The implementation of these resonators in this 90 nm process was the first attempt of using the 90 nm process, therefore the cantilever beams were implemented without self-assembly beams to be on the "safe side". The CC-resonator and PPTF were designed to "push the technology edge", and it turned out that these resonators were successfully released with a gap of 200 nm.



(a) D1 - Cantilever

(b) D2 - Cantilever

(c) D3 - PPTF

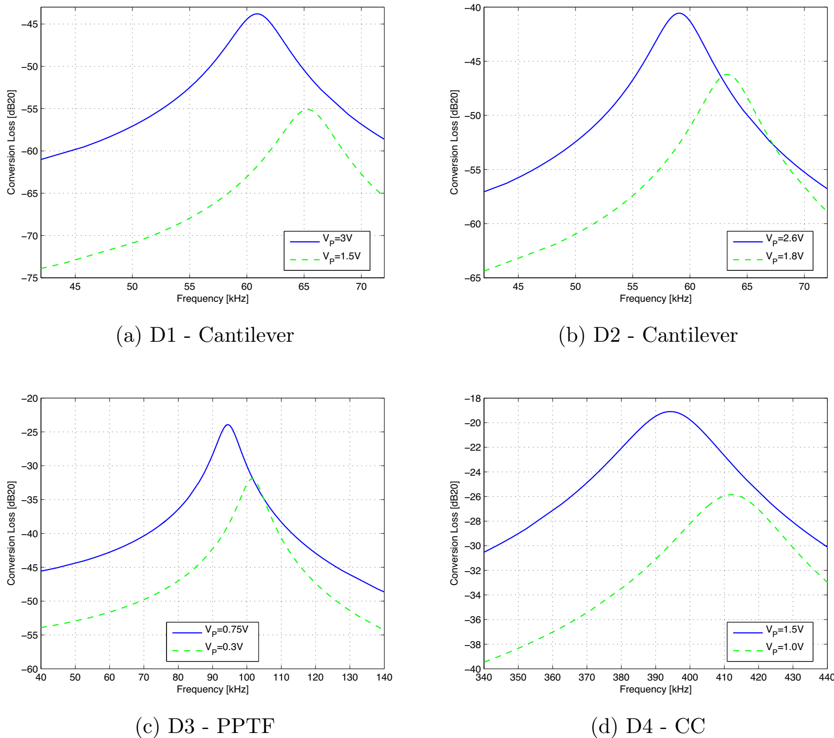
(d) D4 - CC

Figure 5.12: Simulation of f_0 as a function of V_P

Simulations using CW and analytical equations were calculated to model these resonators. The Matlab script describing the resonators was refined to take into account the important non-linear terms which may affect resonator performance. The simulations took a long time due to a large mesh density. The non-linear terms appearing from the FEM simulator was compared to analytical equations.

The frequency tuning range is demonstrated in Fig. 5.12. V_P is increased and f_0 is reduced for these four resonator designs. The four designs are denoted as D1, D2, D3 and D4. From the cantilever types, the D2 has the largest tuning range because it has a static gap of 1000 nm. D3 and D4 are resonators with a gap of 200 nm (using SA electrodes) where the CC-resonator (D4) gives the largest tuning range. The V_P voltage used for the PPTF is rather low compared to the other designs.

An AC plot of the D1 to D4 can be seen in Fig. 5.13. The transimpedance gain of the sustaining amplifier allows for voltage to voltage conversion giving the results in dB. Various voltages for V_P have been chosen because they are not the same for all resonators. A larger V_P results in a reduced resonance frequency and a larger throughput due to an increased motional current i_o.



(a) D1 - Cantilever

(b) D2 - Cantilever

(c) D3 - PPTF

(d) D4 - CC

Figure 5.13: Simulated AC plot showing the frequency tuning using V_P

Fig. 5.14 shows measurements of a CC-beam from the STM90 nm run, comparing results from before and after etching. Fig. 5.15 shows the same results, of the derivative. For a maximum output the derivative is zero. The unetched measurement showed a capacitive coupling of the CC-resonator as this is a 1-port topology. This shows that feedthrough is a factor which will greatly affect performance. The released beam shows a larger throughput due to the smaller electrode gap. The Q-factor of the resonator is rather low as this was measured in air.

A probed test of FDSM was performed as shown in Fig. 5.16. This was performed before and after etching the dies to make sure that the CMOS circuitry survived the post-CMOS etching process. The FDSM worked after etch as seen in Fig. 5.16, although not properly stimulated for the setup. This showed that the tapeout was successful with its special designed CMOS pads and pad ring.

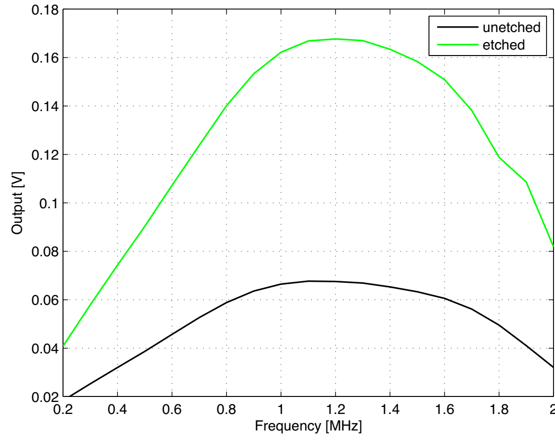


Figure 5.14: Feedthrough measurement for STM 90 CC-resonator

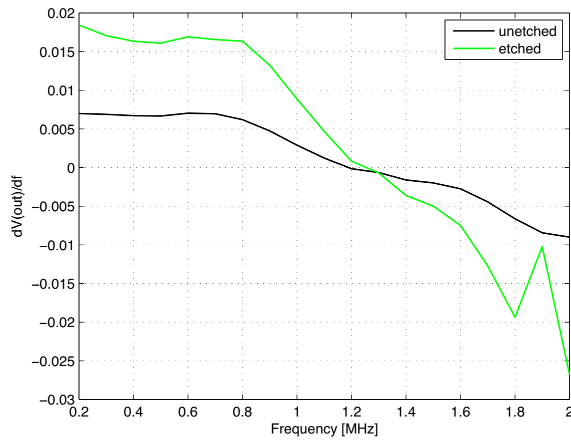


Figure 5.15: Feedthrough measurement for STM 90 CC-resonator (the derivative)

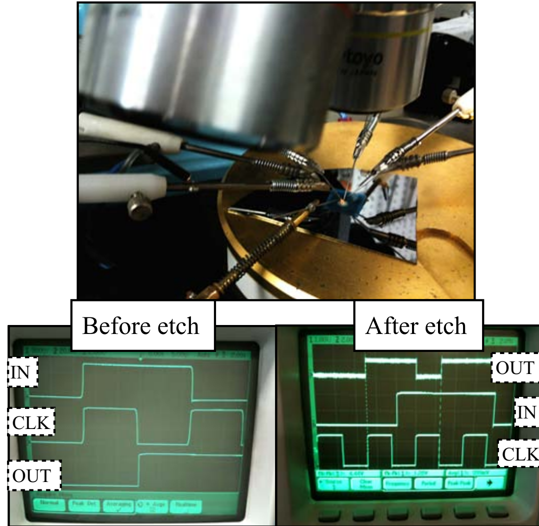


Figure 5.16: Measurement setup and results for measuring before and after CMOS-MEMS etch

The CC resonator has been designed to have a tuning-range of slightly more than 20 kHz using V_P from 0.5 V to 1.4 V. Potentially this results in a Signal-to-Quantization-Noise ratio (SQNR) of 38 dB which is about 6 effective bits. The testing of the FDSM before and after post-CMOS processing was done with 1 V on the ESD pads. The input of the FDSM was stimulated with 1 V at 10 kHz while the CLK signal was applied with 1 V at 40 kHz. The output of the FDSM was measured using an Agilent 54524A oscilloscope. Unfortunately, due to the beams being too soft to allow for a tuning range, the R_z of the resonator was significantly larger than the transimpedance gain provided by the sustaining amplifier, thus the systems would not start to oscillate.

Table 5.3 shows the results of the implemented resonators. The cantilever column is from design D2 with a gap of 1000 nm. The tuning range is best for the CC-beam while the PPTF shows the best percentage tuning range. The electromechanical coupling coefficient is best for the PPTF due to the large electrode area.

	Cantilever	**CC-beam**	**PPTF**
Nominal resonance frequency [kHz]	66.63	424.73	102.84
Frequency tuning range [kHz]	10.4	27.35	7.12
Tunability in percentage [%]	5.00	6.43	6.92
Effective spring stiffness [N/m]	0.074	4.74	4.30
Electromechanical coupling [nN/V]	8.19	35.24	55.34

Table 5.3: STM 90 nm resonator results

5.3 Low-noise amplifier design considerations

The previous section described a sustaining amplifier consisting of a Common-Source topology. That amplifier was designed to provide a gain between 1–10 MΩ, but was not really optimized for other important amplifier parameters. There are many specifications of an amplifier that can be considered: Power consumption, Total Harmonic Distortion (THD), slew rate, stable bias circuit, phase margins, gain, bandwidth, noise and so forth. Research on amplifier topologies for all of these parameters (and more) can be a topic by itself. This work has a specific focus on evaluating some amplifier topologies and at the same time studying the phase margins, gain, bandwidth and the amplifier noise. The different amplifier types studied in this thesis are:

- Common-Source amplifier (STM 90 nm)
- Common-Gate, Common-Source, Common-Source, Source Follower (CG-CS-CS-SF) in TSMC 0.35 μm (single transistor, 4 stages)
- Full differential amplifier with common-mode feedback in TSMC 0.35 μm
- Class AB output buffer in TSMC 0.35 μm and 90 nm
- Differential-to-single-ended amplifier in TSMC 90 nm
- Full differential folded cascode amplifier in TSMC 90 nm
- Inverter amplifier in TSMC 90 nm

In addition to this, the conversion method converting the motional current to an output voltage can be evaluated. Some evaluations of these amplifier implementations will be discussed.

5.3.1 Noise contributions

It is difficult to measure noise levels, so the noise analysis is based on simulations. From an analytical point of view, the following thermal noise contributions are the most important ones:

$$E_{n,C} = \sqrt{\frac{kT}{C}} \tag{5.6}$$
$$E_{n,R} = \sqrt{4kTR\Delta f} \tag{5.7}$$
$$E_{n,M} = \sqrt{4kT\gamma g_m} \tag{5.8}$$

These three thermal noise contributions are given in $V/\sqrt{Hz}$. $E_{n,C}$ is the thermal noise from capacitive contributions, integrating noise over the band of interest. $E_{n,R}$ is thermal noise from resistors while $E_{n,M}$ is thermal noise from transistors.

There are other noise sources, such as flicker noise, shot noise and popcorn noise but for simplicity thermal noise is considered here as it contributes to most of the noise. For transistors, γ depends on the length of the transistor and is 2/3 for short channel transistors and up to 2 for coarse-grain processes with large transistor lengths. The methodology for analytically deriving input referred noise is by collecting all the noise terms at the output and dividing by the transimpedance gain of the amplifier. The end result is an input referred noise current:

$$I^2_{N(in,tot)} = \int_{f_1}^{f_2} I^2_{N(in)} df \tag{5.9}$$

$I_{N(in)}$ is the input referred noise at one particular frequency. However, this noise must be integrated over the band of interest. For micromechanical resonators, $f_2 - f_1$ is equal to the bandwidth of the filter. This leads to the development of the equation for Signal-to-Noise Ratio (SNR):

$$SNR = 20log_{10}\left(\frac{i_o}{I_{N(in,tot)}}\right) \tag{5.10}$$

Eq. 5.10 shows that if the motional current is 10 times the noise, then the SNR is 20 dB which is a target goal. That is, the resonator current should be designed to be at least larger than 20 dB if possible. A general differential amplifier is shown in Fig. 5.17. This is an open-loop configuration with no feedback element. The current from the resonator goes through the parasitic capacitances $C_{p,in}$ which creates a voltage at that node which is then amplified through the open loop gain. Capacitors at the output part of the TIA indicates parasitics which can limit the bandwidth of the amplifier. The parasitic capacitances $C_{p,in}$ can be the internal capacitances of the amplifier (i.e. gate-source capacitance of an input transistor), routing capacitances as well as any capacitance originated from the MEMS resonator. The load capacitance ($C_{p,out}$) at the output is from the routing and the load which the next amplifying stage represents.

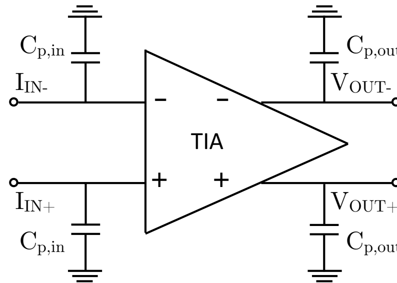


Figure 5.17: General full differential TIA schematic

A simulation of integrated noise is shown in Fig. 5.18. The total noise for this full differential amplifier is 75 fA/$\sqrt{Hz}$. In this example the integration has been done over a bandwidth of 1 MHz, giving 80 pA of noise. For an input of 25 nA

motional current from the filter results in an SNR of 49 dB. If the current is only 1 nA, then the SNR is 21.93 dB, thus the i_o should not be lower than 1 nA.

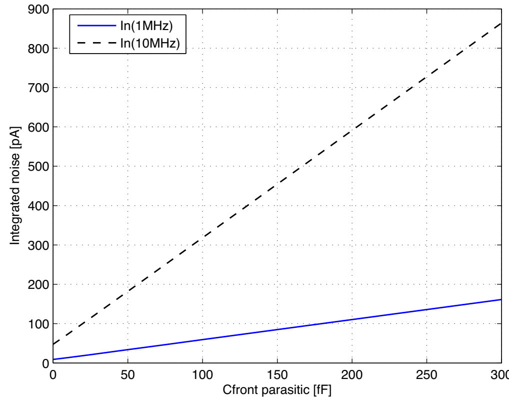


Figure 5.18: Simulated integrated noise for 1 MHz BW at 1 MHz and 10 MHz

Analytical calculations of a CG-CS-CS-SF transimpedance amplifier have been performed to validate the importance of noise contributions from transistors and resistors. Fig. 5.19 shows the schematic of the 4 transistor stage amplifier. The noise study confirmed that thermal noise is the most dominant source of noise and that adjusting transistors accordingly will cause a reduction of noise. The feedback resistor R_F will contribute to noise in addition to the transistors, due to their transconductance g_m.

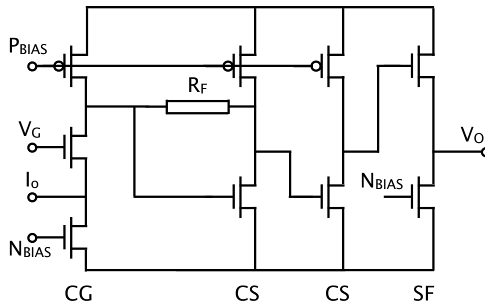


Figure 5.19: Single-ended 4 stage transistor TIA

The CG-CS-CS-SF transimpedance amplifier proved a low input resistance due to the common-gate (CG) configuration at the first stage of the amplifier. The second amplifying stage is a common-source (CS) stage with a resistor in feedback. The second CS stage is without any feedback path and finally the source-follower (SF) provides low output impedance and is able to drive large loads. It should

be noted that although the single-ended transistor topology is simple, this chained four transistor stage resulted in numerous complex poles which complicated the design methodology.

From the CG-CS-CS-SF, the leftmost nMOS and pMOS bias transistors including the CG transistor, provided most of the noise in the circuit. The next largest contribution came from the R_F resistor. This single-ended 4 stage transistor TIA proved to have low noise, however it was relatively difficult to make the biasing and DC voltages become stable for the four corner simulations. Due to the difficulties of the biasing circuit and providing stable DC voltages for the nodes, it was interesting to investigate how to achieve less noise, better phase margins and more stable bias circuitry by using other amplifier topologies.

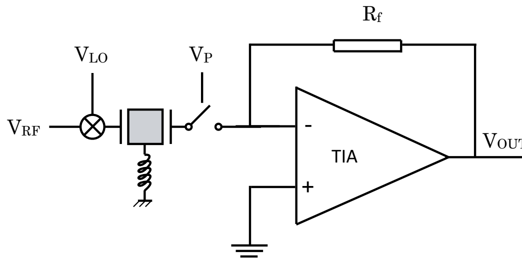


Figure 5.20: Differential-to-single-ended amplifier with resistive feedback

Fig. 5.20 shows the resonator represented as a mixer-filter symbol in combination with a TIA that has a resistive feedback element R_f. A full differential TIA with output buffer is shown in Fig. 5.21. This topology was interesting as the capacitors do not directly contribute to noise, however it was not further investigated due to the non-linear gain from the capacitors and the challenge of setting DC values at the input and output of the amplifier.

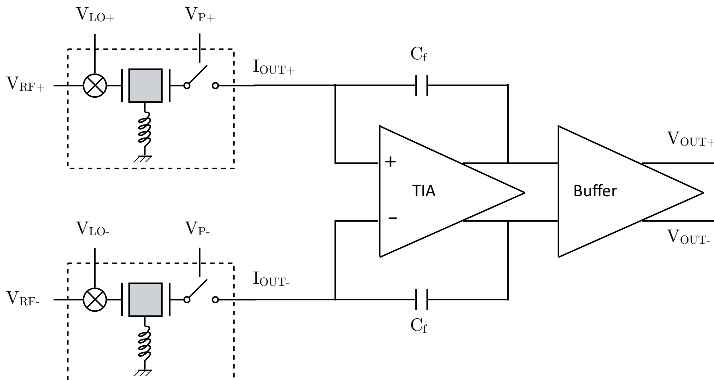


Figure 5.21: Fully differential amplifier with capacitive feedback and output buffer

5.3.2 Investigating amplifier toplogies

The output buffer of Fig. 5.21 can be implemented in various ways depending on the desired usage. For high frequency measurements, or for transmitters, the buffer should provide a low output impedance with very little loss and at the same time be able to drive large loads. An example of such a buffer is the Class AB buffer shown in Fig. 5.22. The Class AB amplifier provides good linearity, although it consumes a lot of power. As seen in Fig. 5.22, the input stage is a push-pull common-drain transistor configuration and the output is a push-pull source-follower which results in a low output impedance.

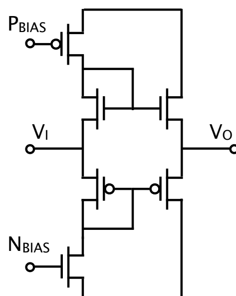


Figure 5.22: Class AB amplifier

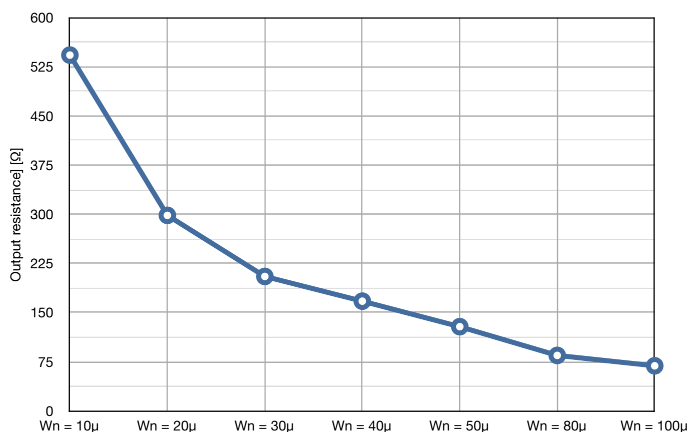


Figure 5.23: Simulated class AB amplifier output impedance as a function of W_n

Achieving a low output impedance is possible by having large transistor widths. Fig. 5.23 shows variation of the output transistor widths W_N (where $W_P = 2W_N$). The output transistor dimensions are quite large in order to achieve good output impedance matching. This example requires a large bias current of 50 μA, thus leading to a power consumption of 582.9 μW. A stable Class AB amplifier is difficult

to make, especially in lower pitch CMOS technologies. There is a tradeoff between power and area consumption for this type of output buffer. For a CMOS-MEMS mixer-filter receiver, the impedance matching and load driving can be provided directly from the transimpedance amplifier with output impedance which matches the succeeding circuitry.

	Input stage	Output stage
Width [μm]	11.5	13
Length [nm]	800	750
# of fingers	13	2

Table 5.4: TSMC 90 nm Class AB transistor dimensions

The sizes of the transistor widths, lengths and number of fingers are shown in Table 5.4. The total width at the output is much larger due to the amount of fingers. This setup was optimized to get an output impedance close to 50 Ω. Transistors that are sliced up with multiple amount of fingers are less prone to process variations and should be centered around a middle finger in order to achieve best symmetry.

	TT	SS	SF	FS	FF
Power [μW]	582.9	533.92	578.52	587.89	623.13
Bandwidth [MHz]	31.59	30.26	31.26	31.92	33.62
Gain @ 10MHz [dB]	26.28	24.1	26.14	26.41	27.62
Z_{out} @ 10MHz [Ω]	50.29	55.21	51.16	49.43	46.64

Table 5.5: Corner simulation results for the TSMC 90 nm Class AB amplifier

The results from corner simulations of the TSMC 90 nm class AB amplifier are shown in Table 5.5. The power consumption is rather large for this amplifier due to the fact that it is able to drive large capacitive loads with a good gain and a low output impedance of about 50 Ω. The Class AB amplifier is relatively stable on all four corners.

	100fF	300fF	1pF	10pF	100pF
Bandwidth [MHz]	31.59	31.62	31.72	32.64	24.60
Gain @ 10MHz [dB]	26.28	26.28	26.27	26.17	23.68
Ringing pole location [MHz]	104.71	104.71	104.71	69.18	13.18

Table 5.6: Results for TSMC 90 nm Class AB amplifier when varying the load capacitance

In Table 5.6 the Class AB amplifier has been simulated with increasing load capacitance. The bandwidth is about 31–32 MHz up to 10 pF and starts to decrease to 24.6 MHz at 100 pF, showing that the circuit is able to drive large loads. The undesired ringing pole has been extracted from the simulator and is constant at 104.71 MHz up to 1 pF, but for about 100 pF the ringing pole location is at 13.18 MHz which is inside the passband, making the circuit unstable.

This shows that the circuit is good to drive off-chip measurement equipment when characterizing CMOS-MEMS resonators. Having evaluated buffer amplifiers, the Trans-Impedance Amplifier (TIA) topologies need to be investigated.

Fig. 5.24 shows an implemented full-differential amplifier with bias circuitry and a common-mode feedback circuit. The implementation is based on an amplifier simulated while staying at CMU and was used in one out of two tapeouts there. The diode connected nMOS transistors between the gate and the drain of the differential input transistors ensures that the DC voltages are correctly set. The setup of the amplifier is the same as shown in Fig. 5.17 where the differential amplifier provides an open-loop gain of 73 V/V at 10 MHz for an output load of 10 pF. The cut-off frequency was simulated to be at 20 MHz. The noise at 10 MHz is simulated to be 74.85 $fA/\sqrt{Hz}$ which leads to an SNR of 70 dB and 65.6 dB for two different filter bandwidths. The gain is rather large due to open-loop gain, however the gain is not precisely controlled and will vary with process variations. This amplifier is used for measurement of mechanically coupled SFRs described in the next section.

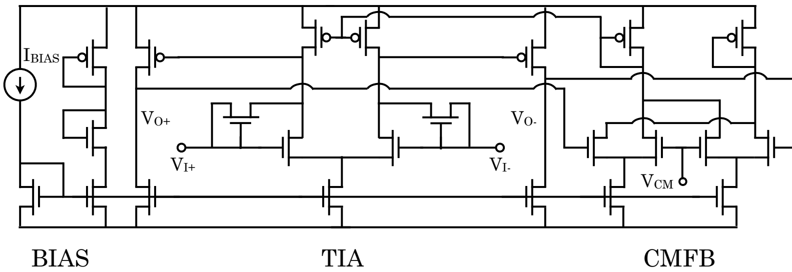


Figure 5.24: Implemented TSMC 0.35 μm full differential TIA w/CMFB

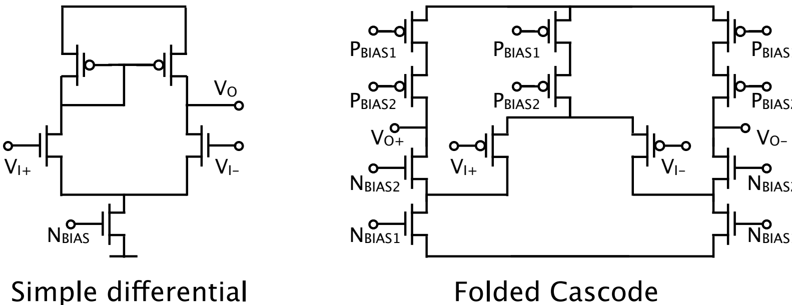


Figure 5.25: Simple Differential and Folded Cascode amplifiers

Based on the TSMC 0.35 μm 4-stage transistor of Fig. 5.19 and the full differential amplifier of Fig. 5.24, the next step was to investigate TSMC 90 nm amplifier topologies which could be suitable for a following tapeout. Fig. 5.25

shows a simple differential to single-ended amplifier and a full differential folded cascode amplifier. The dimensions of the TSMC 90 nm folded cascode amplifier with multiple fingers are shown in Table 5.7. The third amplifier type which was investigated was an inverter based amplifier with one or an odd order multiple of inverters with a feedback resistor R_f.

	Dimensions
Width P_{BIAS1} & P_{BIAS2} output branches [μm]	2
# fingers P_{BIAS1} & P_{BIAS2} output branches	6
Length P_{BIAS1} & P_{BIAS2} output branches [nm]	500
Width P_{BIAS1} & P_{BIAS2} input branch [μm]	2
# fingers P_{BIAS1} & P_{BIAS2} input branch	12
Length P_{BIAS1} & P_{BIAS2} input branch [nm]	500
Width N_{BIAS2} [μm]	1
# fingers N_{BIAS2}	2
Length N_{BIAS2} [nm]	500
Width N_{BIAS1} [μm]	1
# fingers N_{BIAS1}	4
Length N_{BIAS1} [nm]	500
Width input nMOS transistors [μm]	1
# fingers input nMOS transistors	4
Length input nMOS transistors [nm]	500

Table 5.7: TSMC 90 nm Folded Cascode amplifier dimensions

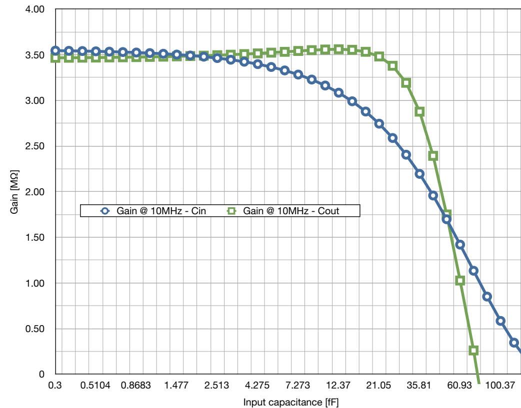
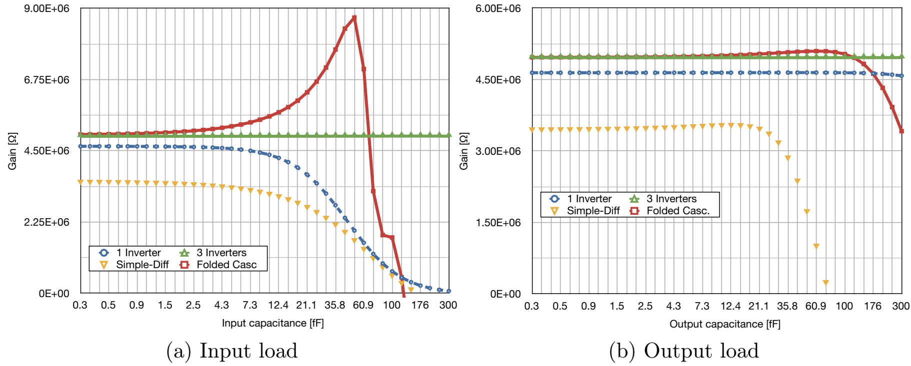


Figure 5.26: Differential amplifier gain as a func. of input and output load capacitances

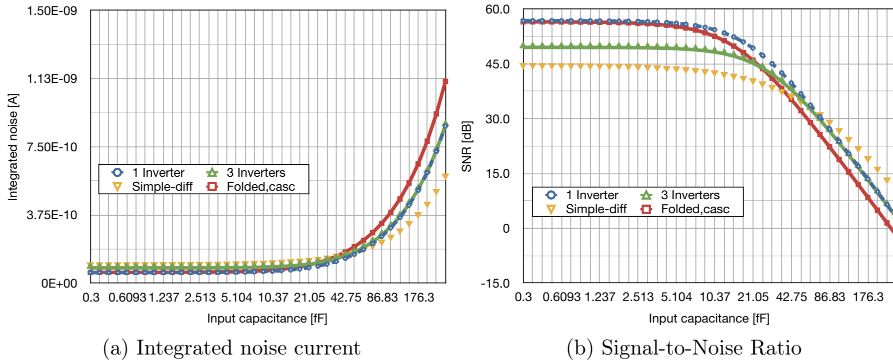
An example of reduction of gain due to increased load capacitance is demonstrated in Fig. 5.26. The simple differential amplifier of Fig. 5.25 has been simulated, showing that the gain is drastically reduced for either input or output capacitive loads in the range of tens of fFs. The designed gain of 3.5 MΩ is able to drive up to a few fF of load capacitance.

In Fig. 5.27, various amplifier architectures are for a TSMC 90 nm process are compared at 10 MHz to see how good they are to drive input and output capacitive loads. The gains that can be achieved vary between 3 and 5 MΩ, where the folded cascode (FC) has the best gain. The inverter based amplifiers were best at driving large output loads as shown in Fig. 5.27.



(a) Input load (b) Output load

Figure 5.27: Simulated gain as a function of input and output capacitive load for various amplifiers



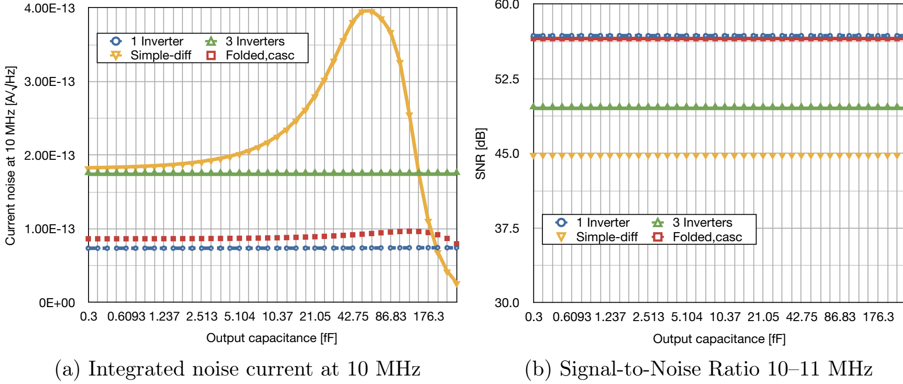
(a) Integrated noise current (b) Signal-to-Noise Ratio

Figure 5.28: Simulated integrated noise and SNR as a function of input capacitive load

The comparison of the four amplifier types is continued in Fig. 5.28, showing integrated noise and SNR. The integrated noise is from 10 MHz to 11 MHz in order to get noise for a 1 MHz bandwidth. This will lead to a certain Signal-to-Noise ratio (SNR) as seen in fig. 5.28(b). These amplifiers have been implemented to test the different noise levels of the amplifiers due to the low current provided by the MEMS resonators.

CMOS amplifiers with low noise are important. Thus, a large gain, large bandwidth and low noise are focused. The folded cascode amplifier stands out as a

possible candidate which will provide good results. However, due to limited time when preparing the tapeout, an inverter based amplifier was chosen. The SNR for the amplifiers varies from 45 dB to around 55 dB where the single-inverter type shows good results. Varying the output capacitance is demonstrated in Fig. 5.29. The integrated noise at 10 MHz will vary while the SNR (integrated over a 1 MHz bandwidth) remains constant for all the amplifier types.



(a) Integrated noise current at 10 MHz (b) Signal-to-Noise Ratio 10–11 MHz

Figure 5.29: Simulated noise at 10 MHz and 10–11 MHz SNR as a function of output capacitive load

	SNR 10–11MHz [dB]	Noise @10MHz [fA/$\sqrt{Hz}$]	Noise 10–11MHz [pA]	Z_{TIA} @10MHz [MΩ]
1 Inv	24.68	73.61	58.35	4.642
3 Inv	21.51	174.0	84.06	4.956
SD	19.50	224.2	105.9	3.562
SD, cap	19.86	15.39	101.6	0.1492
FC	24.55	90	59.2	5.040
FC, cap	27.93	3.54	40.15	1.300

Table 5.8: TSMC 90nm amplifiers with SNR, noise and gain @ 10MHz or 10–11MHz

Table 5.8 is a summary of simulation results in Cadence of different amplifier topologies. The simple differential (SD) and folded-cascode (FC) were tested with capacitive feedback as well. They were all simulated in the TSMC 90 nm kit with a feedback resistor of 5 MΩ or feedback capacitor with 10 fF. A 10 fF capacitor is "low enough" according to the specification of the capacitor of the foundry and will not vary much with the process. The gain of a feedback capacitor, however, is not constant and decreases with increasing frequency. The output load is only set to 10 fF for simplicity.

The results show that the 3 inverter amplifier is next best, even with worse SNR, but with a large gain. The folded cascode with a capacitor has the best

SNR, but the lowest gain. The folded-cascode is more difficult to design and it also requires a common-mode feedback circuit (CMFB) which will increase the power consumption. To make it easier to test the amplifier for the TSMC 90 nm tapeout, an inverter based amplifier was made, although a folded-cascode amplifier was considered. The feedback resistor was chosen instead of the capacitor because it makes the biasing of the amplifier more simple. The noise generated from the resistor will directly add to the input and a resistor in the MΩ range is rather large, so a capacitor is a preferred solution if the input and output of the amplifier is properly biased. The capacitor will not directly add to noise but will be responsible for shaping the noise bandwidth and accumulate the noise over the band.

Another important factor is the input capacitance of the amplifier. An input capacitor will represent the parasitics arising from the input transistors, the routing to the feedback element, routing to the MEMS resonator and possible parasitics to the substrate from the open areas beneath the SA electrode. Careful design and calculations on this has been done for the TSMC 90 nm tapeout, aiming for a rather low input capacitance. Fig. 5.30 shows the TSMC 90 nm inverter amplifier which consists of three amplifiers in series where the first stage converts from current to voltage and the last two stages are voltage-to-voltage gain stages.

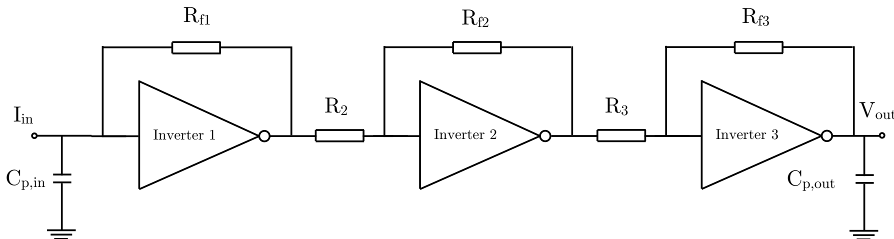


Figure 5.30: TSMC 90 nm inverter TIA schematic

	Resistor value		Transistor width
R_{f1} [kΩ]	800	W_{n1} [μm]	1.6
R_2 [Ω]	200	W_{p1} [μm]	3.36
R_{f3} [kΩ]	800	W_{n2} [μm]	2.4
R_2 [Ω]	200	W_{p2} [μm]	5.04
R_{f3} [kΩ]	10	W_{n3} [μm]	9.6
		W_{p3} [μm]	20.16

Table 5.9: Resistors and transistors sizes in the inverter TIA circuit

Table 5.9 shows the resistor dimensions and the dimensions of the pMOS transistors in the circuit. All transistor lengths are 100 nm. The setup of simulations for the TSMC 90 nm was 1 nA current from the MEMS filter. The routing from the output of the resonator is about 25 fF. The circuit was made to drive an output load of up to 10 pF in order to be able to drive off chip measurement equipment. The

output was expected to be between 10–12 mV. 300 Process & Mismatch variation runs were performed to see the statistical variation of the circuit performance.

	TT	FF	FS	SF	SS	MC_μ	MC_σ
Phase Margin [°]	92.5	95.27	92.78	92.1	88.56	92.34	0.79
Bandwidth [MHz]	38.11	34.62	38.03	38.21	40.59	38.08	0.75
TIA gain @ 10MHz [MΩ]	11.84	12.26	12.19	11.39	9.21	12.02	0.22
SNR 10–11 MHz [dB]	16.56	16.51	16.55	16.58	16.62	16.52	0.01

Table 5.10: TSMC 90 nm inverter amplifier simulation results

Table 5.10 shows the results of corner simulations. The input and output DC voltages are stable around 620–650 mV. The phase margin is very stable, typically above 90°. The bandwidth of the circuit provides a bandwidth of about 38 MHz, which makes it possible to encompass higher order modes of some of the resonators within the passband as explained later. The SNR is roughly 16.5 dB, close to the desired specification of 20 dB.

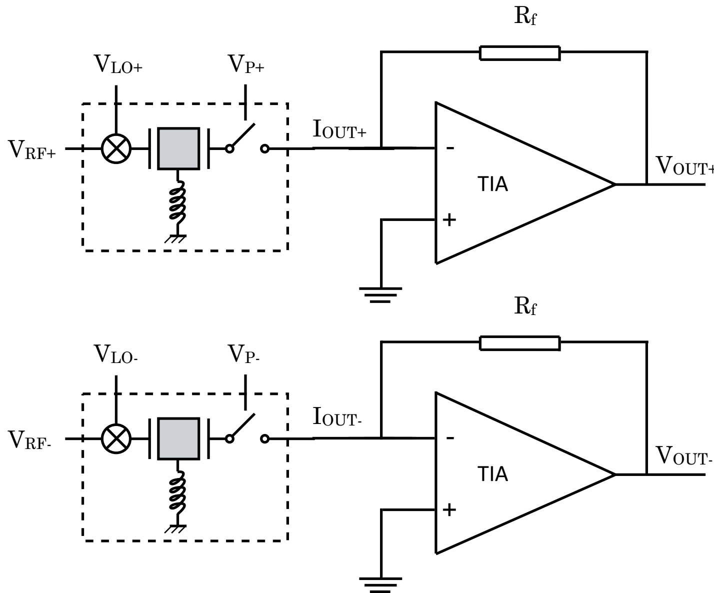


Figure 5.31: Schematic of differential mixer-filter with amplifiers

Fig. 5.31 shows two inverter amplifiers together with their respective resonators making a differential filter in the TSMC 90 nm run. The two mixer-filter symbols are one and the same component (and not two different components), the differential resonator has 8 terminals, creating two differential currents I_{OUT+} and I_{OUT-} which is further processed by two different inverter-amplifiers.

5.4 SFR and PPTF implementations

Square-Frame Resonators (SFRs) have been implemented in coarse-grain and fine-pitch CMOS processes. The FFSFR was first implemented in a TSMC 0.35 μm process, both as a single resonator and as a mechanically coupled higher order filter. Another implementation was performed in a TSMC 90 nm process where FFSFR, CCSFR and PPTF higher order filters were made.

5.4.1 TSMC 0.35 μm FFSFR filters

Two different chip designs in a TSMC 0.35 μm CMOS process were made. The first design consisted of a single FFSFR, one 4th order and one 6th order mechanically coupled FFSFR-filter. The second design consisted FFSFRs coupled electrically, as was described in chapter 4.2.1. All of the composite resonators shown here follow a voltage-to-voltage conversion using Trans-Impedance amplifiers (TIAs). A common measure of performance of a resonator including a succeeding TIA is known as "Conversion Loss" (CL):

$$CL = 20log_{10}\left(\frac{i_o Z_{TIA}}{V_{RF}}\right) = 20log_{10}\left(\frac{Z_{TIA}}{R_z}\right) = 20log_{10}\left(\frac{V_o}{V_{RF}}\right) \quad (5.11)$$

Eq. 5.11 shows the conversion loss of a resonator which produces a motional current i_o due to an input voltage V_{RF}. i_o times Z_{TIA} equals the output voltage detected at the output of the amplifier. Eq. 5.11 can be stated in three different ways, all defining the one and same "Conversion Loss". The reason for the name "Loss" is due to the fact that the resonator and the amplifier typically results in a lower output voltage than the input voltage for these CMOS-MEMS resonators.

Fig. 5.32 shows the implemented chip layout where 1-FFSFR is a standalone resonator and 2-FFSFR & 3-FFSFR are mechanically coupled resonators. The 1-FFSFR was made in two different versions: One which is stimulated as usual with west and east SA electrodes and north and south SA electrodes used for the output. The other type was made with static electrodes and gaps of 1.5 μm seen as version b in Fig. 5.32. This FFSFR is a full-differential resonator with inside and outside electrodes where the outside electrodes stimulate and the inside electrodes are the output. This adds four more terminals to the whole device. The drawback of that device is that it requires intricate routing, and it becomes difficult to implement SA electrodes for the whole device. It is also more difficult to stimulate and test the device and the gap is limited to 1.5 μm.

Fig. 5.33 shows a 4th order mechanically coupled FFSFR including its SA electrodes. The internal routing shows the intricate internal routing of the device, allowing V_{LO-} and V_{LO+} to be routed to the one and same tether beam without electrically short-circuiting each other. The device is stimulated with + and $-$ input signals as well as differential V_{LO} and V_P signals internally in the resonator. The output is a differential current which leads to the full differential amplifier shown in Fig. 5.24 in chapter 5.3.1.

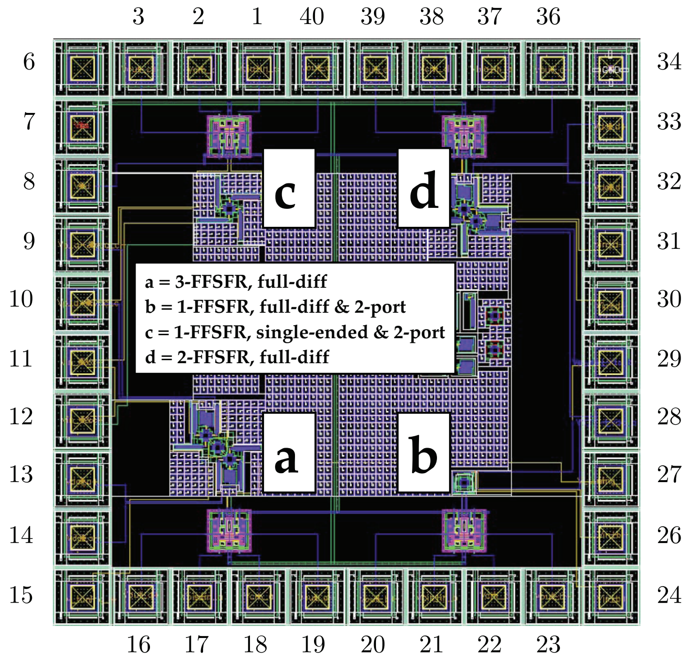


Figure 5.32: Layout of the TSMC 0.35 μm tapeout

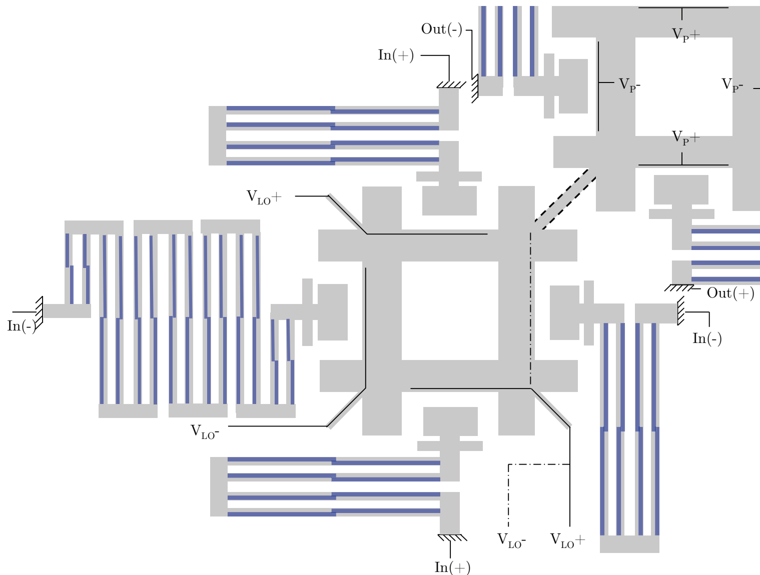


Figure 5.33: Schematic of a 4th order FFSFR with self-assembly and routing

	FFSFR
Resonator length [μm]	47
Resonator width [μm]	4
Electrode length [μm]	16.5
Electrode gap [nm]	300
Tether length [μm]	9.1
Tether width [μm]	0.6
Coupling length [μm]	16.62
Coupling width [μm]	2

Table 5.11: Dimensions for TSMC 0.35 μm FFSFR resonator filter

Table 5.11 shows the dimensions of the 4th order FFSFR implemented in a TSMC 0.35 μm CMOS process. The Free-Free beams are 4 μm wide with a length of 47 μm. The tether beams only have a width of 0.6 μm and are 9.1 μm long. The coupling beams are designed with a $\lambda/4$ length of 16.62 μm and a width of 2 μm. The increased size of the coupling beams was necessary in order to separate the two FFSFRs from each other, making it possible to create a layout of this mechanical filter with self-assembly electrodes.

Fig. 5.34 shows a 6th order FFSFR filter. A zoom in of the middle resonator with dummy electrodes (not connected) is shown in Fig. 5.35. By designing all gaps in the layout to be 1.5 μm before the mechanical structures are released, it is possible to reduce process variations. Fig. 5.36 and 5.37 are SEMs of a standalone FFSFR with SA electrodes. A narrow gap between the SA electrode and the resonator is possible due to the limit stops which prevent the SA electrode from physically touching the FFSFR.

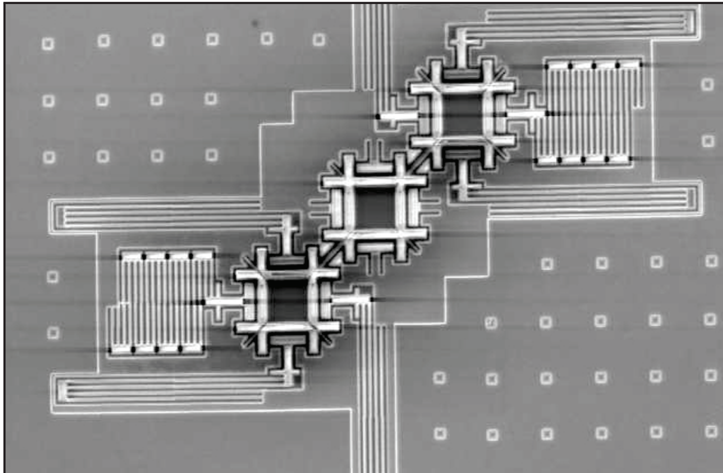


Figure 5.34: SEM picture of implemented 6th order FFSFR

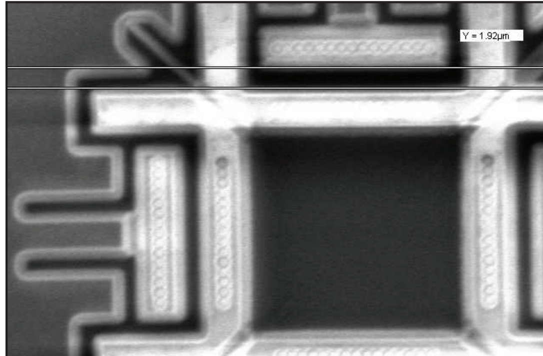


Figure 5.35: SEM of middle part of 6th order FFSFR

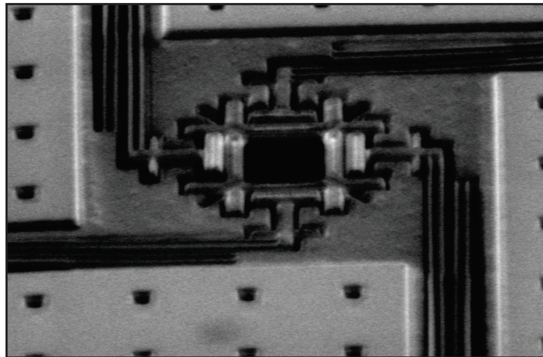


Figure 5.36: SEM of standalone FFSFR with SA

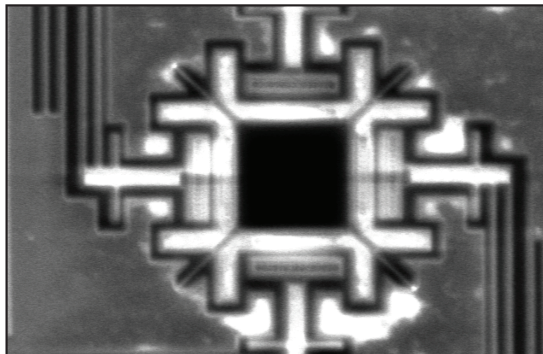


Figure 5.37: SEM of standalone FFSFR with narrow gap

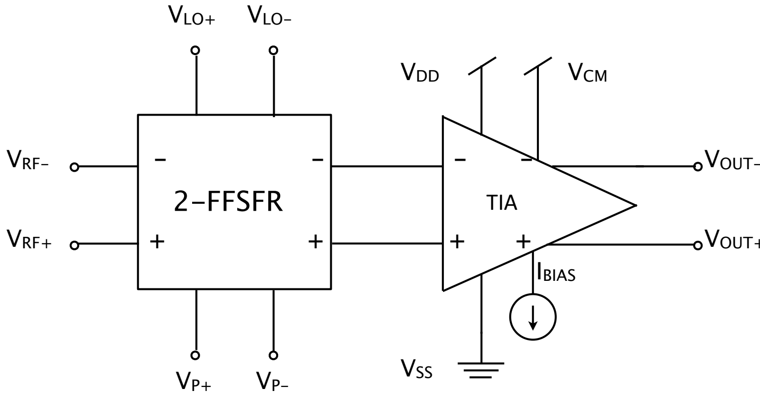


Figure 5.38: Measurement setup for testing differential resonators

The measurement setup for differential resonators is shown in Fig. 5.38. This example shows two mechanically coupled resonators (2-FFSFR) although three mechanically coupled resonators (3-FFSFR) follow the same setup.

A simulated filter response of a 2nd, 4th and 6th order FFSFR filter is shown in Fig. 5.39. The input stimulus is 1 V and V_P is 10 V. The current generated at the output is simulated to be 25 nA, leading to a motional impedance of 40 MΩ. The TIA gain of 6 MΩ from the differential amplifier results in ca 150 mV at the output. The differential amp is designed to have V_{DD}=3.3V and V_{CM}=1.65V. The bias current drawn for the circuit, including the common mode network is 160 μA.

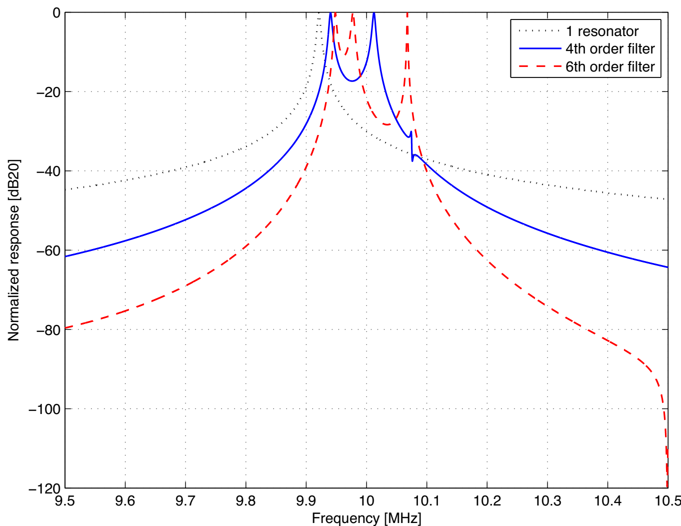
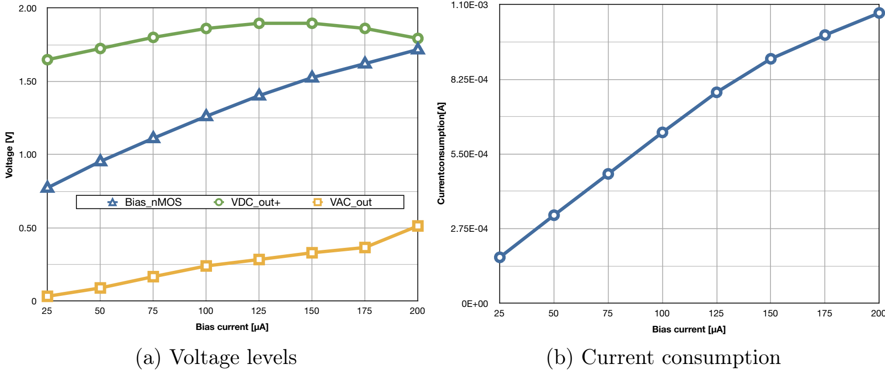


Figure 5.39: Simulated filter response of 2nd, 4th and 6th order SFR filters



(a) Voltage levels (b) Current consumption

Figure 5.40: TSMC 0.35 μm differential amplifier measurements

The differential amplifier was tested with various voltage levels in order to find the optimal biasing conditions. As can be seen in Fig. 5.40, the bias current has been swept and voltage levels and the current consumption have been measured for Run 1, Die 1 (R1D1). The input was stimulated with 1 V and 180 degree phase shift at the resonator input in order to check the desirable operation level of the amplifier with respect to the input and output DC voltage levels. The nMOS bias voltage of the biasing transistor should not be too large either, so it is kept in a mid-range in order to secure proper operation of the amplifier when testing the different dies. The power consumption exceeds 1 mA current consumption if the bias current is more than 175 μA.

Two different post-CMOS etch runs were performed. The first run gave better results than the second run and is used here to show measurements from these voltage-to-voltage FFSFR filters. Fig. 5.41 on the next page shows measurements for five different dies in the first run. R1D6 has an offset in its center frequency compared to the other dies. These measurement results were performed in air, which is why the Q-factor is rather low.

A comparison of 4th and 6th order filters for two different dies is shown in Fig. 5.42 on the facing page. The filter bandwidth is extracted from the -3dB points in these measurement results. Table 5.12 on the next page shows the average of the 3-FFSFR for run 1 where only two values have been averaged. The Q-factor is relatively low with a value of ca 4. The center frequency is about 9.68 MHz and is slightly lower than the the theoretical calculated value.

Fig. 5.43 on page 106 shows a logarithmic comparison of the filter order. The dashed dark green line shows the extracted 4th order of the filter while the dashed purple shows the extracted 6th order a filter. It shows that the 2-FFSFR decreases by 40dB per decade and that the 3-FFSFR decreases by 60dB per decade. Due to measurement feedthrough and an out-of-band mode, the lowest detectable signal floor became higher. The measurement sweep did not go beyond 20 MHz due to the instruments that were used.

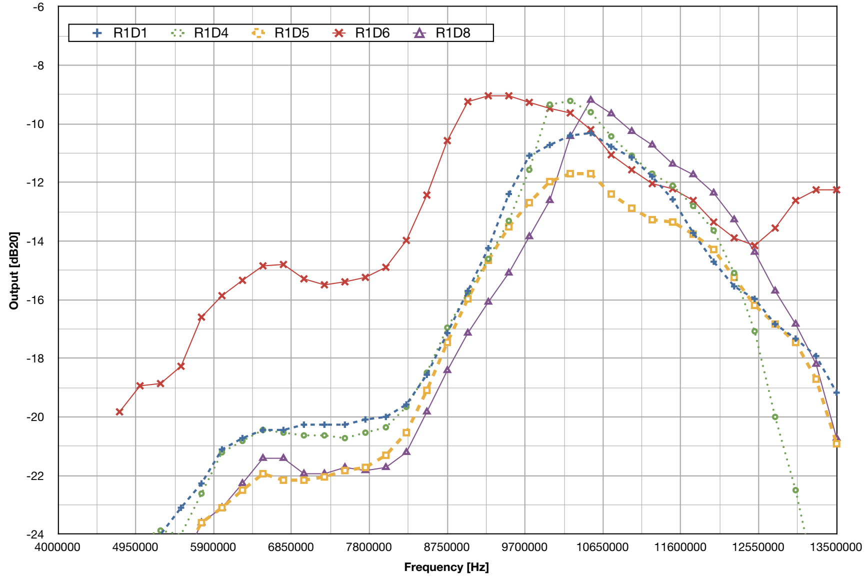
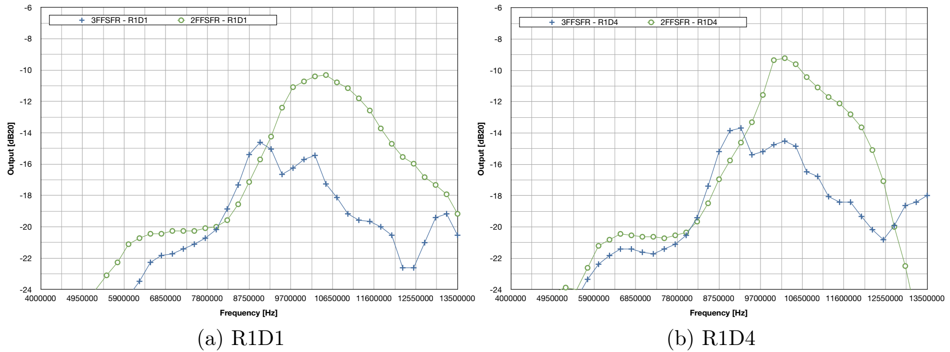


Figure 5.41: TSMC 0.35 μm 2-FFSFR measurements of various dies



(a) R1D1

(b) R1D4

Figure 5.42: TSMC 0.35 μm 2-FFSFR vs 3-FFSFR measurements for two dies

	R1D1	**R1D4**	**Averaging**
f_1 [MHz]	8.5	8.5	8.5
f_2 [MHz]	10.75	11.00	10.88
f_c [MHz]	9.625	9.750	9.688
BW [MHz]	2.250	2.500	2.375
Q	4.278	3.900	4.089

Table 5.12: FFSFR 3-mech, Run 1 average values

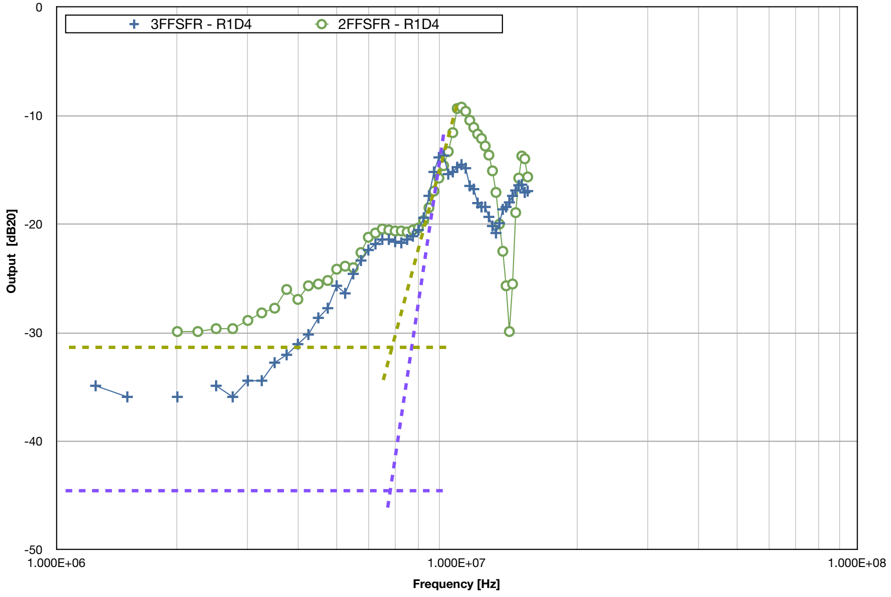


Figure 5.43: 2-FFSFR vs 3-FFSFR measurements to extract filter order

	R1D1	**R1D4**	**R1D5**	**R1D6**	**R1D8**	**Averaging**
f_1 [MHz]	9.25	9.5	9.25	8.75	10.00	9.35
f_2 [MHz]	11.75	11.50	12.00	11.25	11.75	11.65
f_c [MHz]	10.50	10.50	10.63	10.00	10.88	10.50
BW [MHz]	2.50	2.00	2.75	2.50	1.75	2.30
Q	4.200	5.250	3.864	4.00	6.214	4.706

Table 5.13: 2-FFSFR, Run 1 average values

Table 5.13 on the preceding page shows the average values from the 4th order FFSFR filter for run 1. The Q-factor is about 4.7, the bandwidth is about 2.3 MHz and the center frequency is 10.5 MHz which is slightly higher than the theoretical calculated value of f_c.

	2-FFSFR Measurement	**2-FFSFR Analytical**	**3-FFSFR Measurement**	**3-FFSFR Analytical**
f_1 [MHz]	9.350	9.942	8.50	9.95
f_2 [MHz]	11.65	10.014	10.88	10.07
f_c [MHz]	10.50	9.978	9.688	10.01
BW [MHz]	2.30	0.072	2.375	0.12
Q	4.706	139.4	4.089	84.97

Table 5.14: Comparing 2-FFSFR and 3-FFSFR measurements and analytical results

As can be seen in Table 5.14, the measurement results and analytical results are close, except for the lower Q-factor due to measurements performed in air. It can be concluded from the measurement results that the filters were close to the designed specifications. The output voltage from the resonators were from a few mV up tenths of mV. A vacuum chamber is required to perform proper characterization of the resonators which was not available when testing these devices.

The results from these TSMC 0.35 μm mechanically coupled FFSFRs gave the possibility of trying to implement similar structures in a TSMC 90 nm process which is explained in chapter 5.4.2.

5.4.2 TSMC 90 nm SFR filters

The first attempt of implementing MEMS resonators in a 90 nm STM CMOS process was explained in chapter 5.2. Based on the experience from the SFRs in the TSMC 0.35 μm process and the STM 90 nm CMOS-MEMS implementations, higher order SFR filters were made in a TSMC 90 nm process. These resonators are able to resonate at two distinct frequency modes. The material parameters which dictate the resonance frequency of these devices have been extracted from data sheets and other documentations which can not be shown here due to copyright rules. The E/ρ ratio, which dictates the resonance frequency, is given in Table 2.4.

An FFSFR and CCSFR were made in an attempt to compare the two resonator types. The FFSFR is a true Free-Free mode resonator type which may lead to a larger Q-factor depending on the internal material losses. The CCSFR is a Clamped-Clamped type resonator with both ends clamped and has the possibility of using a larger electrode area than the FFSFR. The Parallel-Plate Tuning Fork (PPTF) has a larger electrode length than the CCSFR and FFSFR, however it has only one input and output terminal. The FFSFR and CCSFR, however, have two input terminals and two output terminals. All three composite resonator types are more thoroughly explained in chapter 4.

The layout of the TSMC 90 nm chip is shown in Fig. 5.44, showing six different designs. Three different type of resonators were made as 2nd order resonators. These base models were used to create mechanically coupled (4th order) resonator-filters for comparison reasons.

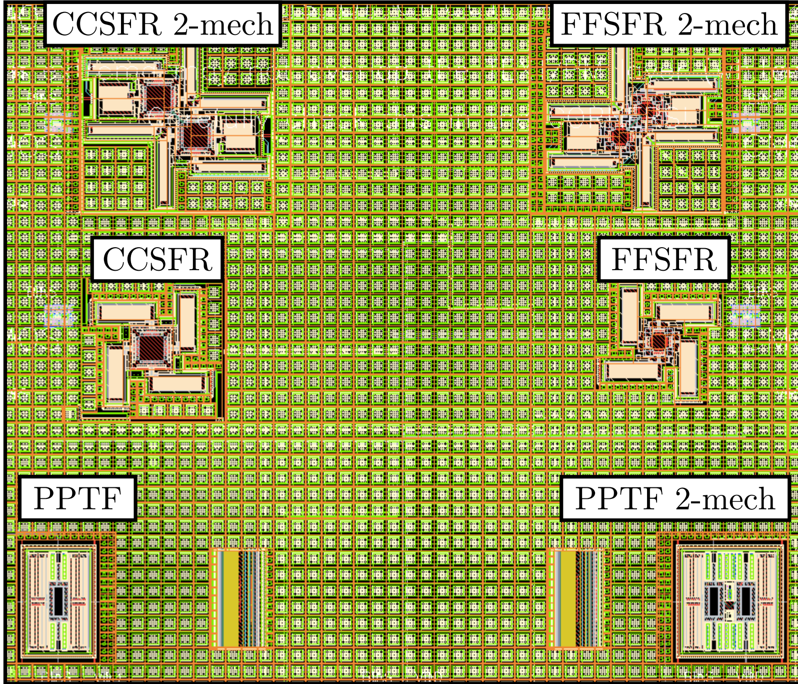


Figure 5.44: Layout of TSMC 90 nm resonator filters

The dimensions for the resonators, tethers and coupling beams for the three resonator types can be seen in Table 5.15. The CCSFR and FFSFR are designed with equal dimensions for direct comparison, the only difference between the two is a larger electrode area for the CCSFR. The PPTF will resonate in two specific modes. For the first mode the equations describing the resonance frequency is based on a soft 60 μm CC-beam with a width of 4 μm and with an extra mass (the squared frame) in the middle. The second mode of the PPTF is a tuning-fork resonance type behavior originating from 50 μm beams with 6 μm width. The two modes of operation for each of these three resonator types are more thoroughly explained in chapter 4.

Fig. 5.45 shows the layout of the FFSFR and SA electrodes. It also shows the internal routing of the V_{LO} (alternatively V_P' for filter operation) signal and the V_P signal. The internal routing of a signal passing through the tether beam is separated using the top metal layer. This causes the resonator to be one mechanically vibrating structure with signals routed to different parts internally in the structure.

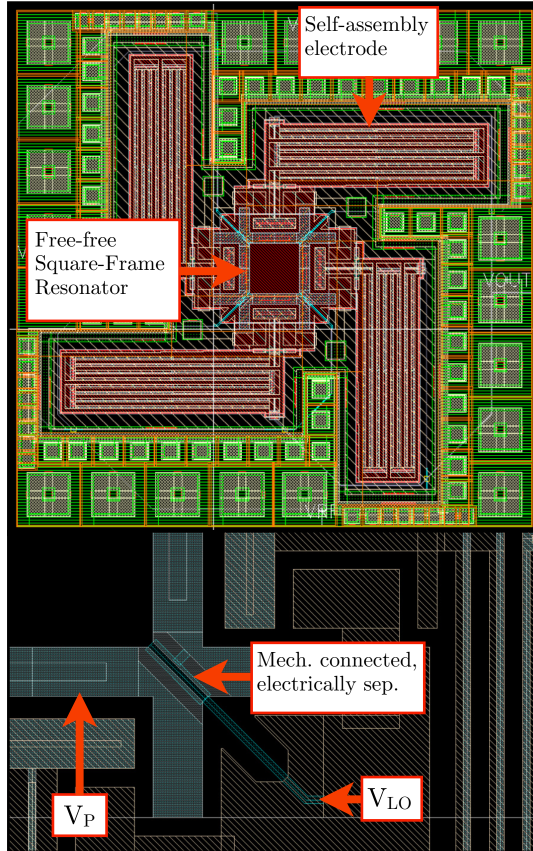
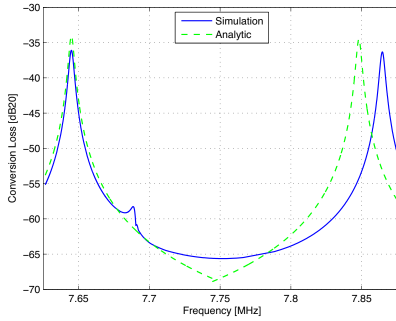


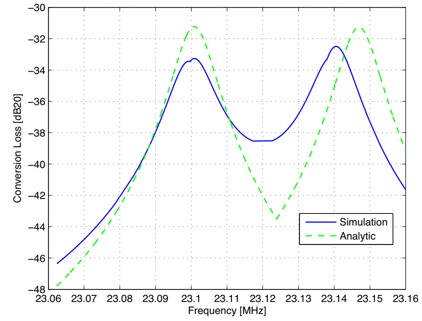
Figure 5.45: Layout of FFSFR with Self-Assembly beams and routing

	FFSFR	CCSFR	PPTF
Resonator length [μm]	47	47	100 and 50
Resonator width [μm]	4	4	6 and 4
Electrode length [μm]	16.5	45	100
Electrode gap [nm]	300	300	200
Tether length [μm]	9.1	9.1	-
Tether width [μm]	0.6	0.6	-
Coupling length [μm]	16.62	16.62	14
Coupling width [μm]	2	2	1

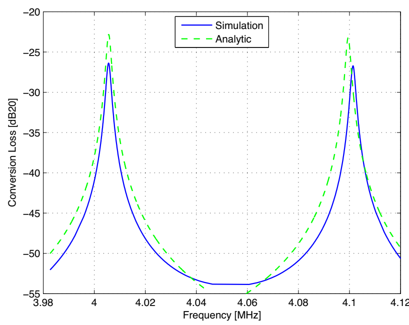
Table 5.15: Implemented TSMC 90 nm resonator and filter dimensions



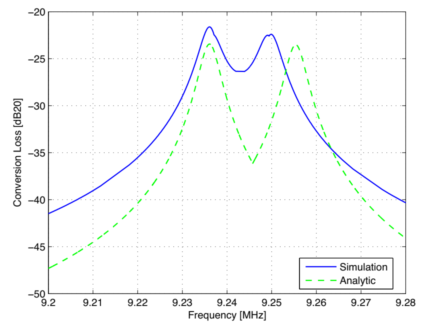
(a) M1 FFSFR



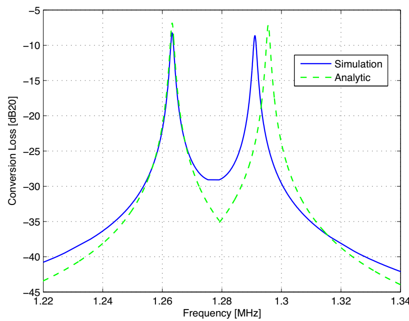
(b) M2 FFSFR



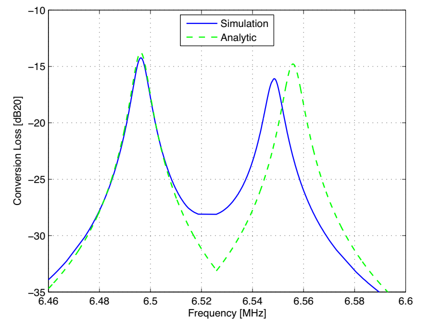
(c) M1 CCSFR



(d) M2 CCSFR



(e) M1 PPTF



(f) M2 PPTF

Figure 5.46: Simulated mode shapes M1 and M2 for the FFSFR, CCSFR and PPTF

Simulation results from the SFRs and PPTF in the TSMC 90 nm process are shown in Fig. 5.46. These simulations include the differential inverter based amplifiers for a voltage-to-voltage conversion. Fig. 5.46(a) and (b) show that the FFSFR operates at around 7.75 MHz at M1 and 23.12 MHz at M2. Fig. 5.46(c) and (d) show that the CCSFR resonates at 4.05 MHz and 9.24 MHz. The bottom two graphs in Fig. 5.46 show that the PPTF filter resonates at 1.27 MHz and 6.52 MHz.

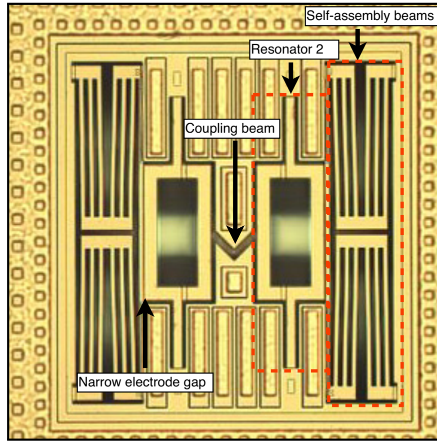


Figure 5.47: 4th order PPTF with SA electrodes

A SEM photo of a 2-mechanically coupled PPTF is shown in Fig. 5.47. It shows the coupling beam as a V-shaped beam between two PPTFs. The SA electrodes consist of double jointed SA beams to create a large electrode area.

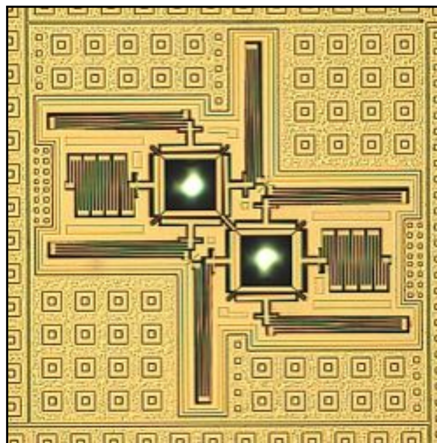


Figure 5.48: 4th order CCSFR with SA electrodes

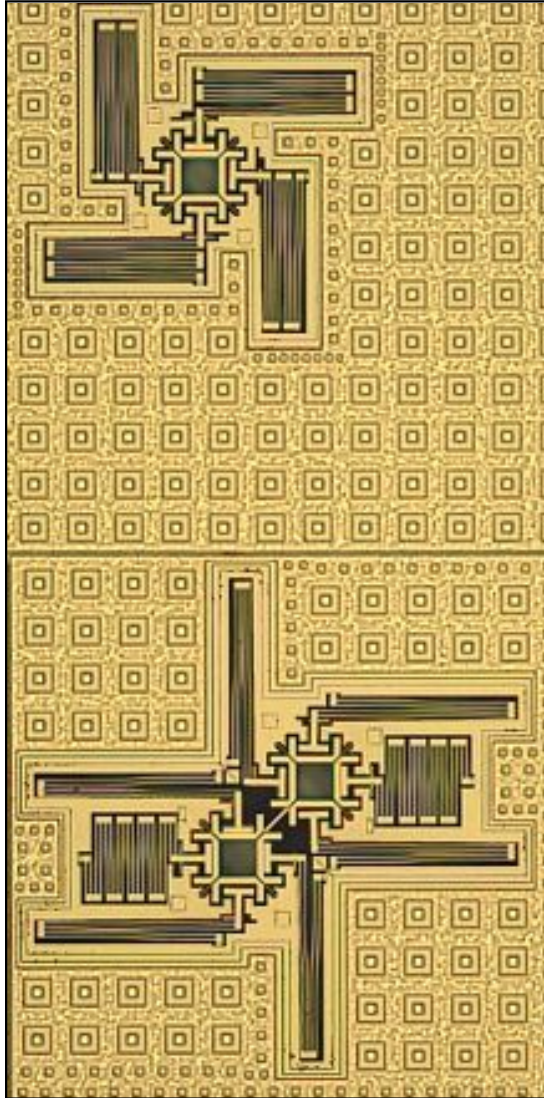


Figure 5.49: 2nd and 4th order FFSFRs with SA electrodes

	PPTF M1	**PPTF M2**	**FFSFR M1**	**FFSFR M2**	**CCSFR M1**	**CCSFR M2**
f_0 [MHz]	1.267	6.578	7.662	23.02	3.982	9.238
m_{eff} [pkg]	16.6	4.89	2.88	4.471	5.83	4.417
k [N/m]	993	8357	6684	93540	3654	14884
η_{in} [nN/V]	42.2	50.63	2.45	2.45	6.68	6.68
η_{out} [nN/V]	422	506.3	49.1	49.1	133.7	133.7
R_z [MΩ]	7	7.88	290	194.1	11	14.09
CL [dB]	3.09	2.06	-29.33	-25.76	-0.89	-2.97
f_c [MHz]	1.277	6.522	7.754	23.12	4.052	9.243
BW [kHz]	29.07	58.7	222.3	52.84	95.92	19.35
Q_{filter}	43.93	111.1	34.89	437.5	42.25	477.5
R_{Qi} [MΩ]	185.1	130.5	3001	109.8	804.9	27.4

Table 5.16: TSMC 90 nm filter results

Fig. 5.48 and 5.49 show the photos of the CCSFRs and FFSFRs. Table 5.16 shows the most important results from the three base resonators. The transimpedance gain from the amplifier is 11.84 MΩ and the bandwidth is 38.11 MHz which was shown in Table 5.10. It can be seen from Table 5.16 that a low R_z does not necessarily result in a low R_{Qi}. Instead, R_{Qi} can be tuned to a more appropriate value depending on the required Insertion Loss (IL) and the filter bandwidth.

The CCSFR has a much lower R_z than the FFSFR due to the larger electrostatic area as well as larger Q_{filter} values. The PPTF has better electrostatic coupling (η_{in} and η_{out}), resulting in a better Conversion Loss (CL) and R_{Qi}, compared to the FFSFR and CCSFR. The resonator spring stiffness, Q_{filter}, and low R_z of the CCSFR mean that this resonator type can be used as an example of improving resonator performance which will be shown in chapter 6.

5.5 Summary of results

This chapter has described implemented CMOS-MEMS resonators used as an oscillator, a filter or a mixer-filter. Implementations were done in 0.35 μm and 90 nm CMOS technologies. A method of co-simulating CMOS and MEMS was discussed by using NODAS with Verilog-A code in CMOS design software to model the micromechanical devices. Most simulations in this thesis have been done as a co-simulation of MEMS and the CMOS together, based on analytical results and CoventorWare FEM simulations.

The MEMS VCO and FDSM design was made in STM 90 nm CMOS as an initial test of implementing MEMS in a newer CMOS process. This meant going from coarse-grain (0.35 μm) CMOS processes with aluminum metal layers to copper composite metal layers. Additionally, the newer processes have dielectric layers with a higher k-factor in order to reduce transistor current leakage. Since the

metal layer and the dielectric are different for newer CMOS processes, the etching procedure is slightly changed. The main advantages for making MEMS in a newer CMOS process is obtaining a larger Young's Modulus, less deposition of polymer residuals on the sidewalls, lower power consumption and reduced parasitics. The STM 90 nm MEMS VCO designs showed this feasibility of making MEMS in fine-pitch CMOS. Special designed bonding pads were made, and the CMOS circuitry was tested before and after etching of the MEMS. However, using post-CMOS resonators as oscillators turns out to be a challenge due to the large R_z value. More research needs to be performed on how to reduce phase noise and R_z in this technology.

Various amplifier types were investigated throughout this thesis. An analytic versus simulated noise analysis was performed on a CG-CS-CS-SF four-stage single transistor amplifier topology. This showed that the first amplifying stages (or transistors) are the most crucial parts which will contribute mostly with thermal noise. A large g_m results in a larger amplification (i.e. for a CS amplifier), although that will also increase thermal noise. The feedback element has been primarily implemented as a resistor in this thesis which will directly add noise to the system. Brownian noise from the micromechanical resonators are much smaller than the noise from the transistors and resistors and is not included in the analysis. An analysis of various amplifiers in 90 nm CMOS was performed, showing that a full differential folded cascode resulted in the lowest noise contribution and the largest gain. Due to difficulties of proper biasing of the folded cascode amplifier and limited time, an inverter based amplifier type was chosen instead.

Implementations of Square-Frame resonators were performed in both 0.35 μm and 90 nm CMOS processes from TSMC. In the TSMC 0.35 μm process, FFSFR resonators and mechanically coupled resonators were made. These resonators showed adequate results when operated in air with results close to analytical calculations and simulations. Based on the experience from the previous runs, FFSFR, CCSFRs and PPTFs were made in a newer TSMC 90 nm process. These three base resonator structures are able to resonate at two distinct mode frequencies. The resonators were also implemented as 4th order mechanically coupled filters.

The main outcome of these implementations is that it shows the feasibility of making more advanced resonator architectures with increased performance as well as the possibility of making these micromechanical resonators in more modern CMOS processes. Using the resonator as a filter or mixer-filter shows a great potential for front-end transceiver signal processing. For the filter designs, a focus has been put on achieving a low R_z and R_{Qi}. However, Insertion Loss and linearity are important performance parameters as well. High-level resonator performance parameters will be shown and discussed in the next chapter, and the most promising SFR from the TSMC 90 nm run is used as an example to show possible improvements of the performance.

Chapter 6

High-level tradeoff parameters

There are several types of parameters which show the performance of MEMS resonators as a filtering device. These performance parameters can be divided into three levels as shown in Table 6.1 - Low, medium and high-level:

Parameter level	**Parameters**
High-level	IIP3, R_{Qi}, IL, ZL, N_{oi}, SFDR
Medium-level	R_z, Z_{TIA}, SNR, CL, k_c, BW, Q_{filter}, C_{feed}
Low-level	f_{IF}, β_N, A_e, ε_r, g, k

Table 6.1: Overview of system parameters in a hierarchical view

The low-level parameters can enhance resonator performance by increasing the electrode area and by reducing the gap between the electrodes and the resonator. The spring stiffness k will also dictate performance for some of the higher level parameters. It is possible to enhance the electrostatic coupling by modifying the relative permittivity, ε_r, typically done by adding a material between the resonator and the electrodes [61]. The medium-level performance parameters are typically the motional impedance R_z of the resonator, the transimpedance gain Z_{TIA}, the signal-to-noise ratio SNR and the conversion loss CL. Another important factor which dictates medium-level performance for higher-order filters is the coupling stiffness k_c which in turn will decide the bandwidth and filter Q-factor. Finally, any capacitive feedthrough between the input and output of the device will also affect the performance.

The high-level parameters in Table 6.1 are typical filter parameters which can be understood even without the knowledge about MEMS filters. By looking in and out of the "black box" or viewing the resonator as a two-port device it is clear that impedance levels, linearity, insertion loss and noise are important parameters to take into consideration.

f_{IF}	BW	FL	IIP3	R_{Qi}
10 MHz	20 kHz	12 dB	9.5 dBm	$<$10 kΩ

Table 6.2: Typical specification list for a sub-GHz front-end mixer-filter

Table 6.2 is a typical specification list for a filter or mixer-filter with a frequency of 10 MHz and BW of 20 kHz [62]. The filter loss (FL) is defined as $\sqrt{P_{in}/P_{out}}$. Any filter is susceptible for out-of-band interference by the third-order input interception point (IIP3) product. The IIP3 is the first odd order frequency component of the filtering frequency which interferes with and distorts the desired band. It is desirable to have a large IIP3 product as possible in order to achieve better linearity of the filter. A final parameter for filter design is the termination resistor(s), R_{Qi}. For best power transfer, an ideal termination resistor should be as low as possible. As will be explained later, the R_{Qi} must be larger than R_z by having a certain filter bandwidth and filter frequency.

There are other important high-level parameters which are important which will be discussed in this chapter and evaluated and compared with other research results in the same research area. These parameters are: Insertion Loss (IL), Input referred noise (N_{oi}), Spurious Free Dynamic Range (SFDR) and the termination impedance to linearity product (ZL). Low to high level parameters all affect each other. If one parameter is improved, another parameter could become worse – a compromise will be needed for some of these performance parameters.

6.1 Discussing the trade-off parameters

When designing MEMS resonator filters, termination resistors, R_{Qi}, are required to flatten the passband. Insertion Loss is a parameter which indicates the impedance mismatch between a termination resistor R_{Qi} and the actual impedance R_z, representing the filter. Summing R_{Qi} and R_z gives the total impedance of the filter which should be as low as possible. Eq. 6.1 defines the Insertion Loss (IL) of the filter:

$$IL = 20log_{10}\left(\frac{R_{Qi} + R_z}{R_{Qi}}\right) \tag{6.1}$$

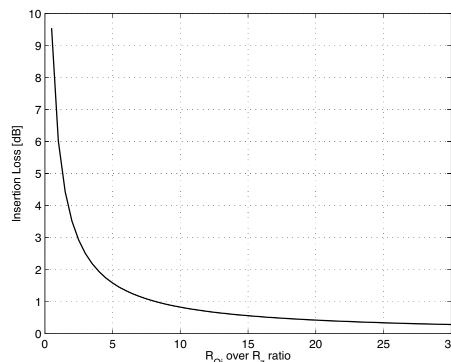


Figure 6.1: Insertion Loss as a function of R_{Qi}/R_z

From Fig. 6.1 it is clear that R_{Qi} must be approximately 8 times larger than R_z in order to achieve an IL of less than 1 dB. R_{Qi} is related to R_z and the filter specifications: $R_{Qi} = (R_z/2n)[(Q/q_i Q_{filter}) - 1]$. Achieving an R_{Qi} that is 8 times larger than R_z is achieved by designing the filter to have a certain bandwidth and center frequency. This relationship is shown in eq. 6.2:

$$IL = 20log_{10}\left(1 + \frac{2nf_c q_i}{QBW}\right) \tag{6.2}$$

Eq. 6.2 is the same as eq. 6.1 by replacing R_{Qi} and R_z. From this relationship it is evident that the filter must be carefully designed in order to achieve an insertion loss of less than 1 dB. The number of electrodes (n), the filter center frequency f_c, the resonator Q-factor and the filter bandwidth are all parameters which decide the IL. The next high-level performance parameter to be discussed is the IIP3 product which depends on some lower-level performance parameters. Fig. 6.2 illustrates the relationship between the signal and the IIP3.

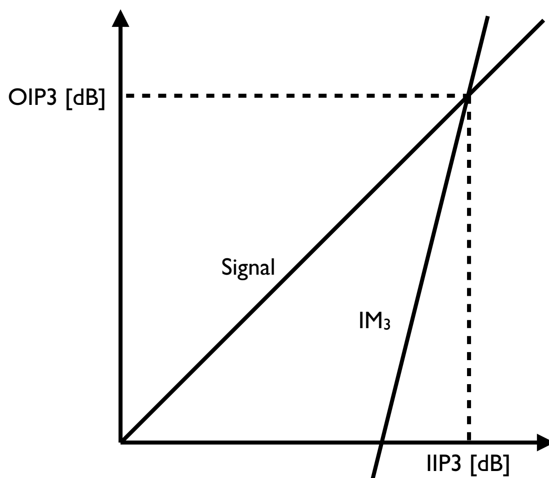


Figure 6.2: Output power as a function of input power, showing IIP3

The desired output signal through the filter is a 1:1 ratio (in terms of power). Both the desired signal and the third order intermodulation signal (IM3) are a function of the input power. At a certain point, the IM3 crosses the real signal as shown in Fig. 6.2. This crossing point is known as the third-order input interception point (IIP3). It can be shown that the IIP3 for MEMS filters can be described as the following equation[1]:

$$V_{IIP3} = 0.577\sqrt{\frac{g^6 k^3}{3C^3 Q^3 V_P^4}} \tag{6.3}$$

[1]For development of the IIP3, see the appendix

The IIP3 in eq. 6.3 shows that a better linearity is achieved by tuning low-level resonator performance parameters. From a perspective of increasing the IIP3 only, it is clear that a large gap and spring stiffness or a low Q-factor, polarization voltage and static capacitance ($C = \varepsilon A_e/g$) will increase the IIP3. This shows us that when designing a filter for low R_{Qi}, R_z and IL it will come for the cost of a decreased IIP3. This is where an important compromise must be made when making filters. A new high level performance parameter is therefore established: Impedance-to-linearity (ZL). This is done by defining ZL as the termination resistance divided by the IIP3:

$$ZL = \frac{R_{Qi}}{IIP3} = \frac{BW}{\omega_0^2 q_i}\sqrt{\frac{3Q^3}{k\varepsilon_0 A_e g}} \tag{6.4}$$

By performing some algebra, dividing R_{Qi} by IIP3 results in eq. 6.4. The ZL should be as low as possible. This ZL parameter will simplify the filter design methodology, allowing the designer to see the compromise which must be made. For the purpose of this analysis and the fact that an intermediate IF filtering frequency has been set, ω_0, q_i and ε_0 are fixed. As can be seen in eq. 6.4 it turns out that ZL will decrease for a low Q-factor or a large gap. This clearly shows that any filter design is susceptible for non-linearities from large Q-factors or small gaps. It turns out from eq. 6.4 that a low filter bandwidth and large spring stiffness or electrode area will contribute to reducing the ZL.

Another high-level performance parameter to evaluate is the total input referred noise, N_{oi} [39]. The N_{oi} is given by

$$N_{oi} = N_{RQi} + IL + 10log_{10}(BW) \tag{6.5}$$

where N_{RQi} is the noise delivered by R_{Qi} to the matched load. It can be seen from eq. 6.5 that the total noise depends on how large R_{Qi}, the Insertion Loss and the bandwidth of the filter are. Keeping all these three factors low will result in a low input referred noise.

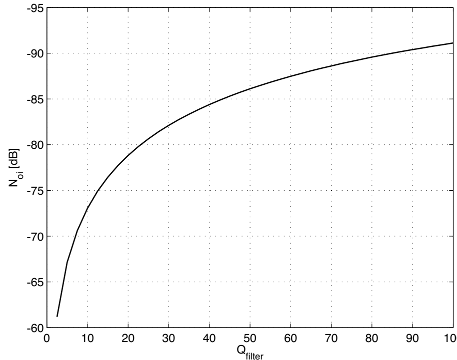


Figure 6.3: N_{oi} as a function of Q_{filter}

Fig. 6.3 shows that the N_{oi} becomes saturated for a large filter Q-factor. However, the filter Q-factor must be 1/10 or 1/20 of the resonator Q-factor and not more. In this case, for a resonator Q-factor of 2000, the Q_{filter} should not exceed 100 for optimal filter design. The last high-level performance parameter to consider is the Spurious Free Dynamic Range (SFDR) parameter [39]. This parameter depends on the IIP3, the input referred noise power (N_{oi}) and the specified minimum signal-to-noise ratio (SNR_{min}) shown in eq. 6.6:

$$SFDR = \frac{2}{3}\,(IIP3 - N_{oi}) - SNR_{min} \tag{6.6}$$

By keeping IIP3 as large as possible, the N_{oi} subtraction from the IIP3 will be larger and the SFDR will be kept on an acceptable level. As can be seen in eq. 6.3, the IIP3 is not related to the filter specifications (BW, Q_{filter}, k_c), while the IL will change with those parameters. A plot of the SFDR as a function of IL is shown in Fig. 6.4:

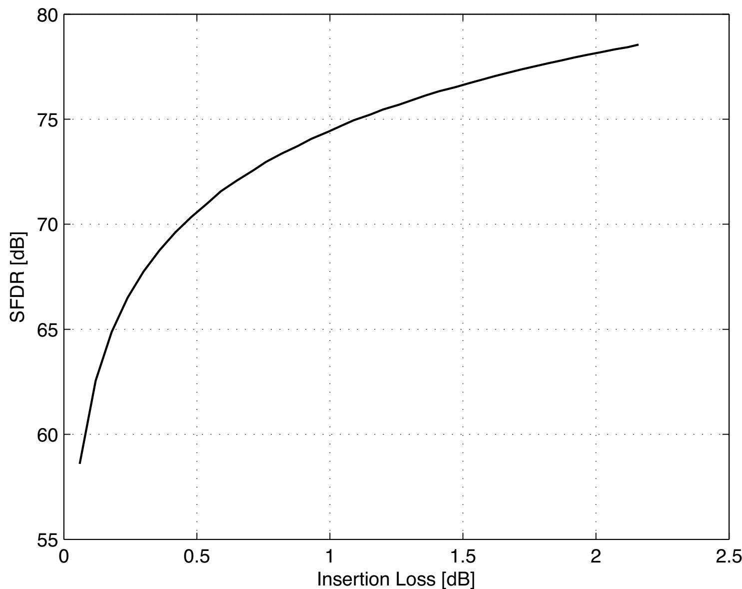


Figure 6.4: SFDR as a function of Insertion Loss

It is evident from Fig. 6.4 that low Insertion Loss, less than 1 dB, will greatly impact the SFDR. A compromise between the IL and the SFDR must be made, and aiming for a filter design of an IL between 0.5 dB and 1 dB is an example of making that compromise. All these high-level parameters are important when designing filters and portraits a complex picture when designing filters. The equations in this section will be used in section 6.3, where I will come with practical examples of what can be done to improve filter design.

6.2 Comparison of research results

When doing research on MEMS resonator filters, it is typical to focus on certain medium or low-level parameters. Many research papers do not mention or discuss the high-level parameters that were presented in Table 6.1. This makes it difficult to compare research results from one paper to another. This section intends to collect some high-level parameters from various research results and compare them with results from this thesis.

Low level	CCSFR	[40]	[34]	[39]	[39]'	[63]
f_0 [MHz]	3.98	10	1.05	8.76	70	72
k [kN/m]	3.65	8230	22	1.89	64.2	70.7
A_e [μm^2]	137	100	35	160	121	540
g [nm]	300	800	800	95	20.3	100
V_P [V]	10	10	10	15	6	35
C_{oi} [fF]	4.04	1.11	0.38	14.9	52.8	47.8
R_z [Ω]	12.1M	195M	1.79G	3.17k	186	478
High level						
R_{Qi} [Ω]	98.2M	219M	9.52G	15.3k	2.82k	12.8k
R_{Qi}/R_z	8.12	1.12	53.1	3.15	10.8	18.8
IL [dB]	1.01	5.54	0.16	2.39	0.77	0.45
IIP3 [dBm]	41.71	54.48	32.42	0.40	6.05	0.71
N_{oi} [dB]	-84.92	-89.68	-55.64	-126.19	-127.31	-119.53
SFDR [dB]	74.42	86.11	85.76	77.53	82.87	69.21
ZL [dB]	63.72	66.04	94.68	45.85	26.68	42.54

Table 6.3: Comparing the specification list with other results

Table 6.3 presents the CCSFR that is described in chapter 5.3. The third and fourth column [40, 34] are CMOS-MEMS based research papers while column five through seven [39, 63] are based on more state-of-the-art MEMS processes. The frequency varies from 1 MHz to 72 MHz and the processing technologies are different, so Table 6.3 is not a concise comparison. It should be mentioned that the 70 MHz filter ([39]') is based on a theoretical assumption of tweaking the process, enabling a very small gap and designing for a larger spring stiffness.

The post-CMOS implemented filters of reference [40, 34] has a rather large R_z and R_{Qi} because of large resonator-to-electrode gaps. This results in a good linearity (large IIP3) and a decent IL. The 8.76 MHz and 70 MHz filter designs of ref. [39] shows low R_z and R_{Qi} and a good IL. However, due to a very narrow resonator-to-electrode gap, the IIP3 becomes rather small. The 72 MHz resonator of ref. [63] has a large spring stiffness and multiple electrodes for electrical summing as well as a low gap of 100 nm, leading to a low R_z, R_{Qi} and IL. However, the IIP3 product is relatively small because of the large V_P. The common denominator for linearity is clearly seen; a small gap and a large V_P will lead to decreased linearity.

The last three columns [39, 63] are based on custom MEMS processes which may be possible to integrate directly with CMOS although that is not addressed in the papers. Therefore it is clear that even the state of the art papers do not completely satisfy the typical filter specifications. The CCSFR resonator in this

thesis and reference [40] and [34] are not as good as the state of the art MEMS resonators, although they show adequate results. It should be mentioned that other research results could have been included, however those papers have a focus on different figures of merit. Research results of CMOS-MEMS integrated resonators from [11, 12] shows promising results within this research field. By using some of the results given in those publications it is possible to analytically calculate R_z, R_{qi}, IL and $IIP3$. Publication [11] results in R_z in the kΩ area with a low insertion loss and at the same time using low V_{LO} and V_P voltages. However, as shown earlier, these results comes at the cost of the linearity. The remaining part of this chapter intends to take the results of the CCSFR even further and come with suggestions for improvements with a special focus on linearity.

6.3 Suggestions for improved filter design

There are two main methods of connecting MEMS resonators together, either electrically (summing currents) or mechanically (adding modes). Fig. 6.5 shows laterally moving square resonators with and without coupling beams. The method of electrical summation (Σ_{el}) is based on stimulating identical resonators with the same signal so that the output consists of filtered currents which can be summed together in a common electrical node as shown in the left part of Fig. 6.5. Coupling the MEMS resonators mechanically (Σ_{mech}) has already been explained and shown in this thesis and can be seen in the middle part of Fig. 6.5. Performing the mechanical coupling of resonators requires differential input and output for these square-framed resonators.

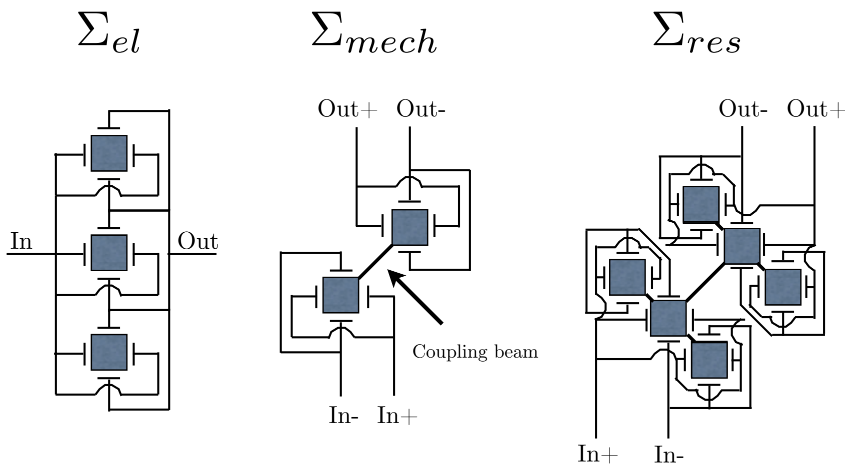


Figure 6.5: Three methods for micromechanical signal processing

Combining these two coupling methods leads to a hybrid electrical-mechanical coupling method (Σ_{res}) seen in the right part of Fig. 6.5. The input resonators

have shared terminals for differential input stimulus and are connected through very small coupling beams (or stubs). These stubs do not (ideally) add any mass to the total transfer function of the filter. A specific resonator (the middle one) is used to couple to an identical output resonator array, thus increasing the order of the filter. By doing this, it is possible to both electrically sum filtered currents, add higher order of the filter and to boost the total mechanical spring stiffness [64, 65, 66].

Summing the resonators both electrically and mechanically will add additional electrodes A_e per extra resonator. A multiplication factor M is used to define the number of arrayed resonators. Stimulating the outer resonators with the opposite phase of the middle resonator will ensure that the first array will act as one resonator with summed electrodes $(M \cdot A_e)$. Due to this type of stimulation, the resonators will together act as one resonating element with more electrodes and a larger total spring stiffness. The increased electrode area leads to a reduced R_z

$$R_z = \frac{k}{M\omega_0 Q\eta^2} \tag{6.7}$$

where the combination of η and k contributes to scaling down R_z by a factor of M. This means that R_{Qi} is reduced by the same amount shown in eq. 6.8:

$$R_{Qi} = \frac{k}{2nM\omega_0 Q\eta^2}\left(\frac{Q}{q_i Q_{filter}} - 1\right) \tag{6.8}$$

Equations 6.7 and 6.8 show that both R_z and R_{Qi} scale down with M. As can be seen in eq. 6.1, if both R_{Qi} and R_z are reduced by the same factor M, then the IL will remain constant. This means that IL can not be improved through this technique. The same goes for the IIP3:

$$V_{IIP3} = 0.57\sqrt{\frac{g^6 M^3 k^3}{3M^3 C^3 Q^3 V_P^4}} \tag{6.9}$$

In eq. 6.9, the k is replaced by $M \cdot k$ and the C is replaced by $M \cdot C$ (where M comes from $C = (MA_e)/g$). As can be seen in eq. 6.9, the M's will cancel each other, meaning that the IIP3 will not change. Instead this technique shows that the impedance-to-linearity product ZL becomes reduced:

$$ZL = \frac{BW}{M\omega_0^2 q_i}\sqrt{\frac{3Q^3}{k\varepsilon_0 A_e g}} \tag{6.10}$$

Eq. 6.10 shows that ZL will be improved because IIP3 does not change while R_{Qi} becomes reduced. This means that this technique can be used to reduce R_{Qi} (and R_z) while maintaining the same linearity. For example, an array of 10 resonators will decrease both R_{Qi} and R_z by 10 while maintaining the same IIP3. A systematic approach for designing for high-level parameters for IF CMOS-MEMS filters is shown in Fig. 6.6.

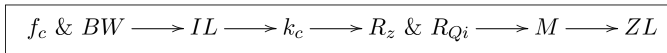


Figure 6.6: CMOS-MEMS filter design flow chart

The design flow in Fig. 6.6 does not take into account resonator architecture, how large A_e can be or how small the gap can be. First the filtering frequency and bandwidth are chosen. This will in turn decide the IL to aim for. Designing the mechanical coupling beam will therefore control both the bandwidth, filter Q-factor and set the compromise for achievable IL. The IIP3 is not affected by this and can only be increased by k or M. The k_c will decide the bandwidth which then sets the R_{Qi}/R_z ratio. The final step is then to decide how many resonators to array together to reduce R_{Qi} and R_z at the same time, thus reducing the ZL. Two key parameters become apparent here: Design the square-frame resonators with as large k as possible without compromising on the electrode area A_e and couple them in an array. An example of improved CCSFR filter performance is shown in Table 6.4:

Low-to-medium level	Regular CCSFR	Improve tech.	Tech. & Σ_{res}
k [kN/m]	3.65	3.65	32.9
A_e [μm^2]	137	225	2003
g [nm]	300	150	150
V_{LO} [V]	1	5	5
V_P [V]	10	10	10
C_{oi} [fF]	4	10	100
R_z [Ω]	12.1M	55.9k	6.21k
High level			
R_{Qi} [Ω]	98.2M	454k	50.4k
R_{Qi}/R_z	8.12	8.12	8.12
IL [dB]	1.01	1.01	1.01
IIP3 [dBm]	41.71	17.93	17.93
N_{oi} [dB]	-84.92	-108.27	-117.81
SFDR [dB]	74.42	74.13	80.50
ZL [dB]	63.72	44.03	34.49

Table 6.4: Suggestion for improved CMOS-MEMS filter design

The middle column is based on a theoretical assumption of tweaking the CMOS-MEMS process and utilizing a CMOS technology with a larger structural stack thickness. The technology part of Table 6.4 is based on a 5 μm thick stack and a 150 nm gap, which could be achievable by tuning the process. By including a stack of silicon from the CMOS it could be possible to achieve a thickness of 10–20 μm [67, 68, 16], however this is not considered in this example. A 5 μm thick stack increases the A_e from 137 μm^2 to 225 μm^2. The static input capacitance C_{oi} increases from 4 fF to 10 fF. The V_{LO} was kept at 1 V for the LO to be able to keep a sub-GHz stable frequency, however with a charge pump it could be possible to get this value larger in order to enhance resonator performance. The V_P is kept at 10 V for all cases.

The right column in Table 6.4 is based on both tweaking the CMOS-MEMS process and utilizing mechanical & electrical summation of signals, known as Σ_{res}. The combination of both tweaking the process and Σ_{res} show that a composite filter array of 9 resonators enhances the spring stiffness from 3.65 kN/m to 32.9 kN/m and increasing the area to 2003 μm^2. This reduces the R_z from 55.9 kΩ to 6.21 kΩ and R_{Qi} from 454 kΩ to 50.4 kΩ which is a much more acceptable level of impedances. The IL and IIP3 remain constant. The input referred noise is improved, leading to an increased SFDR. Finally the ZL parameter is reduced to a level better than other research results, showing the feasibility of reducing R_{Qi} while retaining the linearity of the filter.

This discussion chapter has described some high-level parameters which are important to consider and come with suggestion for improved design. The far right column in Table 6.4 is now comparable with other research results that were presented in Table 6.3, showing the feasibility of making CMOS-MEMS implemented filters with a performance which could be good enough.

Chapter 7

Conclusion

7.1 Thesis summary and conclusions

The main focus of this thesis has been how to use the micromechanical resonator as a signal processing element. Another focus area has been how to combine CMOS and MEMS by choosing one of several possible methods as a platform for these resonators. A survey of the various methods showed that 3D-integration, SOI and post-CMOS are the most popular methods. This work has implemented MEMS resonators by using a simple post-CMOS process. The top metal layer of the CMOS process is used to define the MEMS structures and acts as a mask for free etching. The structures are released through a few mask-less etch steps. A CMOS-MEMS implemented resonator will typically have a small thickness because the bottom metal layers up to the top metal layer from the CMOS process will define roughly 3–5 μm thick structures. Another challenge was to be able to etch and release the narrow gaps required to achieve good electrostatic actuation. The simplicity, compatibility with CMOS foundries and the possibility of implementing resonators as filters, mixer-filters or VCOs in combination with on-chip circuitry has made this method quite attractive.

This thesis has not focused on developing the process itself by enhancing the thickness, varying structural material parameters or achieving narrow gaps. It has instead utilized a "standardized" CMOS-MEMS method (ASIMPS). Collaboration with CMU has made it possible to implement CMOS-MEMS designs in 0.35 μm, 0.25 μm and 90 nm processes from ST Microelectronics and TSMC. Coarse-grain CMOS (0.25 and 0.35 μm) and fine-pitch CMOS (90nm) have been compared to see the pros and cons from each process type. The coarse-grain CMOS processes are cheaper to produce and the metal layers typically consist of aluminum. The fine-pitch CMOS processes offer more metal layers for routing, an increased E/ρ ratio (due to a copper composite material), lower transistor voltages and lower power consumption. Implementations show that the layout design rules for old CMOS processes make it more easy to implement MEMS resonators in these processes compared to implementations in fine-pitch CMOS. However, it is possible to make scripts and parametric cells which will make layout much easier by fulfilling the

metal density “filling” constraints. Layout of parametric cells has been done in this thesis for the “electrically summed resonators” project at CMU. In short, the advantages outweigh the disadvantages when implementing MEMS in fine-pitch CMOS due to the low power consumption, the low parasitic capacitances and that it is more in line with newer CMOS signal processing.

The investigation of the resonator as a signal processing element shows its filtering capabilities through a Q-factor which is larger than on-chip CMOS inductors. The various resonators have been modeled analytically and simulated with the FEM tool CoventorWare to find resonator performance parameters such as the motional impedance and the electromechanical coupling coefficient. It is possible to configure vibrating beams in five principal ways depending on the mode and the anchoring method: Clamped-Free (cantilever), Clamped-Clamped, Free-Free, Pinned-Pinned and Clamped-Pinned. The modes and behavior of these configurations have been investigated. The combination of these beam configurations makes it possible to implement more advanced, composite types of resonators such as the CCSFR, FFSFR and PPTF. Simulation results show that the vibrational modes for these composite resonators are close to analytical calculations.

The FFSFR and CCSFR are square-shaped resonators which are symmetric and are operated differentially. The FFSFR, CCSFR and PPTF have been interconnected by $\lambda/4$ long beams to make higher order filters. FEM simulations are close to analytical calculations for the mechanically coupled resonators. A 6th order filter design has been demonstrated in a 0.35 μm TSMC process. SFRs and PPTFs have been implemented, simulated and measured in 0.35 μm and 90 nm technologies from TSMC.

A part of this thesis was to investigate different methods of converting the resonator motional current to a voltage through the usage of on-chip CMOS amplifiers. At the same time this demonstrates integration of electronics and MEMS. The transimpedance conversion from current to voltage can be done with a feedback element between the input and output of the amplifier. The feedback element can either be a resistor, a capacitor or a transistor. It is obvious from simulations and analytical calculations that a resistor will lead to a larger noise contribution, but on the contrary it is much easier to set node voltages using a resistor. A capacitor or transistor in feedback makes it more difficult to set the node voltages. A capacitor or a transistor in feedback could potentially give a much larger transimpedance gain. However, defining a very small capacitance value is difficult. A capacitor of 1 fF is about the lowest controllable capacitance level offered by the foundry. Amplifier designs have been made according to a single-stage, cascode differential and inverter based procedure.

Modeling and simulation show that the noise levels of a combined MEMS resonator and CMOS amplifier are important to take into consideration. By integrating all noise contributions to the input referred noise current, it is possible to find the total noise for the bandwidth of a filter. Examples of noise simulations resulted in 70 dB SNR for SFRs implemented in TSMC 0.35 μm technology. An investigation of the tuneability of soft cantilever beams and PPTF resonators in

90nm CMOS have been performed. The resonator and a common-source amplifier are put in a feedback loop, and the frequency can be tuned by varying the V_P voltage. Simulations and measurements of a VCO-FDSM system in a STM 90 nm CMOS process show the feasibility of using MEMS directly with analog and digital systems, with a special focus on low voltage operation of the MEMS resonators. However, it turns out that the Q-factor and the phase-noise of the system are not good enough for the intended operation. This indicates that CMOS-MEMS implemented oscillators or VCOs should be fabricated in a manner which would increase the Q-factor and reduce the electrostatic electrode gaps in order to achieve adequate resonator performance.

Comparison of results from this thesis and other research results show that the CMOS-MEMS implemented filter designs in this thesis are currently not good enough to be used as real signal processing elements. Certain high-level parameters show compromises which must be made. A target goal for an IF filter or mixer-filter between 1 and 10 MHz is an IL between 0.5 dB and 1 dB. Equations for linearity and termination resistance show that it is possible to achieve a compromise between IL, SFDR and the impedance-to-linearity product (ZL). The motional impedance of the resonator and the termination resistor for the filter must be reduced while maintaining sufficient linearity (IIP3). The idea of a combination of electrically and mechanically summed resonators shows that the current research work in this thesis becomes "good enough" for the given system requirements or adequate compared to state-of-the-art MEMS resonator research.

7.2 Further work

There is currently still a lot of research to be performed in the field of integrating CMOS and MEMS and research on techniques of how to enhance resonator signal processing capabilities. Implementing MEMS directly in CMOS is a niche market due to several reasons. The electrostatic coupling of these resonators is limited due to the stack thickness. Research is being done on how to include silicon beneath to increase the structural thickness which would help increasing the total electrostatic electrode area [67, 68, 16]. Creating small gaps is possible by using self-assembly beams. However, too small gaps should be avoided because it drastically reduces the IIP3. Non-linear behavior for MEMS resonators still needs to be investigated and is a popular research topic [41, 42, 43].

Summing resonators electrically can prove to be a challenge, but is definitely an interesting research topic [69]. One challenge arises from the process variations of the CMOS or MEMS processing which will result in a large standard deviation of the resonance frequency. A part of the work in this thesis showed the feasibility of summing large arrays of MEMS resonators, selecting the resonators that are within the desired filter bandwidth. Having an array of many resonators and statistically adding them to a desired frequency of operation requires a large chip area. An evaluation of how large area is required must be done, but preliminary results show that the electrically summation method is feasible.

Sub-GHz MEMS resonators can be feasible to implement using post-CMOS. With an increased stack thickness including silicon, a large spring stiffness, a low mass and an array of resonators might prove to give adequate results for signal processing. Further research on this field needs to focus on improving the post-CMOS process to achieve a larger electrostatic area, and using a combination of electrically and mechanically summed resonators in combination with CMOS circuitry to select the best resonators to make the desired filter. Linearity, motional impedance, termination resistors, thermal stability and mechanical stability over time needs to be further addressed. Improved CMOS-MEMS resonators with embedded on-chip electronics will offer very low parasitic capacitances and low power consumption. This offers promising possibilities to create frequency stable filters and mixer-filters with low noise and low power for WSN nodes.

Appendix

This appendix contains description about the different beam boundary conditions, non-linear capacitive filter analysis and implementations of CMOS-MEMS filters.

A Beam boundary conditions

In order to find mode numbers for the beams and resonators used in this work, an analysis on beam bending for the desired beam elements must be performed. A general rectangular beam with displacement z depending on position x throughout its length can have the following trial solution for $z(x)$:

$$z(x) = C_1 sin(\beta x) + C_2 cos(\beta x) + C_3 sinh(\beta x) + C_4 cosh(\beta x) \qquad (\mathbf{A}.1)$$

The general equation for beam bending has four terms C_1 to C_4. These terms have to be solved in order to find an expression for the beam bending based on boundary conditions of the beam. The third derivative of the bending equation $z(x)$ results in the following relationship:

	Resulting parameter
$z(x)$	Beam bending z
$z'(x)$	Beam angle Θ
$z''(x)$	Beam curvature or bending moment M
$z'''(x)$	Beam shear force V

Table A.1: The derivative of $z(x)$

The four relationships listed in Table A.1 is to be used to find the solution for the general beam bending equation, and then to calculate the necessary beam mode constant β_N for that type of boundary condition. The desired mode numbers for the following beam types: Free-Free (FF), Clamped-Clamped (CC), Clamped-Free (CF), Clamped-Pinned (CP) and Pinned-Pinned (PP).

$$cosh^2 - sinh^2 = 1 \qquad (\mathbf{A}.2)$$

$$sin^2 + cos^2 = 1 \qquad (\mathbf{A}.3)$$

The relationships used in the equations above are also used to find the beam boundary conditions.

Free-Free beam

The Free-Free (FF) beam has no anchoring points at the start or end of the beam. It is, however, supported at $L/4$ and $3L/4$ along its length. The analysis is still based on the start and ending point of the whole resonating beam element. At the start and end of the Free-Free beam, there is a displacement and an angle, but no curvature or shear force can occur there. Therefore $z''(0) = 0$, $z''(L) = 0$, $z'''(0) = 0$ and $z'''(L) = 0$.

	Resulting general beam bend eq.
$z''(x=0)$	$-C_2 + C_4 = 0$
$z'''(x=0)$	$-C_1 + C_3 = 0$
$z''(x=L)$	$-C_1 sin(\beta L) - C_2 cos(\beta L) + C_3 sinh(\beta L) + C_4 cosh(\beta L) = 0$
$z'''(x=L)$	$-C_1 cos(\beta L) + C_2 sin(\beta L) + C_3 sinh(\beta L) + C_4 cosh(\beta L) = 0$

Table A.2: Boundary conditions for the Free-Free beam

By using the results above, it is possible to relate all equations to C_1 and C_2. This leads to the following matrix:

$$\begin{bmatrix} sinh(\beta L) - sin(\beta L) & cosh(\beta L) - cos(\beta L) \\ cosh(\beta L) - cos(\beta L) & sin(\beta L) + sinh(\beta L) \end{bmatrix} \cdot \begin{bmatrix} C_1 \\ C_2 \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \end{bmatrix}$$

By taking the determinant of the relationship above leads to

$$sin(\beta L)sinh(\beta L) + sinh^2(\beta L) - sin^2(\beta L) - sin(\beta L)sinh(\beta L)$$
$$-(cosh^2(\beta L) - cosh(\beta L)cos(\beta L) - cosh(\beta L)cos(\beta L) + cos^2(\beta L)) = 0$$

Further analysis of this leads to

$$sinh^2(\beta L) - sin^2(\beta L) - cosh^2(\beta L) - cos^2(\beta L) + 2cosh(\beta L)cos(\beta L) = 0$$

where the relationships in equations **A**.2 and **A**.3 are used to achieve

$$cosh(\beta L)cos(\beta L) = 1 \qquad (\mathbf{A}.4)$$

Mode number β_N	βL
1	4.7300
2	7.8532
3	10.9956
4	14.1371
5	17.2787

Table A.3: First five modes for the Free-Free beam

The first 5 modes which satisfies eq. **A**.4 are shown in Table A.3. In this work, the first two modes of the Free-Free beam are used to model the resonance frequency for the Free-Free Square-Frame Resonator (FFSFR).

Clamped-Clamped beam

The Clamped-Clamped (CC) beam is anchored at both ends. This means that at the anchoring points, the beam cannot move nor have any angle. However, at its anchoring points the beam will have a bending moment and shear forces. This leads to $z(0) = 0$, $z(L) = 0$, $z'(0) = 0$ and $z'(L) = 0$ as shown in Table A.4

	Resulting general beam bend eq.
$z(x=0)$	$C_2 + C_4 = 0$
$z'(x=0)$	$C_1 + C_3 = 0$
$z(x=L)$	$C_1 sin(\beta L) + C_2 cos(\beta L) + C_3 sinh(\beta L) + C_4 cosh(\beta L) = 0$
$z'(x=L)$	$C_1 cos(\beta L) - C_2 sin(\beta L) + C_3 cosh(\beta L) + C_4 sinh(\beta L) = 0$

Table A.4: Boundary conditions for the Clamped-Clamped beam

By using the results above, it is possible to relate all equations to C_1 and C_2. This leads to the following matrix:

$$\begin{bmatrix} sin(\beta L) - sinh(\beta L) & cos(\beta L) - cosh(\beta L) \\ cos(\beta L) - cosh(\beta L) & -sin(\beta L) - sinh(\beta L) \end{bmatrix} \cdot \begin{bmatrix} C_1 \\ C_2 \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \end{bmatrix}$$

By taking the determinant of the relationship above leads to

$$-sin^2(\beta L) - sin(\beta L)sinh(\beta L) + sinh(\beta L)sin(\beta L) + sinh^2(\beta L)$$
$$-(cos^2(\beta L) - cos(\beta L)cosh(\beta L) - cosh(\beta L)cos(\beta L) + cosh^2(\beta L)) = 0$$

Further analysis of this leads to

$$-sin^2(\beta L) + sinh^2(\beta L) - cos^2(\beta L) - cosh^2(\beta L) + 2cosh(\beta L)cos(\beta L) = 0$$

where the relationships in equations **A**.2 and **A**.3 are used:

$$cosh(\beta L)cos(\beta L) = 1 \qquad (\mathbf{A}.5)$$

Mode number β_N	βL
1	4.7300
2	7.8532
3	10.9956
4	14.1371
5	17.2787

Table A.5: First five modes for the Clamped-Clamped beam

The first 5 modes which satisfies eq. **A**.5 are shown in Table A.5. These are the same mode numbers as the Free-Free beam. Be aware that the static bending shape for the CC-beam is not the same as the FF-beam, even though they have the same mode numbers.

Clamped-Free beam

The Clamped-Free (CF) beam is anchored at one end and free to move at the other end. This means that at the anchored point, the beam cannot move nor have any angle. At the free end of the CF-beam there will be no bending moment nor shear force. This means that $z(0) = 0$, $z'(0) = 0$, $z''(L) = 0$ and $z'''(L) = 0$ as shown in Table A.6

	Resulting general beam bend eq.
$z(x = 0)$	$C_2 + C_4 = 0$
$z'(x = 0)$	$C_1 + C_3 = 0$
$z''(x = L)$	$-C_1 sin(\beta L) - C_2 cos(\beta L) + C_3 sinh(\beta L) + C_4 cosh(\beta L) = 0$
$z'''(x = L)$	$-C_1 cos(\beta L) + C_2 sin(\beta L) + C_3 cosh(\beta L) + C_4 sinh(\beta L) = 0$

Table A.6: Boundary conditions for the Clamped-Free beam

By using the results above, it is possible to relate all equations to C_1 and C_2. This leads to the following matrix:

$$\begin{bmatrix} -sin(\beta L) - sinh(\beta L) & -cos(\beta L) - cosh(\beta L) \\ -cos(\beta L) - cosh(\beta L) & sin(\beta L) - sinh(\beta L) \end{bmatrix} \cdot \begin{bmatrix} C_1 \\ C_2 \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \end{bmatrix}$$

By taking the determinant of the relationship above leads to

$$\begin{gathered} -sin^2(\beta L) + sin(\beta L)sinh(\beta L) - sinh(\beta L)sin(\beta L) + sinh^2(\beta L) \\ -(cos^2(\beta L) + cos(\beta L)cosh(\beta L) + cosh(\beta L)cos(\beta L) + cosh^2(\beta L)) = 0 \end{gathered}$$

Further analysis of this leads to

$$-sin^2(\beta L) + sinh^2(\beta L) - cos^2(\beta L) - cosh^2(\beta L) - 2cosh(\beta L)cos(\beta L) = 0$$

where the relationships in equations **A**.2 and **A**.3 are used:

$$cosh(\beta L)cos(\beta L) = -1 \tag{A.6}$$

Mode number β_N	βL
1	1.8751
2	4.6940
3	7.8547
4	10.9955
5	14.1372

Table A.7: First five modes for the Clamped-Free beam

The first 5 modes which satisfies eq. **A**.6 are shown in Table A.7. These mode numbers are lower compared to the FF and CC beam mode numbers.

Clamped-Pinned beam

The Clamped-Pinned (CP) beam is anchored at one end and pinned at the other end. This means that at the anchored point, the beam cannot move nor have any angle. At the pinned end of the CP-beam there will be no displacement nor any bending moment. This means that $z(0) = 0$, $z'(0) = 0$, $z(L) = 0$ and $z''(L) = 0$ as shown in Table A.8

	Resulting general beam bend eq.
$z(x = 0)$	$C_2 + C_4 = 0$
$z'(x = 0)$	$C_1 + C_3 = 0$
$z(x = L)$	$C_1 sin(\beta L) + C_2 cos(\beta L) + C_3 sinh(\beta L) + C_4 cosh(\beta L) = 0$
$z''(x = L)$	$-C_1 sin(\beta L) - C_2 cos(\beta L) + C_3 sinh(\beta L) + C_4 cosh(\beta L) = 0$

Table A.8: Boundary conditions for the Clamped-Pinned beam

By using the results above, it is possible to relate all equations to C_1 and C_2. This leads to the following matrix:

$$\begin{bmatrix} sin(\beta L) - sinh(\beta L) & cos(\beta L) - cosh(\beta L) \\ -sin(\beta L) - sinh(\beta L) & -cos(\beta L) - cosh(\beta L) \end{bmatrix} \cdot \begin{bmatrix} C_1 \\ C_2 \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \end{bmatrix}$$

By taking the determinant of the relationship above leads to

$$-sin(\beta L)cos(\beta L) - sin(\beta L)cosh(\beta L) + sinh(\beta L)cos(\beta L) + sinh(\beta L)cosh(\beta L) -$$
$$(-cos(\beta L)sin(\beta L) - cos(\beta L)sinh(\beta L) + cosh(\beta L)sin(\beta L) + cosh(\beta L)sinh(\beta L)) = 0$$

Further analysis of this leads to

$$2(sinh(\beta L)cos(\beta L) - sin(\beta L)cosh(\beta L)) = 0$$

which finally results in

$$sinh(\beta L)cos(\beta L) - sin(\beta L)cosh(\beta L) = 0 \qquad (\mathbf{A}.7)$$

Mode number β_N	βL
1	3.9266
2	7.0685
3	10.2101
4	13.3518
5	16.4934

Table A.9: First five modes for the Clamped-Pinned beam

The first 5 modes which satisfies eq. **A**.7 are shown in Table A.9. These mode numbers are slightly lower compared to the FF and CC beam mode numbers.

Pinned-Pinned beam

The Pinned-Pinned (CP) beam pinned at both ends. At both of the pinned ends of the CP-beam there will be no displacement nor any bending moment. At the pinned ends there will be an angle and a shear force. This means that $z(0) = 0$, $z''(0) = 0$, $z(L) = 0$ and $z''(L) = 0$. Table A.10 shows that this analysis becomes even more simplified

	Resulting general beam bend eq.
$z(x = 0)$	$C_2 + C_4 = 0$
$z''(x = 0)$	$-C_2 + C_4 \neq 0$

Table A.10: Boundary conditions for the Pinned-Pinned beam

Because of the two boundary conditions of $z(x = 0) = 0$ and $z''(x = 0) = 0$ leads to different results means that there are only two degrees of freedom, reducing the beam bending equation to:

$$z(x) = C_1 sin(\beta x) + C_2 cos(\beta x) \tag{A.8}$$

Eq. **A**.8 shows that there are only two constants. Using $z(x = 0) = 0$ leads to

$$z(x = 0) = C_1 \cdot 0 + C_2 \cdot 1 = 0 \rightarrow C_2 = 0$$

Thus the final equation for the beam bending for a Pinned-Pinned beam is defined as:

$$sin(\beta L) = 0 \tag{A.9}$$

This equation is much more simple than the other analysis' with mode numbers given as:

Mode number β_N	βL
1	π
2	2π
3	3π
4	4π
5	5π

Table A.11: First five modes for the Pinned-Pinned beam

The first 5 modes which satisfies eq. **A**.9 are shown in Table A.11. These mode numbers are lower compared to the Pinned-Pinned beam and is defined by an integer multiple of π. This was the final analysis of five different beam bending conditions used in this thesis. The Clamped-Clamped Square-Frame Resonator (CCSFR) uses a Pinned-Pinned mode for its first lateral frequency and a proper Clamped-Clamped mode for the second lateral frequency. The coupling beams to make higher order filter utilizes the Pinned-Pinned mode and all tether beams connecting any Square-Frame Resonator (SFR) to an anchored point utilizes the Clamped-Pinned mode.

B Non-linear capacitive higher order components

This section contains non-linear behavior of the resonator, due to mixing of higher order components into the filter passband [39, 40, 63]. The input force of the resonator is related to the mass, damping and spring stiffness:

$$F_{in} = m\frac{dz^2}{dt^2} + b\frac{dz}{dt} + kz$$

Using LaPlace and rearranging, this relationship can be rewritten as a function of displacement $Z(j\omega)$

$$Z(j\omega) = \frac{F_{in}(j\omega)}{k} \underbrace{\frac{1}{1 + \frac{j\omega}{Q\omega_0} - (\frac{\omega}{\omega_0})^2}}_{\Theta(j\omega)} \quad (\mathbf{B}.1)$$

where $\Theta(j\omega)$ becomes equal to Q if $\omega = \omega_0$. Both the input force F_{in} and the transfer function Θ are susceptible of mixing out of band frequencies into the desired bandwidth of the filter. Two out of band frequencies are defined as ω_1 and ω_2:

$$2\omega_1 - \omega_2 = \omega_0$$

where ω_1 and ω_2 are spaced by $2\Delta\omega$ and $\Delta\omega$ respectively. The input force F_{in} is due to an electrostatic force from the electrode and is expressed as

$$F_{in} = \frac{1}{2}(V_P - v_{ac})^2\frac{dC}{dz} = \frac{1}{2}(V_P - v_{ac})^2\frac{d}{dz}\left[C\left(1 + \frac{z}{g}\right)^{-1}\right]$$

where the input force can be expanded with non-linear terms:

$$F_{in} = \frac{1}{2}(V_P - v_{ac})^2\frac{-C}{g}\left[1 - \frac{2}{g}z + \frac{3}{g^2}z^2 - \frac{4}{g^3}z^3 + ...\right] \quad (\mathbf{B}.2)$$

The non-linear force is related to an ac input voltage v_{ac} and a displacement z which both are susceptible to undesired out-of-band frequency components and are given by

$$v_{ac} = V_1 cos(\omega_1 t) + V_2 cos(\omega_2 t)$$

The displacement can be written as

$$z = Z_1 cos(\omega_1 t) + Z_2 cos(\omega_2 t)$$

It is possible to rewrite eq. **B**.1 as a function of the following:

$$Z(j\omega) = \frac{V_P C}{kg}V(j\omega)\Theta(j\omega) \quad (\mathbf{B}.3)$$

$Z(j\omega)$ is now rewritten with the polarization voltage V_P, the static capacitance C, the effective spring stiffness k and the gap g. $Z(j\omega)$ also includes the non-linear

voltage $V(j\omega)$ and the gain $\Theta(j\omega)$. By assuming that $V_1 = V_2$, v_{ac} becomes $V_{in} = V_1(cos(\omega_1 t) + cos(\omega_2 t))$. The same is valid for z as it becomes $Z = Z_1(cos(\omega_1 t) + cos(\omega_2 t))$.

In order to derive the equation for the third order intermodulated fore (F_{IM3}), a weak parameter must be defined. The electrode gap is set as the weak parameter in this analysis. The displacement and force consist of a linear term and non-linear higher terms. An iterative process must be performed where the displacement of non-linear force terms are collected. Doing this results in the F_{IM3} product [39]:

$$F_{IM3} = V_{in}^3 \left[\frac{\varepsilon_0^2 A_e^2 V_P}{2g^5 k}\Theta_1 + \frac{\varepsilon_0^2 A_e^2 V_P}{4g^5 k}\Theta_2 + \frac{3\varepsilon_0^3 A_e^3 V_P^3}{4g^8 k^2}\Theta_1^2 + \frac{3\varepsilon_0^3 A_e^3 V_P^3}{2g^8 k^2}\Theta_1\Theta_2 + \frac{3\varepsilon_0^4 A_e^4 V_P^5}{2g^{11} k^3}\Theta_1^2\Theta_2 \right] \tag{B.4}$$

From the above equation it is possible to express the F_{IM3} in terms of voltage

$$V_{IIP3} = \left[\frac{\varepsilon_0 A_e}{2g^3 k}\Theta_1 + \frac{\varepsilon_0 A_e}{4g^3 k}\Theta_2 + \frac{3\varepsilon_0^2 A_e^2 V_P^2}{4g^6 k^2}\Theta_1^2 + \frac{3\varepsilon_0^2 A_e^2 V_P^2}{2g^6 k^2}\Theta_1\Theta_2 + \frac{3\varepsilon_0^3 A_e^3 V_P^4}{2g^9 k^3}\Theta_1^2\Theta_2 \right]^{-\frac{1}{2}} \tag{B.5}$$

where $\Theta_1 = \Theta(\omega_1)$, $\Theta_2 = \Theta(\omega_2)$ and

$$\Theta(\omega) = \frac{1}{1 + j\omega/(Q\omega_0) - (\omega/\omega_0)^2} \tag{B.6}$$

The equation for V_{IIP3} is not easily analyzed with Θ_1 and Θ_2. A similar expression for V_{IIP3} is therefore derived [40]. The output voltage (IM) due to the first non-linear input term V_{in}^3 will be used in this case. For simplicity it is possible to assume that an output voltage is detected at the output of the resonator through a parasitic capacitance C_P. Later on in this analysis, the C_P will cancel out and a final equation for the IIP3 is achieved. Using the gap as the weak parameter and expanding the force and displacement with these terms results in a rewritten displacement Z:

$$Z = -jV_{in}\left(\frac{CV_PQ}{gk}\right)[cos(\omega_1 t) + cos(\omega_2 t)] + V_{in}^3 \left[\frac{6C^2 V_P Q^2}{g^7 k^4}\left(4C^2 V_P^4 Q^2 + j3Cg^2 k V_P^2 Q - g^4 k^2\right) \right] cos(\frac{\omega_1 - \omega_2}{2}t) cos(\frac{\omega_1 + \omega_2}{2}t) \tag{B.7}$$

The Z in eq. **B**.7 is used to obtain the V_{out,ω_1} in eq. **B**.8. Following the same analysis as earlier, the output motional voltage can be expressed as

$$V_{out,\omega_1} = \frac{Z}{C_P}\frac{dC}{dZ}V_P = V_{in}\left(j\frac{C^2 Q V_P^2}{C_P g^2 k}\left[1 + V_{in}^2 (j\frac{9C^3 Q^4 V_P^4}{g^6 k^3} - \frac{27C^2 Q^3 V_P^2}{2g^4 k^2})\right]\right) \tag{B.8}$$

Only the first term in eq. **B**.8 will be used in the analysis to derive the IIP3. The IM tone for the resonator and its first non-linear product is given by

$$V_{out(IM)} = V_{in}^3 \left[\frac{3C^3Q^2V_P^2}{4C_Pg^4k^2} - j\frac{9C^4Q^3V_P^4}{2C_Pg^6k^3} - \frac{3C^5Q^4V_P^6}{2C_Pg^8k^4} - \frac{3C^5Q^4V_P^6}{2C_Pg^8k^4} \right] \qquad (\mathbf{B}.9)$$

For narrow gap, high-Q resonators, the two last terms in eq. **B**.9 dominates. The linear output from eq. **B**.8 and the IM tone of eq. **B**.9 are used to derive the V_{IIP3}:

$$V_{IIP3} = \sqrt{\left| \frac{\frac{C^2QV_P^2}{C_Pg^2k}}{\frac{3C^3Q^2V_P^2}{4C_Pg^4k^2} - j\frac{9C^4Q^3V_P^4}{2C_Pg^6k^3} - \frac{3C^5Q^4V_P^6}{2C_Pg^8k^4} - \frac{3C^5Q^4V_P^6}{2C_Pg^8k^4}} \right|} \qquad (\mathbf{B}.10)$$

The two last terms in eq. **B**.10 will dominate which gives

$$V_{IIP3} = \sqrt{\left| \frac{\frac{C^2QV_P^2}{C_Pg^2k}}{-\frac{3C^5Q^4V_P^6}{C_Pg^8k^4}} \right|} = \sqrt{\left| -\frac{g^6k^3}{3C^3Q^3V_P^4} \right|} \qquad (\mathbf{B}.11)$$

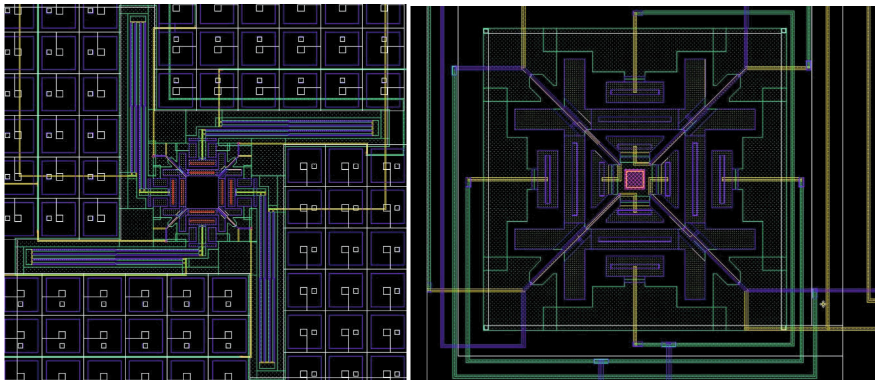
which results in the equation for IIP3:

$$V_{IIP3} = 0.577\sqrt{\frac{g^6k^3}{C^3Q^3V_P^4}} \qquad (\mathbf{B}.12)$$

The final equation for the V_{IIP3} is given in eq. **B**.12. It should be noted that this analysis takes into account an analysis with the resonator as a filter. The same analysis can be performed for a non-linear mixer-filter which will result in a very similar end equation and is therefore not done here. The result from these equations will give insight in how to design and model a MEMS resonator with respect to linearity.

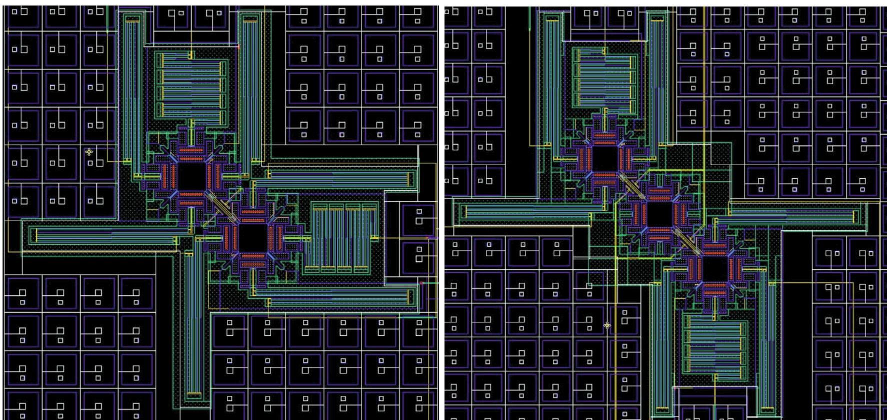
C Resonator filter & amplifier layouts and results

This part of the appendix contains simulation results, measurement results, layout screenshots and SEM photos from various CMOS-MEMS implementations in this thesis. These figures and tables are from the TSMC 0.35 μm and the TSMC 90nm process, as well as from the STM 0.25 μm and the STM 90 nm process. Results from the Self-Healing MEMS (SH MEMS) project at CMU from 2009–2010 are shown.



(a) FFSFR - Normal

(b) FFSFR - Full differential



(c) FFSFR - 2mech

(d) FFSFR - 3mech

Figure C.1: Layout of four FFSFR filters in TSMC 0.35 μm

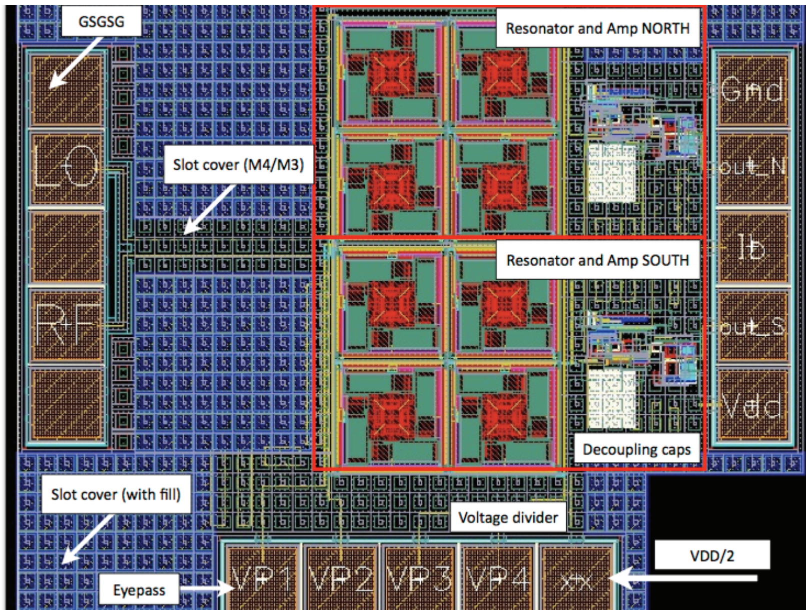


Figure C.2: Layout of electrically summed array (Self-Healing MEMS project at CMU)

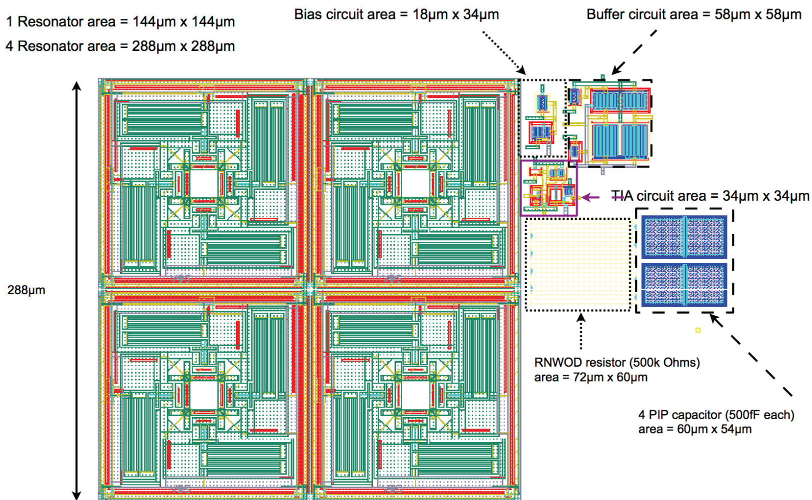


Figure C.3: 2 systems of 4 electrically summed resonators (SH MEMS project at CMU)

	TT	SS	SF	FS	FF
Power [mW]	16.5	4.84	6.1	37.6	30.98
Gain @ 10MHz [dB]	137.8	130.4	128.7	140.8	140.3
Gain @ 11.23MHz [dB]	137.5	129.8	128.5	140.4	140.2
BW [MHz]	18.35	12.78	18.63	15.37	21.35
Noise 10–11.23MHz [pA]	888.5	860.9	890.1	884.5	908.4
Noise @ 10MHz [fA / $\sqrt{Hz}$]	880	851.9	881.6	876	900.4

Table C.1: Self-Healing MEMS project @ CMU: Amplifier results

	TT	SS	SF	FS	FF
f_0 [MHz]	9.999	9.999	9.999	9.999	9.999
BW [MHz]	4454	4463	4456	4453	4449
Q	2245	2241	2244	2246	2248
i_o [nA] @ f_0	14.99	15.02	15.02	14.98	14.97
V_{out} [mV] @ f_0	110.8	46.97	39.75	154.4	148
Z_{TIA} [MΩ]	7.389	3.128	2.647	10.3	9.88

Table C.2: SH MEMS project @ CMU: Standalone resonator with amplifier

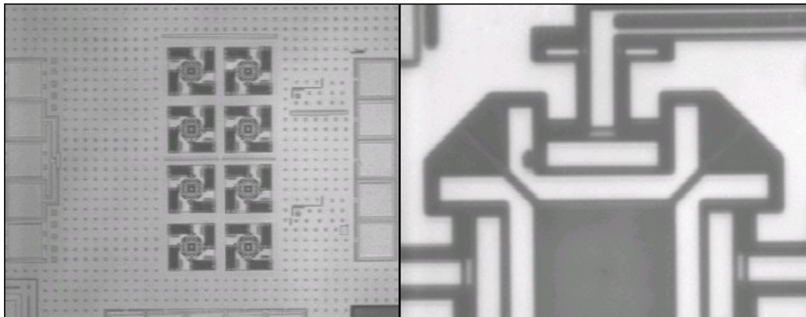


Figure C.4: Released TSMC 0.35 μm FFSFR array (SH project at CMU)

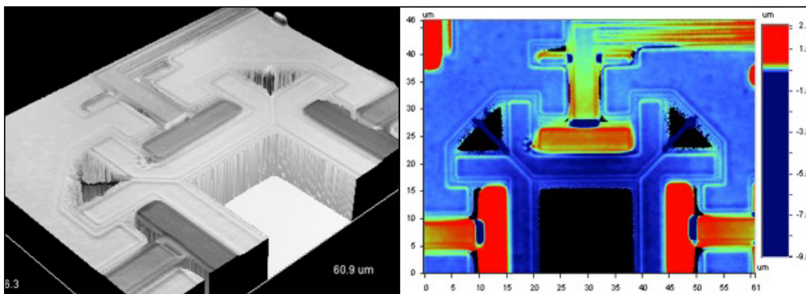


Figure C.5: Wyco measurement showing slight curling of released FFSFR (SH project at CMU)

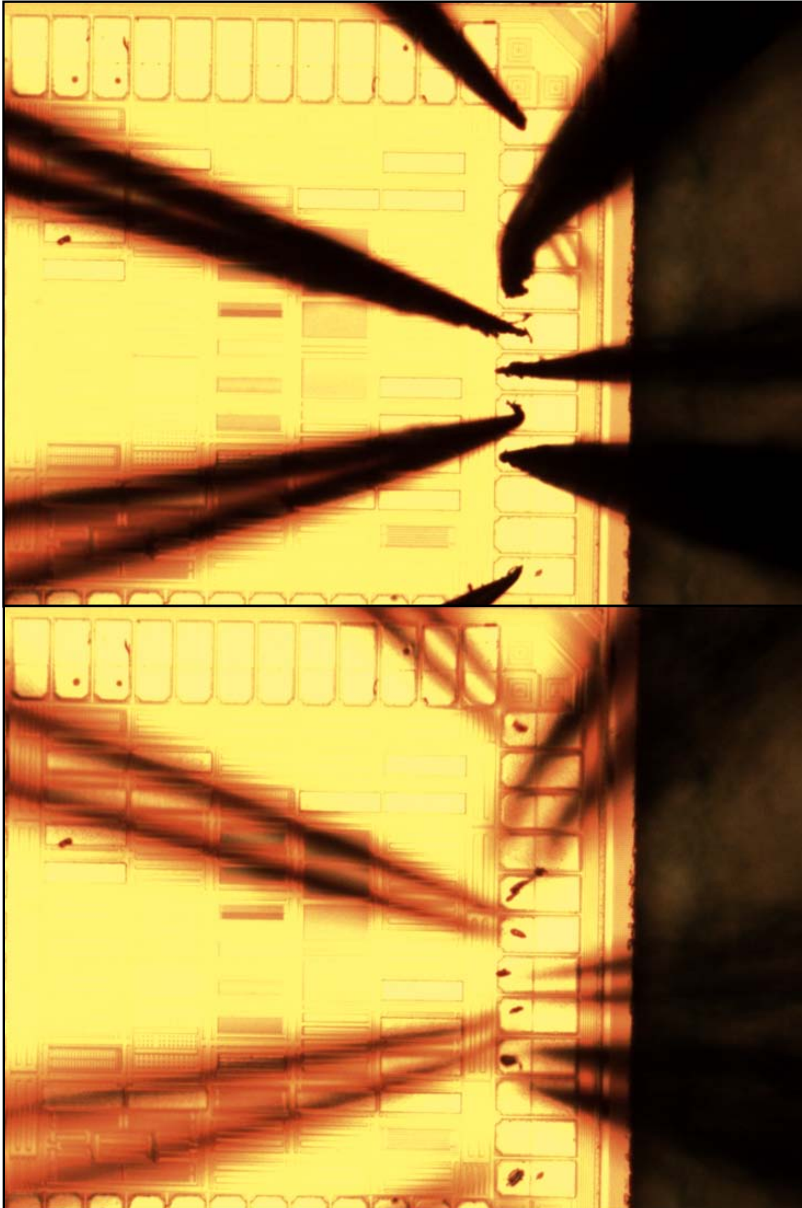


Figure C.6: STM 90 nm die with probes, testing CMOS circuitry before and after etch

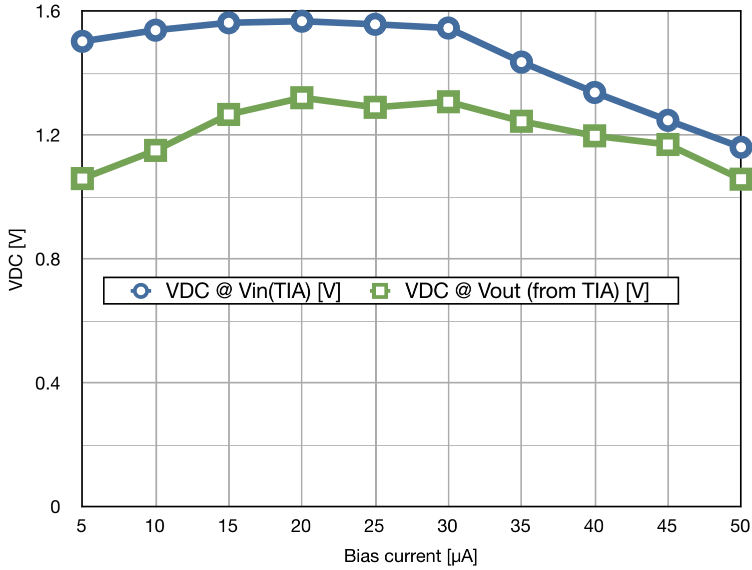


Figure C.7: In & out V(DC) results TIA with CS buffer (SH project at CMU)

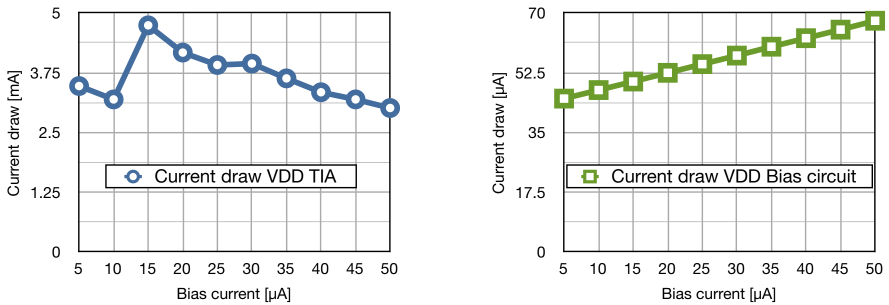


Figure C.8: In & out I(DC) results TIA with CS buffer (SH project at CMU)

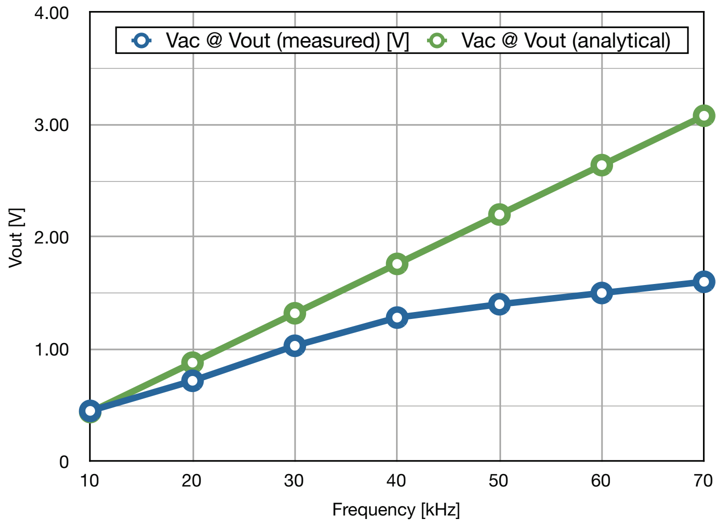


Figure C.9: AC measurement, testing feedthrough (SH project at CMU)

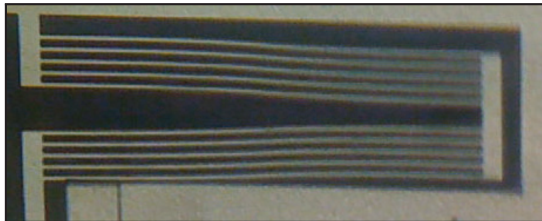


Figure C.10: STM 0.25 μm lateral moved Self-Assembly electrode

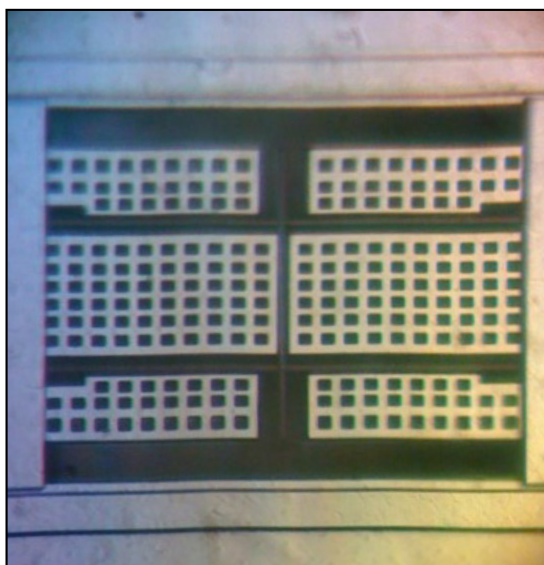


Figure C.11: STM 0.25 μm lateral Free-Free resonator

Acronyms

A/D Analog-to-Digital

ALC Automatic Level Control

ASIMPS Application Specific MEMS Process Service

BAW Bulk Acoustic Wave

CAD Computer Aided Design

CC Clamped-clamped

CF Clamped-free

CMFB Common Mode Feedback

CP Clamped-pinned

CCSFR Clamped-clamped Square-Frame Resonator

CG Common-Gate

CMOS Complementary Metal-Oxide Semiconductor

CMU Carnegie Mellon University

CS Common-Source

CW CoventorWare

DEMUX Demultiplexer

DRIE Deep Reactive Ion Etching

ESD Electrostatic discharge

FC Folded Cascode

FDSM Frequency Delta Sigma Modulator

FEM Finite Element Method

FFSFR Free-free Square-Frame Resonator

FF Free-free

LNA Low Noise Amplifier

MEMS MicroElectroMechanical Systems

NODAS Nodal Design of Actuators and Sensors

PP Pinned-pinned

PPTF Parallel Plate Tuning Fork

RF MEMS Radio Frequency MEMS

RIE Reactive Ion Etch

SA Self-Assembly

SD Simple Differential

SF Source-Follower

SFR Square-Frame Resonator

SOI Silicon On Insulator

SQNR Signal-to-Quantization-Noise Ratio

STM ST Microelectronics

STS Surface Technology System

TCE Thermal Coefficient of Expansion

TED Thermoelastic damping

THD Total Harmonic Distortion

TIA Trans-Impedance Amplifier

TSMC Taiwan Semiconductor Manufacturing Company

VCO Voltage Controlled Oscillator

WSN Wireless Sensor Networks

Nomenclature

β_N Resonator mode constant

β_c Coupling beam mode constant

β_{te} Tether beam mode constant

κ Topographical scaling factor

ω_0 Nominal resonator radial frequency

ρ Effective material density

A_V Amplifier voltage-to-voltage gain

A_{el} Resonator-to-electrode area

BW Filter bandwidth

C_z Resonator motional capacitance

CL Total system conversion loss in dB

E Effective Young's Modulus

$F_{e,in}$ Mechanical force at the resonator input

f_{eff} Effective resonance frequency

f_{nom} Nominal resonance frequency

H Resonator thickness

IL Insertion Loss

$IIP3$ Third-order Input Interception Point

I_N Amplifier input referred noise current

i_o Resonator motional current

k Static resonator stiffness

k_{ij} Normalized filter coefficient

k_r Effective resonator stiffness

k_{sij} Coupling beam stiffness

L Resonator length

L_c Coupling beam length

L_z Resonator motional inductance

L_{te} Tether beam length

m Static resonator mass

m_{eff} Effective resonator mass

n_{in} Resonator input electromechanical coupling coefficient

n_{out} Resonator output electromechanical coupling coefficient

q_i Filter scaling factor

Q_{eff} Effective Q-factor

Q_{nom} Nominal Q-factor

R_z Resonator motional resistance

R_{Qi} Filter termination resistance

$SFDR$ Spurious Free Dynamic Range

SNR Signal-to-Noise ratio

V_{LO} Resonator Local Oscillator voltage

V_P Resonator polarization voltage

V_{RF} Resonator (RF) input voltage

W Resonator width

W_c Coupling beam width

W_{te} Tether beam width

z Resonator displacement

ZL Termination Impedance to Linearity Product

Z_{TIA} Amplifier current-to-voltage (transimpedance) gain

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