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High-precision beamforming with UWB impulse radar

Master thesis

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Abstract

Indications from this years Consumer Electronics Show 2009 shows that the adoption of the Ultra-Wideband (UWB) technology is starting to arise. Mainly, the show-cased UWB technologies was based around high transfer-rates of data, but the potensial of the technology is not limited to this. Position localization and radar applications are other areas where this technology shows great potensial. For reducing power-consumption, improving positioning accuracy or improving radar resolution a beamforming scheme can be adopted.

Close-range beamforming of Electromagnetic Waves (EMW) is a challenging task. For achieving beamforming with very high resolution, extremely accurate high-resolution phase/timing circuits are required. In this thesis such circuits have been accomplished using standard CMOS technology.

Most published results of UWB beamforming is based around the idea of receiving a directional signal. In this thesis, we will look at how to design a UWB beamforming *transmitter* that can create directional wavefronts or focus its energy to a point in space using very accurate timing circuits.

As a part of this thesis, a prototype beamformer system has been developed which shows some very promising features. The proposed timing circuit should be of great interest for further development in for example the UWB impulse radar field.

Contents

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1 Introduction

1.1 Goal of this thesis

The goal of this thesis is to explain the foundations of UWB beamforming and to develop a prototype impulse radio beamformer based upon this theory implementable in Complimentary Metal-Oxide-Semiconductor (CMOS) technology. This thesis will thrive to explain how to achieve high-resolution accurate beamforming using standard digital CMOS technology. It is desired that this thesis could be used as reference material for further developments of UWB beamforming applications. To inspire others to use this thesis to build applications, it has been the goal to explain the process of making the prototype beamformer as practical as possible without leaving out the essential theory.

1.2 Motivation

The motivation behind this thesis is to explore how to achieve high-resolution beamforming using UWB impulse radio in CMOS technology. Hopefully this will enable the emergence of several new applications and help boost the development of new devices. The emergence of UWB applications have been happening way too slow after the Federal Communications Commission (FCC) approved of the new UWB mask in 2002. Some journalists even announced the death of the UWB technology. Because of the great potensial that UWB technology offers, this master thesis aims to inspire others to explore the technology further and create so far unthinkable new devices within several application areas.

Improved beamforming resolution will open up possibilities within lots of areas. For example improved imaging systems that might enable the possibility for an electromagnetic camera for medical imaging or pipe surveillance in the oil industry. Very accurate position localization can help streamline storage routines or enable high-resolution 3D-tracking for motion virtualization.

1.3 The process

This thesis has been completed through an ongoing process for approximately 16 months. It can largely be divided up in four phases:

- Pre-study
- Prototype design
- Prototype measurement
- Writing

The pre-study phase consisted of reading about UWB theory and to get a good understanding of the principles of UWB and beamforming.

In the next phase, the focus was on making a good prototype design that could be implemented in CMOS. Here, the different building-blocks required to make a beamformer was investigated and different alternatives for design was discussed and simulated. A very promising design was made and sent to an Application-Specific Integrated Circuit (ASIC) manufacturer (STMicroelectronics). To be able to test the chip, a Printed Circuit Board (PCB) was designed with focus on testability. Several programs and MATLAB scripts were made to assist in testing the different aspects of the chip that needed testing.

The prototype measurement phase consumed many many hours in the laboratory both for debugging and verification of measurement-results. Because the prototype chip is a custom made chip, there is no standard measurement programs or equipment. Therefor, everything had to be planned from scratch and a lot of coding had to be done.

At the end, the complete project was documented based upon the notes written during the testing period. This written thesis is intended to serve as a documentation of the complete process using both theory and practical explanations.

1.4 A brief historical overview

1.4.1 The early history of radio

The era of wireless radio began in 1865 with James Clerk Maxwell who used a mathematical approach to describe the behavior of EMW. A few years later Heinrich Hertz conducted a series of experiments based upon Maxwell's equations. Hertz managed

to transmit and receive EMW over several meters using a spark-gap transmitter. A spark-gap transmitter creates a spark which induces Electromagnetic (EM) radiation.

In 1901, Guglielmo Marconi was the first to transmit Morse-code over a longer distance. As more people was trying to transmit Morse code wireless, the more impossible it became to understand what was being sent because the different transmissions were interfering with one another.

1.4.2 Moving towards narrow band

The technology of the time was not very advanced compared to today's technology, therefore the transmissions was characterized by very bad Signal-to-Noise Ratio (SNR). This led to the exploration of narrow-band technology. In 1905 Reginald Fessenden came up with the concept of Amplitude Modulation (AM). This technology was based upon a carrier-frequency with the information modulated as amplitude variations of the carrier-frequency. This was a significant step forward from the impulse-based Morse-code both when it came to SNR and the possibility of sending audio. Because of problems with interference, regulations at the time eventually prohibited wide-band transmission.

1.4.3 Small steps towards wider bands

In 1933 Edwin Howard Armstrong came up with the idea of modulating the information in frequency instead of amplitude. This led to a much clearer sound compared to AM and the technology was static-free. This technology required wider frequency bands for transmission to make room for the frequency modulated information.

Claude Shannon, an American electronic engineer and mathematician, discovered in 1948 that under certain conditions, the more a data signal is spread in bandwidth such that it resembles noise in frequency, the more data it can contain. He introduced the concept of transmitting with low power-density and high bandwidth instead of high power-density and low bandwidth which was the usual way of transmitting.

1.4.4 More advantages using wider bands

Lots of experiments with wideband technology have been conducted through the years. In the late 1970's and 1980's there was demonstrations showing low-power UWB transmission based on impulse-radio and position localization applications.

At the 14th of February 2002 FCC defined a UWB mask which permitted transmission within the 3.1 GHz - 10.6 GHz band with certain limitations. Since then, several companies and research institutes have been exploring the UWB technology and possible applications. Amongst several things, UWB has shown very promising features when it comes to high-speed data-transfer over short ranges.

1.5 Outline of thesis

The next chapters of this thesis will include the following:

In Chapter 2, the basics of UWB technology and beamforming will be explained. The principles behind beamforming is found here.

In Chapter 3, a simple architecture for a UWB beamformer is presented and some practical beamforming examples are shown. Further, a design for a High-Resolution Programmable Delay Line (HRPDL) is presented in detail and a complete beamforming system for implementation on a chip is explained.

Chapter 4 presents both simulated and measured results for the proposed circuit and at the end a result from beamforming in practice is shown.

In Chapter 5 we conclude the thesis and present some thoughts on further development.

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2 UWB and beamforming

2.1 Chapter overview

In this chapter some basic UWB theory will be presented. The generation of a UWB signal will briefly be explained and the concept of radar will be presented. Further, we will look at the foundations of beamforming and some of the published work within this field.

2.2 UWB technology

2.2.1 Basic UWB

The basic idea behind UWB technology is to transmit impulses of EMW as opposed to the traditional narrow-band approach were transmission is modulated on a carrier-frequency.

An ideal impulse (Dirac delta-pulse) is a signal which has infinitely high amplitude and infinitesimal time-duration. An impulse's frequency spectrum covers all possible frequencies.

It is not possible to create an ideal impulse in the real-world, so the UWB technology uses a pulse with a finite amplitude and very short duration as a realistic approximation. Such a pulse still has a very wide frequency spectrum, hence the name Ultra-Wideband.

We can divide UWB technology in three basic application areas:

- Communication and sensors
- Position localization and tracking
- Radar

Communication and sensors

These are application that transfer data wirelessly. The focus is often on high transfer-rates of data for example in a Personal Area Network (PAN) or transfer of sensor data in a medical setting to relieve a patient from being wired.

Position localization and tracking

These are applications that are aiming at achieving high-precision localization of an object, for example combined with RFID in a storage facility. The tracking of an object is also interesting and might help streamline a production process. In this field it is important with cleverly designed timing architectures, for example an active echo architecture as proposed in [Ande 07].

Radar

These are applications that transmit EMW and look at the reflected energy to get information about the environment. Examples of applications are intrusion detection, vehicular collision radar or an EM camera. Very accurate and high-resolution timing-circuits are important components within this area.

2.2.2 Generating and transmitting UWB signals

In a world without restrictions, a UWB signal could be created simply by making impulse-like pulses. But due to regulations, there are some limitations to what we are allowed to transmit. There are different frequency-assignment authorities for different parts of the world. In this thesis we will base our design on the regulations made by the FCC for the United States. The limitations are necessary to enable several technologies to work side-by-side without interfering with each other.

Regulations

The FCC states that the transmitted frequencies for a UWB signal must be within a limit of 3.1 GHz - 10.6 GHz. Permitted emission level is -41 dBm/MHz and is referred to as the maximum limit of Effective Isotropically Radiated Power (EIRP). For a signal to

be recognized as a UWB signal it must have a bandwidth larger than 500 MHz or a fractional bandwidth larger than 20 %. Fractional bandwidth: $BW = 2\frac{f_H - f_L}{f_H + f_L}$.

UWB signal generation

There are many ways to generate UWB signals. In [Siwi 04a] three methods are suggested. A very simple way is to generate an impulse-like pulse and send it through a band-pass filter to make sure it stays within the 3.1 GHz - 10.6 GHz frequency limit and that the total EIRP does not exceed -41 dBm/MHz. This approach is very efficient and easy to build, but the method lacks the ability to place the pulse accurately in the frequency spectrum to utilize the allowed emission of spectrum energy. A second approach is to generate a precise UWB pulse shape at base-band and then shift it up accurately to the desired location in the frequency spectrum. A third method is to modify the modulation method of conventional radio systems so that the resulting signal is within the UWB definition of required minimum bandwidth set by the FCC.

In [Moen 06] a CMOS implementation of pulse shaping at base-band and frequency shifting is explored and achieved using very simple circuitry.

2.2.3 UWB impulse radar

The radar concept

The basic concept behind radars is to transmit EMW. The waves propagate until they hit an object, then scatters in all directions (Fig. 2.1). Some of the scattered energy will return to the radar and by analyzing it the radar can extract information about the environment.

An UWB radar system

A simple UWB impulse-based radar is transmitting a pulse, then looks at the signal on the receiver antenna after a certain time-delay. If this time-delay is programmable, and we know the propagation speed of the transmitted EMW, then we can look at what is going on at a certain distance away from our radar. In [Hjor 06] such a system has been designed with great success.

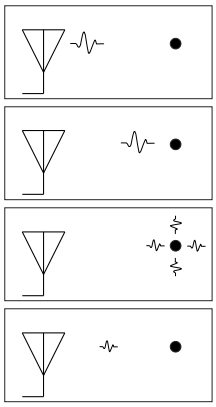

Figure 2.1: The concept of radar. A transmitted signal is reflected.

2.3 Beamforming

Beamforming is the act of transmitting or receiving a directional signal and the principles are used for both EMW and sound waves. This thesis will focus on EM beamforming by transmitting a directional signal.

Basically there are two ways of achieving beamforming: Mechanical and electronic.

Mechanical Mechanical beamforming is achieved by shaping antennas so that they transmit most of the energy in a certain direction, for example a horn antenna, and/or by using mechanically moving antennas, for example the standard rotating radar which is common on ships. The directional antenna can be very effective, but has the limitation that it cannot move its beam. By moving antennas physically we can obtain a moving beam, but moving parts are not always practical and it also puts great limitations on how fast the beam can be moved.

Electronic Electronic beamforming is directional EMW without any moving parts or directional antennas. The beamforming is achieved by electronics combined with an array of crude antennas that utilize the effect of interference. Electronic beamforming can be done very precise and has the advantage of being able to move an EM beam over a relatively large area much faster than the rotating radar mechanism.

2.3.1 Interference

The term *interference* refers to the situation when two or more waves in space overlap. When interference occur, the total wave at any point at any instant of time is governed by the *principle of superposition*. [Youn 04] states the principle of superposition as: *When two or more waves overlap, the resultant displacement at any point and at any instant is found by adding the instantaneous displacements that would be produced at the point by the individual waves if each were present alone.* The term *displacement* is used in a general sense. For waves in the water, the term displacement is used to describe the actual displacement of the water surface above or below its normal level. For EMW, displacement is usually referring to a specific component of the electric or the magnetic field.

Constructive and destructive interference

Let us assume we have two radio transmitters located at different locations and transmitting the same continuously sinusoidal signal in phase. If we draw a line between the two transmitters and look at the point in the middle, we are now equally distanced from both of the transmitters and the waves from the two transmitters will be in phase in this point. From the principle of superposition, the resultant wave amplitude in this point equals the sum of the two amplitudes. This is called *constructive interference*.

Now, if we look at a point a quarter of a wavelength closer to one of the transmitters, the EMW from one of the two is $+90^\circ$ out of phase relative to the middle point and the other is -90° out of phase. The phase-difference between the two is now 180° and the two waves are exactly out of phase. The sum of the two amplitudes are now opposite of each other and will cancel each other out, resulting in an amplitude of zero. This is called *destructive interference*. The effects of constructive and destructive interference is illustrated in Fig. 2.2

By taking advantage of the effects of constructive and destructive interference, we can construct an EM beam in a certain direction or create a directional wavefront of EMW.

2.3.2 Lobes

The term *lobe* refers to an identifiable segment of an antennas radiation pattern. The main-lobe is the lobe containing the most power. Side-lobes are usually smaller undesired lobes that appear because of the interference pattern. In some cases an aliasing effect makes some side-lobes substantially larger than most of the other side-lobes. These lobes are referred to as grating lobes and they often appear in uniformly spaced

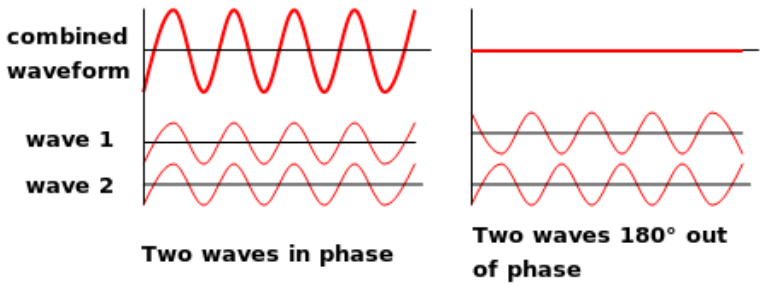

Figure 2.2: The effects of constructive and destructive interference. (Based on figure from Wikipedia.)

antenna arrays if the spacing between adjacent antennas is to large [Ante]. This effect is shown in Fig. 2.3.

2.3.3 Two approaches to electronic beamforming

While a fixed directional transmission or reception could be achieved mechanically, this thesis will focus on the electronic signal processing technique used with sensor arrays to achieve beamforming.

Electronic beamforming is often achieved by using a *phased array* transmitting a signal with carrier wave. A phased array is an array of antennas where each of the antennas are transmitting a phase shifted version of the signal. Usually this is accomplished by using phase-shifters. This technique is referred to as *frequency-domain beamforming*.

For pulse-based signals, the phase shifters are often replaced with time delays. By controlling the firing-sequence when each of the antennas are transmitting, we can control the direction of the major part of the transmitted energy. This way of achieving beamforming is referred to as *time-domain beamforming*.

Even though both frequency-domain beamforming and time-domain beamforming is within the definition of phased arrays, frequency-domain beamforming is usually the method referred to when talking about phased arrays. A more common term for time-domain beamforming when controlling the firing-sequence of impulses is *timed array*.

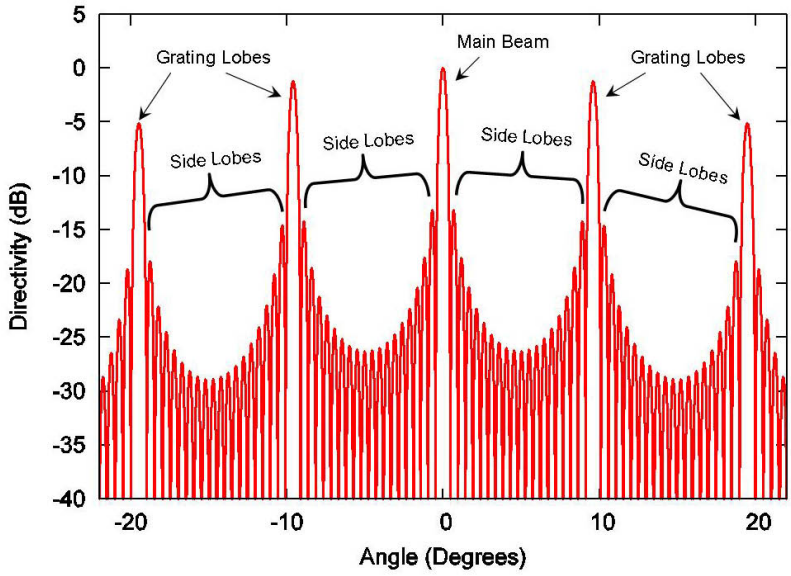

Figure 2.3: A typical radiation pattern using a phased-array structure with antenna spacing much larger than one half of a wavelength. (Figure copied from Wikipedia.)

2.3.4 Phased array beamforming

By controlling the relative phases and amplitudes in a transmitting antenna array, the radiation pattern can be reinforced in a certain desired direction.

When transmitting a directional signal, the transmitter controls the phase and amplitude of the transmitted signal from each of the antennas, taking advantage of constructive and destructive interference. This way, a controllable beam is achieved. When receiving a directional signal, the received signal from each of the antennas in the receiver array is combined in such a way that we are able to ”listen“ in a certain direction.

Frequency-domain beamforming is achieved by using variable phase-shifters and optional weighting with each antenna. The achieved spatial selectivity is dependent only upon array-size and not the number of antenna-elements [Chu 07]. In phased arrays, the antenna-spacing is usually fixed at $\lambda/2$. Therefor more antennas need to be added in order to increase the spatial selectivity. Antenna spacing could be increased above $\lambda/2$, however this will come at the expense of multiple large side-lobes or grating-lobes. Therefor the array-size dictates number of antennas in a phased-array beamformer.

2.3.5 Timed array beamforming

For a timed array *receiver*, a delay and sum scheme is used for beamforming. Each receiver-antenna is delayed by a time-delay circuit and the result is summed to recover the signal received from the desired direction. To achieve a time-domain beamforming *transmitter* using impulses, each antenna have to transmit a time-delayed version of the original signal.

Wide-band time-domain pulse beamformers offers several benefits over narrow-band phased-array beamformers. In [Kais 06], one of the major benefits mentioned is that time-domain beamformers do not have any grating-lobes no matter how large the antenna spacing is. This is a very beneficial property that makes the signal recognition on the receiver circuit much easier. Also, the side-lobes are fixed and will only be affected by the number of antennas, not the spacing between them. The main-lobe width is dependent upon the ratio of the center wave-length over array-size as is the case for conventional narrow-band beamforming.

As opposed to the phased-array case, weighing of different antennas is meaningless and will only be detrimental to the main-lobe to side-lobe ratio [Ries 05].

A very interesting feature mentioned in [Kais 06] is the fact that the UWB peak gain is doubled compared conventional phased array beamforming. This means that for UWB applications we can use only half the number of antennas and thus reduce energy consumption.

It was showed in [Funk 96] that by using N simultaneous triggered antennas in a timed-array scheme, the electric fields from each of the individual elements combine coherently in free space at an angle $\alpha = 0^\circ$. Hence, the peak power received by a far-field antenna scales to N^2 when placed at 0°.

2.3.6 Antenna array architectures

There are different ways of arranging the antennas in an antenna array depending on the desired outcome. A 2-dimensional beamformer can be achieved by using a simple 1-dimensional straight-line architecture. All the antennas are arranged side-by-side on a straight line.

If we want to control the focal point of the beam in a third dimension, we need to introduce a second dimension to our antenna array. The antenna array could possibly have lots of different shapes. For example a circle of antennas or two crossed lines of antennas. A very common shape know as patch antenna consists of a rectangular

matrix pattern using $n \times m$ antennas.

2.3.7 UWB beamforming

In this thesis we will focus on Ultra-Wideband Impulse Radio (UWB-IR) time-domain beamforming. There are two typical uses of beamforming for different purposes. Focusing energy in a point or creating a directional wavefront.

Creating a directional wavefront

For a communication system, energy consumption can be reduced if the radiated energy is directed towards the target(s) instead of transmitting in all directions. Localization information can often, with varying precision, be extracted from a communication system. If a transmitter knows that the recipient for the information about to be sent is located somewhere in a direction of approximately 60°, it can create a directional wavefront towards the recipient by using beamforming techniques. This way the transmitter can radiate less energy compared to sending in all directions. Receivers located elsewhere will not receive a strong enough signal to recognize it as anything other than noise and does not consume any power in decoding and processing the data.

A directional wavefront is created by firing all the transmitting antennas at the same time for a 0 degree wavefront. For a wavefront directed a little to the left, the rightmost antenna fires first, followed by each of the other antennas (right to left) with a fixed amount of delay between each of them.

At close range, the wavefront will not be as effective because the different wavefronts have not yet started to interfere. At more distant ranges, the wavefronts add up and the effect of the directional wavefront becomes apparent.

Focusing energy

In a UWB impulse radar, the goal is to get information about the surroundings. The radar sends out energy and looks at the received back-scattered energy. Without any beamforming scheme, it is hard to say anything about where the reflected energy is coming from unless focused antennas are used.

If we apply beamforming using an energy-focus approach, we are able to focus most of the radiated energy in a specific point as shown in Fig. 2.4. In this approach, a specified

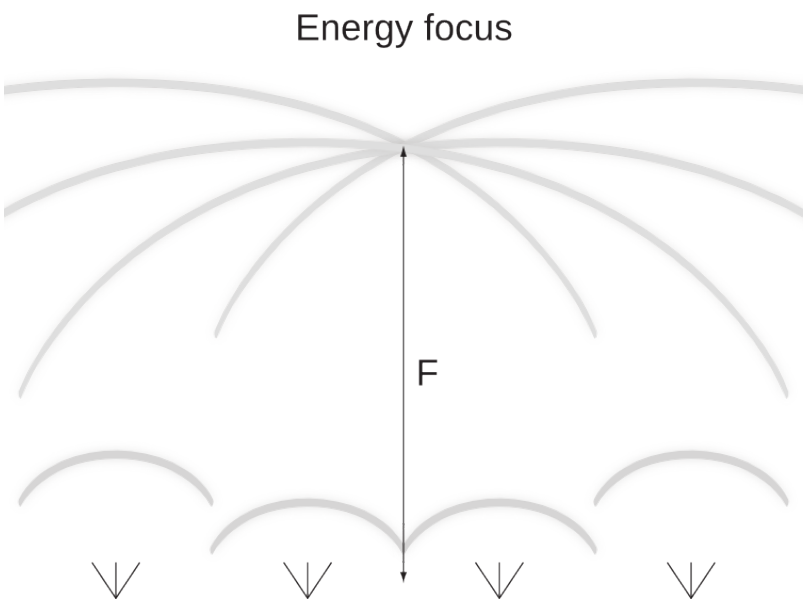

Figure 2.4: Focal point beamforming

location in space for focus is determined. By using simple trigonometry, the length from each of the antennas to the specified location can be calculated. Then if we know the speed of which the EMW are propagating, we can calculate the point in time that each of the antennas must transmit for their pulses to arrive together at the specified location.

An important thing to notice is the nature of the pulses being transmitted. The achieved focal point is not an infinitesimal point but rather a small area in space. This is because the impulses being transmitted are not ideal impulses, because that is physically impossible, instead they often appear as a Gaussian pulse of some order with a length of a few hundred picoseconds. This means that a pulse with length $t_{pulse} = 200$ ps will stretch out

$$d_{pulse} = t_{pulse} \times c = 200 \text{ ps} \times 3 \cdot 10^8 \text{ m/s} = 60 \text{ mm}$$

in space assuming speed of light propagation.

Propagation speed of EMW

The speed of EMW in medium other than vacuum is given by the refractive index of the current medium. The excact propagation speed of EMW in vacuum is $c =$

299792458 m/s. [Meik 01] states that the refractive index in the atmosphere of Europe is 1.000320. This results in a propagation speed of

$$v_{prop} = \frac{c}{1.000320} = 299696555 \text{ m/s}$$

In this thesis a propagation speed of $3 \cdot 10^8$ m/s will be used as a good approximation.

Advantages of beamforming

There are many advantages for using beamforming both in radar and communications. First of all the energy waste is reduced. While a standard omnidirectional antenna transmits its energy in all directions, a beamformer is capable of directing its emitted power in a certain direction. This way a receiving antenna can receive more of the radiated energy, thus reducing the requirements on transmission power.

One of the challenges working with low-power CMOS technology is available power-supply. Since modern CMOS technologies are limited to 1V power-supply, transmitting enough power from a single transmitter to reach the permitted radiation limit set by the FCC is a challenging task even with rail-to-rail operation. By introducing more transmitters, the radiation limit can be reached using beamforming techniques.

High-resolution beamforming may have several interesting applications within the radar field. For example, light-weight EM cameras could be developed to replace the heavy imaging systems currently in use at hospitals.

There are many good reasons to conduct further research into the field of beamforming. In Chapter 3 of this thesis, we will focus on designing a prototype beamformer.

2.4 UWB beamforming today

Most of the published work within UWB beamforming today is focused towards receiving a directional signal. In [Chu 07] an integrated directional receiver has been implemented in 0.13 µm CMOS. The presented design has a true time delay resolution of 15 ps with a maximum delay of 225 ps. The receiver provides 11 scan angles with approximately 9° of spatial resolution for an antenna spacing of 3 cm.

A design with much better time delay resolution is presented in [Rode 06]. The 4-bit

programmable delay-line provides a resolution of 4 ps and a total delay of 64 ps. For an antenna spacing of 1 cm, this design achieves 7° of spatial resolution.

An EM camera has been proposed in [Chu 08]. This camera provides 7x7 simultaneous active pixels by using a 2x2 antenna array and a 17.5 ps internal delay resolution between adjacent pixels.

[Safa 08] presents a UWB beamforming transmitter. This beamformer is designed to transmit a directional wavefront using four transmitters. The time-difference between the transmitters can be controlled with a resolution of 180 ps. Maximum time-difference between two channels is 880 ps. A scan angle resolution of 10° within ±60° was achieved with antenna spacing of 30 cm.

2.5 Summary

In this chapter we have explained the basics of UWB technology and beamforming. In Section 2.2 the signal shape and regulations was explained and the concept of radar was introduced.

In Section 2.3 the principles behind beamforming was explained. The superposition principle was presented and we looked at how this principle cause constructive and destructive interference.

We looked at the difference between a phased array beamformer and a timed array beamformer and saw that impulse-radio time-domain beamforming has some very nice advantages over carrier-based frequency-domain beamforming. Advantages are that timed array beamformers have no grating lobes and much more freedom in antenna-array design. In addition, a timed array beamformer can achieve twice as much energy gain.

At the end, we presented some of the achievements within UWB beamforming that has been done earlier. Later we will see that the beamformer prototype presented in this thesis will outperform all of the UWB beamformers that was found in the jungle of published results.

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3 Circuit implementation

3.1 Chapter overview

In this chapter we will develop the architecture of a transmitting beamformer. We will investigate further how a beamformer can be implemented in 90 nm CMOS technology and present a prototype system which will be used for testing.

3.2 Beamforming architecture

In this section we will develop an architecture for a timed array beamformer using impulse radio transmitters. To achieve beamforming we need an array of crude antennas. As explained in Section 2.3.1, by using this array we can exploit the effect of interference between transmitted EMW to our advantage. We will derive the architecture design based on the focal-point beamforming method.

What is important in a focal-point beamformer is that all the transmitted pulses arrive at the desired location at the same time (Fig. 3.1). This results in a greater accumulation of energy in that exact spot compared to the energy that only one transmitter could provide. In this work we refer to it as focusing the energy in a point.

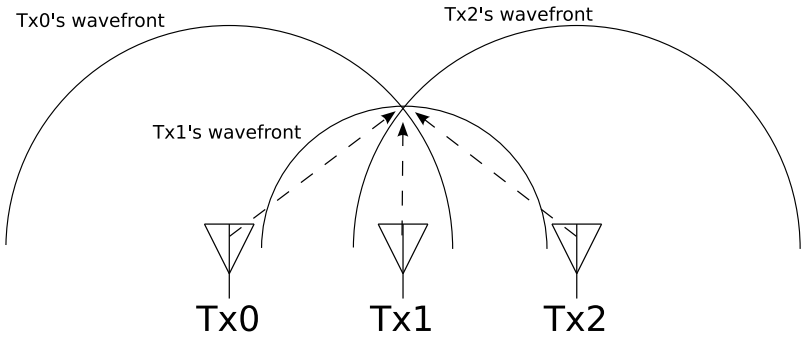

Figure 3.1: Basic idea of a time-domain focal-point beamformer.

For a UWB radar, the reflection of an object is what is interesting, therefore, energy accumulation in a controllable spot is of great interest. To obtain the objective of making the transmitted signal from each of the transmitters arrive at a certain spot in space at the same time, we only have to care about the time of which each of the antennas transmit their pulse.

The beamformer has to generate a time-delayed copy of the original signal for each of the antennas in the array. This way we can operate in time-domain and easily calculate the delay for each antenna by using simple trigonometry to find the distance and combine this with the propagation speed of the electromagnetic waves. By using programmable delay-lines for each of the transmitters, we can control the firing-sequence of the transmitters, and hence the direction of the beam.

A very important design parameter that affect the accuracy of the UWB beamformer directly is the resolution of the programmable delay line. This resolution must be as high as possible, that is, the programmable steps must be as small as possible to obtain a beamforming-resolution as high as possible. The number of antennas in the antenna array and the shape of the antenna array are two additional factors which is important to consider when designing a beamformer. Different objectives demands different antenna arrays. The design of the individual antennas is also an important parameter which limits the beamforming accuracy, therefore good antenna design is important, but in this application simple antennas are adequate. Antenna design is a large field and is out of the scope for this thesis.

3.2.1 A UWB beamforming architecture

To design a UWB time-domain beamformer we need beamformer elements, at least two, together with a control unit. A beamformer element can be built using three different components. First of all we need an antenna (Fig. 3.2(a)). Second, we need a pulse generator to generate the UWB pulse for each of the antennas (Fig. 3.2(b)). Third we need a component that can control when the pulse generator is going to generate its pulse. For this we use a programmable delay-line (Fig. 3.2(c)) which will delay a trigger pulse according to the programmed value. It is in the programmable delay the potential of the beamformer lies. Poor resolution in programmable delay results in inaccurate beamforming. Each assembly of these three different components make up one beamformer element. The control unit controls the trigger pulse and the programming of each of these elements to get a complete beamformer system (Fig. 3.3).

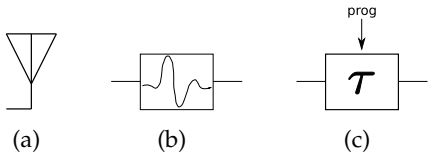

Figure 3.2: Antenna, UWB pulse generator and a programmable delay-line needed for a beamformer element

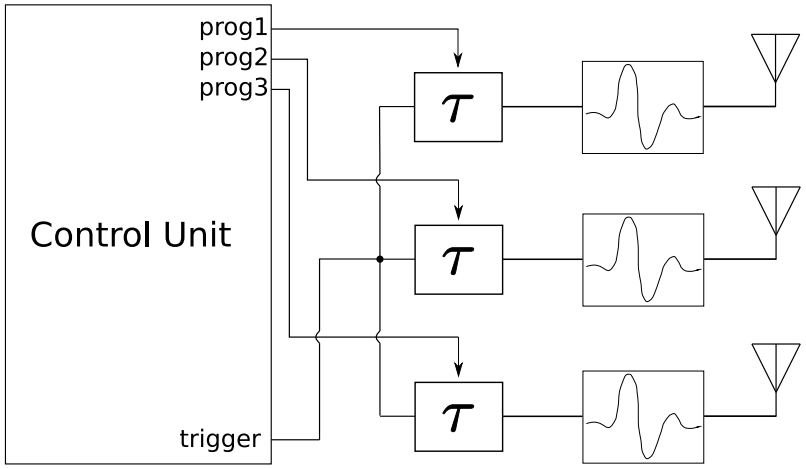

Figure 3.3: A complete beamformer system.

3.2.2 Practical UWB beamforming example

To understand the simplicity of a UWB time-domain beamformer, an example is presented. Let us look at a simple beamformer with three aligned antennas (A, B and C) placed $d = 20$ cm apart from each other. We want to focus most of the transmitted energy in focus point P which is $F = 30$ cm away from the antenna array (Fig. 3.4).

First we need to find the length from each antenna to point P, that is the distance each wavefront has to propagate. This distance is easily found using basic trigonometry:

$$\begin{aligned} |\overrightarrow{BP}| &= 30 \text{ cm} \\ |\overrightarrow{AP}| &= \sqrt{|\overrightarrow{AB}|^2 + F^2} = \sqrt{(20 \text{ cm})^2 + (30 \text{ cm})^2} = 36.056 \text{ cm} \\ |\overrightarrow{CP}| &= |\overrightarrow{AP}| = 36.056 \text{ cm} \end{aligned}$$

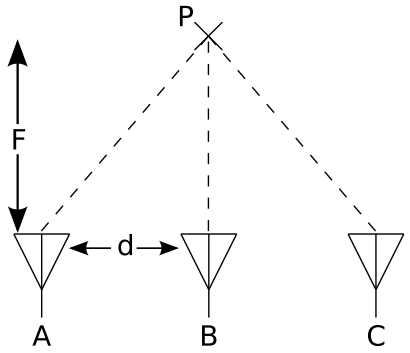

Figure 3.4: A simple beamforming example.

Now, the time it takes for each of the wavefronts to arrive at point P is calculated from the propagation speed of the wavefront, $c = 3 \cdot 10^8$ m/s.

We can find the time it takes for an EMW to propagate from the antenna to focus point P with the formula $time = \frac{distance}{velocity}$:

$$\begin{aligned} t_A &= \frac{0.36056 \text{ m}}{3 \cdot 10^8 \text{ m/s}} = 1.2019 \text{ ns} \\ t_B &= \frac{0.3 \text{ m}}{3 \cdot 10^8 \text{ m/s}} = 1.0 \text{ ns} \\ t_C &= \frac{0.36056 \text{ m}}{3 \cdot 10^8 \text{ m/s}} = 1.2019 \text{ ns} \end{aligned}$$

Then if we extract the difference between the longest propagation time and each of the rest, we get the value that the respective delay-line must be delayed by:

$$\begin{aligned} t_{max} &= max(t_A, t_B, t_C) = 1.2019 \text{ ns} \\ \tau_A &= t_{max} - t_A = 0 \text{ ps} \\ \tau_B &= t_{max} - t_B = 1.2019 \text{ ns} - 1.0 \text{ ns} = 201.9 \text{ ps} \\ \tau_C &= t_{max} - t_C = 0 \text{ ps} \end{aligned}$$

This means that antenna B has to transmit 201.9 ps after antenna A and C to arrive at the same time at point P and this is the value we program its delay-line with.

We can sum this up in a formula which gives us the time delay for the transmitter in the middle for a certain focal length F:

$$\tau = \frac{\sqrt{F^2 + d^2} - F}{c}$$

When more antennas are added or if we want a focal point with an angle, the equations get more complicated. Some examples will be presented later in Section 3.3.1 that should provide the reader with enough understanding to be able to calculate delay-values for any desired focal point.

3.3 Programmable delay-lines

In order to achieve programmable delay lines with very high resolution, careful design consideration is required. As we will see later on, what we are aiming at here is programmable delay-lines with tunability as small as 1 ps. Considering that the delay of a fast switching inverter implemented with 90 nm CMOS technology has a delay of about 15 ps, this is a demanding task. Since we only care about the time from one transmitter sends until another sends, the task gets a little less complicated.

3.3.1 Specifications

The main issue of achieving high-resolution beamforming is to design programmable time-delay elements with the high resolution and accuracy that is required. To give an understanding of the tiny magnitudes in delay-lengths that are required we can do some simple calculations.

Focal point zoom

Let us assume we have antenna spacing of $d = 10$ cm and we want a focal point one meter away $F = 1$ m. For this case we need a delay value of

$$\tau = \frac{\sqrt{F^2 + d^2} - F}{v}$$

$$= \frac{\sqrt{(1\text{ m})^2 + (10\text{ cm})^2} - 1\text{ m}}{3 \cdot 10^8\text{ m/s}}$$
$$= 16.6\text{ ps}$$

If we want to move this point 10 cm closer to our antennas, that is $F = 0.9$ m, we need a delay-value of

$$\tau = \frac{\sqrt{F^2 + d^2} - F}{v}$$
$$= \frac{\sqrt{(0.9\text{ m})^2 + (10\text{ cm})^2} - 0.9\text{ m}}{3 \cdot 10^8\text{ m/s}}$$
$$= 18.5\text{ ps}$$

This means we need a delay-line resolution of $18.5\text{ ps} - 16.6\text{ ps} = 1.9$ ps. This is a daunting task which require unorthodox design strategies.

In addition we need some larger coarse-tuning elements to account for focal points where the travel distance for the transmitted energy of two transmitters has a much larger difference.

Changing the angle

We do not only want to change the distance of the focal point, but also the angle. Let us assume we want to set our focus 1 cm to the right of the previous focal point (Fig. 3.5). We introduce F_y and change the name of F to F_x. F_y represent the distance from the point at distance F_x from the current antenna to the focal point. We now have $F_x = 0.9$ m and we remove the dependency on antenna spacing by introducing a F_y for each of the antennas. For our example, this gives us three different F_y's.

To calculate the new delay values, we first find the time it takes for a pulse to propagate from each of the antennas to the focal point:

$$t = \frac{\sqrt{{F_x}^2 + {F_y}^2}}{v}$$
$$t_A = \frac{\sqrt{(0.9\text{ m})^2 + (0.09\text{ m})^2}}{3 \cdot 10^8\text{ m/s}} = 3.0150\text{ ns}$$

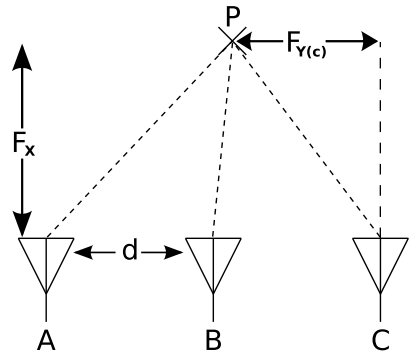

Figure 3.5: Focal point moved to the right.

$$t_B = \frac{\sqrt{(0.9\text{ m})^2 + (0.01\text{ m})^2}}{3 \cdot 10^8\text{ m/s}} = 3.0002\text{ ns}$$
$$t_C = \frac{\sqrt{(0.9\text{ m})^2 + (0.11\text{ m})^2}}{3 \cdot 10^8\text{ m/s}} = 3.0223\text{ ns}$$

Then we subtract each of the propagation values from the longest propagation-time

$$t_{max} = max(t_A, t_B, t_C) = 3.0223\text{ ns}$$
$$\tau = t_{max} - t$$

which gives us the delay value for each of the delay-lines

$$\tau_A = 3.0223\text{ ns} - 3.0150\text{ ns} = 7.3\text{ ps}$$
$$\tau_B = 3.0223\text{ ns} - 3.0002\text{ ns} = 22.1\text{ ps}$$
$$\tau_C = 3.0223\text{ ns} - 3.0223\text{ ns} = 0\text{ ps}$$

Design parameter equations

While the above example shows a practical approach to finding design parameters, some simplified equations are listed here to easily calculate the necessary design parameters for a desired design.

For focal point beamforming we have

$$t_{prop} = \frac{\sqrt{{F_x}^2 + {F_y}^2}}{v} \tag{3.1}$$

which gives the propagation time for an antenna. To find the required delay-value we find the propagation times for all the antennas and take the difference between the longest propagation time and the propagation time of the current antenna

$$\tau = t_{max} - t \tag{3.2}$$

and we have the delay-value for each of the antennas. The required resolution for the delay-line is then given by the lowest of all the delay-values. For very precise beamforming, the differences between the τ-values must also be considered. The time-resolution have to be small enough to also handle these differences.

For directional wavefront beamforming we have

$$\tau_{max} = \frac{L}{c} \times \sin\theta_{max} \tag{3.3}$$

where θ_{max} is the maximum scan angle and L is the length between the outermost antennas. And the required time resolution is found by

$$\tau_{res} = \frac{d}{c} \times \sin\theta_{min} \tag{3.4}$$

where $\sin\theta_{min}$ is the scanning resolution and d is the antenna spacing.

3.3.2 Fine tuning

To calculate the desired resolution of the delay-line we need to consider the spacing between each antenna and the beamformer range we want. The prototype beamformer is going to have near-field beamformer abilities. Eight transmitters will be used. Spacing between each of the antennas will be approximately 10 cm. We want the beamformer to have a zooming resolution of approximately 10 cm around 1 m away from the antennas. This resolution will of course improve when the focal point is closer to the antennas. As shown in Section 3.3.1, this requires a resolution of 1.9 ps.

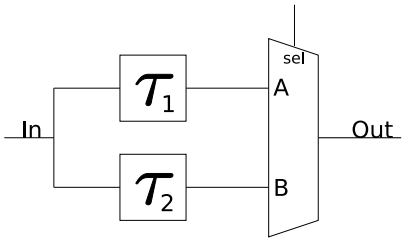

Figure 3.6: Tuning using a MUX.

In addition, we want a scanning resolution of 0.2° and a maximum scan angle of 70° for directional wavefronts. To find the minimum resolution required for a directional wavefront with scanning resolution of 0.2° we use Eq. 3.4.

$$\begin{aligned} \tau_{res} &= \frac{0.1 \text{ m}}{3 \cdot 10^8 \text{ m/s}} \times \sin 0.2^\circ \\ \tau_{res} &= 1.16 \text{ ps} \end{aligned}$$

Then we use Eq. 3.3 to find required total programmable delay

$$\begin{aligned} \tau_{max} &= \frac{0.7 \text{ m}}{3 \cdot 10^8 \text{ m/s}} \times \sin 70^\circ \\ \tau_{max} &= 2.19 \text{ ns} \end{aligned}$$

To meet the desired resolution of 1.16 ps, a HRPDL has to be designed. There are several ways to accomplish a programmable delay-line with very high resolution. In this section, a few alternatives will be presented.

Alternative design strategies

Tuned Inverter Comparison This design method consists of using two delay elements with different delay-value. A delay-element could be two subsequent inverters. Then by increasing the size of the inverters in one of the delay-elements and connecting each of them to an input on a Multiplexer (MUX) we get a programmable tuning element (Fig. 3.6). This way we can create very small time-delays by making the size of one of them only slightly different from the other one.

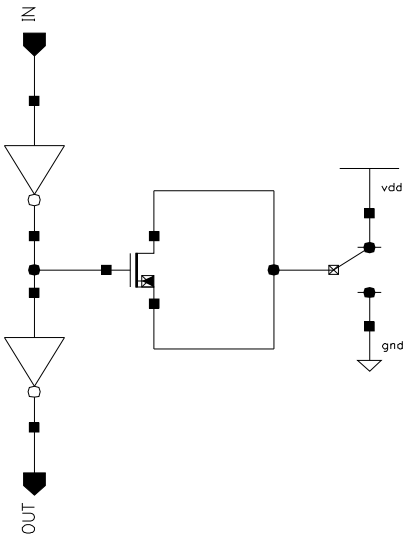

Figure 3.7: Tuning using capacitive load.

Capacitive tuning This method requires the use of an inverter-chain. By adding a transistor and connecting its gate between each inverter in the inverter chain, extra capacitive load will be added to the inverters which will have an impact on the total delay. Because the transistor is a non-linear device, we can vary the voltage on the source, drain and bulk and thereby change the capacitance on the gate (Fig. 3.7), hence the delay of the inverter chain will change.

Back-gate tuning A CMOS transistor has connections to the bulk/substrate which enables us to set the bulk/substrate voltage. This connection is called the *back-gate*. In normal operation the back-gate is connected to V_{DD} for PMOS transistors or GND for NMOS transistors. By changing the voltage on the back-gate (Fig. 3.8) of one of the transistors in an inverter, the threshold-voltage of that inverter will change which makes the delay of the inverter change (Fig. 3.9). This effect is typically called *body effect* [John 97]. Applying a voltage on the back-gate is often referred to as body-biasing [Ande 07].

In fine-pitch CMOS processes, the effect of body-biasing is reduced [Arni 05], which in our case is used as an advantage to enable very precise tuning. When this technique is used on one of the transistors in an inverter, the inverter becomes an inverting variable delay-element. The voltage variation on the back-gate can determine the size of the programmable delay-value for the delay-element.

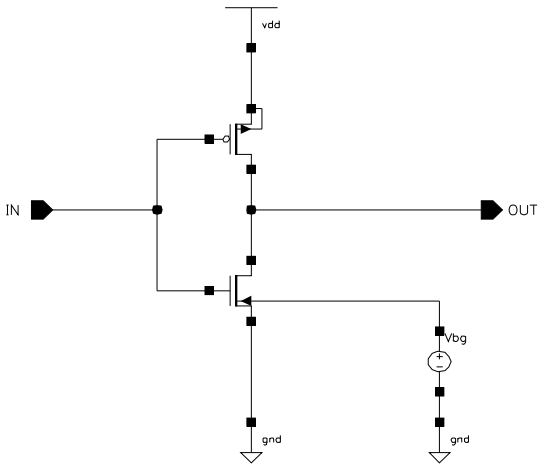

Figure 3.8: Body-biasing the NMOS transistor in an inverter.

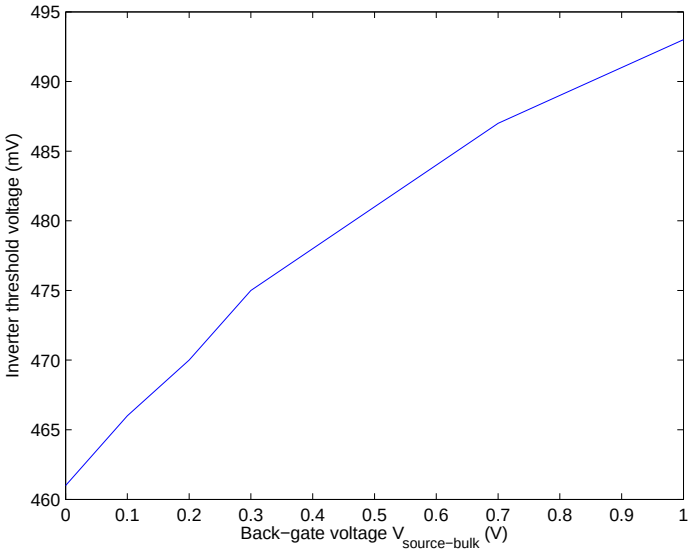

Figure 3.9: The effect of body-biasing a PMOS transistor in an inverter.

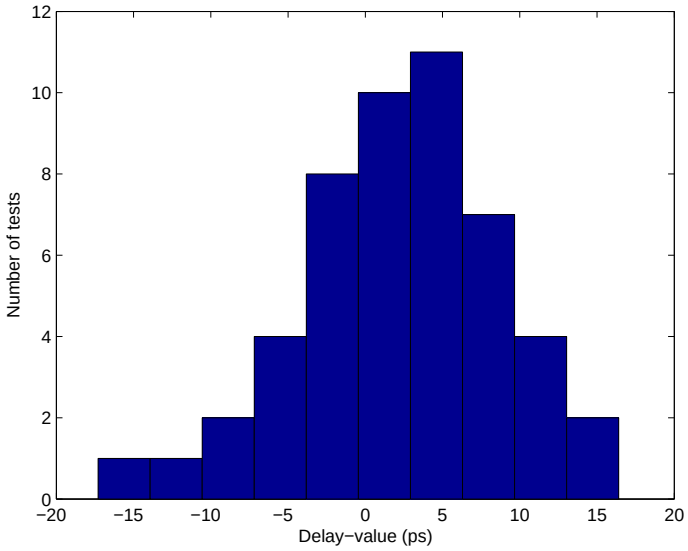

Figure 3.10: Probability distribution of design using a MUX.

Simulations

For each of the alternatives, an example circuit was designed to test the performance. The three different alternatives were simulated with Monte Carlo analysis in Cadence to identify amount of mismatch.

For the MUX alternative, an example circuit with a delay-value of approximately 2 ps was designed and simulated in Cadence. By running a Monte Carlo mismatch analysis, the design proved to be very vulnerable to mismatch (Fig. 3.10). These values are not very promising for a high-resolution delay-line.

An example circuit for the capacitive load alternative was designed with a programmable value of approximately 1 ps. To increase or decrease the programmable value of this type of design, we can increase or decrease the width of the transistor. A Monte Carlo analysis on mismatch proved the reliability of this design (Fig. 3.11) to be much more resistant to mismatch errors than the tuned inverter comparison design. Still, this is not adequate for the desired accuracy of a delay-element.

A test-circuit for the back-gate alternative was designed in Cadence with approximately 1 ps of programmable delay. By looking at the probability distribution of this design approach (Fig. 3.12), we can see that this design is superior to the others when it comes to mismatch resistance.

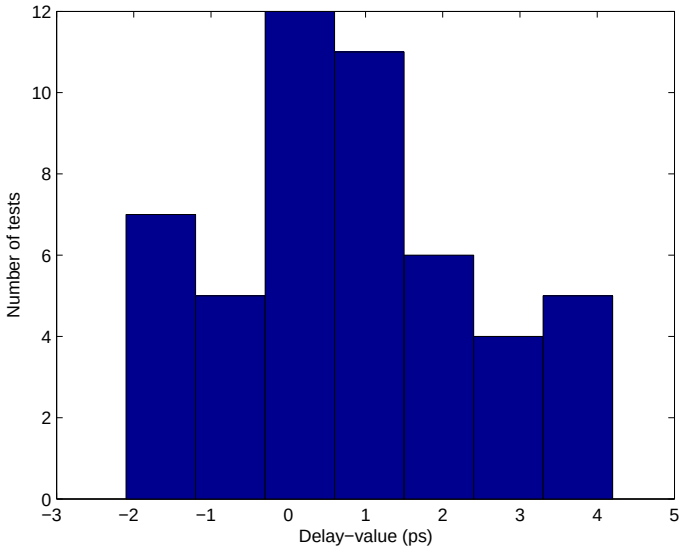

Figure 3.11: Probability distribution of the design using capacitive load.

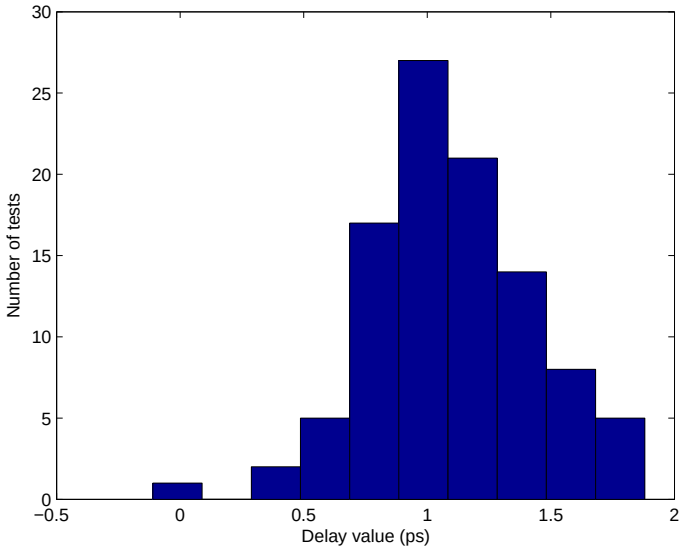

Figure 3.12: Probability distribution of the back-gate tuning design.

Table 3.1: Simulation results for the three alternatives

Circuit	Mean (μ)	Std (σ)	Within 1σ	Within 2σ
MUX	2.2 ps	6.6 ps	72%	92%
CAP	0.79 ps	1.65 ps	62%	92%
Back-gate	1.1 ps	0.3 ps	74%	94%

Choosing a design alternative

The circuit chosen for the prototype chip should be resistant against mismatch, consume very little energy while idle, it should be easily implemented on a microchip and it should be able to work with high pulse repetition rates.

The results from the simulations are summed up in table 3.1. The results show that both the alternative using a MUX and the capacitive tuning approach has relatively large mismatch errors compared to the back-gate tuning approach. This is due to the fact that the delay-value for capacitive tuning and MUX are very much dependent upon transistor-sizes and a small variation in size will cause a relatively large variation in delay-value. The delay-value for the back-gate alternative is more dependent on the amount of doping which is a fixed value.

Mismatch errors will affect the overall accuracy of the delay-line and should be reduced to a minimum. The table shows clearly that the back-gate tuning alternative is the best. It is much better than the other designs and a good choice for designing a high-accuracy delay-line with high resolution. Therefore the alternative using body-biasing is chosen for the prototype chip.

Design considerations

NMOS vs PMOS tuning Simulations with back-gate tuning on both an NMOS transistor and a PMOS transistor shows that the size of the programmable delay is about the same in both cases. For an inverter with transistor widths $W_P = 0.24$ µm and $W_N = 0.12$ µm and both lengths $L = 0.12$ µm, the maximum programmable delay value, that is the difference in delay with a back-gate voltage of $V_{bg} = 1$ V and $V_{bg} = 0$ V, is approximately 5 ps for either case.

To change the back-gate voltage of a single transistor, the substrate of the transistor must be isolated. For the current technology, a cross section of a standard NMOS transistor and a standard PMOS transistor is shown in Fig. 3.13. As we can see there is two layers of substrate, p-substrate and n-substrate.

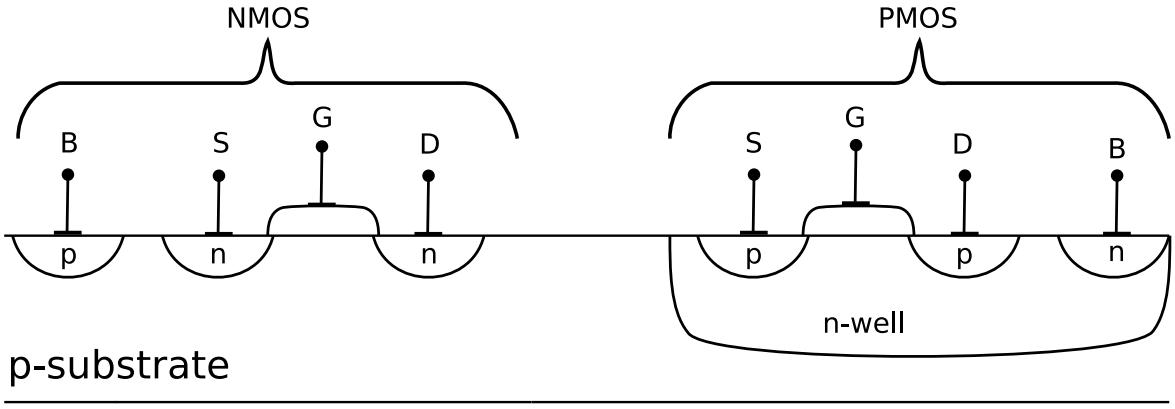

Figure 3.13: A cross-section of two standard MOS transistors.

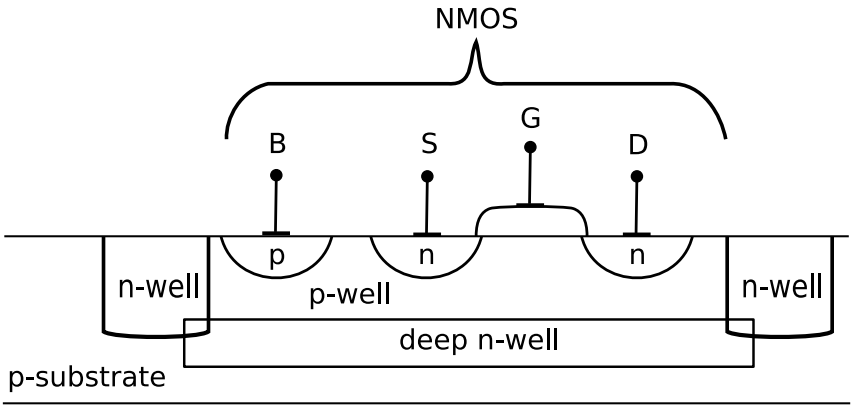

Figure 3.14: Cross-section of an isolated NMOS transistor.

For NMOS transistors in the current CMOS technology, isolation must be done by using a deep n-well under the transistor itself, then implementing an n-well around the transistor so that the n-well merges with the deep n-well and makes a ´´bowl" with a p-well for the transistor (Fig. 3.14) [Chew 02].

Isolation of a PMOS transistor is done by simply making sure each transistor is placed in a separate n-well. Separate n-wells are slightly easier to implement in a design than deep n-wells, therefore, the PMOS transistor is used as the tunable transistor in the design.

Schematics To reduce the power consumption, a diode-coupled transistor is connected from the back-gate of the PMOS transistor to V_{DD}. An inverter is used to act

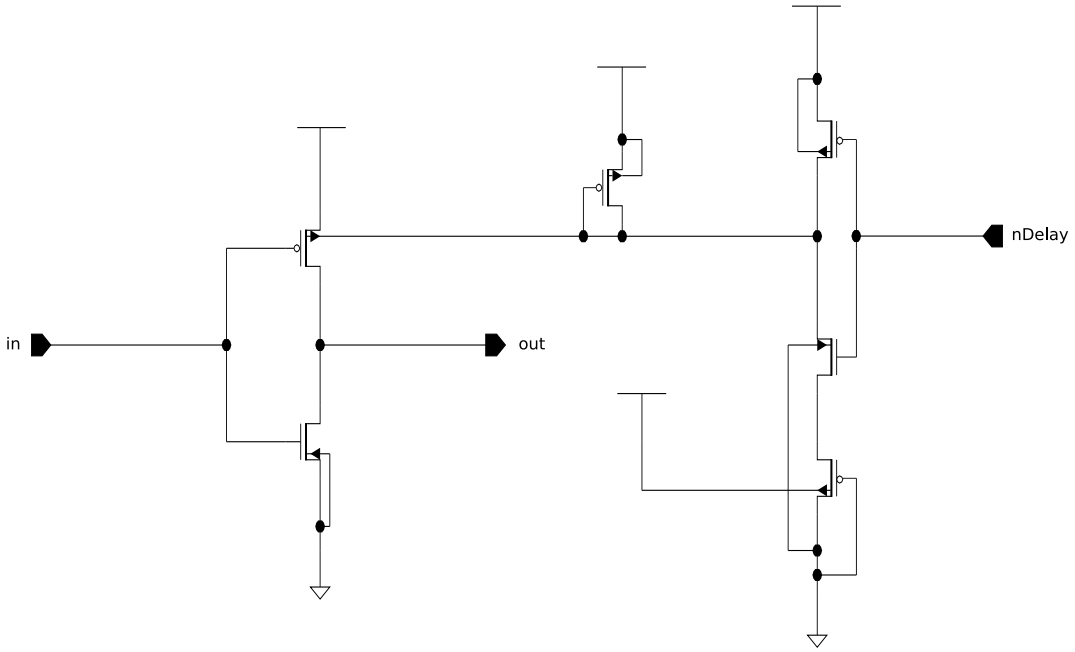

Figure 3.15: Schematics of the tunable part of one element in the HRPDL.

as a simple inverting buffer and pulls the voltage between two states.

A low level on the input of the back-gate inverter sets the back-gate voltage to 1 V. This is the standard operating level for a PMOS transistor. A high level on the input of the back-gate inverter pulls the back-gate voltage down to 600 mV. The voltage drop on the back-gate makes the inverter switch about 1 ps faster.

The delay element can now be programmed by setting the input of the inverter to either a logical “1” or “0”. A high input level turns the delay OFF and a low input level turns the delay ON. So we have a delay-element with active low input.

The schematic (Fig. 3.15) for the tunable part of one element of the HRPDL shows an energy efficient, fast and area effective programmable delay element, with programmability close to 1 ps.

The pulse generator is edge-triggered, which means it only cares about transitions from “low” to “high”. A fast switching inverter is used before the tuned-inverter to restore the fast-switching signal. The fast switching inverter combined with the tunable inverter makes up one delay-element in the complete fine-tuning delay-line as shown in Fig. 3.16.

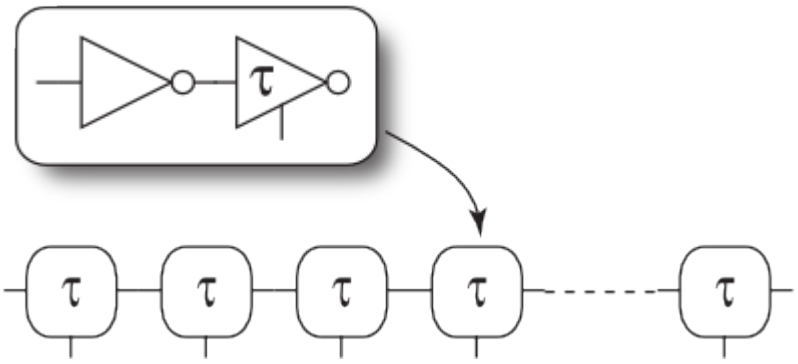

Figure 3.16: The components of the HRPDL. Based on a figure courtesy of Tor Sverre "Bassen" Lande.

The layout of the fine-tuning element is attached in Appendix B.

3.3.3 Coarse-tuning

For the cases where larger delay-values are required, a coarse-tune delay-line must be added. Both for beamforming at very close-range and for compensating for deviations in the absolute delay-line value, there is a need for longer delay-values. A tapped delay-line of consecutive delay-elements designed by Håkon A. Hjortland was used for the prototype chip. The delay-elements, made of dual-inverters, are lined up in a chain with tapping between each element out to a MUX. The MUX is controlled by six bits and enables us to set the delay-line by choosing between 64 different tapped outputs from the chain of delay-elements. The unit delay of the dual inverters are simulated to be $\tau \approx 35$ ps which gives us a programming range of 0 to 63×35 ps ≈ 2.2 ns.

3.3.4 Complete delay-line

We combine the 64 step (0-63) coarse-tuning delay-line with the fine-tuning delay-line of 64 individually controllable delay-elements. The complete delay-line consists of a delay-line with maximum programmability of approximately 2.2 ns and a resolution of approximately 1 ps. A block-diagram of a complete delay-line is shown in Fig. 3.17

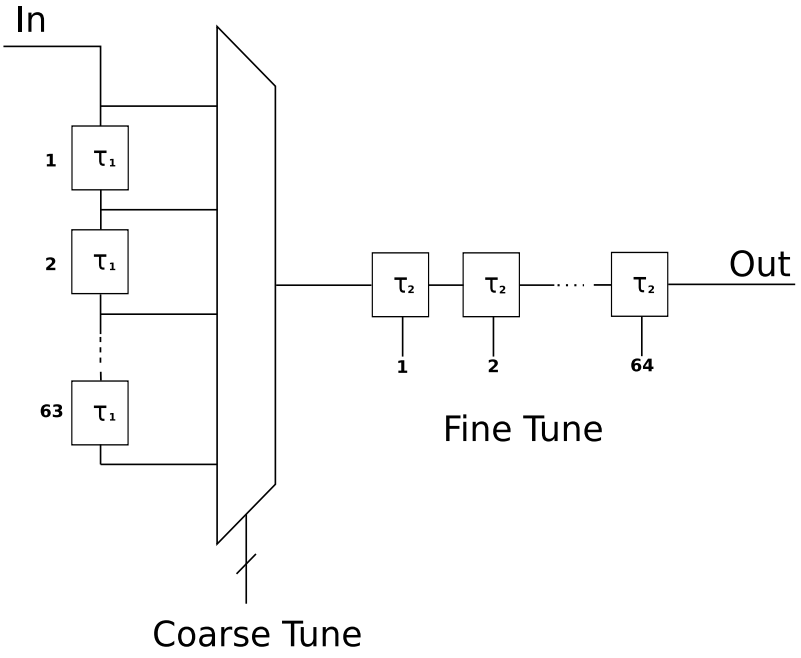

Figure 3.17: Block diagram showing the complete delay-line with coarse and fine tuning. Based on figure courtesy of Håkon A. Hjortland.

3.4 System overview

3.4.1 Beamformer element

One beamformer element consists of one coarse-tuning delay-line, one fine-tuning delay-line followed by a dual-slope Gaussian pulse transmitter. Eight of these beamformer elements were used in the prototype chip. The pulse generators are designed by Novelda AS and will not be covered in this thesis. They generate a dual-slope Gaussian shaped pulse using only a handful of components.

3.4.2 Programming control

For controlling the coarse-tune delay-line, one 8-bits register is used for each delay-line. Only 6 of the bits are in use since it is a 64 step delay-line. For controlling the fine-tune component, one 64-bits register is used for each delay-line. Each of the 64 bits controls one single fine-tuning delay-element directly and thus gives us the freedom to look at each of the delay-elements individually.

Table 3.2: Decoding table for the SPI

Bit #	Name	Description
15 (msb)	Execute	Always 1
14	PulseGenS2	Select Tx(0:7)
13	PulseGenS1	
12	PulseGenS0	
11	Coarse/nFine Select	Select Coarse or Fine
10	FineAddress2	Address in Fine-register (0:7)
9	FineAddress1	
8	FineAddress0	
7	Data7	Value of selected register
6	Data6	
5	Data5	
4	Data4	
3	Data3	
2	Data2	
1	Data1	
0 (lsb)	Data0	

A Serial Peripheral Interface Bus (SPI) scheme designed by Håkon A. Hjortland is used as an interface between the internal registers and the outside world.

Serial Peripheral Interface Bus (SPI)

The SPI component is the interface between the internal microchip and the outside world. Through this component the value of the delay-lines are controlled.

SPI is a synchronous serial communication link between a master and one or more slaves. The master initiates communication by setting the Slave Select (SS) signal for the current slave active and by creating a clock signal on the Serial Clock (SCK) line. Then the master transfers data through the Master Out Slave In (MOSI) line and receives data from the slave through the Master In Slave Out (MISO) line. Data is transferred on the rising or falling edge of the SCK line depending on the current settings.

The SPI circuit used in the prototype chip can only operate as a slave component. It is dependent on a master to activate its SS signal and provide a clock input on the SCK line. For each transfer, a master transfers 2 bytes of data to the SPI circuit. The 16 bits are then decoded by the SPI-slave using a predetermined coding system as shown in Table 3.2.

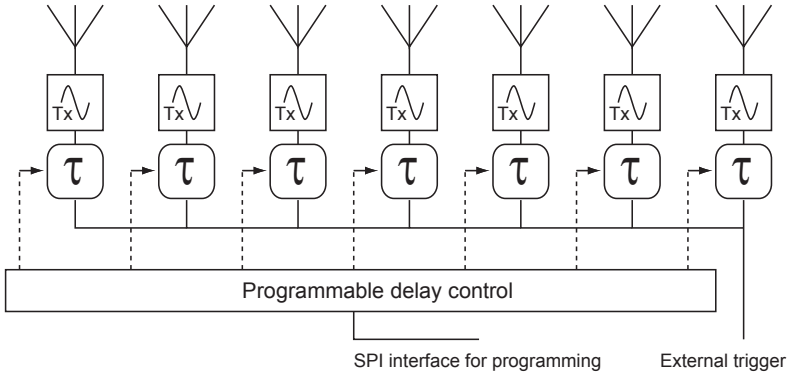

Figure 3.18: A programmable beamformer system. Courtesy of Tor Sverre "Bassen" Lande.

In the chip there are eight 8-bit registers and eight 64-bit registers. The 8-bit registers can be accessed by setting the correct value on the "Pulse Generator Select" (PulseGenS) bits and setting the Coarse/nFine signal high. Each byte in the 64-bit registers can be accessed by setting the correct PulseGenS bit-values, setting Coarse/nFine low and by setting the FineAddress bits to the desired byte (0-7).

3.4.3 Layout

In Fig. 3.18 a beamformer block-diagram with 7 beamformer elements is shown. This block-diagram shows the basic elements of which the prototype beamformer was built.

Programming of the delay-lines is through SPI. Through the SPI, the registers can be set to a delay value. The registers are connected to the delay-lines and controls them directly. Each complete delay-line consist of a coarse tune delay line with 64 tuning steps, then followed by a fine-tune delay line with 64 single directly controllable delay-elements. 6 bits from a 8-bit register controls the value of the coarse tune delay-line and a 64-bit register controls each of the delay elements in the fine-tune delay line. Eight UWB pulse generators are used, each with a complete delay-line in front.

In Fig. 3.19 the complete layout of the chip is shown.

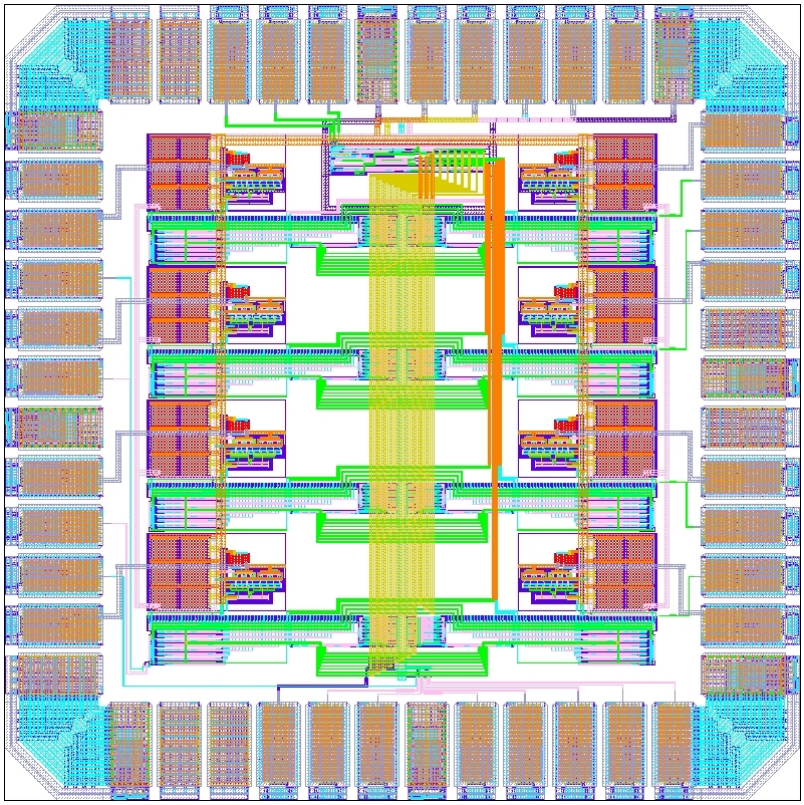

Figure 3.19: The complete layout of the chip

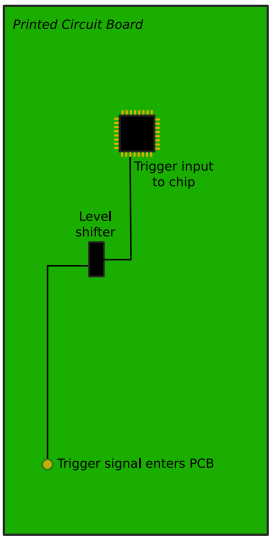

Figure 3.20: The first part of the signal-path of the trigger-signal.

3.4.4 Signal-path consideration

The signal-path through the complete system must be considered with care. Impedances, resistances and capacitances are introduced along the path. The length, width and placement of the signal-path is factors that affect the resulting performance of the path. When we are working with delay-values in the picosecond range, small variations between the different signal paths can introduce relatively large performance-variations from transmitter to transmitter.

The rising edge of the trigger-signal arrives at the PCB from an external source of some kind. It is usually a 3.3 V - 5 V signal that needs to be level-shifted to a 1 V signal. This means we need to route a signal-path from the external input on the PCB to a level-shifter. Then we need a signal-path from the level-shifter in to the trigger-input pin on the chip. The first part of the signal-path is shown in Fig. 3.20.

From the input pin, the signal will pass through a bond-wire onto a pad on the actual silicon surface (Fig. 3.21).

Now the trigger-signal is routed using a metal-layer from the internal pad into a buffer circuit. From the buffer output, eight paths of metal-layer are routed to the input of each of the eight delay-lines. The signal on each delay-line passes through the delay-line and arrives at the input of the UWB pulse generator. When the pulse generator input switches from low to high it produces a dual-slop Gaussian pulse on its output. The resulting pulse must now be routed out of the chip so that it can be transmitted

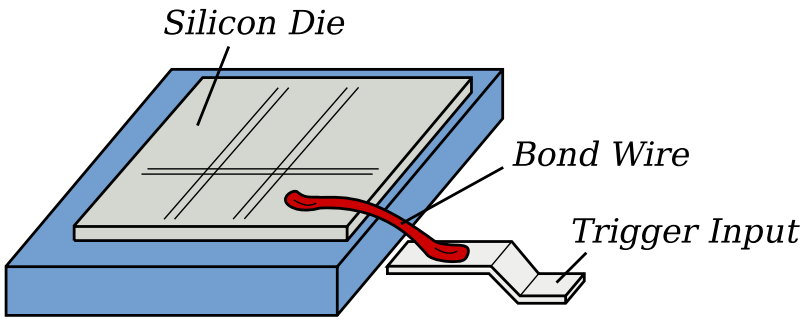

Figure 3.21: A metal wire connects the pin to the chip die.

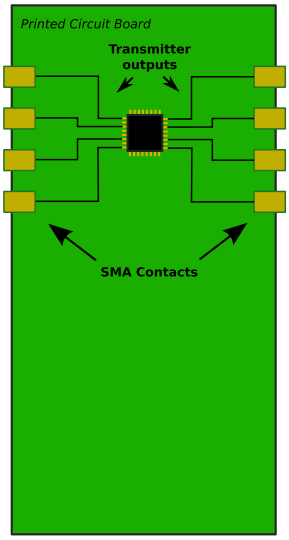

Figure 3.22: Signal paths from the chip outputs.

through an antenna.

A path made of metal-layer transports the pulse to the internal pad, where a bond-wire is ready to transmit it to the output pin from the chip. Now the pulse is outside the chip and continues through a routed path that will transport the pulse to a suited contact for antenna connection (Fig. 3.22). A cable might be attached to this contact before the signal is allowed to radiate into space through an antenna. This is a long way for a signal to be transported and there are a lot of things that can make the path for one of the transmitted signals to be slightly different from the others.

The signal-path from the point where the external trigger arrives at the PCB to where it is divided up into eight different paths is not very critical. As long as it can transport a

nice rising edge, the delay it introduces is not significant because all of the transmitters will receive the exact same amount of delay. From the point where the path is divided into eight different paths, more consideration must be taken. Any differences in path-length will introduce a difference in total delay-time between the paths.

A key point that makes this task a little less difficult is that as long as the introduced delay-variations between delay-lines is small enough, they can be eliminated by calibration using the programmable delay-lines. After all, the absolute delay-value of a path is just a constant.

3.4.5 System Example

For a complete system, a controller chip can be used to handle communication with the beamformer chip through SPI. The controller chip can then provide a more high-level communication protocol to communicate with more sophisticated devices, like a computer or an oscilloscope. For the prototype chip, a PCB was designed with a socket for a plug-in microcontroller module designed by Olimex to be able to control the chip from the computer.

3.5 Summary

In this chapter we have looked at a simple beamformer architecture and practical examples of how to calculate the required time-resolution and minimum total programmable delay of the delay-line. A few alternatives for a HRPDL design was presented and one design was chosen to implement in the prototype beamformer. The design's simulated behaviour shows a HRPDL with 1.1 ps resolution and a coarse-tune delay-line with up to 2.2 ns of programmability.

By using Eq. 3.4 and Eq. 3.3 we get two equations that will gives us maximum scanning angle θ_{max} and the scanning resolution θ_{min} for a directional wavefront given our delay-line resolution and maximum programmable value. With 8 antennas we have

$$\begin{aligned} \theta_{max} &= \arcsin\left(\frac{c \times \tau_{max}}{L}\right) \\ \theta_{max} &= \arcsin\left(\frac{3 \cdot 10^8 \text{ m/s} \times 2.2 \text{ ns}}{0.7 \text{ m}}\right) \\ \theta_{max} &= 70.5^\circ \end{aligned}$$

$$\begin{aligned}\theta_{min} &= \arcsin\left(\frac{c \times \tau_{min}}{d}\right) \\ \theta_{min} &= \arcsin\left(\frac{3 \cdot 10^8 \text{ m/s} \times 1.1 \text{ ps}}{0.1 \text{ m}}\right) \\ \theta_{min} &= 0.19^\circ\end{aligned}$$

for an antenna spacing of $d = 10$ cm.

By using an antenna spacing of 1 cm, the proposed design gives a scanning resolution of approximately 2° and full angle scanning.

The simulated results are very good compared to other published results. In the following chapter the circuit has been implemented in 90 nm CMOS technology and will be measured to investigate the actual behaviour.

-

4 Measurements

4.1 Chapter overview

Simulations show that the fine-tune delay elements can be programmed with a resolution of approximately 1 ps. This is an extremely short period of time which is very susceptible to noise. In this chapter we will evaluate the performance of the delay-lines in the real world by measurements. We will present measurement results showing the resolution of the coarse-tune and the fine-tune delay-lines. We will look at sources of noise that affect the resolution of the delay-line and how these problems may be overcome to preserve the high accuracy of the delay-line At the end of the chapter, measurements of the prototype beamformer system in action will be presented.

4.2 Time-delay measurements

4.2.1 Measurement setup

The complete setup for measuring time-delays (Fig. 4.1) have been carefully designed to introduce as little noise as possible and measure time as accurately as possible.

The prototype chip is soldered on a PCB. The PCB consists of a connector for a microcontroller module. This module controls the value of the delay-line registers in the chip through SPI. The microcontroller module can be controlled by a computer using Universal Serial Bus (USB). Each of the transmitter outputs are connected to a SubMiniature version A (SMA) connector. An SMA connector offer excellent electrical performance from Direct Current (DC) to 18 GHz. Four of the transmitters in the chip has been equipped with a buffered test-point after the delay-line and before the pulse-generator. These test-points are also connected to four SMA connectors. The PCB is shown in Fig. 4.2.

To test an output, a high-performance cable is connected between the desired output and an oscilloscope. The cables introduce some delay to the signals, therefore it is important that the cables are of the same length when more outputs are to be compared

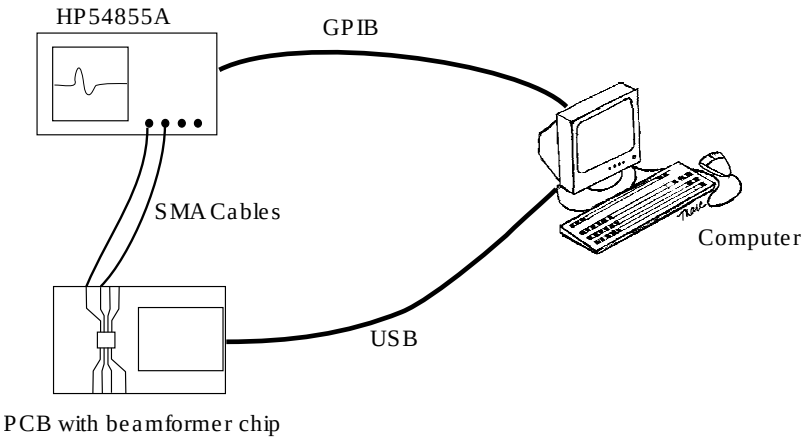

Figure 4.1: Measurement setup

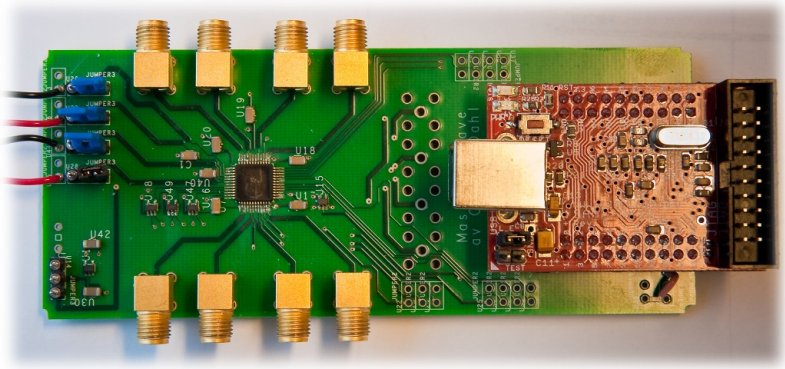

Figure 4.2: PCB with chip and microcontroller module. (SMA contacts for test-points not added)

so that the delay introduced by the cables are as similar as possible. To be able to measure the delay-lines accurately we need very accurate equipment. The "Agilent 54855A Infiniium Oscilloscope" in the setup states in its specification sheet [Tech 05] that its delta-time accuracy between two edges on a single channel is as low as 70 fs. Our experience shows that the oscilloscope provides a time-resolution of approximately 3 ps. By using several different test methods, averaging and interpolation, we are able to determine the time step of each of the elements to an acceptable accuracy.

The measurements are controlled by MATLAB scripts on a computer. The scripts define delay-line values by communication with the microcontroller module and reads out measurement data from the oscilloscope using General Purpose Interface Bus (GPIB).

Software

Several pieces of software was written for the measurement phase. Basically three types of software was written:

- Firmware
- Matlab-scripts
- Windows software (MS Visual C++)

Firmware For the microcontroller to work as intended it needs firmware. Modifications of an already existing firmware (by Håkon A. Hjortland) was done in cooperation with Håkon A. Hjortland to customize the firmware for easy control of the prototype chip. Functions for setting the value of each register was implemented so that the registers could easily be changed by simple text-commands sent via the USB communications device class. This means the microcontroller shows up as a serial port on the computer it is connected to, and communication between the computer and the microcontroller module happens through standard serial port communication.

Matlab-scripts For measurements and some simulations, Matlab was used for data collection to easily plot and do calculations. Measurements was done using an oscilloscope and data was transmitted to the computer using GPIB. Strings of text containing commands and parameters are sent to the oscilloscope and responses containing the requested data are returned as text strings. Commands and parameters in strings of text are also sent to the microcontroller module to control the delay-values.

A simple script for measuring the amplitude of a signal on the oscilloscope channel 3:

```
% This example assumes that the two commands:
%
% -GPIB_Write(<command string>, <channel>)
% -GPIB_Read(<channel>)
%
% are properly defined


%Set correct channel for instrument:
GPIB_chan = 7;

%Create a string containing command and parameters
command_string = ':MEAS:VAMP? CHAN3;'

%Send text string:
GPIB_Write(command_string, GPIB_chan);

%Read response string:
meas_value = GPIB_Read(GPIB_chan);

%Convert string to number:
meas_amp = str2num(meas_value);
```

A simple script for setting the value of all the coarse delay-lines to zero:

```
%This script assumes a unix-like system
%where a send_ascii script is located
%in the current folder.
%
%The send_ascii script simply takes its
%arguments and transmits them over a
%serial port


%Path to script for sending data to Olimex:
cmd = './send_ascii';

%Reset all coarse delay-lines:
for tx = 0 : 7
  %Create a command string for the microcontroller:
  reset_value = 0;
  param = sprintf('"coarse %d, %d"', tx, reset_value);

  %Combine send_ascii path with command string
  unixcmd_string = [cmd,' ',param];

  %Execute unix-command:
  unix(unixcmd_string);
end
```

Windows software A program with a Graphical User Interface (GUI) was developed for easy manual tuning of the delay-lines and simple control of the focal point of the beamformer. Because of small variations in the signal-path both internal on the chip and external on the PCB and through cables, the absolute delay of the delay-lines will never be exactly equal. But by careful design-consideration, the variations can be reduced to such a small amount that it can be compensated for by tuning the delay-lines.

The GUI also includes an intuitive way of setting the focal point by just clicking in a two-dimensional grid at the desired point. The delay-value of each step of both the coarse and fine tune delay-lines can be set and the speed of which the EMW are traveling can be set.

To be able to study in two dimensions how the EMW are theoretically behaving if transmitted from an omnidirectional antenna, a beamformer visualization program was made. The program visualizes where wavefronts add up and gives us the possibility to study the wavefront positions at any given time. This program was very handy in verifying that the calculations made from other programs gave the expected results.

Screenshots are provided in Appendix C.

4.2.2 Fine time-delay tuning measurements

The HRPDL is the most crucial part in the circuit. This delay-line determines the smallest available time-step between two transmitters sending. The smaller this time-step is, the higher the potential resolution of the beamforming is.

Working with time differences in the picosecond range is a demanding task. Light only travels 0.3 mm during 1 ps. A fast-switching inverter in the 90 nm process introduces a time delay about 15 times larger. By combining high-performance measurement equipment and clever design using standard CMOS technology we are able to produce cutting edge results that will make high-resolution beamforming possible.

Results showing that when a pulse-generator triggers it will affect the delay-value of other delay-lines, was found and will be introduced later in 4.2.4. Therefore, to test one of the HRPDL as accurately as possible, we have to ensure that the transmitter-under-test is the first transmitter to be triggered. This is to ensure that the delay-line is not affected by any of the other transmitters. To get the position of the output-pulse, a reference trigger-pulse for the oscilloscope is needed. This reference pulse should ideally not be any of the other output-pulses to ensure uninterfered operation. Because the PCB was designed without any high-performance output connectors for the trigger, there was no way of getting an accurate trigger-signal to the oscilloscope. Therefore, one of the other outputs is used as a reference.

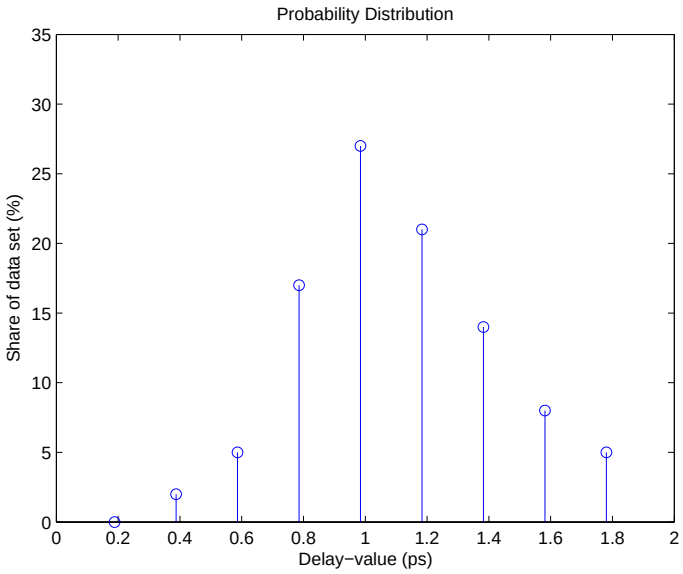

Figure 4.3: Monte Carlo simulations of mismatch with 100 runs

The measured delay-value is obtained by using an oscilloscope function called *TMAX*. This function finds the maximum amplitude of the chosen channel on the oscilloscope screen, then returns the time of which the maximum amplitude was found. By setting the delay-value of a delay-line to zero, we can use TMAX to find the offset value. Now we can set the delay-line to whatever value we want to look at and use TMAX and subtract the offset value to find the time-value that corresponds to the value of the delay-line register.

Simulations

The accuracy of a delay-line is determined by how much the delay-line is affected by mismatch throughout the chip-area. Equally designed transistors on the same chip can sometimes behave differently from each other. This problem is referred to as mismatch. To simulate this effect we perform a Monte Carlo simulation with 100 runs in Cadence. This way we can get a sense of how accurate the delay-line will be when implemented on a chip.

By looking at the probability distribution (Fig. 4.3), we can see that the mean value is somewhere around 1 ps. Calculations show that the mean value is $\mu = 1.1$ ps with a standard deviation of $\sigma = 0.3$ ps. 74 % of the times, the value is within one σ. 94 % are within 2σ.

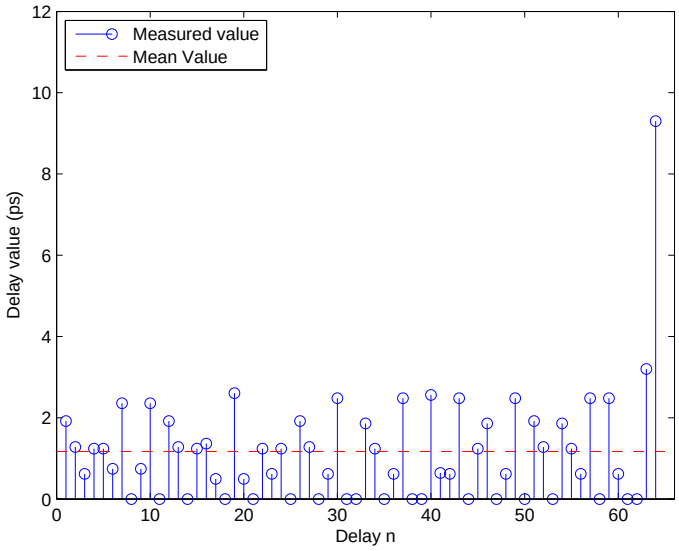

Figure 4.4: Measurement of each element in a HRPDL

Measurements of single delay-elements

As a first-approach to determining the value of each time-step of the HRPDL, all the elements of one HRPDL is measured one-by-one. This measurement reveals the time-resolution of the oscilloscope to be $\Delta t_{osc} \approx 3$ ps. Since each delay-element is expected to be $\tau \approx 1.1$ ps, we have to take an average-approach to find the different values. In the first test, each delay-value is measured 5 times and the average value is recorded (Fig. 4.4). The test results say that each delay element has a value somewhere between $\tau \approx 0$ ps and $\tau \approx 3$ ps, except the last element in the delay-line. The last element has a higher value because this element is connected directly to the signal generator and thus have greater load. A test where more than one element is measured at a time must be conducted in order to give a more accurate picture of the value of each element.

In the following test, the last delay-element will be omitted.

Measurements of several delay-elements at a time

Since the resolution of the oscilloscope is $\Delta t_{osc} \approx 3$ ps, we need to test several delay elements together to get a more accurate approximation to each delay-value. By randomly selecting 40 delay-elements and measuring their total value several times, we

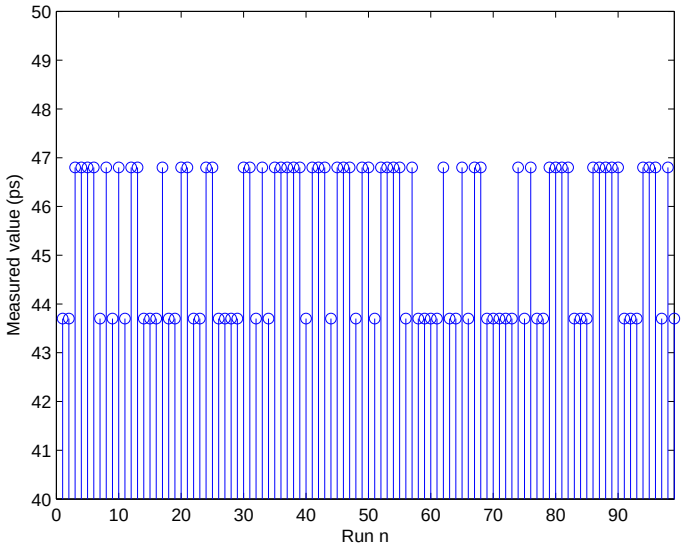

Figure 4.5: Recorded values for each of the 99 runs on Tx6

can estimate the expected value of one delay-element. This test was repeated 99 times per delay-line, each time a new random selection of delay-elements were chosen to get reliable results.

For the different runs in each delay-line, the results showed only two or three different values. The recorded values from measuring Tx6 is shown in Fig. 4.5.

The average value and the highest measured deviation relative to the average value was extracted for each of the delay-line measurements and is presented in Table 4.1. The results show that the individual delay elements are almost identical. The highest deviation from the average value measured for each delay-line corresponds approximately to the time-resolution of the oscilloscope. There is reason to believe that the delay-elements are actually more accurate than measured because of inadequate measuring equipment. To get the expected delay-value of one element in each delay-line, the measured time is divided by 40. The results are extremely good and implies that high-resolution beamforming should be achievable.

Comparing the measured results with the simulated performance shows that the measured behaviour is not very far from simulated behaviour.

Table 4.1: Measurements of all the delay-lines on a chip

Tx	# Runs	Avg	Peak deviation	Avg/40
0	99	53.8 ps	2.4 ps	1.3 ps
1	99	44.0 ps	2.8 ps	1.1 ps
2	99	59.6 ps	2.9 ps	1.5 ps
3	99	53.1 ps	3.1 ps	1.3 ps
4	99	56.5 ps	2.9 ps	1.4 ps
5	99	45.4 ps	1.7 ps	1.1 ps
6	99	58.5 ps	2.1 ps	1.5 ps
7	99	47.0 ps	3.3 ps	1.2 ps
Avg	792	52.2 ps	2.7 ps	1.3 ps

4.2.3 Coarse time-delay tuning measurements

The accuracy of the coarse-tune delay-line is an important parameter to be aware of. If the accuracy is bad, it can reduce the overall performance of the beamforming significantly. It is not very useful to change the delay value of a delay-line with 1 ps if we do not know if the current value of the delay-line is 50 ps or 80 ps.

If we can identify the value of each steps and the variations are not too large, the delay-lines can be calibrated to remove the differences. After all, these are just constants.

Simulations

To find the expected amount of mismatch, a Monte Carlo simulation on the the coarse delay-line was performed. The circuit was simulated 87 times.

What we see measured (Fig. 4.6) is the absolute time it takes for a trigger pulse to travel through the complete coarse-tune delay-line for a selected programmed value. The information we extract from this is the expected standard deviation for a step in the coarse-tune delay-line. Calculations show that the expected standard deviation is $\sigma \approx 3.5$ ps. In (Fig. 4.7) we can see the probability distribution of the delay-value. 68 % of the simulations are within one σ. 99 % are within 2σ.

This is a good enough reliability for our purpose.

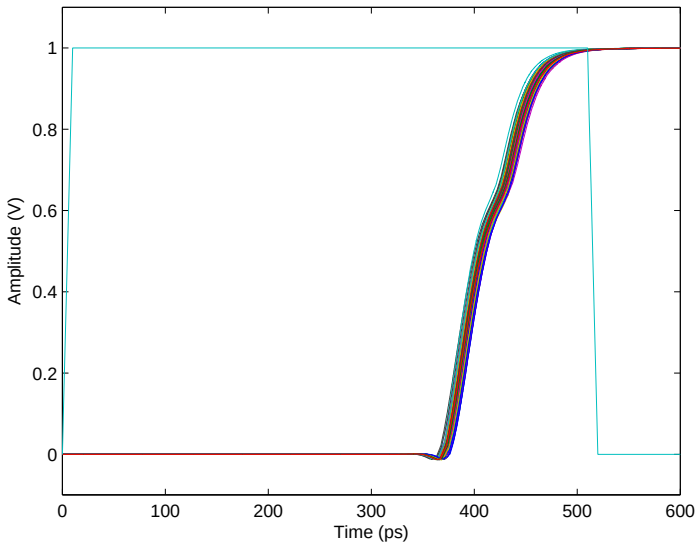

Figure 4.6: Monte Carlo simulation of coarse-tune delay-line

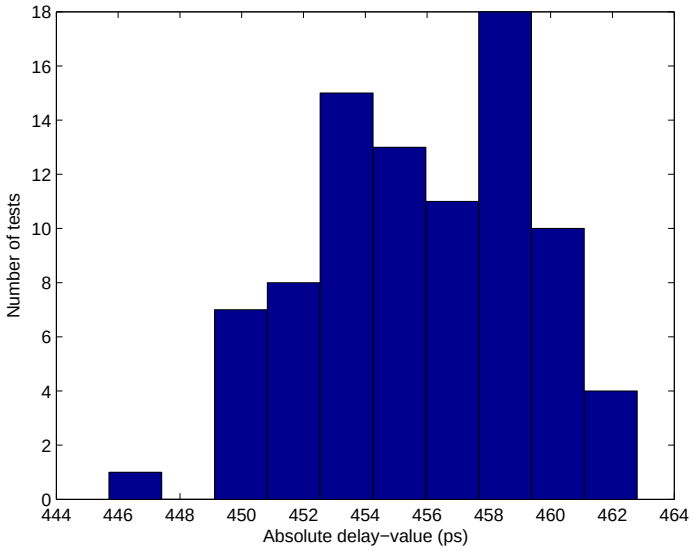

Figure 4.7: Statistics from Monte Carlo simulation with 87 runs

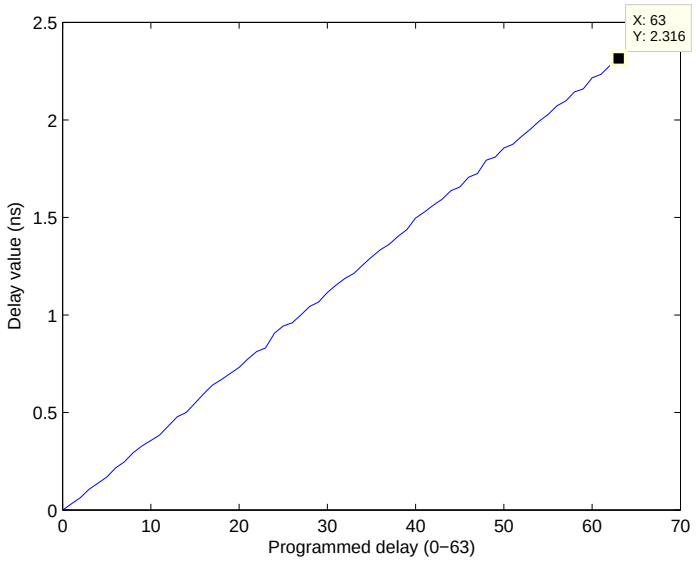

Figure 4.8: Delay value of a coarse-tune delay-line

Measurements

Simulations show that the total delay of each delay-element in the coarse delay-line is $\tau_{buffer} = 35$ ps. The delay-line consists of 63 of these buffers which should gives us a total programmable value of 35 ps $\times$ 63 $\approx$ 2.2 ns. The measurement of a coarse delay-line, shows this property (Fig. 4.8). By measuring each step in a delay-line and presenting the results as probability distribution, we are able to say something about the mismatch. To get reliable measurement data, each step is tested in random order. The oscilloscope function TMAX is used. This function gives us the time of when the amplitude on the oscilloscope screen is at its highest. The time which corresponds to a delay-value of zero is first recorded to give us the offset. This offset is then subtracted from all the measured values to give us the real delay. When all the values are recorded, the difference between each step gives us the delay-value for each step.

To determine the accuracy of this delay-line we can look at the probability distribution of the delay-values of each step (Fig. 4.9). We can see that the delay-values has a Poission-like distribution. The results show that the steps of the delay-line has a mean value of $\mu = 35.1$ ps, and a standard deviation of $\sigma = 7.6$ ps. Approximately 77 % of the steps are within one σ and approximately 97 % are within 2σ.

To get a better statistical foundation, all of the 8 transmitters on a chip are tested (Fig. 4.10). This gives us a mean value of $\mu = 35.2$ ps, and a standard deviation of $\sigma = 8.9$ ps.

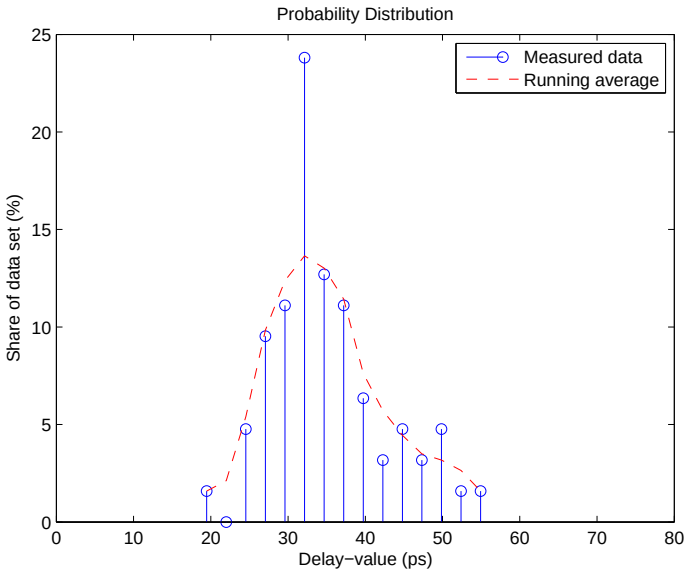

Figure 4.9: The probability distribution of one coarse-tune delay-line

Here, approximately 75 % of the steps are within one σ and approximately 96 % are within 2σ.

The standard deviation of the measured delay-line shows a different value than what was simulated which showed a standard deviation of $\sigma \approx 3.5$ ps. The simulation was conducted using a Monte Carlo analysis of one step instead of the entire delay-line This might be the reason for such a large difference between measured and simulated σ.

4.2.4 Noise between delay-lines

Observations

During measurements of the delay-lines, observations of noise between them was made. The measurements show that a transmitter does not necessarily transmit at the time it is suppose to every time. A transmitter's relative position in relation to the other transmitters can change when one of the other transmitters delay-value is changed. This noise affects the overall system resolution and must carefully be taken into consideration.

To test the effect of induced noise from one transmitter to another one, we sweep the position of one transmitter output while measuring the position and delay value of

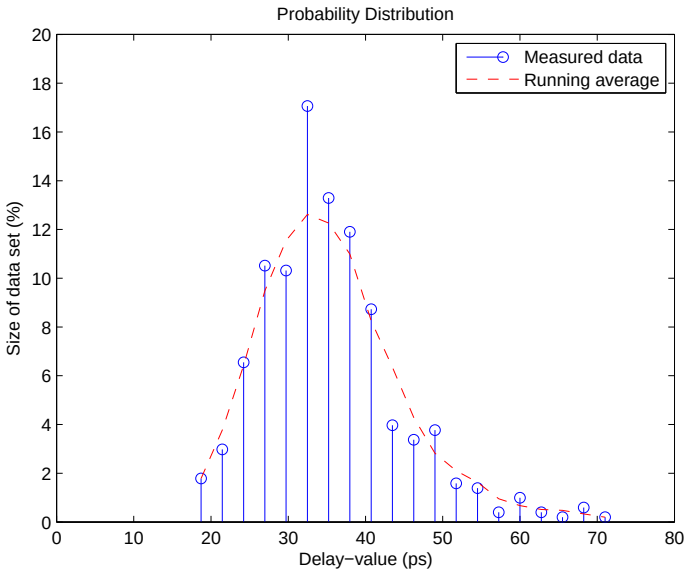

Figure 4.10: The probability distribution of eight coarse-tune delay-lines

another transmitter output (Fig. 4.11). What we observe, is that the position of the measured transmitter is changing according to the position of the swept transmitter. To determine the position of a pulse, we look at the time-difference between the pulse and a trigger-pulse.

From measurements (Fig. 4.12) we can see that pulse position displacement caused by one transmitter is quite significant, $\Delta t_{max} \approx \pm 15$ ps. These are the results of two sweeps. One sweep shows the result when the transmitter-under-test's programmed value is high to see how it is affected early in the travel-path. The other sweep shows the results when the transmitter-under-test's programmed value is medium to see that the effect disappears when the distance between the two outputs goes from negative to positive. The observation was made independent of transmitter-placement on chip.

Another interesting observation is that when more than one transmitter is triggered at the same time, the amplitude of the output-pulses is reduced.

Cause of noise

The trigger-pulse has a long path (Fig. 4.13). First the trigger pulse travels through the coarse-tune delay-line. This is essentially a line of inverters tapped out to a MUX. The trigger-pulse then goes through the fine-tune delay line which consists of tunable

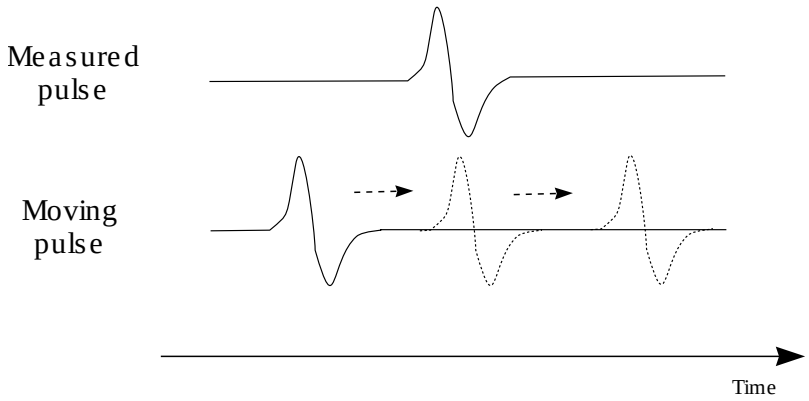

Figure 4.11: Sweeping the delay-line of one transmitter

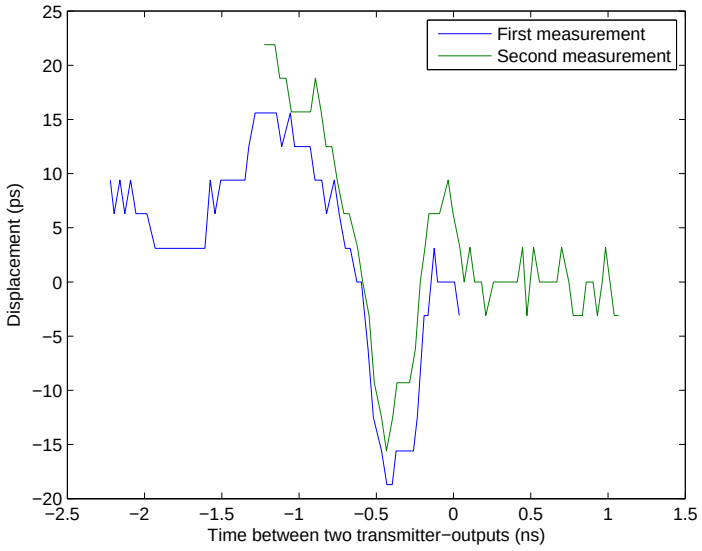

Figure 4.12: The displacement of one transmitter when sweeping a different transmitter's delay-line

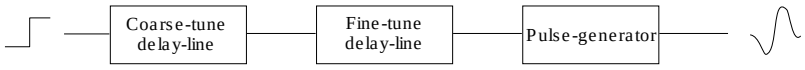

Figure 4.13: The path that the trigger travels to create a UWB pulse

inverters. Then the trigger-pulse arrives at the pulse-generator which creates the UWB pulse shape. From the rising edge of the trigger pulse arrives at the trigger-input on the chip to a rising edge arrives on the pulse generator input, it takes approximately 1.6 ns - 3.8 ns (rough estimate) depending on the programmed delay-value.

When a pulse generator triggers, power-supply ripple occurs. The total delay-value of each element in the delay-line is dependent on the power-supply, so if there is any power-supply ripple while the trigger-pulse is somewhere in this path, the time it takes for the trigger-pulse to travel through the current element will change. Power-supply ripple results in a change in total travel-time in which causes the output pulse to be displaced backwards or forward in time. Only the first transmitter to send will be unaffected.

To be able to determine that power-supply ripple is the cause of noise, more measurements need to be carried out. A test-point has been implemented in the chip between the delay-lines and the pulse-generator. By removing the voltage on the power pads of the pulse generators, we can look at the output from the test-point to see if this reduces the noise. The results are different for each measurement conducted and shows only random noise. No reoccurring pattern of the noise measured from sweeping a different delay-line is present. This could be due to the fact that the random noise is too large, but most likely the noise is removed.

Because the fact that a delay-line is no longer affected if the pulse-generator triggers later than the current trigger, and that the amplitude of an output pulse is reduced when more than one transmitter is sending at the same time, the conclusion is that the pulse-generators must be the source of noise. When a pulse-generator triggers, power-supply ripple occurs changing the delay-value of the other transmitters.

An attempt to measure rail-noise on the outside of the chip was made, but no noise could be measured. This could be due to inadequate measurement equipment or, more likely, this shows that the power-supply ripple is kept internally on the chip.

How to deal with noise

The noise can make a great impact on the resolution of the beamformer. With noise-errors of up to ± 15 ps, the accuracy will be reduced accordingly. If the noise pattern

is properly identified, the errors can be taken into account in the software controlling the delay values. The accuracy is then determined by how accurate we can identify the noise.

There are several work-arounds that can be implemented to help solve the problem with rail-induced noise. Since the prototype circuit consist of both analog and digital circuits, guard rings should be used around the analog parts. Other factors to consider in a future implementation includes using very wide rail-lines, carefully designed power distribution and multiple substrate-contacts.

As a different approach to dealing with rail-induced noise, an auto-tune feedback circuit could be introduced. This circuit could be designed to keep the delay difference between two delay-lines constant. A time-measurement circuit has been introduced in [Ande 07] and could be further developed using feedback to automatically make up for errors in delay-value. This circuit would have to be cleverly designed so that it is not susceptible to noise itself.

4.3 Propagation

4.3.1 Simulated performance

Signal propagation in free space

The propagation of UWB signals in free space happens as three-dimensional geometrically expanding waves. For an omnidirectional antenna, the energy remains constant over the surface of the sphere. This means that the energy density decreases with distance. The energy transfer between two unity-gain antennas can be described with a form of the Friis transmission formula [Siwi 04b]

$$P_L = \left(\frac{c}{4\pi d f_m} \right)^2$$

where f_m is the geometrical mean between the upper and lower signal frequency limit.

Using this formula with $f_m = \sqrt{3.1\ \text{GHz} \times 10.6\ \text{GHz}} = 5.73\ \text{GHz}$, we can look at the path gain for a UWB signal as a function of distance d as shown in Fig. 4.14.

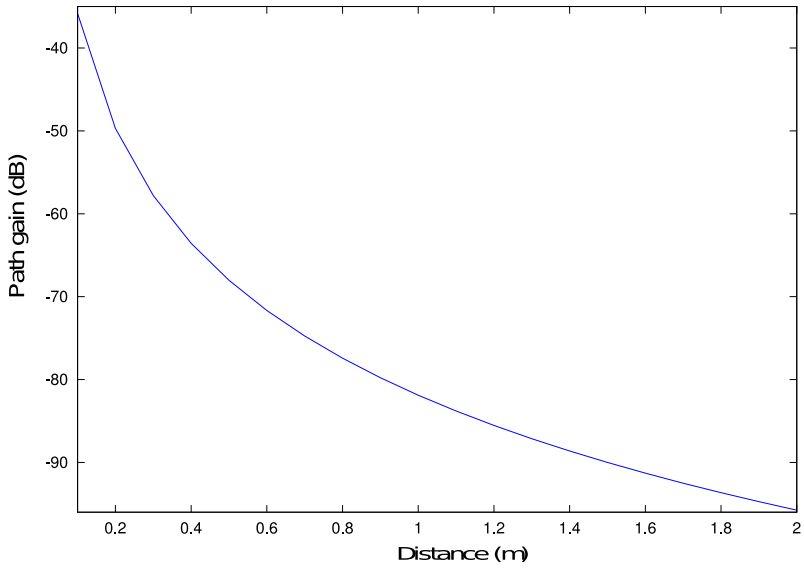

Figure 4.14: The energy path gain as a function of distance

Theoretical Beamforming Performance

For simulating the beamformer a Matlab script was designed by Håkon A. Hjortland. This script is based upon Friis transmission formula combined with the superposition principle and simulates the performance of a beamformer's ability to focus energy. The script is based upon using 7 antennas with 10 cm spacing. In Fig. 4.15 we see the energy profile when the beamformer is configured with a focal point 40 cm in front of the middle antenna. We can see that the beamformer has an area right in front of the antennas where there is a lot of energy. Further away the energy is decreasing, but in a small area around the focal point, we see that we have an energy peak.

4.3.2 Measured performance

The prototype beamformer was tested in order to prove the concept. Unfortunately the measurement context was not ideal and the instruments were not good enough for this kind of testing, so the presented results are not as accurate as they should have been. The beamformer measurements was conducted in a small lab with very little room for moving around to place the equipment accurately.

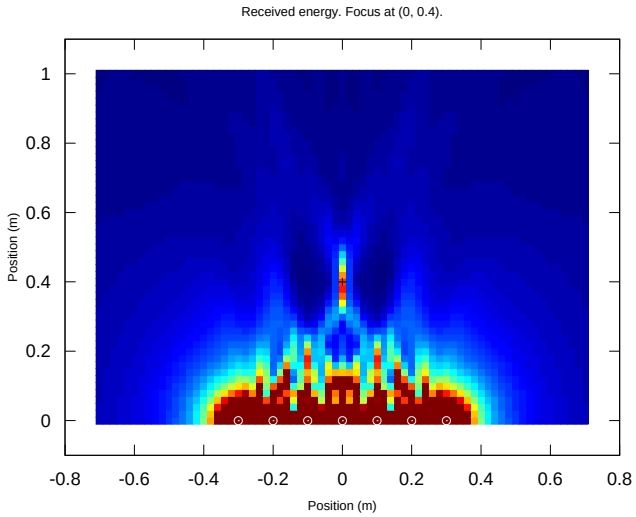

Figure 4.15: Simulated beamforming performance

Measurement Setup

Beamforming measurements was done by using a straight wooden rig mounted on a photography rack. Seven antennas connected from transmitter outputs was placed in the wooden plank and one transmitter output was connected directly to an oscilloscope for triggering. The antennas was placed 10 cm apart. A drawn grid was placed on a table for guiding the placement of the receiver. A receiver antenna was mounted in a chuck of wood to be moved around on the grid. The receiver antenna was connected directly to an input on the oscilloscope.

Beamforming measurements

To measure the performance of the beamformer, the beamformer was programmed to focus its energy on a point 30 cm away from the antenna in the middle. Received amplitude was measured with steps of 5 cm in the area in front of the antenna array.

In Fig. 4.16 we can see a surface plot of the measured data. It shows a clear and distinct point about 15 cm away from the antennas where the received amplitude is clearly larger than other places. This does not match the expected as the beamformer was

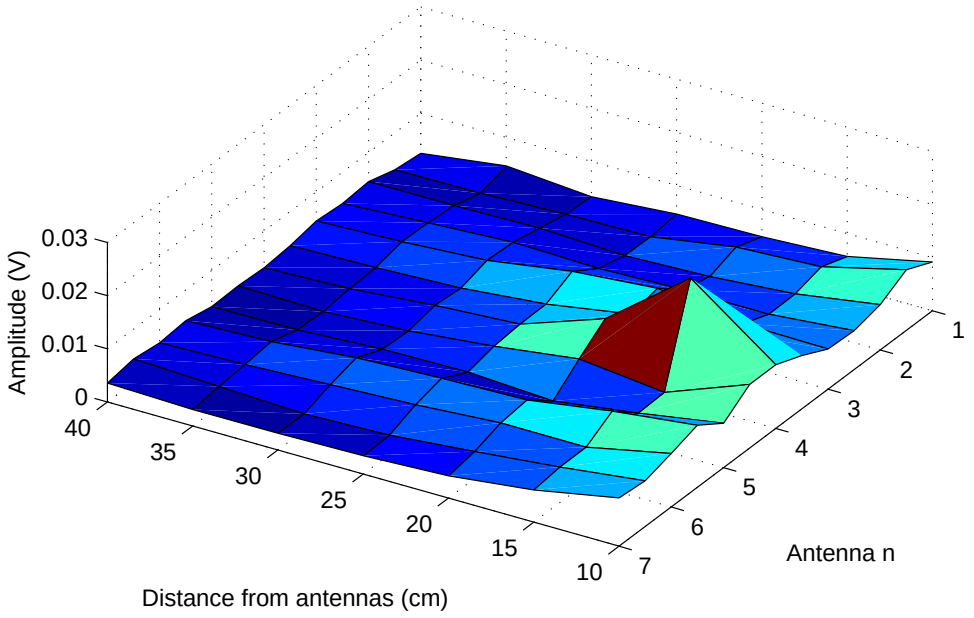

Figure 4.16: Measuring the performance of beamforming focus

configured to focus the energy 30 cm away. The measurement was conducted a second time with a different focal point, but with very similar results. This time the focal point was configured at 20 cm, but appeared at 10 cm in the measurements.

The difference between measured performance and configured performance is due to a quite crude measurement environment where a lot of distance approximations was taken. In section 4.2.4, noise between delay-lines was observed. A delay-value displacement of up to ± 15 ps was observed and this will affect the accuracy of the beamformer. The main reason for the difference though, was due to a calculation error where the delay-values was accidentally calculated using a EM propagation speed of only 70 % of the speed of light which is much too low.

Because of lack of time, additional measurements to investigate the results further were not conducted.

4.4 Summary

The measured results from the HRPDL show a delay-line with very high precision and resolution. Because of inadequate measurement equipment, there is no hard evidence of the accuracy of individual delay-element, but simulations and measurements all point in the direction of a very accurate delay-line.

The coarse delay-line proved to be somewhat inaccurate, but no more than what can be compensated for with tuning. By collecting the individual values of each of the steps, these values could be saved in the beamformer's firmware and automatically be taken into account.

Some noise was observed between the individual delay-lines that decreases the overall accuracy of the beamformer. A few tests were conducted and the conclusion was that this noise must be due to V_{DD} ripple induced by a firing pulse generator.

At the end, crude measurement results from the beamformer was presented which showed the focal point principle in action.

5 Conclusion

The principle behind both UWB and beamforming has been around for a while. Throughout history lots of beamforming experiments have been conducted both with a carrier-based frequency-domain approach and a impulse-based time-domain approach.

Since the FCC released the UWB definition mask, the explosion of new application has yet to come. As with every technology it all boils down to cost. As the CMOS technology develops, more and more clever design approaches for achieving integrated UWB systems are emerging. A simple UWB pulse generator was designed in [Moen 06] and a very promising radar system was developed in [Hjor 06].

During this year's Consumer Electronics Show (CES), more than 10 companies showcased different types of UWB-based high-speed data transfer chips [EUWB]. This could indicate that we are on the edge of a break-through regarding the adoption of UWB technology. If this is the case, chances are we will see lots of cutting-edge applications using UWB technology in the near future. To help speed up the development, we need low-cost and easy-to-implement circuits that utilize the standard CMOS technology in new ways.

5.1 Achievements

In this thesis a simple way of using standard CMOS transistors in a non-traditional way makes very accurate high-resolution timing-circuits a reality. Even though in this thesis we are using this technique for achieving high-resolution beamforming, the technique could be utilized for many different purposes. A prototype beamformer has been produced and measurements indicate that the HRPDL design is very promising for all kinds of applications that require programmable tuning down to 1 ps.

The purpose of this thesis was to investigate the idea of a counterpart to the phased array structure used in traditional Radio Frequency (RF). The basic idea was to replace the quite complex phase adjustment circuits with a simple impulse-based time-delay structure. A very promising design has been suggested and measurements show that the circuit seem to be very robust against mismatch errors.

There was not many publications found on the topic of transmitting a directional UWB signal. This could indicate that there are not many accomplishments within this field. One publication presented a UWB transmitting beamformer [Safa 08], but is largely outperformed in regards to time and scanning resolution by the work presented in this thesis.

A UWB receiver presented in [Rode 06] comes close in regards to this work's time resolution, with 4 ps resolution. But this is still 4 times higher than the results achieved in this work.

5.2 Future development

The main design challenge for this thesis was to find a simple delay-line design that showed very good properties in regards to achievable resolution and mismatch resistance. The delay-value of approximately 1 ps could easily have been reduced further with simple modifications in the design. This is however not investigated further with regards to mismatch.

As the delay differences between delay-lines decrease, the demand for well-designed signal paths increase. For UWB beamforming, there is no obvious reason for even lower delay-values as the pulse itself often is in the order of a few hundred picoseconds.

The most important future improvement of the beamformer design is to implement good power distribution and shielding of the analog circuits from the digital circuits to remove the noise between the channels.

The next step in developing the presented beamformer could be the implementation of the beamformer integrated in a radar application. This would enable some sort of an EM camera that would have the possibility of looking through walls, looking inside a human being or determining the surface profile of an object.

A Paper submitted to ICUWB2009

The following paper has been submitted to "2009 IEEE International Conference on Ultra-Wideband". The status of acceptance is as of this writing not yet known.

Close Range Impulse Radio Beamformers

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***Abstract*—Beamforming electromagnetic waves, especially at close range, is challenging. Extremely accurate control of phase/timing is required. In this work we present a digital programmable delay-line suited for transmission beamforming using multiple senders. Back-gate tuning of inverter delays are measured to give relative temporal tuning in the range of 1.1 ps.**

I. Introduction

The emergence of Ultra Wideband (UWB) technology in the marketplace is slower than anticipated when the UWB band was released by FCC several years ago. A major obstacle has been to implement solutions in standard CMOS technology. Only a few single-chip CMOS transceiver solutions are currently available either for multi-band or impulse radio [1], [2] and lately several journalists have announced UWB to be dead. In the end it all boils down to cost so single-chip, low-cost CMOS solutions may have significant impact on the UWB market.

At the Nanoelectronics group at Dept. of Informatics, University of Oslo we are pursuing unconventional design paradigms enabling impulse radio solutions in standard digital CMOS operating at microwave frequencies. The Continuous-Time Binary-Value (CTBV) design paradigm has been explored to make a fully functional, single chip impulse radar [3]. A more elaborate treatment of CTBV circuit design for CMOS impulse radio may be found in [4]. An important feature of CTBV circuits is the exploration of inherent gate delay instead of rigorous and power-demanding clocked schemes. One good CTBV example is the high-speed sampler of the impulse radar measuring backscattered energy for every 5^{th} millimeters in depth. This is equivalent to a sampling rate of more than 30 GHz. The short-range CTBV radar is giving remarkably good results using coherent integration. However, unless focused antennas are used, the radiated pulses are spread widely giving backscattered energy from all over the place. In some applications like level measurements the lack of directionality is desirable, but for more detailed information, a controllable electromagnetic (EM) beam would facilitate something like an electromagnetic camera [5]. A focused horn antenna used for scanning would require some mechanical rig but techniques known as beamforming in two dimensions would enable a scannable EM beam. Most EM beamformers are found in radar applications and is named phased arrays. By adjusting the relative phase differences of signals transmitted by several antennas, constructive and destructive interference will set up a radiation pattern a process known as beamforming. A simple time-domain solution is to introduce suitable delays in the signal paths before transmission. Although most beamformers are adjusting phases of some sinusoidal signal, we are exploring accurate adjustment of the "firing" sequence of Gaussian pulse transmitters.

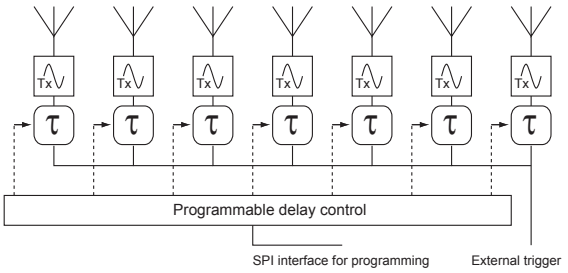

Fig. 1. The transmitter beamforming is achieved by delayed trigger of pulse transmitters.

Another major challenge doing impulse radio solutions in standard CMOS is the low power supply, approaching 1 V in nanometer technology. Even with rail-to-rail operation, it is hard to radiate the permitted energy level set by the US FCC part 15 limit of -41.3 dBm/MHz. Again adding antenna gain would improve directional power, but beamforming would allow for simple and small antennas. With very power-efficient and low-device-count Gaussian transmitters feasible in CMOS technology [2], adding several on-chip transmitters is simple. By beamforming, significant increase of directional, radiated power is feasible without increasing on-chip power supply. Multiple-antenna arrangements are often named MIMO (multiple-input multiple-output) in communication systems.

II. Impulse Radio Beamformer

As shown in Fig. 1 the idea of impulse radio beamforming is simple. A number of identical Gaussian transmitters are individually controllable with a trigger pulse. The power efficient transmitters employing only a handful of transistors are provided by Novelda AS [2] as part of a technology exchange agreement with Dept. of Informatics, University of Oslo. On the rising edge of the trigger, a Gaussian dual-slope pulse is transmitted on the antenna.

In order to generate a suitable sequence of transmitted pulses, a delay element is inserted between a global trigger pulse and each of the transmitters. In order to focus an EM beam the antennas must be arranged with a suitable spacing. For a given focal distance F and an antenna spacing of δd the

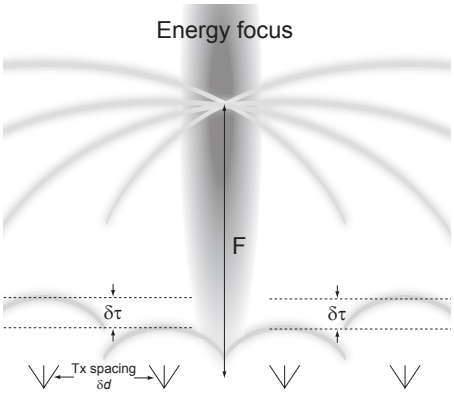

Fig. 2. The radiation from several transmitters will interfere and build up energy when coordinated.

required temporal correction is given by

$$\delta\tau = \frac{\sqrt{F^2 + \delta d^2} - F}{c},$$

when we assume signal propagation close to the speed of light $c = 3 \cdot 10^8$ m/s and aligned antennas. For an energy focus at 1 m with antennas spaced 0.1 m apart, the $\delta t \approx 16.6$ ps, while an EM focus at 0.9 m would require $\delta t \approx 18.5$ ps. In this antenna configuration an adjustment of 0.1 m requires a timing adjustment of approximately 1.9 ps. These fine time adjustments are hard to make, especially with the inherent transistor mismatch found in advanced technology. The spatial size of the focused energy is determined by frequency content of the transmitted pulses. In general, higher center frequency will improve focus.

A. Programmable Delay Element

Based on the proposed time-domain impulse radio beamforming, an accurate and programmable delay element tunable in the picoseconds range is required. Even for nanometer technology this is really challenging. The nominal inverter delay is estimated to be approximately 12 ps. An important observation is by using a global edge-trigged topology, we are left with tuning the *relative* time-differences. Adding an overall delay after trigging is acceptable, but the relative delays between the delay-lines must be adjusted accurately in the picoseconds range. So slightly manipulating the individual inverter delays of a longer delay-line is sufficient. Now, cascading several inverters adding latency is acceptable as long as all delays are balanced to approximately the same accumulated time. Minor changes of inverter delays may be done by design with transistor sizing, but a programmable delay is harder to come about. In this approach we are exploring back-gate tuning or body-biasing. Back-gate efficiency is reduced in nanometer technology [6], which in this application is traded in as an advantage enabling fine-tuning of inverter delays.

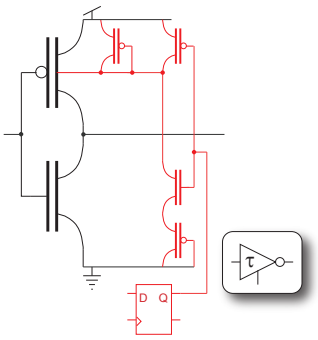

Fig. 3. Binary back-gate inverter tuning using a weak pulldown over a PMOS diode-connected transistor.

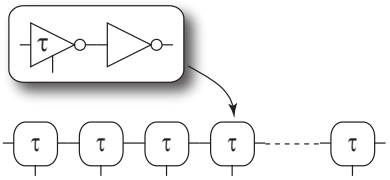

Fig. 4. A programmable delay is constructed by cascading inverters and tunable inverters.

The circuit topology explored in this work is a simple binary tuning of a PMOS back-gate as shown in Fig. 3. An inverter with weak pull-down is used to switch the body-bias between two voltages. When the inverter output is high, the diode-connected PMOS transistor will drive the well potential to V_{dd} for normal inverter operation. When the inverter is pulling down through the series PMOS load, the well-potential or back-gate is pulled downwards approximately one diode offset, imposing a slight decrease of the front-gate threshold voltage. The effect is a slightly faster PMOS. With a triple-well process, a similar procedure might be used for the NMOS as well, but we are working with edge-trigged transmitters and only need to adjust the positive-going transition. The inverter state is set digitally by storing a bit in a register.

As shown in Fig. 4 the tunable inverter is followed by a normal inverter for signal reconstruction and state inversion. Then a suitable number of delay stages are cascaded to establish required tuning range.

B. Impulse Radio Beamformer Chip

In order to evaluate the quality of delay-line programming a test-chip was made in ST 90 nm CMOS process. Eight identical, edge-trigged impulse radio transmitters for dual-slope Gaussian-shaped pulse transmission were used.

As shown in Fig. 5, the firing of each transmitter is controlled by a programmable delay-line consisting of one programmable coarse-tune delay element and 64 programmable fine-tune delay elements. The coarse delay element is made of

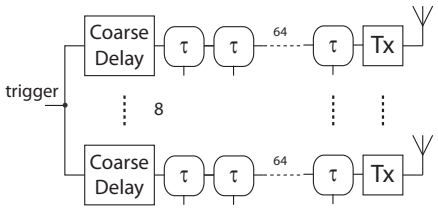

Fig. 5. The evaluation chip consists of eight dual-slope Gaussian pulse transmitters preceded by programmable delay-lines.

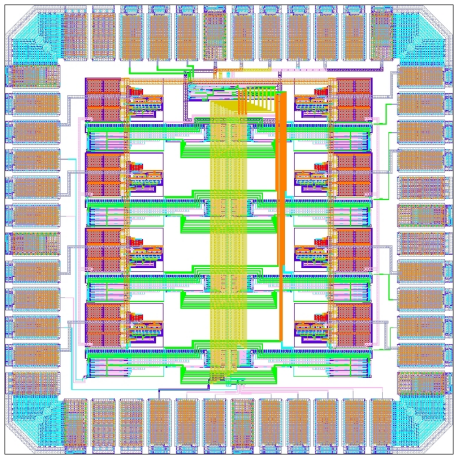

Fig. 6. A chip was designed in STMicroelectronics 90 nm technology with eight transmitters each equipped with programmable delay-lines.

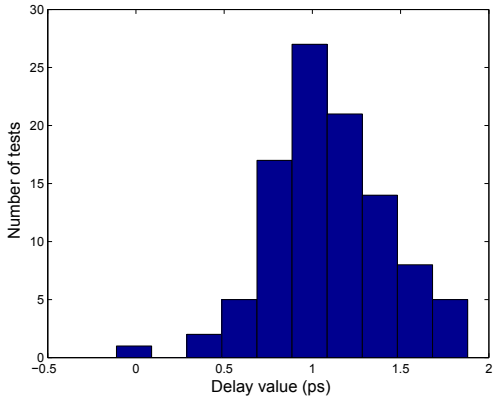

Fig. 7. Simulated probability distribution of the value of one delay-element.

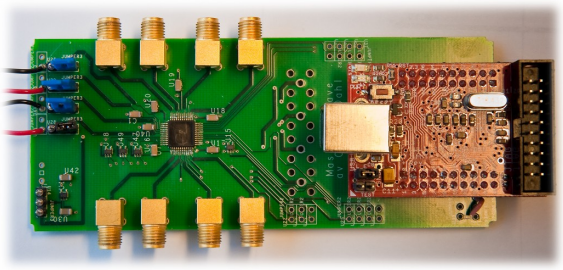

Fig. 8. Photo of PCB made for chip measurements (photo: T. Sæther).

a chain of 64 dual inverter delays. Each of the delay-outputs are tapped to a multiplexer for control of the delay-value. The multiplexer enables us to choose the number of dual inverter delays to cascade. The unit delay of the dual inverters are approximately 35 ps, which gives us a programming range of 0 to 63×35 ps ≈ 2.2 ns. The firing sequence is trigged by an external trigger for all transmitters and a simple SPI scheme is used for programming the different delay-elements integrated on the chip. Fig. 6 shows the chip topology, where the eight transmitters are clearly visible along the pad-frame.

C. Simulated and Measured Performance

As transistor mismatch in fine-pitch processes is significant, a statistical treatment of chip performance is required. As a first approximation a delay-element was simulated in Cadence using foundry parameters for Monte Carlo modeling.

The probability distribution in Fig. 7 gives an expected tunable delay of approximately 1 ps. More accurately, we have a mean value of $\mu = 1.1$ ps with a standard deviation of $\sigma = 0.3$ ps. In 74% of the tests, the value is within one σ. In 94% of the tests the value is within 2σ. This simulation indicates that tuning is remarkably accurate, facilitating close range beamforming.

In order to evaluate the chip performance, high quality instruments are required. Our equipment is somewhat limited with a 20 Gsample/s scope (Agilent 54855A Infiniium Oscilloscope). However, by using averaging the specification sheet [7] indicates a delta-time accuracy between two edges on a single channel down to 70 fs, provided at least 256 samples are averaged. Based on a number of experiments, we find the practical resolution of the oscilloscope to be approximately 3 ps. Because of these measurement limitations, we have to design our experiments accordingly.

The prototype chip is mounted on a printed circuit board (PCB). The PCB is also equipped with a connector for a microcontroller module hooked up to a PC via USB. The microcontroller is programmed to control the value of the delay-line registers using SPI. The transmitter outputs are routed to eight different SMA connectors. The piggy-back microcontroller is mounted on the right side of the PCB in Fig. 8, while the SMAs are mounted along the edges.

For debugging purposes we have tapped four transmitter trigger signals to separate SMAs (not mounted in Fig. 8). The antenna outputs are connected to the oscilloscope with equal-length cables (1 m) and 50 Ω impedance matching.

The measurements are controlled by MATLAB scripts on a computer interfacing the chip registers through the USB-

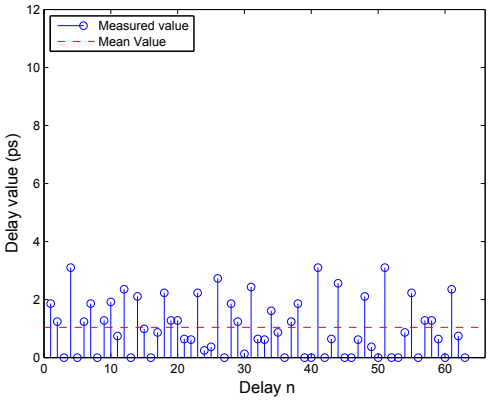

Fig. 9. Measured values for each of the delay-elements in a delay-line.

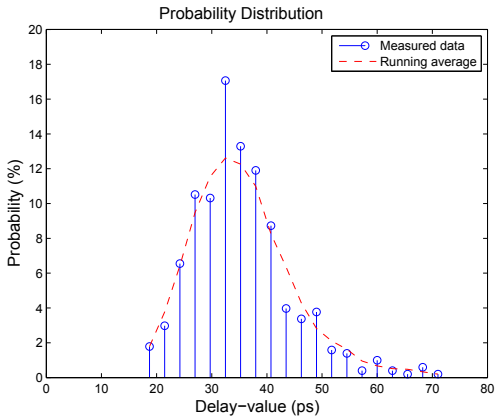

Fig. 10. Measured delay distribution of the eight coarse delay-elements on a single chip.

TABLE I
MEASUREMENTS OF 8 DELAY-LINES ON A PROTOTYPE CHIP, SELECTING 40 RANDOM DELAY ELEMENTS.

Delay-line	# Runs	Mean	Peak deviation	Mean/40
1	99	53.8 ps	2.4 ps	1.3 ps
2	99	44.0 ps	2.8 ps	1.1 ps
3	99	59.6 ps	2.9 ps	1.5 ps
4	99	53.1 ps	3.1 ps	1.3 ps
5	99	56.5 ps	2.9 ps	1.4 ps
6	99	45.3 ps	1.7 ps	1.1 ps
7	99	58.5 ps	2.1 ps	1.5 ps
8	99	47.0 ps	3.3 ps	1.2 ps
Avg	792	52.2 ps	2.7 ps	1.3 ps

connected microcontroller and reading results from the oscilloscope using GPIB.

The simplest measurement is to enable each delay element individually and measure the incremental change. The measured values flip between 0 ps and 3 ps, so each delay-element is measured five times and the average value is recorded (Fig. 9). The average value over all delays is approaching 1 ps.

A better estimation is possible by randomly selecting 40 delay-elements and measure the total delay. By averaging we may estimate the unit delay. Again we do repeated measurements, this time each experiment was repeated 99 times.

The results listed in TABLE I indicate good match with simulations. Largest peak deviation is 3.3 ps which is within the known precision of our oscilloscope. By averaging we estimate the unit delay to be $\tau \approx 1.3$ ps. All these measurements are from one chip, but results from other chips are similar.

The accuracy of the coarse-tune delay-line is also affecting the overall performance, but can be mended by calibration. These coarse delays are only required for large offsets and are expected to have significant variations in actual delay value.

By measuring each tap of the delay-line and presenting the results as a probability distribution, we are able to analyze the impact of mismatch. These variations are significant, but may to some extend be calibrated by offsetting the fine-tune delay.

By inspecting the probability distribution in Fig. 10, we

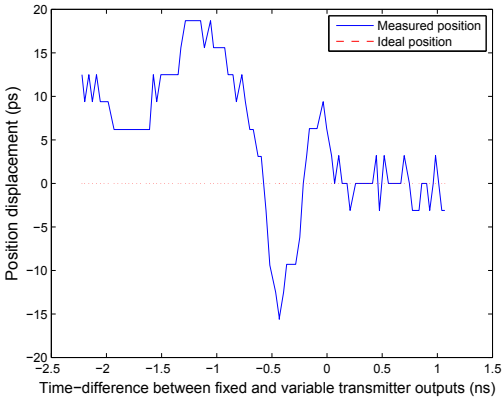

Fig. 11. Interference to the timing of one transmitter caused by another transmitter.

can see that the delay-values have a somewhat Poisson-like distribution shape. The results show that the steps of the delay-line has a mean value of $\mu = 35.2$ ps, and a standard deviation of $\sigma = 8.9$ ps. Approximately 75% of the steps are within one σ and approximately 96% are within 2σ.

During testing, significant interference between delay-lines were observed. Initially a constant delay value was established in one delay-line (A). Then another delay-line (B) was systematically changed by incrementing the programmed delay. Fig. 11 shows how the presumably constant delay-line A is affected by interference from setup of another delay-line. As delay is increased in delay-line B, we see the presumably constant delay of delay-line A is first increased, then decreased and then increased again. When the firing of transmitter B is done after the firing of transmitter A, no further interference is detected. We observe this effect regardless of physical on-chip distance.

We explain this behavior by rail induced noise. Gates like inverters are rail referred with quite poor power-supply rejection ratio (PSRR). When the pulse transmitters are trigged, rails are strongly loaded, feeding back correlated interference. This systematic interference is showing up as significant change to the delays.

To verify this theory, the pulse generators were turned off by disconnecting the separate rail pads. By measuring the buffered transmitter trigger we find no interference. Based on these observations, we see that great care must be taken to prevent cross-talk between pulse generators and delay-lines.

III. Conclusion

In this paper, we have presented a novel programmable delay element exploring back-gate tuning. A programmable delay with a relative tuning of 1.1 ps may be used for accurate, close-range beamforming by controlling the trigging of impulse radio transmitters. Although some inaccuracies and interference is observed, the back-gate tuning is usable for close range beamforming, provided layout is done carefully with appropriate shielding.

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B Layout of the delay-line

The following picture shows the layout of one element in the High-Resolution Programmable Delay Line (HRPDL).

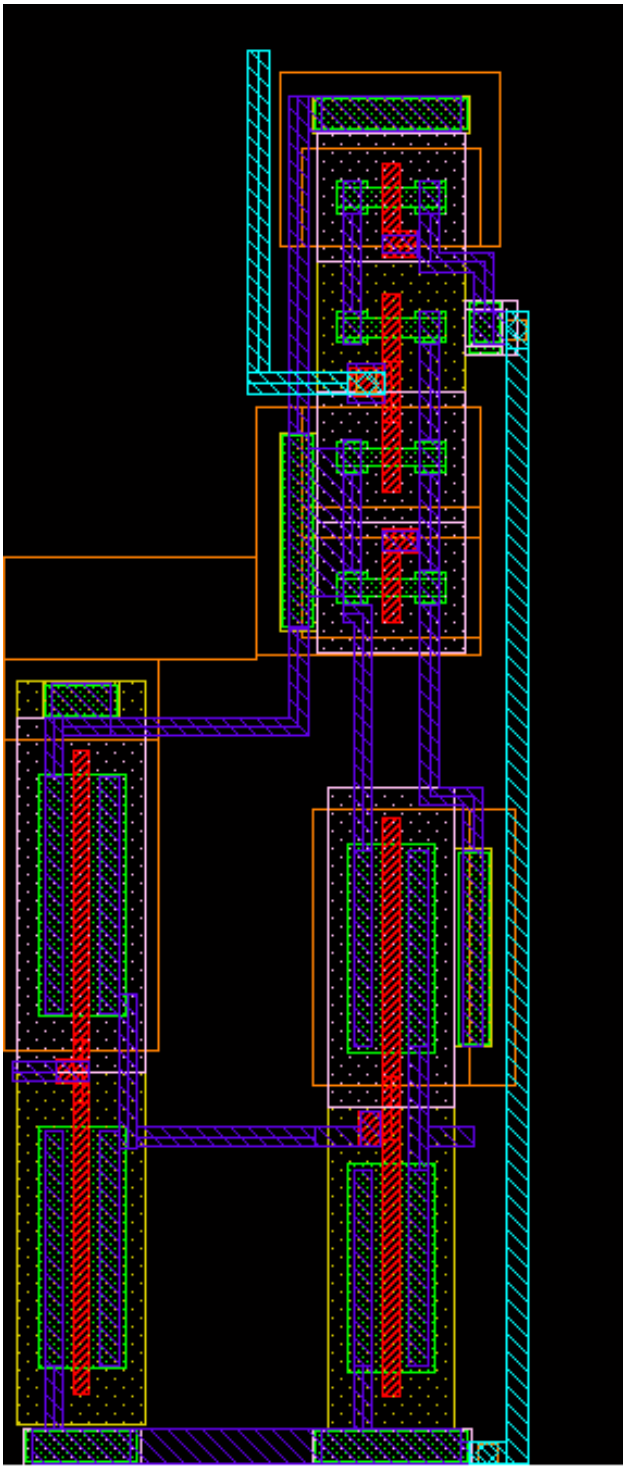

Figure B.1: The layout of one programmable fine-tuning element

C Screenshots of beamformer programs

Two programs for Windows was developed to ease the configuration of the beamformer system and to study the behaviour of impulses in two dimensions. The following pictures show screenshots of the programs.

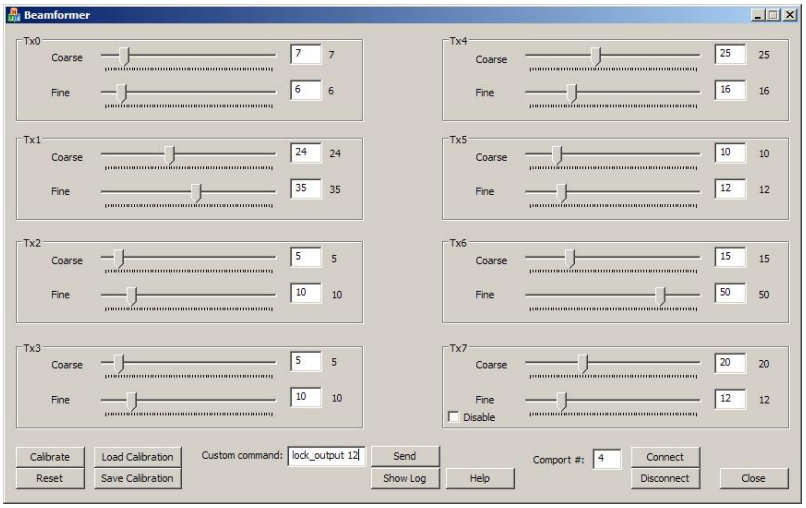

Figure C.1: The main window of the Beamformer program, used for tuning of the delay-lines.

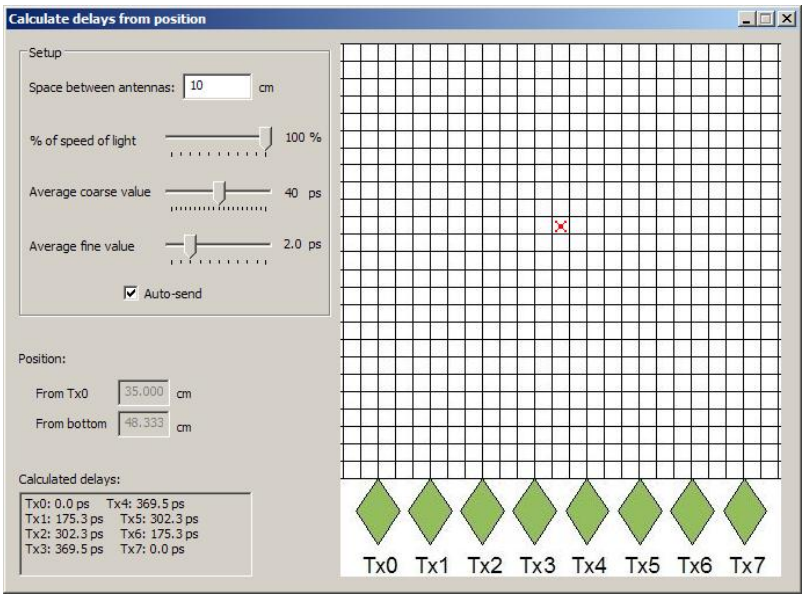

Figure C.2: The focal-point beamforming window for easy setting of a specific focal point.

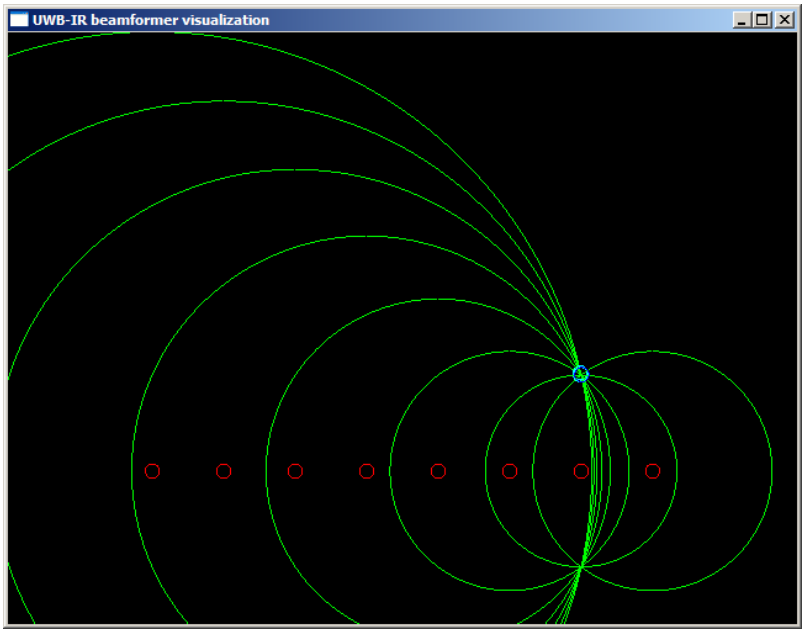

Figure C.3: The beamformer visualization program for studying the behaviour of impulses from eight antennas.

List of acronyms

AM	Amplitude Modulation
ASIC	Application-Specific Integrated Circuit
AWGN	Additive White Gaussian Noise
CES	Consumer Electronics Show
CMOS	Complimentary Metal-Oxide-Semiconductor
DC	Direct Current
EIRP	Effective Isotropically Radiated Power
EM	Electromagnetic
EMW	Electromagnetic Waves
FCC	Federal Communications Commission
GPIB	General Purpose Interface Bus
GUI	Graphical User Interface
HRPDL	High-Resolution Programmable Delay Line
lsb	Least Significant Bit
MISO	Master In Slave Out
MOSI	Master Out Slave In
msb	Most Significant Bit
MUX	Multiplexer
PAN	Personal Area Network
PCB	Printed Circuit Board
RF	Radio Frequency
SCK	Serial Clock
SMA	SubMiniature version A
SNR	Signal-to-Noise Ratio
SPI	Serial Peripheral Interface Bus
SS	Slave Select
USB	Universal Serial Bus

UWB Ultra-Wideband

UWB-IR Ultra-Wideband Impulse Radio

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