UNIVERSITY OF OSLO
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Simulation of Nanoscale CMOS

Master thesis

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Abstract

Device scaling is directly responsible for Moore's law and has enabled remarkable improvements in CMOS (Complementary Metal-Oxide-Semiconductor) device performance. As device dimension shrinks, the channel resistance decreases, this in turn allows faster circuit operation. However, as the intrinsic device continues to improve, parasitic components such as the series resistance in the source/drain region start to limit device performance. Controlling these parasitic components, through proper design, are therefore essential.

TCAD (Technology Computer Aided Design) can be an important tool that allows us to understand various design parameters on device performance. Furthermore, it allows the investigating of different internal quantities that are not available experimentally.

This document presents the results of a thorough study of the scaling down the MOSFETs and its impact on the device performance. A major challenge is to maintain a good control of short channel effect in the low threshold voltage case. Moreover, high-field effects that are related to the increased electrical field in the channel owing to the reduction of the dimensions will be dominant for very small dimensions.

The simulations are based on using a selected doping profile and oxide thickness according to channel length to cope with the variable specification of the ITRS Roadmap in order to improve the device performance. The simulated results of the devices design at the 25 nm channel length generation are considered to be the most promising candidate

for an excellent procedure in suppressing the short channel effects in the today's technology.

While the results and conclusions from this study are the main focus of this thesis, considerable attention is paid to the software that enabled the successful implementation of the study and processing of the simulation results.

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CHAPTER 1

INTRODUCTION

1.1 The Perspective of CMOS Technology

The microelectronics industry has achieved amazing improvement in the last three decades; it has steadily moved to occupy a central position in modern electronic system design. It has grown in a large part because of its ability to continually improve performance while reducing costs. There is a constant drive to make devices that occupy less space, consume less power and have shorter delays.

This is responsible for smaller feature size and the increase in clock-speed that implies the assumption of the continuation of Moore's law, which states that the transistor density on integrated circuits doubles every 18 months [6]. A large part of the success of the CMOS transistor is due to the fact that it can be scaled to increasingly smaller size. The

ability to improve performance while decreasing power consumption has made the CMOS the dominant technology for Very Large Scale Integration (VLSI) circuits.

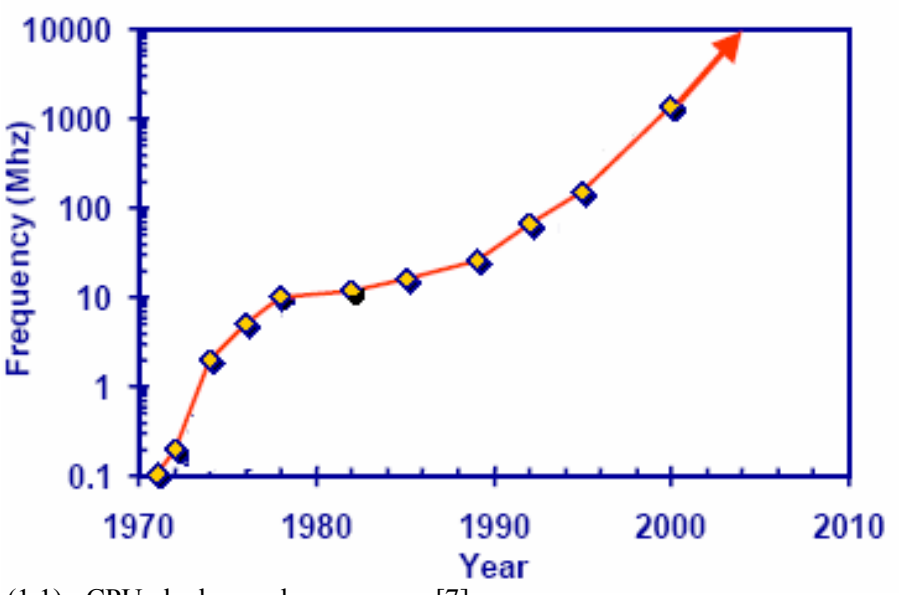

Fig. (1.1): CPU clock speed versus year [7]

1.2 International Roadmap for Semiconductors

The international Technology Roadmap for Semiconductor (ITRS), which was established by a group of experts, serves several purposes within the semiconductors ground field. Its main objective is to specify the device design parameters values as predicted for future device technology. In addition to that, it highlights the challenges that might face the device scaling in the coming generations.

The (ITRS) main projection in the MOSFET and front-end process areas is high performance while keeping the low power logic. A major element of semiconductor device production is devoted to digital logic ICs as well as to memory ICs. Key considerations are performance, power, and density requirements and goals.

The main focus is high speed and low power, which drives the technology forward. The approaches for reaching these goals are different. For high performance logic such as microprocessors the main objective is maximum chip speed, with a tradeoff relative to leakage current. For low power logic approaches such as for mobile systems, the

objective is to obtain long operating time by minimizing the chip power dissipation, particularly the static power dissipation, with a tradeoff of reducing MOSFET speed.

Moreover, the aim of the Roadmap is to identify key technical requirements and challenges critical to sustaining the historical scaling of CMOS technology (i.e., according to Moore's Law [6]), and to encourage the needed research and development to meet the key challenges.

In this thesis, we shall investigate in detail the ITRS predictions regarding device properties that have attracted significant attention in the literature as critical limiting factors of device scaling: the short channel effects that signify the loss of gate control, lowering of the threshold voltage, how to compensate the high substrate doping density to avoid hot electron effects and the reduction of the junction depth that leads to high extrinsic resistances.

Year	Physical Gate Length (nm)	Oxide Thickness (nm)	D/S Extension Depletion X_j (nm)	D/S Contact Depletion X_j (nm)	Extension Lateral Abruptness (nm/dec)
2003	45	1.3	24.8	49.5	5
2004	37	1.2	20.4	40.7	4.1
2005	32	1.1	17.6	35.2	3.5
2006	28	1.0	15.4	30.8	3.1
2007	25	**0.9**	13.8	27.5	2.8
2008	22	**0.8**	8.8	Not applicable	To be determined
2009	20	**0.8**	8.0	Not applicable	To be determined

Table 1.1: International Technology Roadmap for Semiconductors 2003 Edition. Red, and Bold numbers indicate no known solutions [1].

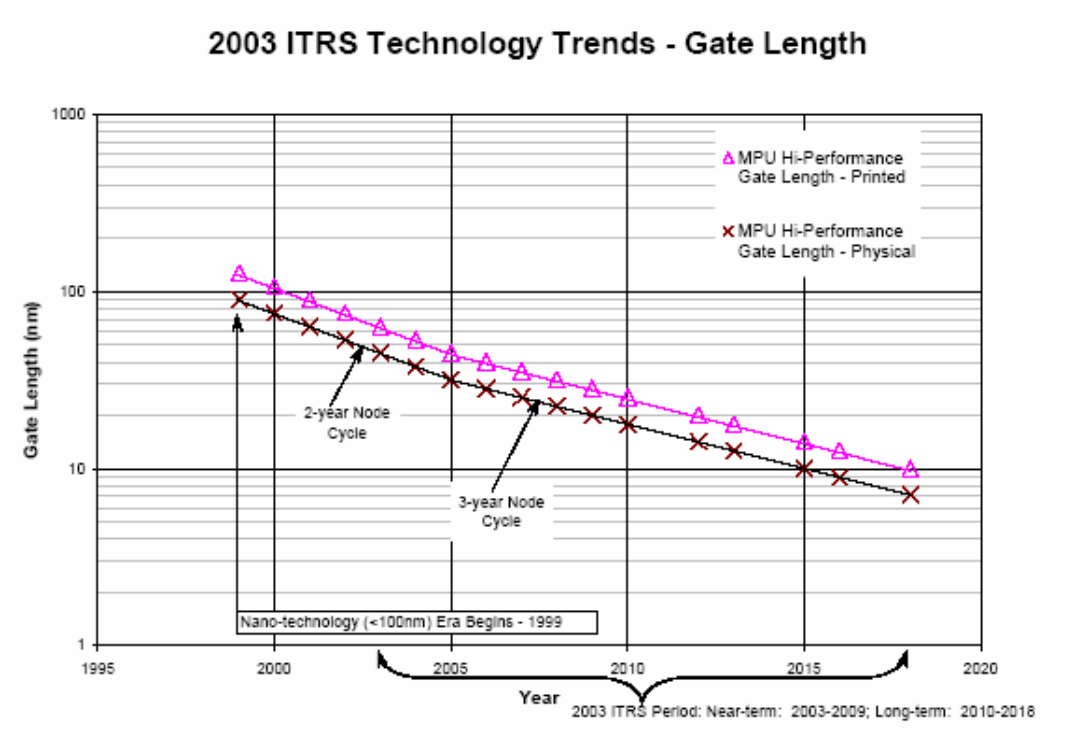

Fig. (1.2): Device Scaling, MOS device gate lengths versus year. ITRS 2003 [1]

1.3 Simulation and Tech CAD

Technology Computer Aided Design (TCAD) can be a powerful tool for reducing design costs, improving device design productivity and obtaining better device and technology designs. While the cost of building a state-of-the art fabrication plant continues to go up, computing power has become a relatively cheap product, due to Moore's law and the resulting improvements in the performance and in the demand by buyers for reduction in the price.

Instead of going through an expensive and time consuming fabrication process, computer simulations can be used to predict the electrical characteristics of a device design quickly and cheaply. Process modelling and simulation of the fabrication process, can be predicted so that physical characteristics such as oxide thickness and doping distribution can be produced with high precision.

Device modelling and simulation can then be used to predict the electrical characteristics of the given device structure.

An important benefit of using TCAD is that it can help in understanding how semiconductor devices work. Examination of detailed device operation, such as how the energy levels and the carrier (electrons and holes) distribution inside the device varies with the biasing conditions, can provide valuable insight into the relationship between a change in process conditions or device design and the resulting impact on device performance. These quantities are often difficult to obtain experimentally. In contrast, they are readily available through computer simulations, which directly provide feedback and guidance for device design.

Technology computer aided design has become a central part of semiconductor modelling and design. It is important to note that the accurate TCAD simulations and modelling of physical devices depend significantly on calibrated physical models and proper input data.

One of the most usable TCAD is Smart Spice; a very high quality computer tool which serves to a large degree for the general design purposes for circuit simulation of nonlinear DC, nonlinear transient, and linear AC analyses. SmartSpice simulates a circuit by calculating the behavior of all circuit components simultaneously. Through its many reliable models, SmartSpice bases its simulation on physical properties, as well as electrical parameters, to simulate the behavior of complex circuits. It simulates circuits and sub-circuits consisting of the five most common semiconductor devices: Diodes, JFETs, BJTs, MOSFETs and MESFETs, and in addition it simulates resistors, capacitors, inductors, dependent and independent voltage and current sources, switches, and transition lines. SmartSpice is the result of intensive research and development; and is a circuit simulator with high speed, great convergence, high accuracy, and powerful pre- and post-processing [14].

1.3.1 ATLAS Overview

ATLAS is a physically-based device simulator [14]. It provides general capabilities for two (2D) and three-dimensional (3D) simulation of semiconductor devices.

It specifies the device simulation problems by defining: the physical structure to be simulated, the physical models to be used, and the bias conditions for which electrical characteristics are to be simulated.

ATLAS can be used in conjunction with the V.W.F. (Virtual Wafer Framework) Interactive Tools. These include Deckbuild, Tonyplot, DEVEDIT (Device Edit), MaskViews, and Optimizer. Deckbuild provides an interactive run time environment. Tonyplot supplies scientific visualization capabilities. DEVEDIT is an interactive tool for structure and mesh specification. MaskView is an IC Layout Editor. The Optimizer supports black box optimization across multiple simulators. ATLAS is often used in conjunction with the Athena process simulator which predicts the physical structures that result from processing steps. The resulting physical structures are used as input by ATLAS, which then predicts the electrical characteristics associated with specified bias conditions. The combination of ATHENA and ATLAS makes it possible to determine the impact of process parameters on device characteristics. The electrical characteristics predicted by ATLAS can be used as input by the UTMOST device characterization and SPICE modelling software. Compact models based on simulated device characteristics can then be supplied to circuit designers for groundwork circuit design. Combining ATHENA, ATLAS, UTMOST, and SmartSpice makes it possible to predict the impact of process parameters on circuit characteristics. ATLAS can be used as one of the simulators within the V.W.F. Automation tools. V.W.F. makes it convenient to perform highly automated simulation-based experimentation. It therefore links simulation very closely to technology development, resulting in significantly increased benefits from simulation use.

ATLAS produces three types of output files. The first type of output file is the run-time output, which gives us the progress and the error and warning messages as the simulation proceeds. The second type of output file is the log file, which stores all terminal voltages and currents from the device analysis. The third type of output file is the solution file, which stores 2D and 3D data relating to the values of solution variables within the device at a given bias point [14].

CHAPTER 2

Background

2 Effect in Scaled-down Devices

Scaling down MOSFETs has many benefits; we see the benefits of scaling down the device in terms of improved packaging density, speed, and power dissipation. A major concept in scaling is that the various structural parameters of the MOSFETs should be scaled in concert if the device is to keep functioning properly. If lateral dimensions such as channel length and the width are reduced by the factor α, so should the vertical dimensions such as source/drain junction depth (X_j) and the gate thickness. However, if we just reduce the dimensions of the device and the power supply voltage is kept the same, then the internal electric fields in the device would increase.

For proper device scaling, power supply voltages should also be reduced to keep the internal field constant, but in practice power supply voltages have not been scaled with

the device dimension, owing of some other system related constrains. As a result, a variety of problems related to device performance have then emerged which are known as short channel and high-field effects.

Parameter	Constant Field	Constant Voltage
Length (L)	1/α	1/α
Width (W)	1/α	1/α
Gate-oxide thickness (t_{OX})	1/α	1/α
Supply Voltage (V)	1/α	1
Junction Depth (X_j)	1/α	1/α
Depletion layer thickness(d)	1/α	1/α
Substrate Doping(N_A)	α	α
Gate delay	1/α	$1/\alpha^2$
DC power Dissipation(P_S)	$1/\alpha^2$	α
Dynamic power dissipation (P_d)	$1/\alpha^2$	α
Power-delay product	$1/\alpha^3$	1/α

Table (1.1): Influence of Scaling on MOS-Device Characteristics [4].

The depletion region of the source and drain determine how small we can make the channel. In fact, the distance between the source and drain must be greater than the depletion layers to ensure that the gate is able to have a control over the channel. Therefore, in order to reduce the length of the channel, we need to reduce the depletion layers by increasing the substrate doping [4]. Changing a particular device parameter in order to improve performance (such as decreasing oxide thickness to improve current drive) can lead to an intolerable degradation in reliability [18].

2.1 Threshold Voltage

Theoretically, the threshold voltage is simply the applied gate-to-source voltage needed to turn on a MOS device. The threshold voltage for a uniformly doped long channel device can be approximated by solving the one-dimensional Poisson's equation:

For an n-channel device

$$V_T = V_{FB} + 2|\varphi_p| + \frac{1}{c_i}\sqrt{2\varepsilon_s q N_a (2|\varphi_p| - V_B)} \tag{2.1}$$

For a p channel device

$$V_T = V_{FB} - 2|\varphi_n| - \frac{1}{c_i}\sqrt{2\varepsilon_s q N_d (2|\varphi_n| + V_B)} \tag{2.2}$$

Here V_{FB} is the flat-band voltage, c_i is the insulator capacitance, q is charge carrier density, ε_s is the dielectric permittivity of the semiconductor and V_B is the bulk bias. While

$$\varphi_n = \frac{kT}{q}\ln\left(\frac{N_d}{n_i}\right) \qquad \text{and} \qquad \varphi_p = -\frac{kT}{q}\ln\left(\frac{N_a}{n_i}\right)$$

are Fermi potentials of the *n*- and *p*-channel MOS device structures; N_a and N_d are the acceptor and donor dopant concentrations in the substrates respectively, k is Boltzmann constant, T is the absolute temperature and n_i is the intrinsic electron density.

Note that the threshold voltage is strongly dependent on doping concentration. As we increase the doping level, the threshold voltage becomes more positive for an *n*-channel and more negative in a *p*-channel device.

2.2 Short-Channel Effects

Threshold voltage equations (2.1) and (2.2) are based on the solution of Poisson's equation in one dimension. They are suitable for long channel devices, for which the influence of electric fields that come from the source/drain regions is much less important than those coming from the gate, since the center of the channel is far from the source/drain region.

This is not the case for devices with short channel lengths. To calculate the threshold voltage in these cases, the full multi-dimensional charge balance must be considered. This can have a significant impact on the threshold values. In practice, short channel effects provide the lower limit of achievable channel lengths for a given technology. Short channel effects have a tendency to lower the threshold voltage for short *n*-channel devices. In turn, this leads to larger I_{off} and higher power consumption for a given voltage swing. Short channel effects also have implications on the matching of device threshold in analog circuits, since the threshold voltage for devices with different channel lengths are no longer the same.

The definition of a short channel is when the gate length L is of the same magnitude as the depletion region of the drain and source junctions. An empirical formula for short channel effect is given by the equation,

$$L < L_{min} = 0.4\left[r_j(\mu m)\, d_i(\text{Å})\, (W_d + W_s)^2\, (\mu m)^2\right]^{1/3} \qquad (2.3)$$

where L_{min} is the minimum length that the gate can have before short channel effects to be considered, by the other means as transition from long channel to a short channel behavior. The vertical dimension accounts for the oxide thickness d_i, the source and drain junction depths r_j, and the source and drain junction depletion depths W_s and W_d.

When the MOSFETs dimensions are scaled down, the MOSFETs threshold voltage V_t is directly affected in many ways as a result of reduced gate control. In other words, in short-channel devices the source and drain contacts will share the control of the depletion charges with the gate. The shared charges will become a relatively large fraction of total depletion charge, which gives rise to a shift in V_t when the gate length is decreased. In addition to that, with increasing drain-source bias, the shared charge near the drain will extend further. As a result of this extension, an additional shift in the threshold voltage will take a place known as the DIBL (Drain Induced Barrier Lowering) effect.

2.2.1 Drain Induced Barrier Lowering (DIBL)

The threshold voltage is a measure of the strength of the barrier against carrier injection from the source to the channel [3]. In the short-channel regime (equation (2.3)), this

barrier may be significantly modified by the application of a drain bias as shown in figure (2.1). As the voltage between the source and drain increases, the depletion region under the drain will lower the potential barrier from the source to the channel junction.

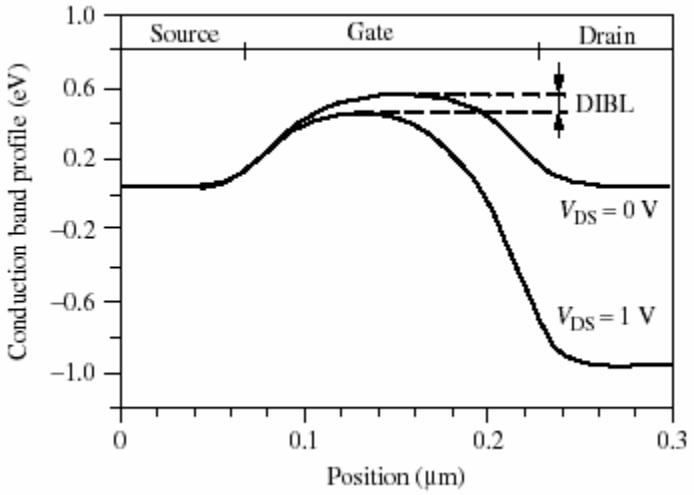

Fig. (2.1): Conduction band profile at the semiconductor–oxide interface of a short n-channel MOSFET with and without drain bias. The figure indicates the origin of DIBL [3].

When the barrier between the source and the channel is decreased, there will be more injected electrons into the channel region causes excess injection of charge carries into the channel and gives rise to an increased subthreshold current [16], [19]. This results in a lowering of the threshold voltage and the gate has reduced control over the channel current.

The DIBL effect on the threshold voltage can be expressed as:

$$V_T(L) = V_{TO}(L) - \sigma(L)V_{DS} \tag{2.4}$$

where $V_{TO}(L)$ can be describe as the scaling of V_T at zero drain bias resulting from charge sharing and $\sigma(L)$ is the channel length dependant DIBL parameter.

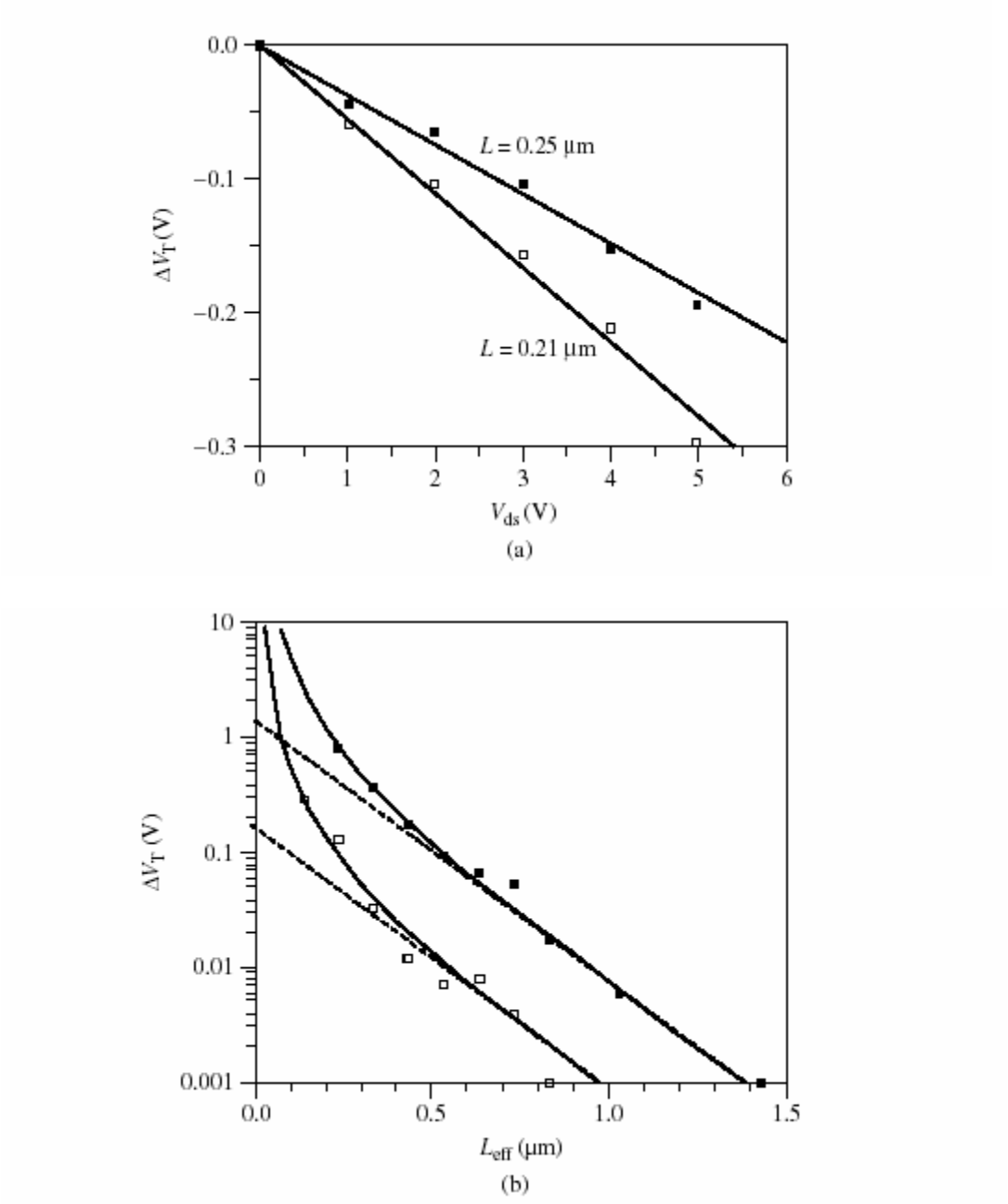

Fig. (2.2): DIBL effect: (a) threshold voltage shift versus drain-source voltage for two n-MOSFETs with different gate lengths and (b) threshold voltage shifts versus gate length [3].

2.2.3 Gate leakage and effective oxide thickness

Furthermore, under quantum theory, there is a finite chance that carriers could tunnel through the oxide barrier and result in non-zero gate current we can assume that the gate

currents for MOS device are negligible, but this is no longer holds in the deep sub-micron regime.

Direct tunneling gate current through the insulator thickness has a huge impact on the device characteristics with oxide thicknesses approaching 1 nm, and it can not be ignored.

This non-zero gate current has several implications on device operation. The gate current leaks away the inversion charge, leading to abnormal capacitance-voltage curves. This makes the task of estimating the effective electrical oxide thickness more difficult. Moreover, it contributes to the leakage current of the device. It is estimated that for nitride oxides, the gate tunneling current would replace the source/drain leakage current as the dominant component of off-currents for devices in the 50 nm technology nodes and beyond. This in turn imposes a lower limit on the allowable dielectric thickness. The increased leakage current also degrades the operation of dynamic CMOS circuit techniques.

An active area of research is the use of alternative high-permeability (high-K) material as the gate insulator. The goal is to maintain a high level of inversion charge with a thicker gate insulator layer than the SiO2 case. This minimizes the gate currents and at the same time allows device scaling to continue.

2.3 High-Field Effects

In the past decade, it was assumed that the drift current is proportional to the electric field. This assumption is valid over a wide range of E. However, since the electric field in the channel tends to increase while MOSFET's are scaled down to sub-micrometer dimensions, large electric field can cause the drift velocity and therefore the current to exhibit a sub-linear dependence on the electric field [8]. Short-channel MOSFETs may experience high electric fields if the drain-source voltage is large. While the drift velocity of carriers saturate at high fields, the instantaneous velocity and hence the kinetic energy of the carriers continues to increase, especially as they accelerate towards the drain. These are called hot carriers. In the surrounding area of the drain region, hot carriers may strike the silicon atoms at high speeds, thereby creating impact ionization [20]. As a

result, new electrons and holes are generated, with the electrons absorbed by the drain and the holes by the substrate. Thus, a finite substrate current appears. Moreover, if the carriers acquire a very high energy, they may be injected into the gate oxide and even flow out the gate terminal, introducing a gate current.

The substrate and gate currents are often measured to study hot carrier effects.

The scaling of technologies proceeds so as to minimize hot carrier effects. This limitation and other breakdown phenomena make the supply voltage scaling inevitable.

2.3.1 Channel-length modulation

When the drain-source bias of a FET approaches the drain saturation voltage, a region of high electric field forms near the drain and the electron velocity in this region saturates. In saturation, the length ΔL of the high-field region expands in the direction of the source with increasing V_{DS}, and the MOSFET behaves as if the effective channel length has been reduced by ΔL. This phenomenon is called channel-length modulation (CLM) [3]. The following simplified expression links V_{DS} to the length of the saturated region:

$$V_{DS} = V_p + V_\alpha \left[\exp\left(\frac{\Delta L}{\ell} \right) - 1 \right] \tag{2.5}$$

where V_p, V_α, and ℓ are parameters related to the electron saturation velocity, the field effect mobility, and the drain conductance in the saturation regime. In fact, V_p is the potential at the point of saturation in the channel, which is usually approximated by the saturation voltage V_{sat}. The CLM effect can be described by the output conductance in saturation, which tends to remain constant over a wide range of drain biases. The output conductance increases with increasing the gate bias.

CHAPTER 3

The Nature of Physically-Based Devices Simulation

As mentioned before ATLAS is a physically-based device simulation program [14]. It predicts the electrical characteristics that are associated with specified physical structures and bias conditions. This is achieved by approximating the operation of a device into a two or three dimensional grid, consisting of a number of grid points called nodes. By applying a set of differential equations, derived from Maxwell's laws, into this grid we can simulate the transport of carriers through such structure. This means that the electrical performance of a device can now be modeled in dc, ac or transient modes of operation.

A device structure can be defined in three different ways for use in ATLAS.

The first way is to read an existing structure from a file. The structure is created either by an earlier ATLAS run or another program such as ATHENA or DEVEDIT. A mesh statement loads in the mesh, geometry, electrode positions, and doping of the structure.

The second way is to use the Automatic Interface feature from Deck-build to transfer the input structure from ATHENA or DEVEDIT.

The third way is the one that has been performed in implementing the simulations in this thesis, where the structures of the devices have been created by using the ATLAS command language.

To define a device through the ATLAS command language, we must first define a mesh. This mesh or grid covers the physical simulation domain. The mesh is defined by a series of horizontal and vertical lines and defining spaces between them. Then, regions within this mesh are allocated to different materials as required to construct the device. The definition of a MOSFET device requires the specification of silicon and silicon dioxide regions. After the regions are defined, the locations of the electrodes must be specified. The final step is to specify the doping in each region.

3.1 Define a Device Structure

When using the command language to define a structure, the information described in the following four sub-sections must be specified in the order listed [14].

3.1.1 Specifying the Initial Mesh

The first statement must be: **mesh space.mult =<value>**, then it will be followed by a series of **x.mesh** and **y.mesh** statements.

x.mesh location= <value> spacing=<value>

y.mesh location= <value> spacing=<value>

The **space.mult** parameter value is used as a scaling factor for the mesh that created by the **x.mesh** and **y.mesh** statements. The default value is 1. Values greater than 1 will create a coarser mesh for fast simulation. Values less than 1 will create a finer mesh for increased accuracy. The x and y mesh statements are used to specify the locations in microns of vertical and horizontal lines, respectively, together with the vertical or horizontal spacing associated with that line. At least two mesh lines must be specified for each direction. ATLAS automatically inserts any new lines required to allow for gradual transitions in

the spacing values between any adjacent lines. The x and y mesh statements must be listed in the order of increasing x and y. Both negative and positive values of x and y are allowed.

3.1.2 Specifying Regions and electrodes

Once the mesh is specified, every part of it must be assigned to a material type. This is done with **region** statements. For example:

region number = <integer> <material_type> <position parameters>

Region numbers must start at 1 and are increased for each subsequent region statement. If a composition-dependent material type is defined, the x and y composition fractions can also be specified in the **region** statement.

The position parameters are specified in micrometers using the **x.min, x.max, y.min**, and **y.max** parameters. Materials must be assigned to all mesh points in the structure. If this is not done, error messages will appear and ATLAS would not run successfully.

We can use the **material** statement to specify the material properties of the defined regions. But we must first complete the entire mesh and doping definition before any **material** statements can be used. Materials are divided into three classes: semiconductors, insulators and conductors. Each class requires a different set of parameters to be specified. For semiconductors, these properties include electron affinity, band gap, density of states and saturation velocities.

The **material** statement is used to specify material name or a specified region. For example, the statement:

material material = silicon EG=1.12 MUN=1100

This sets the band gap and low field electron mobility in all silicon regions in the device.

Once we have specified the regions and materials, we must define at least one electrode that contacts a semiconductor material. This is done with the electrode statement. For example:

electrode name = <electrode name> <position_parameters>

The position parameters are specified in micrometers using the **x.min**, **x.max**, **y.min**, and **y.max** parameters. Multiple electrode statements may have the same electrode name (e.g. multiple gates). Nodes that are associated with the same electrode name are treated as being electrically connected. Some shortcuts can be used when defining the location of an electrode. If no y coordinate parameters are specified, the electrode is assumed to be located on the top of the structure. Right, left, top, and bottom parameters can be used to define the location.

For example: electrode **name=source left length=0.5**

This specifies the source electrode to start at the top left corner of the structure and extends to the right for the distance length.

3.1.3 Specifying Doping Distribution

We can specify analytical doping distributions, or have ATLAS read in profiles that come from other process simulations. In the thesis frame work we only use the analytical doping distributions, by specifying the doping using the **doping** statement, as followed:

doping <distribution_type> <dopant_type> <position_parameters>

Analytical doping profiles can have uniform or Gaussian forms. The parameters defining the analytical distribution are specified in the **doping** statement.

doping uniform concentration=<value> < dopan_type> region=number

doping gaussian concentration =<value> characteristics=<standard deviation> <dopant_type> x.left=<value> x.right=<value> peak=<value>

The first **doping** statement specifies a uniform dopant type of a density per cm^3 in the region which is labelled as an integer region number.

The second **doping** statement specifies a Gaussian dopant type profile with a peak concentration of density per cm^3. This statement specifies that the peak doping is located along horizontal line from **x.left** to **x.right**. In the vertical line, the doping drops off according to a Gaussian distribution with a standard deviation of some values of the micrometers.

3.1.4 Specifying Physical Models

Physical models are specified using the **models** and **impact** statements. The physical models can be grouped into five classes: Mobility, Recombination, Carrier Statistics, Impact Ionization, and Tunneling. All models with the exception of impact ionization are specified on the models statement. Impact ionization must be specified in the **impact** statement. Examples of physical models statements can be used as followed:

```
Models   conmob fldmob   srh   fermidirac

Impact   selb
```

It specifies that the standard concentration dependent mobility (**conmob**), parallel field mobility (**fldmob**), Shockley-Read-Hall recombination (**srh**) with fixed carrier lifetimes, Fermi Dirac statistics (**fermidirac**) and Selberherr (**selb**) impact ionization models should be used.

3.1.5 Obtaining Solutions and Parameter Extraction

ATLAS is able to calculate dc, ac small signal, and transient solutions. Usually the voltages on each of the electrodes in the device are defined. ATLAS then calculates the current through each electrode. ATLAS also calculates many internal quantities, such as potential profile, carrier concentrations, electric fields, and energy band throughout the device. This information is difficult to measure.

In all simulations, the device starts with zero bias on all electrodes. Solutions will be obtained by stepping the biases on electrodes from the initial equilibrium condition and then saving results using the **log** or **save** statements.

In dc solutions, the voltage on each electrode is specified using the **solve** statement as followed:

```
solve vgate=1.0

solve vgate=2.0
```

That solves a single bias point with 1.0 V and then 2.0 V on the gate electrode. When the voltage on any electrode is not specified in a given **solve** statement, the value from the last **solve** statement will be assigned to the electrode.

Another solution is for a drain voltage of 1.0 V and a gate voltage of 2.0 V as followed:

```
solve vgate=2.0

solve vdrain=1.0
```

When the voltage on a particular electrode is not defined in a **solve** statement, the voltage is zero, for example in a MOSFET, if vsubstrate is not specified, then V_{bs} defaults to zero.

The **extract** command is provided within the Deckbuilt environment. It is a useful way to extract device parameters. A typical example of using **extract** is the extraction of the threshold voltage of an MOS transistor. The threshold voltage is extracted by calculating the maximum slope of the I_{ds} / V_{gs} curve, finding the V_{gs} and then subtracting half of the applied drain bias.

```
Extract   name=" nvt"   xintercept ( maxslope (curve (v. " gate ", ( i. " drain "))) -
                        ( ave ( v. " drain "))/2.0)
```

The results of the extraction will be displayed in the run-time output and will be stored in the file **results.final**.

3.2 Mobility Modeling

Electrons and holes are accelerated by electric fields, but their momentum will be reduced as a result of various scattering processes. The scattering mechanisms include lattice vibrations (phonons), impurity ions, carrier mobility in inversion layers. This mechanism will directly affect all mobility transport within the channel, where the mobility transport equations are therefore functions of the electric field, temperature, and doping concentration.

Mobility modeling is normally divided into: low field behavior, high field behavior, and substrate doping and inversion layers.

The low electric field behavior has carriers almost in equilibrium. The mobility is related to phonon and impurity scattering.

But high electric field behavior shows that the carrier mobility declines with electric field because the carriers that gain energy can take part in a wider range of scattering processes. The mean drift velocity no longer increases linearly with increasing electric field, but rises more slowly. In the long run, the velocity does not increase any more with increasing field but saturates at a constant velocity. Impurity scattering is irrelevant for energetic carriers, and so velocity saturation for the most part is a function of the lattice temperature. Modeling mobility in substrate material includes: mobility of electrons and holes as a function of doping and lattice temperature, characterizing velocity saturation as a function of lattice temperature, and describing the transition between the low field mobility and saturated velocity regions. Carrier mobility in inversion layers is subjected to surface scattering, and quantum mechanical effects.

These effects must be accounted in order to perform accurate simulation of MOS devices. The transverse electric field is often used as a parameter that indicates the strength of inversion layer phenomena

3.2.1 Low Field Mobility Models

The low field carrier mobility can be defined by using ***(*conmob*)*** to relate the low field mobility at 300K to the impurity concentration, or by choosing a carrier-carrier scattering model (**ccsmob**) that relates the low field mobility to the carrier concentrations and temperature.

3.2.2. Inversion Layer Mobility Models

To obtain accurate results for MOSFET's simulations, we have to account for the mobility degradation that occurs inside inversion layers. The degradation normally occurs as a result of the higher surface scattering near the silicon to insulator interface.

ATLAS treats the effects of mobility degradation by three methods: the first one is a surface degradation model (**surfmob**); the second way is by using transverse electric field

shirahata model. Or by specifying inversion layer mobility **cvt, yamaguchi,** and **tasch** models

The **cvt, yamaguchi**, and **tasch** models are assigned as separate models which include all the effects required for simulating the carrier mobility.

3.2.3 Grid Sensitivity

Physical models, involving highly non-linear terms as well as complex coupled equations will tighten requirements on both the grid and solver technologies, are needed for modeling short channel effects. Addition of the poly depletion effect requires physical simulation of the poly-silicon gate region. In the bulk, sufficient grid density is needed for calculation of the series resistance, and to resolve the lateral abruptness of source/drain junctions.

All these impose constraints on the minimum grid that can be used.

At the same time, we must avoid excessively dense grids which lead to unreasonable simulation times. This is especially important for devices where a large number of simulations is required.

The optimal grid required for simulation of short channel devices is related not only to the doping profiles, but also to the choice of physical models. Scaling the device dimensions necessitates the emergence of more complicated models, introducing additional nonlinearities, to account for poly depletion, quantization effects as well as bias dependence of carrier mobility. These models impose more severe constraints on the grid needed for convergence and accuracy. It is therefore important to talk about grid sensitivities in the framework of specific physical models [14].

CHAPTER 4

Silicon Based Semiconductor Device Design

4.1 Classical MOSFET

The classical MOSFET can be thought to consist of two perpendicular 1D device; a lateral device composed of a resistive channel with two ohmic contacts called source and drain and a perpendicular MOS device that controls the mobile charge by capacitive coupling which has been denoted as the field effect.

Generally, in a MOSFET a layer of silicon dioxide is placed between the gate contact and the channel for electrical isolation. The charge carriers of the conducting channel will consist of an inversion charge at the Si-SiO_2 interface whenever a sufficiently high voltage is applied to the gate electrode. The onset of strong inversion is defined in terms of a threshold voltage V_t applied to the gate relatively to source. When a bias voltage is applied to the gate, the dioxide layer will block charge carrier transport between gate and channel, owing to its high resistivity.

First, we test the Device 2D ATLAS software package simulator from Silvaco, by considering classical *n*-channel MOSFETs with lengths of 250 and 210 nm. The schematic geometry view is showed below:

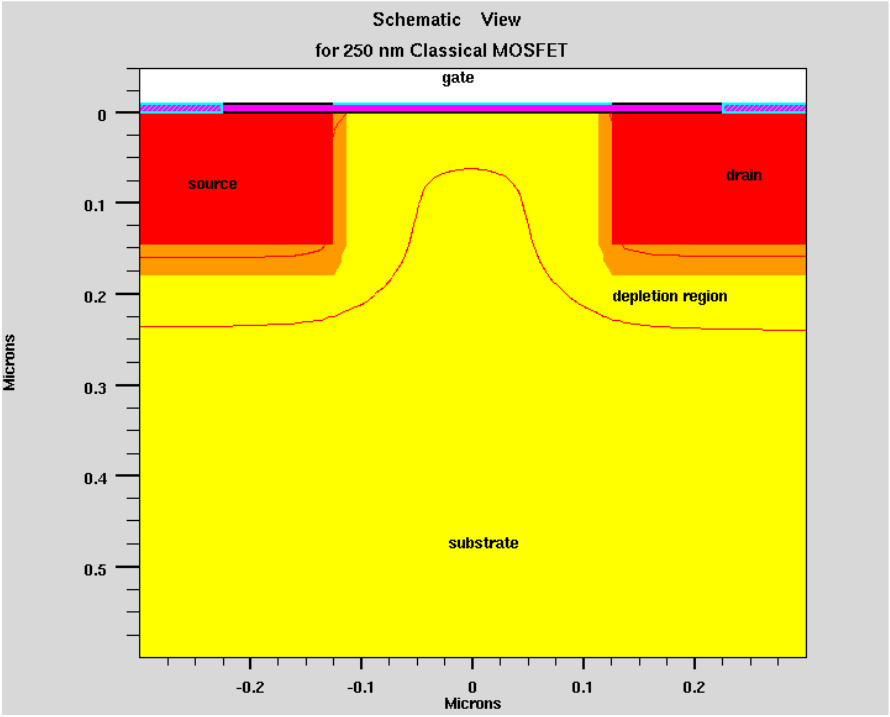

Fig. (4.1): shows the schematic view of a simulated long channel MOSFET. The red line indicates the depletion region.

To achieve a proper simulation result, we build up the device to be more comparable to the modeling work that was been carried out in [2]. First we used a lightly doped substrate of $2x10^{17}$ cm^{-3} and a silicon dioxide with thickness of 8.6 nm. We specified the junction depth for the Source and Drain in the all cases to be 0.16 µm. Beside that, we defined the doping concentration for the drain and source to have a Gaussian distribution profile of a maximum doping concentration of $1.4x10^{18}$ cm^{-3} at the surface and a standard deviation of $1.0x10^{-2}$ µm.

Results for the channel potential profile, and DIBL effect are compared to the model results in [2]. In addition to that, the substrate doping concentration and the dioxide

dielectric material thickness were modified to $4x10^{17}$ cm^{-3} and 5.6 nm, respectively, and sub-threshold characteristics are calculated.

The figures below show the vertical cut of the net doping profile within the drain- and source-contact regions (donor doping $1.2x10^{18}cm^{-3}$) into the substrate (acceptor doping $1.8x10^{17}cm^{-3}$). The oxide thickness is 8.6 nm.

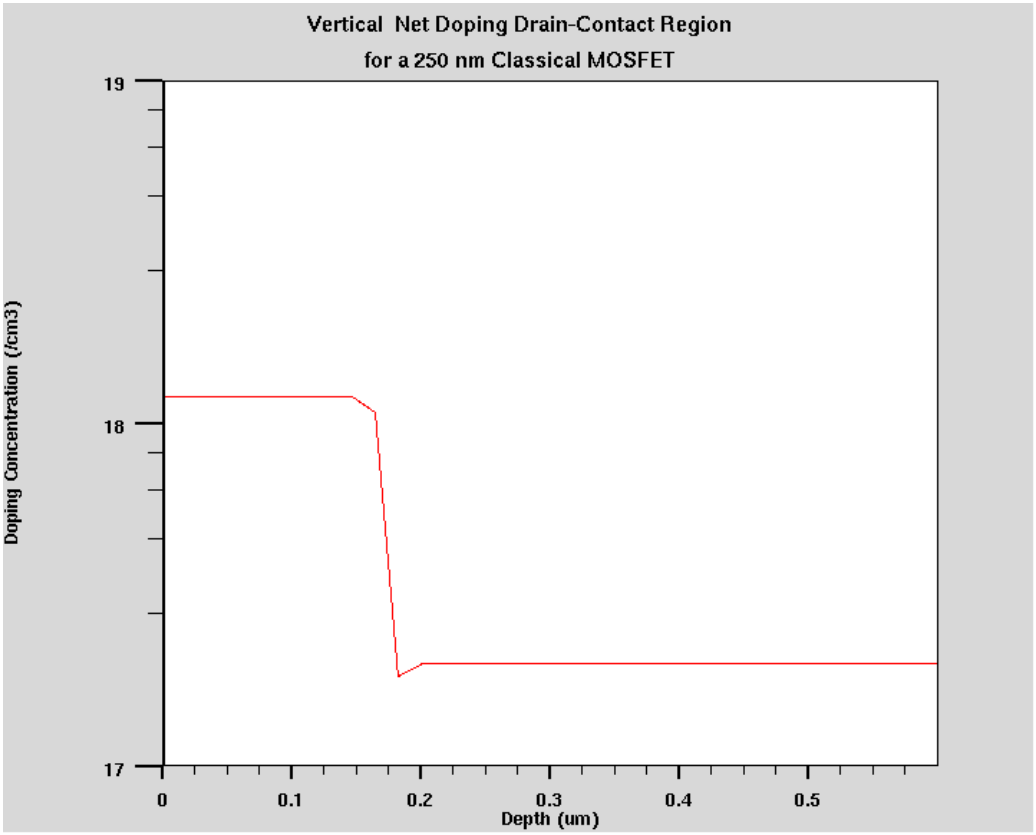

Fig. (4.2): Vertical cut of net doping profile within the drain-contact region for a 250 nm classical MOSFET.

4.2 Super-steep-retrograde channel MOSFET

The short channel effects resulting from the down-scaling of the classical MOSFET may be compensated by improved engineering techniques. The most practical method is by changing the doping profile in the channel region, then the distribution of the electric field and potential contours can be changed.

The goal is to optimize the channel profile so as to minimize of the off-state leakage, maximize the linearity, and optimize the saturation characteristics.

Super Steep Retrograde MOSFETs have been used as a means of scaling the channel length beyond the sub-100 nm range. The implementation of this technique enables suppression of several unfavorable effects that appear from imposing higher substrate doping which comes from the need to contain the source and drain depletion layers.

For a MOS device with a uniform doping, the maximum depletion depth and the threshold voltage cannot be controlled independently from each other. A uniform doping level that yields acceptable depletion depth (and thus short channel effects) may lead to undesirable threshold voltages.

Super-Steep-Retrograde MOSFET utilizes lower retrograde doping profile toward the Si-SiO_2 interface and a high doping deeper under the surface. The use of a low-high (retrograde) doping profile is to provide a full decoupling of the control of short channel effects from the threshold voltage level [15].

The N-type source and drain contacts are designed to have shallow but highly doped extensions connecting the channel, with a deeper doping further on.

We considered an *n*-channel Super-Steep-Retrograde channel MOSFET device with a 70 nm gate length as in [2]. This device has a retrograde doping of about $2.8 \times 10^{17} cm^{-3}$ at the surface that increases to about 1.8×10^{18} cm^{-3} at the depth of 60 nm. An advantage of the present device design is the used of very shallow source and drain extensions with a thickness of 50 nm.

In the simulation, the device substrate doping was approximated in the same way as in the SSR MOSFET mentioned in [2], using a two-layer structure each with a constant doping. We have assigned the thickness and the doping concentration to be 35 nm and

$9.2x10^{17}$ cm^{-3}, respectively, in the retrograde region close to the surface. For the rest of substrate, the higher substrate doping was used to be $1x10^{18}$ cm^{-3}, which was enough to contain the source and drain depletion layer.

In addition, we assumed that the source and drain contacts and the extension regions to have a Gaussian distribution profile of maximum $1x10^{20}cm^{-3}$ with a standard deviation of $1.2x10^{-2}$µm.

Reducing the source and drain extension junction depth will improve the short channel characteristics by reducing the amount of channel charge controlled by the drain. The potential contours extend further into the channel for devices with deep junctions.

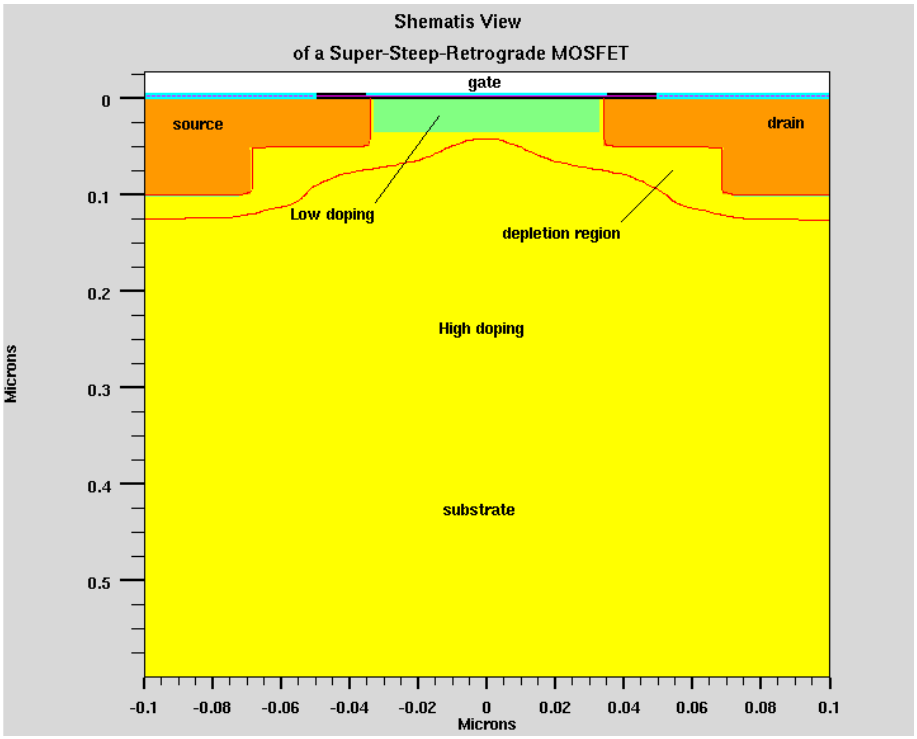

Fig. (4.3): shows the schematic view of a 70 nm Super-Steep-Retrograde MOSFET. The lower red line indicates the depletion region.

The simulated SSR MOSFET has an N+ polysilicon gate, and a silicon nitride oxide with 3 nm thickness.

The resulting structure of the SSR MOSFET in figure (4.3) has a general agreement with the schematic geometry showed in the model paper [2]. The device reflects that the depletion layer stretches into the higher doped region, which insures that the thickness is well protected from further penetration by the gate depletion layer.

The Channel Engineering type identifies specific doping and deposition solutions for simultaneously meeting threshold voltage, channel mobility, and sub-threshold current requirements of the developing device structures. We expect the channel engineering to apply to almost all device approaches in the future, with highly doped and super steep retrograde channels giving way to low doped devices for full-depleted SOI and multiple gate devices.

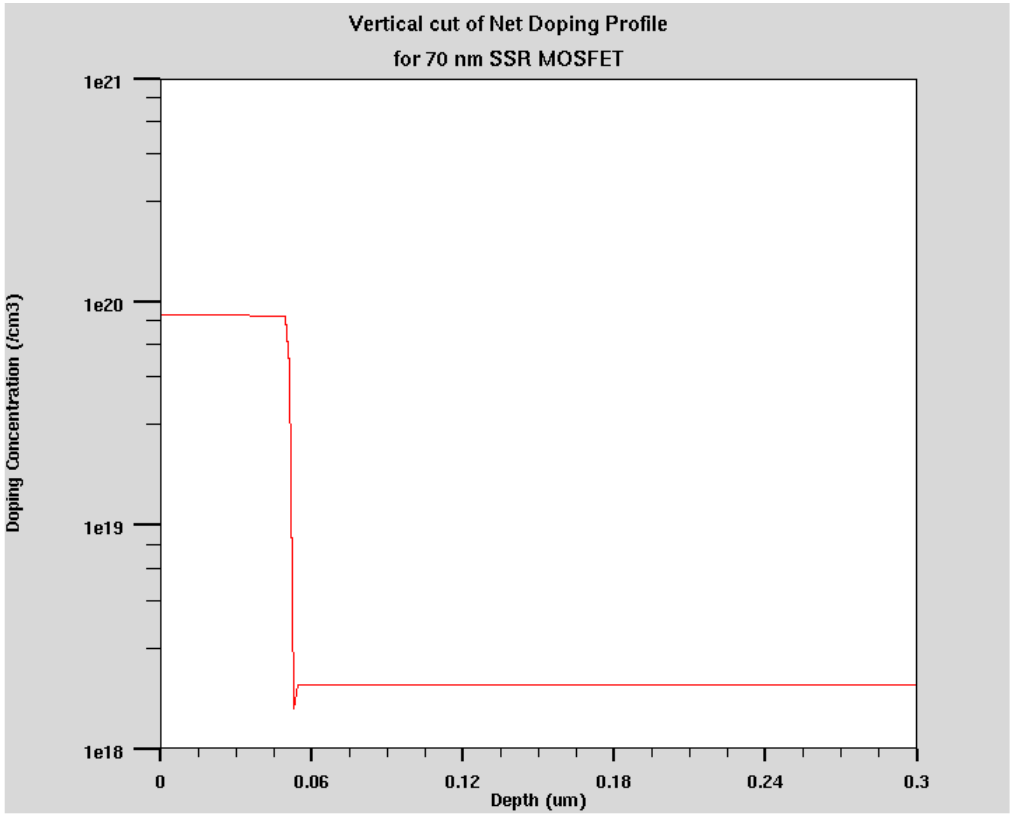

Fig. (4.4): Vertical cut of net doping profile within the drain-contact region for a 70 nm Super-Steep-Retrograde MOSFET.

4.3 Template Bulk MOSFET

The traditional scaling of CMOS devices that have served the semiconductor industry for over two decades is becoming increasingly impractical due to rising off-state power consumption, as a consequence, introduction of new materials and device structures are anticipated within the next years to come.

Challenges for scaling MOSFETs, can consist of controlling leakage currents and short-channel effects; increasing saturation current while reducing the power supply; controlling the device parameters (e.g., threshold voltage, leakage) across the chip and from chip to chip.

New transistor structures seek to improve the electrostatics of the MOSFET, and provide a platform for introduction of new materials, which include the high-κ dielectric and electrode materials. Thicker dielectric layers can be used; the same inversion layer characteristics can be maintained, less carrier tunnelling, and they will permit further scaling of the effective oxide thickness.

Additionally, the combination of new device structures and new materials enables new operating principles that may provide new behaviour and functionality beyond the constraints of bulk planar or classical CMOS.

However, the projected device structures of Bulk MOSFET and a DG-SOI MOSFET with a gate length of 25 nm are conceived to accompany the high-performance MOSFETs of the forthcoming 65 nm technology node [10].

4.3.1 Source/Drain Contact

The channel doping profile is not the only thing important for device performance.

The doping profile in the source/drain region can also have an impact on short channel effects. The conventional means of shunting the contact regions with a self-aligned silicide will be challenged by the need to achieve low gate sheet resistivity while at the same time continuously minimizing silicon consumption in the source/drain contact

region. In addition, scaling of the contact area will result in undesirable parasitic resistance if the specific contact resistivity of the silicon/silicide interface cannot be correspondingly reduced. The achievement of an acceptable contact resistivity will require that the maximum concentration of activated dopant be achieved in the silicon at the silicide interface, and may also require that the metal/semiconductor barrier height be reduced. As a result, considerable effort has been put into the optimization of the source/drain doping by the semiconductor industry.

However, to compensate the increase of the substrate doping density, the need of the source/drain extension region in modern device design is more essential for avoiding the detrimental hot electron effects [1].

4.3.2 Source/Drain Extension

The source/drain extension is a commonly found feature in modern MOS device. It was originally motivated by a desire to reduce high electric fields and the resulting breakdown of the device due to hot electron effects; for high performance devices however, the source/drain extension is motivated more by the trade-offs between short channel effects and source/drain resistance.

The short channel effects improve with decreasing junction depths in the source/drain region. However, source/drain junctions would lead to high extrinsic resistances, which is detrimental to the device performance. The source/drain extension presents a shallow effective source/drain junction to the channel region, while at the same time, minimizes the contribution of the source/drain region to extrinsic resistance through the presence of the deep source/drain region.

4.3.3 Lateral Source/Drain Abruptness

A key parameter in the source/drain extension region is the lateral doping abruptness. An abrupt junction is important for drain current drive; the spreading resistance depends on lateral abruptness.

The formulation of shallow and abrupt source-drain (S/D) extension junctions is a significant challenge in the continued scaling of MOSFET transistor technology beyond the 65 nm technology node. According to the ITRS [1], bulk-Si MOSFET devices with physical gate lengths ≤ 50 nm will require ultra-shallow S/D extension junctions (junction depth $x_j \leq 30$ nm) for acceptable short channel performance. In addition to being very shallow, extension junctions will also need to be heavily doped in order to meet roadmap requirements for the S/D series resistance ($R_s \leq 200\ \Omega$) to improve device drive current and extremely abrupt (slope ≤ 3 nm) for improved short channel performance.

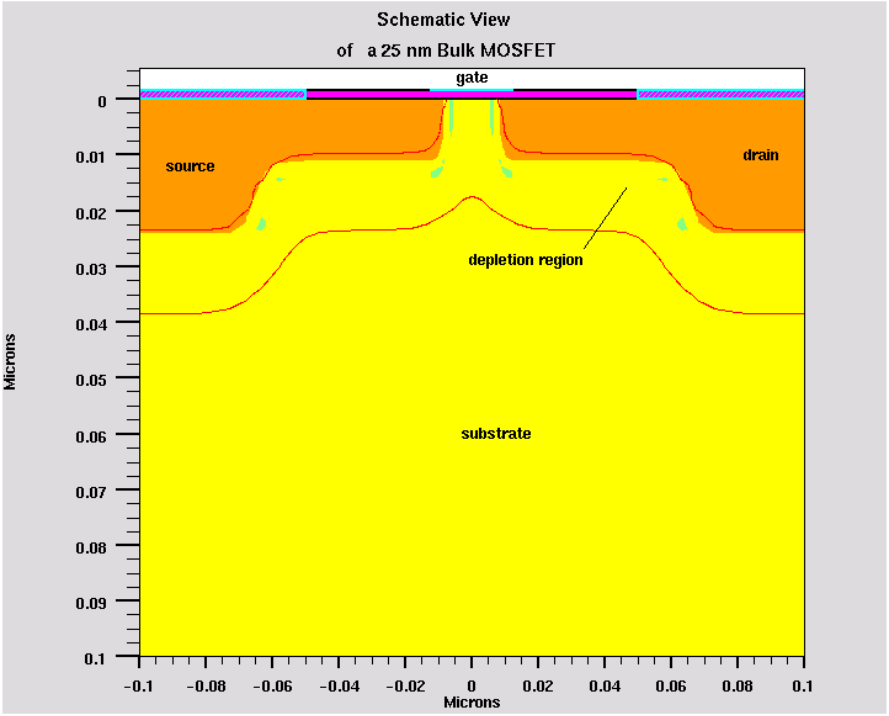

Fig. (4.5): shows the schematic geometry view of a 25 nm Bulk MOSFET. The red line indicates the depletion region.

The doping profile for the bulk and the SOI devices are set to be identical with the obvious exception of the depth of the SOI source-drain junctions that are limited by the silicon thickness of for example 12 nm.

The oxide features a physical thickness of 1.6 nm and $\varepsilon_{OX} = 7\ \varepsilon_O$ for a nitride gate oxide.

The two-dimensional doping profile of the extension is assumed to be well-described by a function of the form

$$N(x, y) = G(y).L(x)$$

where $G(y)$ represents the profile along the vertical direction and $L(x)$ describe the lateral diffusion [10].

To simplify the definition of lateral abruptness, exponentially varying doping is assumed at the junctions. To simplify the simulations, and to isolate the effects of the lateral abruptness, a uniform channel doping is used with the value of $3x10^{18}cm^{-3}$ for the Bulk MOSFET, while the vertical and the lateral doping profile of the extension are varied. The lateral abruptness has dropped down from $10^{20}cm^{-3}$ down to $10^{18}cm^{-3}$.

Meanwhile, the N-type extension source/drain profiles are assumed to have Gaussian distributions with a peak concentration of $1x10^{20}cm^{-3}$ at $y = 0$ and the standard deviation of $\sigma_y = 5.64x10^{-3}\ \mu m$

for the vertical direction of y its given as follows:

$$G(y) = N_{peak}.e^{-\frac{1}{2}\left[\frac{y}{\sigma y}\right]^2} \quad ; \qquad y > 0 \tag{4.2}$$

and for lateral direction of x its given by:

$$L(x) = 1 \quad ; \qquad x < x_0 \tag{4.3}$$

where x_0 is lateral length of the source/drain extensions.

$$L(x) = e^{-\frac{1}{2}\left[\frac{x - x_0}{0.28.\sigma_y}\right]^2} \quad ; \qquad x > x_0 \tag{4.4}$$

On the other hand, the N-type of the source-drain contacts profile have the peak concentration of $1x10^{20}cm^{-3}$ in $y = 0$ and standard deviation of $\sigma_y = 1.12x10^{-2}\ \mu m$

for the vertical direction of y its given as follows:

$$G(y) = N_{peak}.e^{-\frac{1}{2}\left[\frac{y}{\sigma_y}\right]^2} \quad ; \qquad y > 0 \tag{4.5}$$

and for lateral direction of x its given by:

$$L(x) = 1 \quad ; \qquad x < x_1 \tag{4.6}$$

$$L(x) = e^{-\frac{1}{2}\left[\frac{x-x_0}{0.35.\sigma_y}\right]^2} \quad ; \qquad x > x_1 \tag{4.7}$$

and x_1 is lateral length of the source/drain contacts.

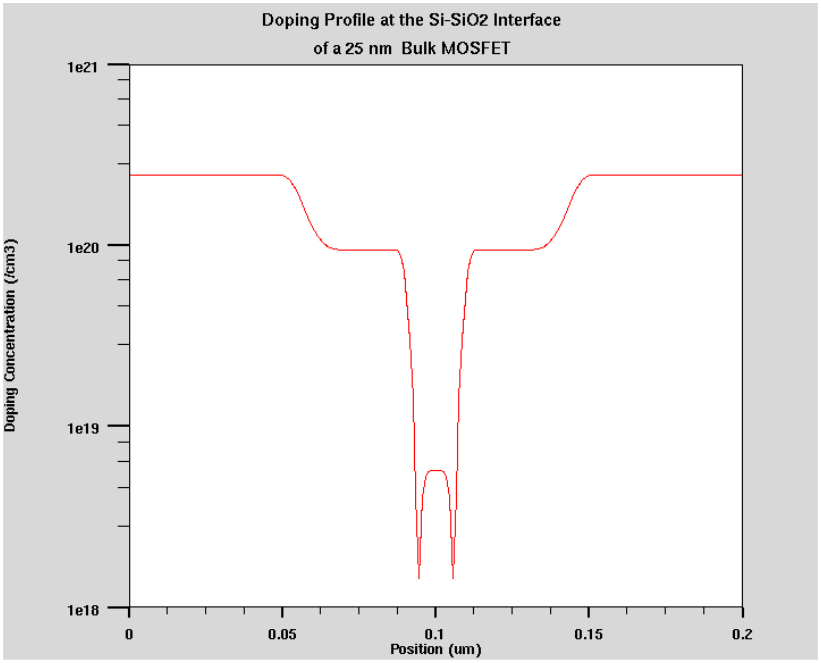

Fig. (4.6): The net doping profile at the Si-SiO_2 interface (middle region) of a 25 nm Bulk MOSFET along the device.

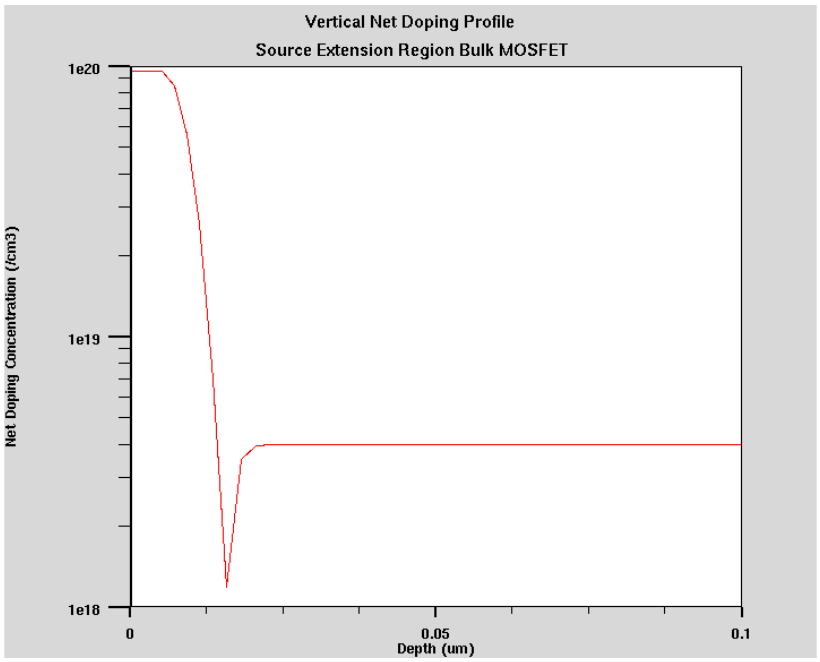

Fig. (4.7): Vertical cut of the net doping profile within the source extension region at (x=-0.025 µm)

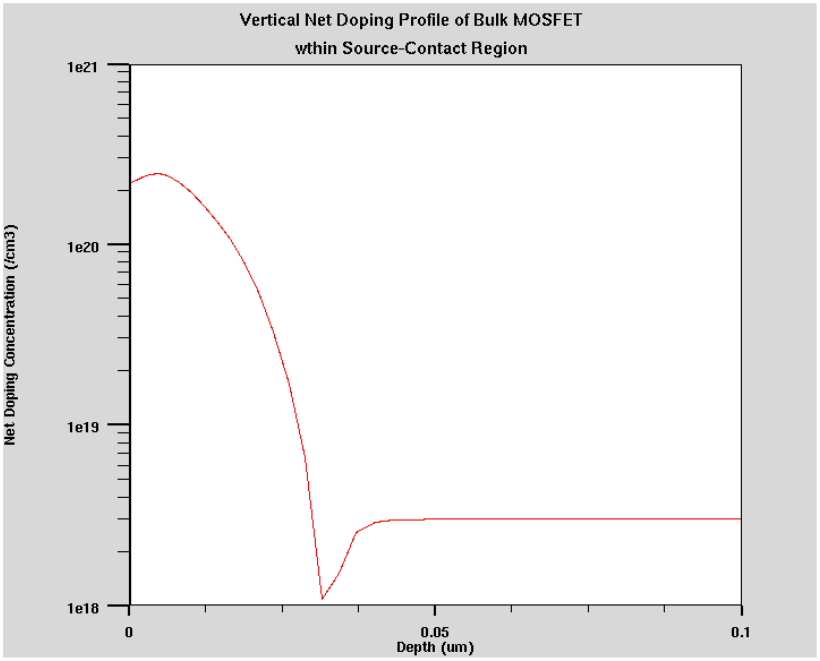

Fig. (4.8): Vertical cut of the net doping profile within the source contact region at (x=-0.075 µm)

4.4 Double-Gate SOI MOSFET

The Double-gate SOI MOSFET structure has been proposed to further improve engineering of the channel electrostatics and, in some cases, to provide independent control of the two isolated gates for the benefit of low-power [1].

A Double-gate transistor is a device in which the current flows horizontally (parallel to the plane of the substrate) between the source and drain, along opposite channel surfaces. The thickness of the silicon body is small (smaller than the channel length) to provide adequate control of short-channel effects.

Double-gate MOSFETs are promising devices for the future of a high-performance CMOS circuits. The main reason is their internal structure that reduces the short channel effects. In the double-gate configuration, the passive substrate is replaced by actively biased gates, so that the channel is controlled by top and bottom gates which are self-aligned to each other. Unlike single gate MOSFETs, $t_{ox1} = t_{ox2}$ in DG MOSFETs for effective short channel effects control. The short channel effect is suppressed in this structure because there is no part of the channel which is far away from a gate electrode. Ideally, the drain and source electric field lines should end on the dual gates, which allows the drain and source to be coupled from each other. Thus, the leakage current is controlled and V_t roll-off is suppressed along with DIBL.

As seen from the simulation of DG MOSFETs, the scaling advantage of the device is best achieved by a thin silicon body, where charge transport is governed by quantum effects, causing the threshold voltage of the DG MOSFET to be more sensitive to the variation of thicknesses [12]. Then the peak inversion layer electron concentration will be shifted away from the gate oxides and toward the centre of the silicon body in the device. In the DG MOSFETs, the electric field is defined by both the front- and back-gate oxide barriers and the quantum effect is governed by electric field in the body.

As mentioned above the doping profile for the bulk and the DG-SOI MOSFET devices are set to be identical with the obvious exception of the depth of the SOI source-drain junctions that are limited by the silicon thickness of 12 nm and the substrate doping of SOI silicon film is limited to $10^{15}cm^{-3}$, it is assumed to be uniform[10] .

The *N*-type source/drain profiles of the DG-SOI MOSFETs are assumed to be similar to that of the *N*-type Bulk MOSFETs. Meanwhile, due to a much lower concentration of the silicon layer, the *N*-type lateral profile of the source/drain extensions drops down to very low concentration as shown in figure (4.10) below, with a very large lateral abruptness profile at or below 1.5 nm as the doping converts from 10^{20}cm^{-3} *N*-type to 10^{15}cm^{-3} *P*-type.

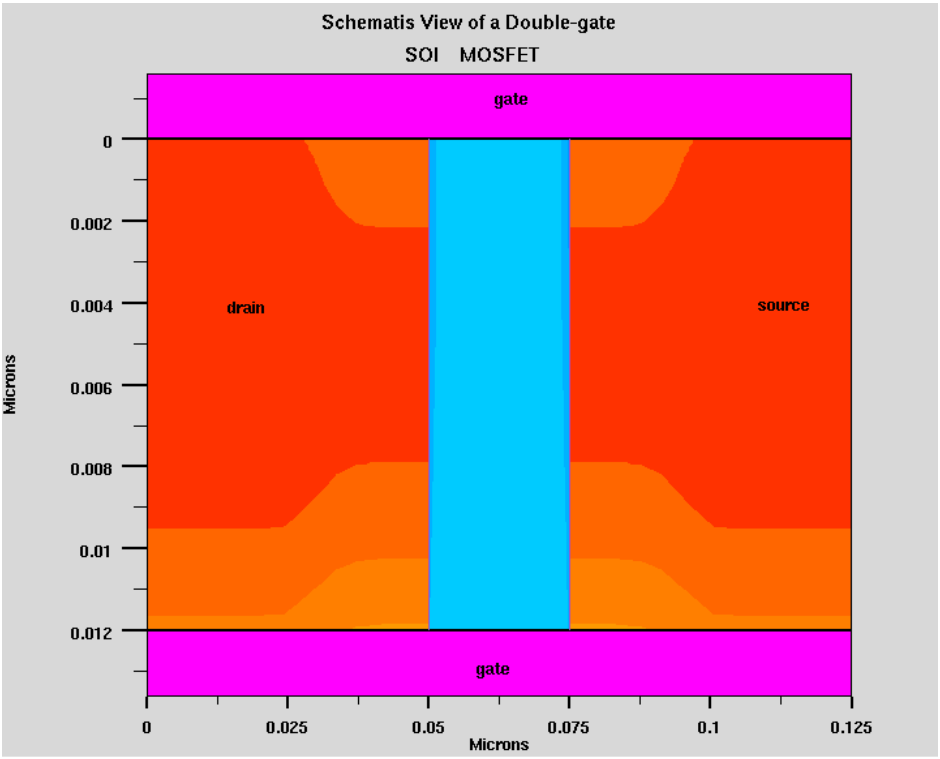

Fig. (4.9): shows the schematic geometry view of a 25 nm Double-gate SOI MOSFET.

4.4.1 *N*-type extensions source-drain profiles

The *N*-type source/drain extension profiles are assumed to have Gaussian distributions with a peak concentration of $1x10^{20}$cm^{-3} in $y = 0$ and the standard deviation of $\sigma_y = 5.64x10^{-3}\,\mu m$.

The two-dimensional doping profile of the extension is assumed to be well-described by a function of the form

$$N(x,y) = G(y).L(x)$$

where $G(y)$ represents the profile along the vertical direction and $L(x)$ describe the lateral diffusion [10].

for the vertical direction of y its given as follows:

$$G(y) = N_{peak}.e^{-\frac{1}{2}\left[\frac{y}{\sigma_y}\right]^2} \quad ; \qquad y > 0 \qquad (4.8)$$

and for lateral direction of x its given by:

$$L(x) = 1 \quad ; \qquad x < x_0 \qquad (4.9)$$

$$L(x) = e^{-\frac{1}{2}\left[\frac{x-x_0}{0.28.\sigma_y}\right]^2} \quad ; \qquad x > x_0 \qquad (4.10)$$

where x_0 is lateral length of the source/drain extensions.

4.4.2 Source-drain contact profile

On the other hand, the *N*-type source-drain contact profile has the peak concentration of $2\text{x}10^{20}\text{cm}^{-3}$ in $y = 0$ and standard deviation of $\sigma_y = 1.12x10^{-2}\,\mu m$.

For the vertical direction of y its given as follows:

$$G(y) = N_{peak}.e^{-\frac{1}{2}\left[\frac{y}{\sigma_y}\right]^2} \quad ; \qquad y > 0 \qquad (4.11)$$

and for lateral direction of x is given by:

$$L(x) = 1 \quad ; \qquad x < x_1 \qquad (4.12)$$

$$L(x) = e^{-\frac{1}{2}\left[\frac{x-x_0}{0.35.\sigma_y}\right]^2}; \qquad x > x_1 \tag{4.13}$$

and x_1 is lateral length of the source/drain contacts.

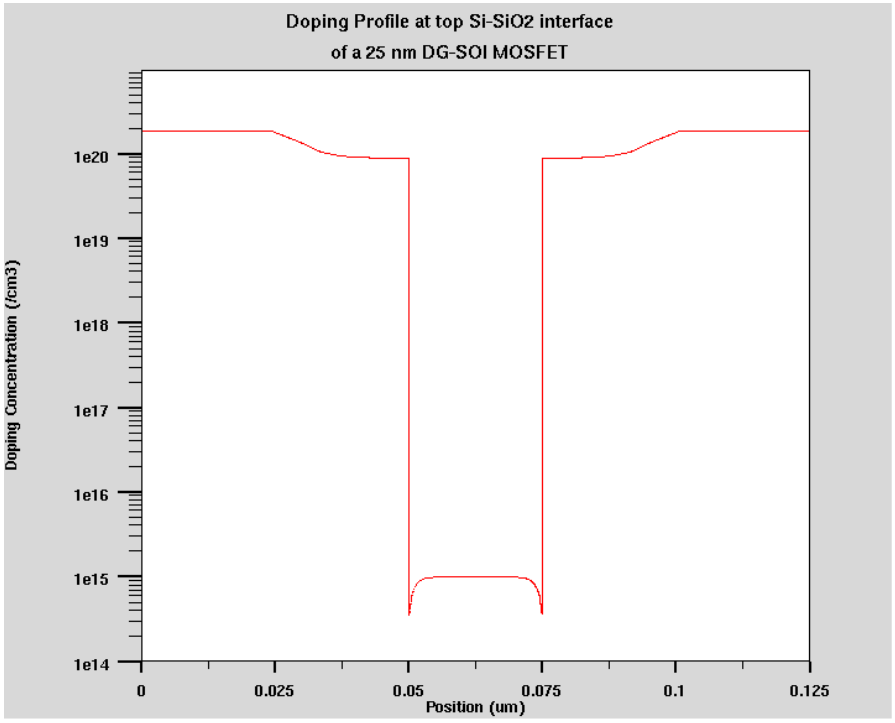

Fig. (4.10): The net doping profile at the top Si-SiO_2 interface of a 25 nm double-gate SOI MOSFET along the device.

CHAPTER 5

2D device modeling and simulation

5.1 Classical MOSFET

The classical MOSFET's are assumed to have gate lengths of 250 and 210 nm. The device mesh, region specification and electrode definition are done using the mesh, region, and electrode statements of the input file. The channel doping is presumed to be constant. Gaussian source and drain profiles are used. Both 8.6 and 5.6 nm thick gate oxide are considered, the later one for sub-threshold characteristics.

5.1.1 Id/Vgs and Threshold Voltage Extraction

The first task in simulating MOSFET's is the simulation of I_d/V_{gs} curve and extracting threshold voltage and other SPICE parameters. It demonstrates a simple I_d/V_{gs} curve

generation with V_{ds}=0.1V parameter extraction for the threshold voltage V_t, a linear gain (beta) and mobility roll-off (theta).

The **CVT** (Yamaguchi) and **SRH** (Shockley-Read-Hall recombination) mobility models are used to give a fast runtime. **CVT** is a general purpose mobility model including concentration, temperature, parallel field and transverse dependence and **SRH** for fixed carrier lifetimes. The poly-silicon gate is used as a gate contact.

The sequence of solve statements are set to ramp the gate bias with the drain voltage at 0.1V. Solutions are obtained in intervals from 0 V up to 3.0V for the gate voltage.

The extract Statements at the end of the file are used to measure the threshold voltage and other SPICE parameters such as the gain and the mobility role-off.

The results from the extract statements are printed in the run-time output, saved to a file called results.final. The name parameter specifies only a user-defined label. The routines are not hard-coded to these names. Thus the first extraction statement reads: extract the value called nvt found by taking the V_{gs} intercept of the maximum slope to the curve of drain voltage versus drain current and subtracting half the drain voltage. This is just one possible definitions of threshold voltage.

The extract statement measures the gain (or Beta). This is defined as the value of the steepest slope to the I_d/V_{gs} curve divided by the drain voltage. The final extraction is for the SPICE level 3 is mobility roll-off parameter (or Theta). It shows the use of the threshold voltage and the gain by substituting the previously extracted values of threshold and beta into these places in the equation.

From the extract statements, the threshold voltage was found to be 0.4 V when a drain bias voltage was set to be 0.1 V. Meanwhile, the gain (beta) and the mobility roll-off (theta) were found to be 0.5×10^{-3} and 0.33 V^{-1} respectively.

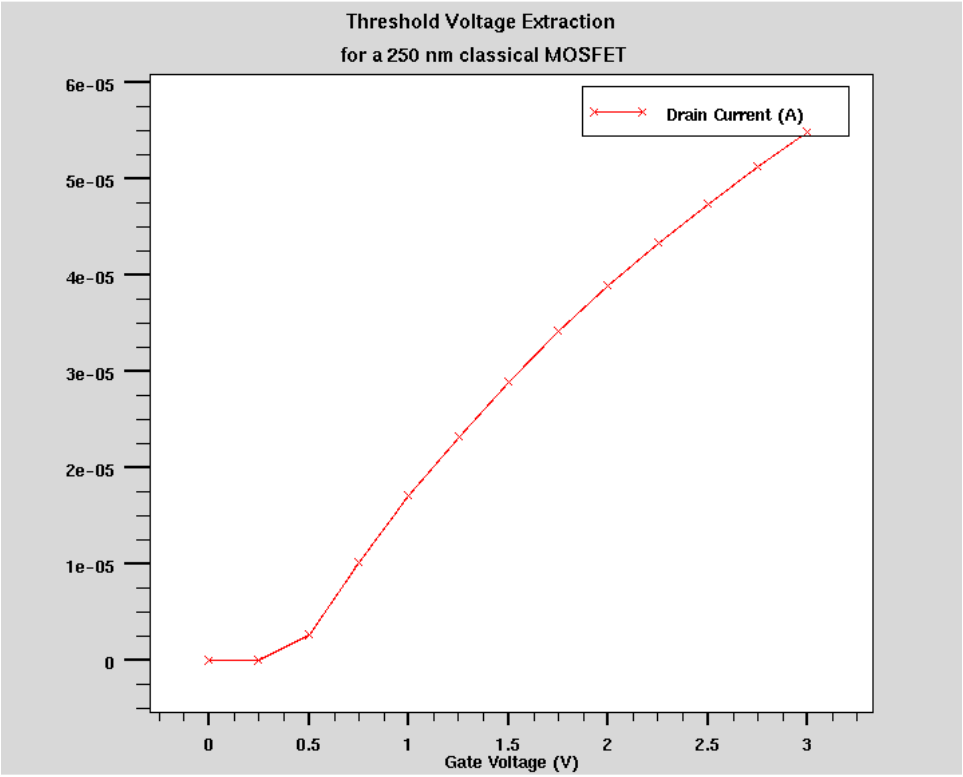

Fig. (5.1): Threshold extraction for an n-channel MOSFET of a 250 nm gate length with V_{DS}=0.1 V.

The process simulation, process parameter extraction and electrode definition for current-voltage family curves are exactly the same as mentioned in the threshold extraction, but a more advanced sequence of solve statements is used in this section. Five I_d /V_{ds} curves are required at different gate voltages. For each of the five gate voltages a solution with V_{ds} = 0 Volt is simulated and the result is saved to a solution file. A log file is opened and the ramp of V_{ds} is set. At the end of the simulation the extract statement is used to measure the peak current and the saturation slope.

From the shape of the I_d/V_{ds} curves the saturation slope is clearly the minimum value of the gradient along the curve. Finally the five I_d/V_{ds} curves are overlaid in TonyPlot.

From figure (5.2), it can be seen that the drive current I_{on}=270 µA/µm at V_{gs}=1.5 V.

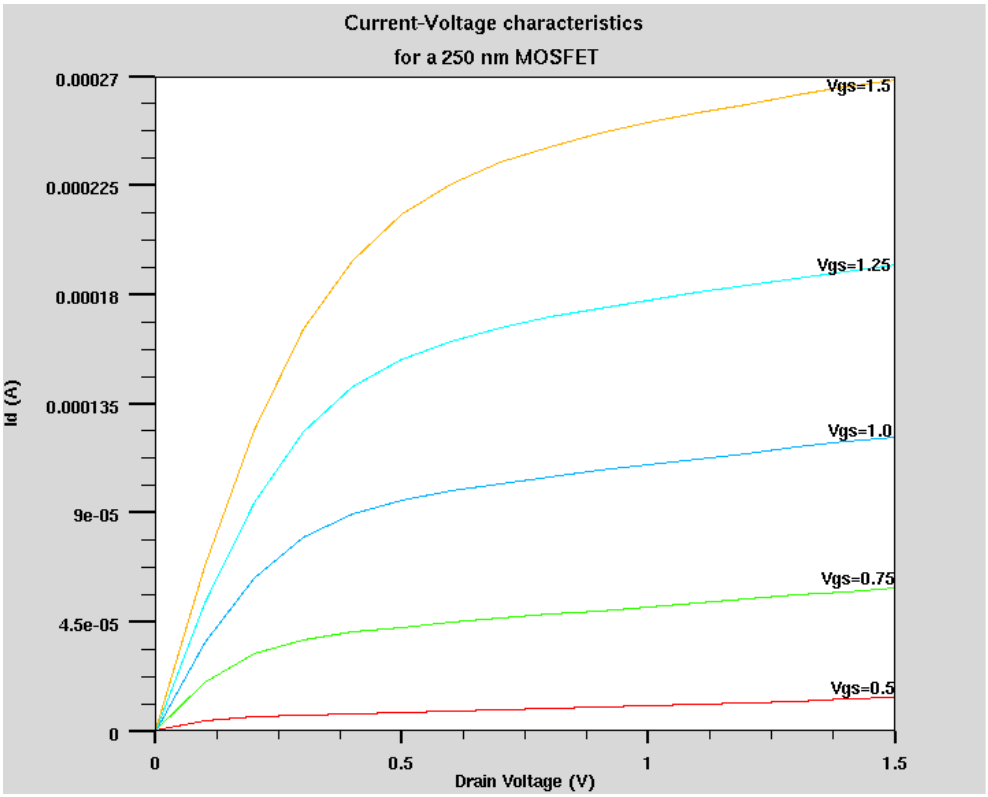

Fig. (5.2): Current-voltage characteristics of an n-channel classical MOSFET of a 250 nm gate length. The threshold voltage is found to be Vt =0.4 V

5.1.2 Channel Potential Distribution Profile

To make a full comparison for our simulation results to the model of sub-100 nm MOSFET presented in [2], we have to mention the analysis concept that has been performed in the central region under the gate.

The threshold and sub-threshold properties are basically determined by the channel potential profile:

$$\Phi_0(x) = \phi_0 + \varphi_0(x) \tag{5.1}$$

ϕ_0 is the channel potential according to the 1D long-channel and $\varphi_0(x)$ is the contribution from the 2D Laplacian in the region under the gate.

The channel potential $\Phi_0(x)$ has to be determined from the normal electrical field $E_n(x)$ which consists of the field contribution E_0 from the 1D analysis and the contribution $E_{2D}(x)$ from the 2D analysis.

The boundary conditions for the 2D Laplacian in Region 1 (including the oxide) are defined in terms of the potential distributions along at the oxide-gate interface (y = 0) and at the vertical boundaries at x = 0 and x = L.

At the vertical boundaries, the potential distributions are derived from the 1D Poisson equations in Regions 1-3, the potentials of the source and drain contacts, and the potential at the vertical sidewalls of the oxide.

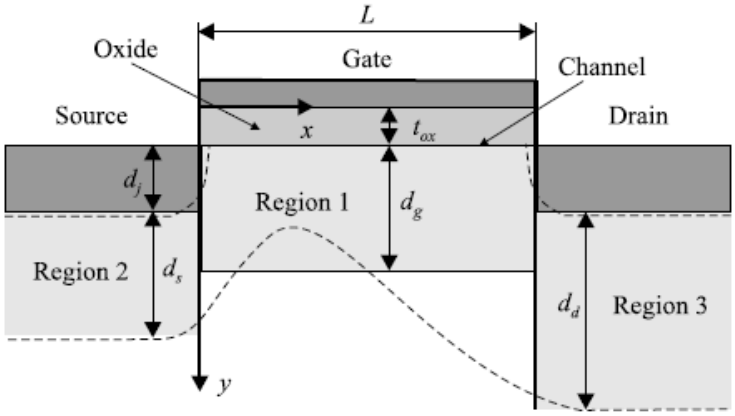

Fig. (5.3): Closed-form model for MOSFET geometry [2]. The lower dashed line indicates the depletion boundary.

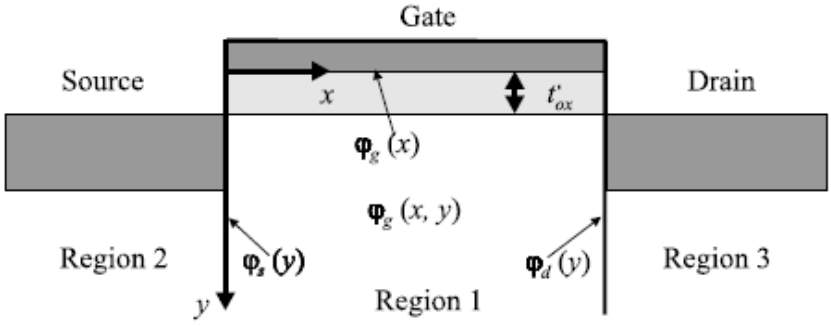

Fig. (5.4): The Boundary conditions for the Laplacian of Region 1 [2].

In the 1D approximation, the potential distribution $\phi_g(y)$ relative to the substrate interior in Region 1 becomes:

$$\phi_g(y) = \begin{cases} \varphi_g + (\phi_0 - \varphi_g)\dfrac{y}{t_{ox}'} & 0 \le y < t_{ox}' \\ \phi_0 + \dfrac{qN_s}{2\varepsilon_s}(y - t_{ox}')^2 - E_0(y - t_{ox}') & t_{ox}' \le y < d_g + t_{ox}' \\ 0 & y \ge d_g + t_{ox}' \end{cases} \tag{5.1}$$

Where φ_g is the potential at the gate-oxide interface and $t_{ox}' = t_{ox}\dfrac{\varepsilon_s}{\varepsilon_{ox}}$ where t_{ox} is the oxide thickness while ε_s and ε_{ox} are the dielectric permittivity of the oxide and semiconductor respectively.

$$d_g = \sqrt{\frac{2\varepsilon_s \phi_0}{q N_s}} \tag{5.2}$$

is the depletion depth , and

$$E_0 = \frac{q N_s}{\varepsilon_s} d_g = \sqrt{\frac{2 q N_s \phi_0}{\varepsilon_s}} \tag{5.3}$$

is the magnitude of the vertical 1D electric field contribution at the semiconductor-oxide interface. At threshold, the 1D channel potential is $\phi_0 = V_{SB} + 2\varphi_b$, where $\varphi_b = V_{th} \ln \dfrac{N_s}{n_i}$ is the bulk Fermi potential.

And below threshold, the channel potential becomes:

$$\phi_0 = V_{SB} - V_{FB} + \frac{q N_s}{\varepsilon_s} t_{ox}' + 2t_{ox}' \sqrt{\frac{q N_s}{2\varepsilon_s}(V_{GB} - V_{FB} + \frac{q N_s}{2\varepsilon_s} t_{ox}'^{\,2})} \ , \tag{5.4}$$

where V_{GB} is the gate-substrate voltage and V_{FB} is the flat band voltage. It is assumed that the oxide thickness is much smaller than the gate length.

The total 2D potential distribution in Region 1 is

$$\Phi_g(x,y) = \phi_g(x,y) + \varphi_g(x,y) \tag{5.5}$$

where $\varphi_g(x,y)$ is the solution of the Laplacian.

The potential distributions in Regions 2 and 3 are initially approximated by 1D distributions of the following form:

$$\phi_{s,d}(y) = \begin{cases} \phi_g + (V_{S.,D} - \phi_g)\dfrac{y}{t'_{ox}} & 0 \le y < t'_{ox} \\ V_{S,D,} & t'_{ox} \le y \le d_j + t'_{ox} \\ V_{S,D} + \dfrac{qN_s}{2\varepsilon_s}(y - d_j - t'_{ox})^2 - E_{0(s,d)}(y - d_j - t'_{ox}) & d \le y \le d_j + d_{s,d} \\ 0 & y > d_j + d_{s,d} + t'_{ox} \end{cases} \tag{5.6}$$

Here $V_S = V_{SB} + V_{bi}$ and $V_D = V_S + V_{DS}$, are the potentials at the source and drain contact regions relative to the substrate, V_{bi} is the built-in voltage, and V_{DS} is the drain-source bias.

Meanwhile $d_{s,d}$ is the 1D depletion widths of the two regions,

$$d_{s.d} = \sqrt{\frac{2\varepsilon_s V_{S,D}}{q N_s}}\,. \tag{5.7}$$

On the two side, E_{0s} and E_{0d} stand for the vertical electric fields at the interface of the source and drain contact regions, respectively, at the depth of $y = d_j$.

$$E = \frac{q N_s}{\varepsilon_s} d_{s,d} = \sqrt{\frac{2 q N_s V_{S,D}}{\varepsilon_s}}\,. \tag{5.8}$$

To solve the Laplacian in Region 1, the boundary conditions for the three interfaces should be determined as indicated in Figure (5.4).

The metal-oxide interface is given as followed:

$$\varphi_g(x) \equiv \varphi_g(x,0) = V_{GB} - V_{FB} \tag{5.9}$$

The requirement of continuity of the potential at the vertical boundaries must be accomplish. Therefore, the source and drain side interfaces are given by the following form:

$$\varphi_{s.d}(y) = \phi_{s,d}(y) - \phi_g(y)$$

$$\varphi_{s.d}(y) = \begin{cases} (V_{S,D} - \phi_0)\dfrac{y}{t'_{ox}} & 0 \le y < t'_{ox} \\ V_{S,D} - \phi_0 + E_0(y - t'_{ox}) - \dfrac{qN_s}{2\varepsilon_s}(y - t'_{ox})^2 & t'_{ox} \le y \le d_j + t'_{ox} \\ V_{S,D} - \phi_0 + E_{0(s,d)}d_j + \dfrac{qN_s}{2\varepsilon_s}d_j{}^2 & \\ \quad + (E_0 - E_{0(s,d)} - \dfrac{qN_s}{\varepsilon_s}d_j)(y - t'_{ox}) & d_j + t'_{ox} \le y \le d_g + t'_{ox} \\ V_{S,D} - E_{0(s,d)}(y - d_j - t'_{ox}) + \dfrac{qN_s}{2\varepsilon_s}(y - d_j - t'_{ox})^2 & \\ & d_g + t'_{ox} \le y \le d_j + d_{s,d} + t'_{ox} \\ 0 & y > d_j + d_{s,d} + t'_{ox} \end{cases} \tag{5.10}$$

The initial 1D estimate for the channel potentials are $\Phi_0(x) = \phi_0$, or $\varphi_0(x) = 0$

Figure (5.5) below shows the model calculation of the corresponding central parts of the potential distributions in the channel at threshold, for V_{DS} = 0.05 V and at 3 V.

These curves clearly illustrate the lowering of the threshold voltage (DIBL-effect) related to the reduction of the energy barrier with increasing drain-source bias. Also the shift of

the potential minimum in the direction of the source with increasing drain-source bias is indicated.

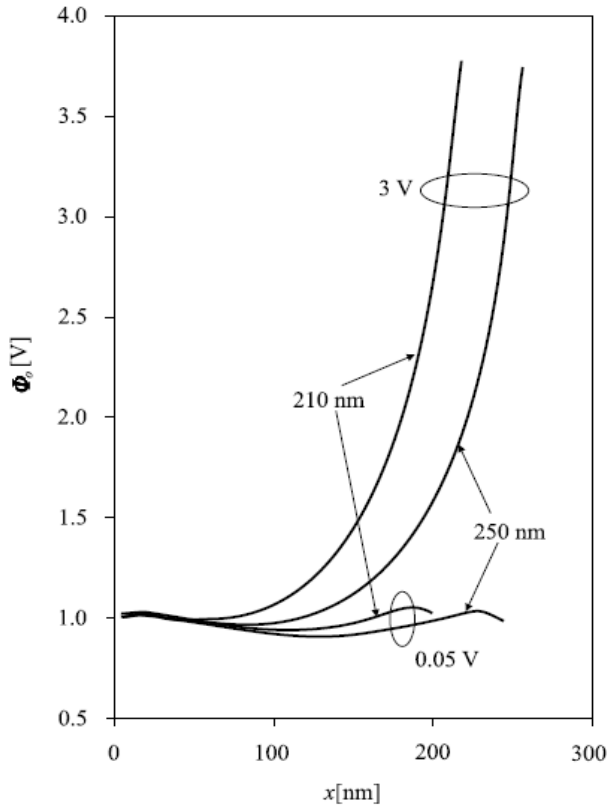

Fig. (5.5): Model calculation from Closed-form 2D model of the channel potential relative to the substrate for V_{DS}=0.05 V and 3 V for gate lengths of 210 and 250 nm and t_{ox}=8.6 nm.

Meanwhile, based from our simulations for the same devices parameters, two devices structures are designed with a same substrate doping, oxide thickness, but with 250 nm and 210 nm gate lengths.

We assigned the drain biasing voltage to be 0.05 V and 3 V for both structures and from the 2D Mesh plot, the Cutline tool is used to create 1D cross section plots from any arbitrary positions within a 2D structure. The horizontal line close to the Si-SiO_2 is drawn to obtain the channel potential profile. The result shows a good quantitative agreement with the 2D model result for the channel potential profile [2].

The simulated result for two gate lengths, 250 nm and 210 nm is shown below:

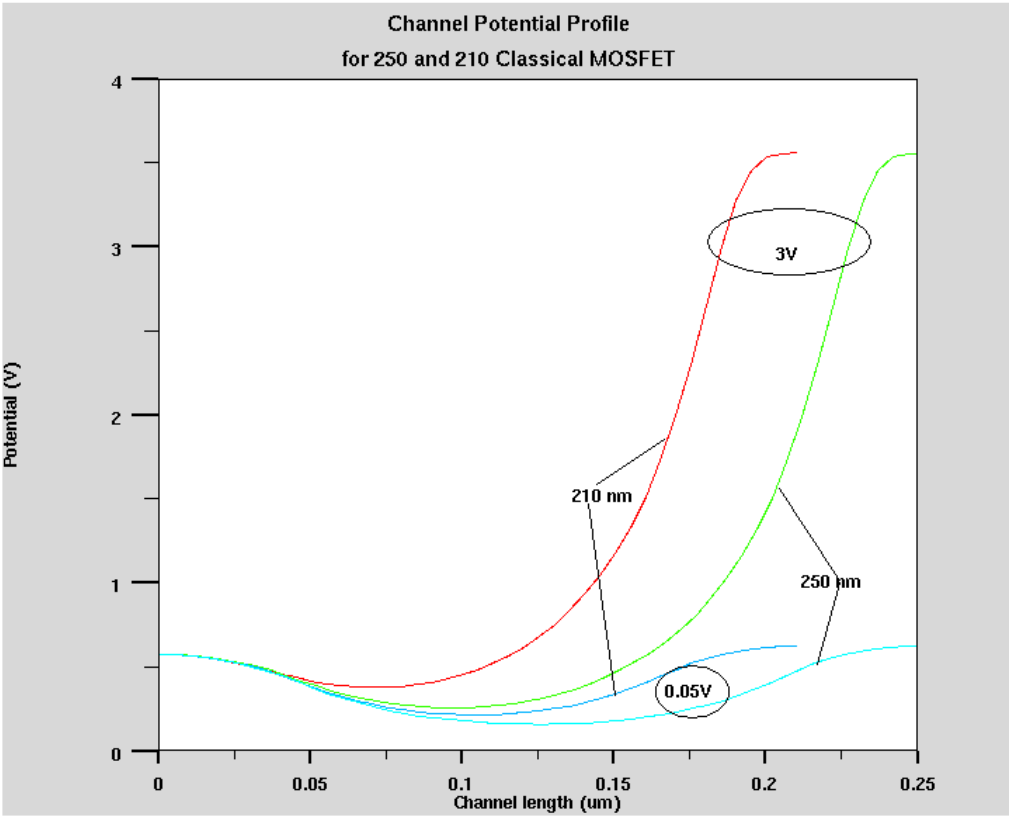

Fig. (5.6): Simulation result of the channel potential relative to substrate for V_{ds}=0.05V and 3 V for gate lengths of 210 nm and 250 nm where the t_{ox}=8.6 nm.

To explain this phenomenon, we consider an n-channel device with a long channel and a target threshold voltage of Vt_1. It was observed that the threshold voltage V_{t2} of another device with the same technology design but a shorter channel length can be significantly smaller than Vt_1, as indicated by Figure (5.6). This is known as threshold voltage roll-off. This phenomenon can be explained through a charge sharing argument. Unlike the long channel device, in a short channel device, a significant part of the field lines coming from the bulk charge will terminate in the source and drain regions instead of at the gate. As a result, it is easier for the gate to deplete the channel, lowering the threshold voltage of the device.

5.1.3 Sub-threshold Transfer Characteristics

A comparison of the simulated result with the modelled sub-threshold transfer characteristics for a 250 nm device with t_{ox} = 5.6 nm are shown below, where V_{DS} = 0.05 V. The device has a different oxide thickness and doping than the 250 nm device that discussed above, where a $4x10^{17}cm^{-3}$ of the substrate doping were used. However, except for N_s and t_{ox} the rest of parameter were the same.

The sub-threshold transfer characteristic is simulated as direct input data by using the command language for defining the structure in ATLAS, with the same sequences of statements that described in chapter 2.

A simple I_{Ds}/V_{GS} curve is generated with V_{DS}=0.05 V. The gate voltage is ramped from zero to 0.4 V only in 0.025 V steps. The specification of reciprocal of the steepest slope to the curve of V_{GS} versus the log (I_{DS}) is plotted.

The simulation results compare to the modelling strategy in [2] indicate that the modelling approach is adequate for MOSFET's operating in the sub-threshold regime.

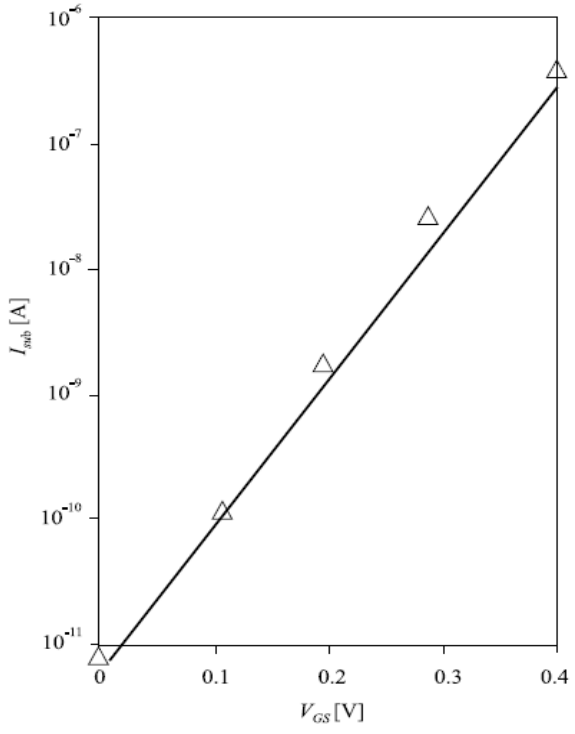

Fig. (5.7): Form Closed-form 2D model shows measured (symbols) and the modeled (line) of the sub-threshold transfer characteristics for a 250 nm MOSFET with t_{ox} =5.6 nm at V_{DS}=0.05 V

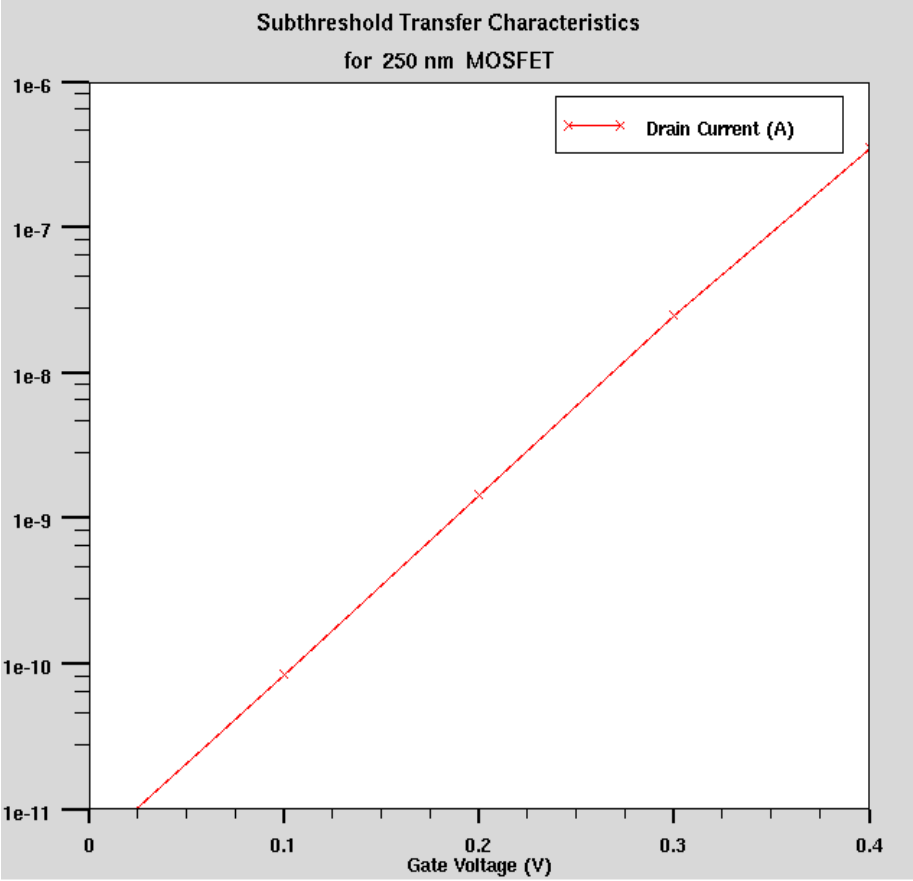

Fig. (5.8): The sub-threshold transfer characteristics for 250 nm classical MOSFET with a 5.6 nm oxide thickness at V_{DS}= 0.05 V

To obtain the potential profile at the source and drain interfaces, it will be clear to set the vertical boundary conditions as described by figure (5.3).

At the metal-oxide interfaces, where $y = 0$ we have:

$$\varphi_g(x) \equiv \varphi_g(x,0) = V_{GB} - V_{FB}$$

In the Silvaco simulator, at zero applied voltage relative to the substrate is set to 0.5 V.

In additional to that, equation (5.10) gives us a description to the vertical potential distribution at the source/drain interfaces at the Boundary conditions shown in figure (5.9).

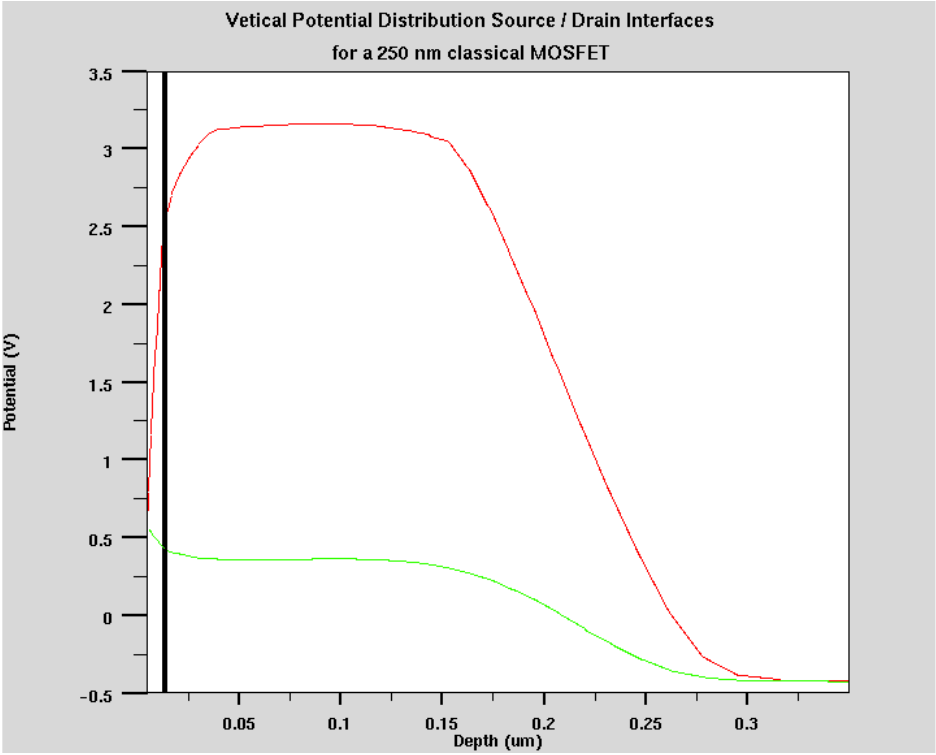

Fig. (5.9): shows the vertical potential profile at the source/Drain interfaces for a 250 nm classical MOSFET at V_{DS}=1.5 V. The red lined for Drain side interface and the green for source.

5.1.3 Drain Induced Barrier Lowering (DIBL)

For short channel devices, application of a high drain-to-source bias can lower the threshold voltage and increase the off-currents, as shown in Figure (5.6). This is known as drain induced barrier lowering (DIBL), and is another expression of the short channel effects.

Conceptually, drain barrier lowering is caused by the lowering of the potential barrier at the source of a MOSFET due to applied drain bias [19]. There are no known closed form expressions for predicting the threshold shift resulting from DIBL.

However, DIBL effects increase with increasing junction depth of the source/drain region.

A measure of DIBL can be defined as follows

$$DIBL = \frac{V_{t1} - V_{t2}}{V_{DS1} - V_{DS2}} \tag{5.11}$$

where V_{t1} and V_{t2} are threshold voltages at the drain-source voltages V_{DS2} and V_{DS2} respectively [9].

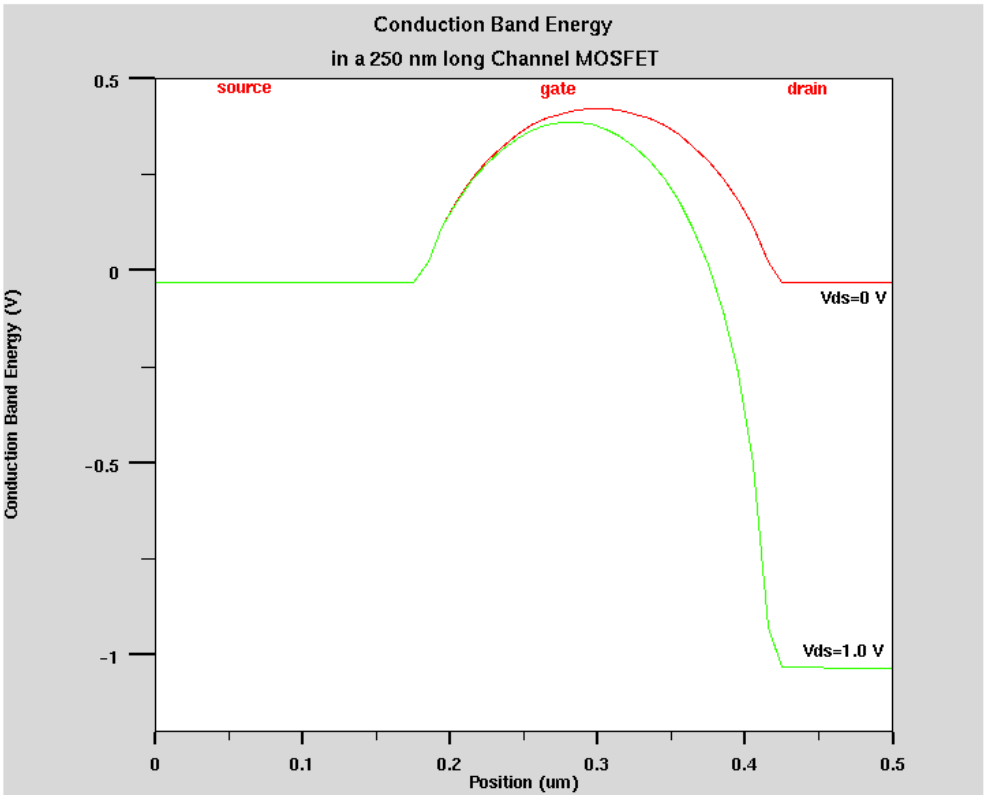

Fig. (5.10): Conduction Band Energy Profile at the Si-SiO_2 interface of a 250 nm n-channel MOSFET with V_{DS}=0 V and 1.0 V.

Figure (5.10) shows the effect of the applied voltage distributed over the channel length which will give a rise to a shift of the conduction band edge close to the source-channel edge. Such a shift will lead to a lowering of the injection barrier between the source and the channel, and since the governing injection mechanism is thermionic emission [3], it translates into a significant increase in the injected current. This fact can be described in term of a shift in the threshold voltage.

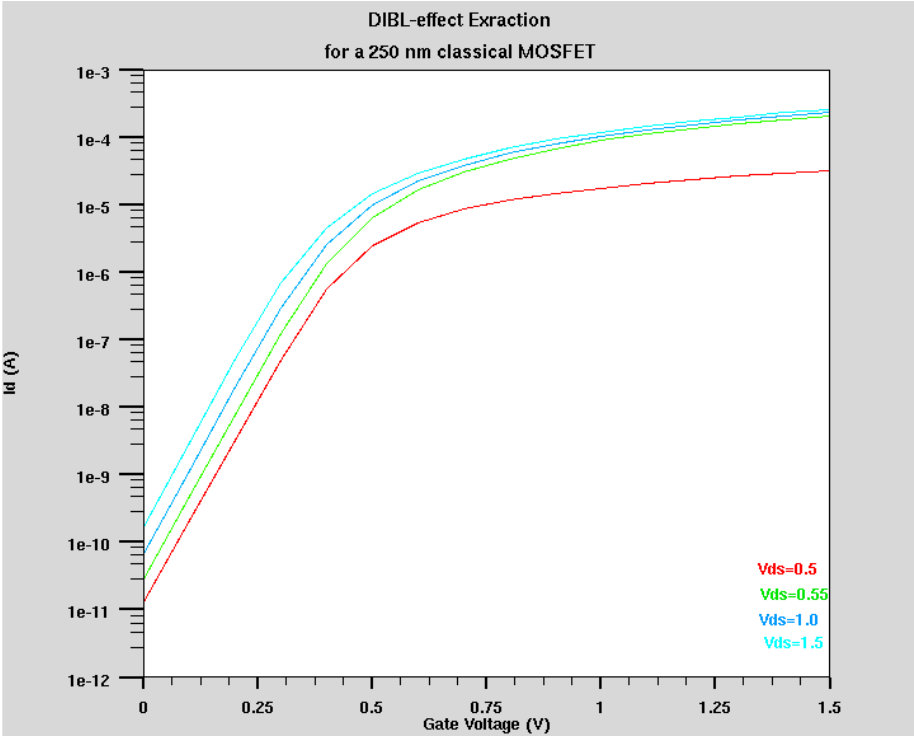

Fig. (5.11): Semilog plot of the extraction of the DIBL effect where the lowering of threshold voltage related with increasing the drain-source bias.

From figure (5.2), it can be seen that the I_{on}=270 µA/µm at V_{gs}=1.5 V. In the mean time, the I_{off} is above 0.10 nA/µm at drain voltage of V_{ds}=1.5 V as shown in figure (5.11).

The threshold voltage is widely used to determine short channel effects; the magnitude of the threshold voltage is directly affected by non-uniform doping effects. Hence, DIBL is a better indicator of short channel effects. As such, it is an important device characteristic that should be monitored.

5.2 Super-Steep-Retrograde MOSFET

5.2.1 Above threshold Characteristics

The process simulation, process parameter extraction and electrode definition for current-voltage family curves are exactly the same as mentioned in the classical current-voltage characteristics; five I_d / V_{ds} curves are required at different gate voltages. For each of the five gate voltages a solution with V_{ds} =0 Volt is simulated and as the result a log file of the ramped V_{ds} is set. At the end of simulation, the extract statement is used to measure the peak current and the saturation slope.

From the shape of the I_d/V_{ds} curves the saturation slope is clearly the minimum value of the gradient along the curve. Finally the five I_d/V_{ds} curves are overlaid in TonyPlot. From figure (5.12), it can be seen that the I_{on} at 925µA/µm at V_{gs}=1.5V.

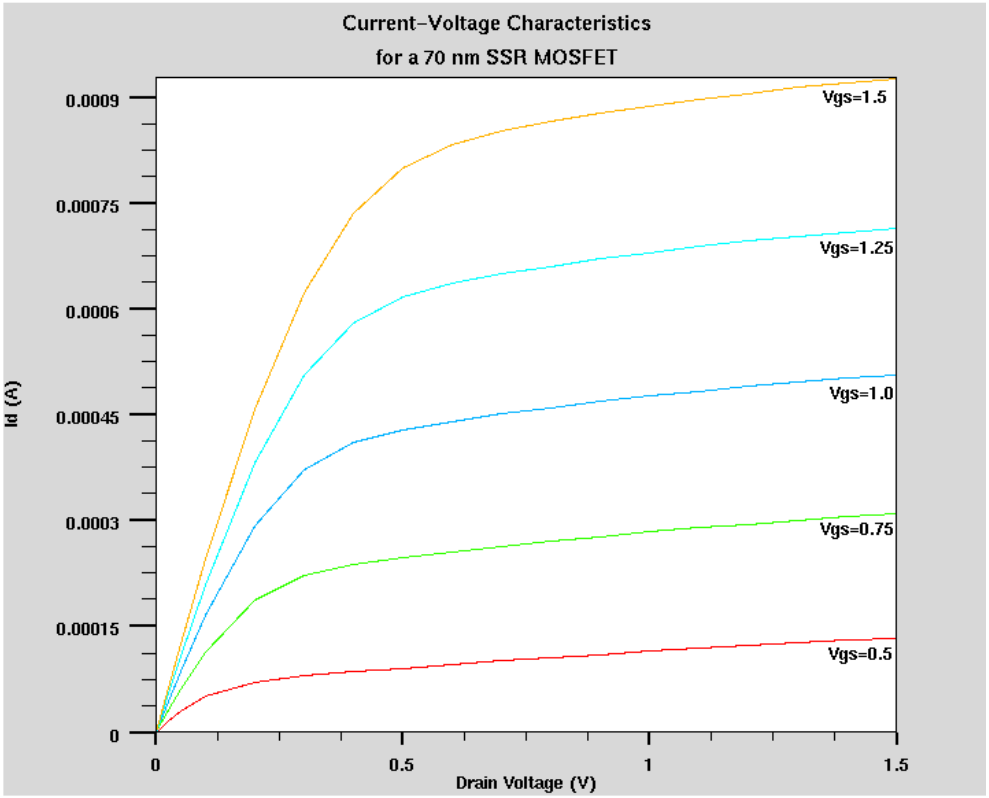

Fig. (5.12): shows the Current-voltage characteristics of an n-channel Super-Steep-Retrograde MOSFET of a 70 nm gate length.

The threshold voltage extraction was demonstrated as a simple I_D/V_{GS} generation curve at V_{ds}=0.1V. We followed the same procedure as mentioned in extracting the threshold voltage in the classical MOSFETs. The **CVT** (Yamaguchi) and **SRH** (Shockley-Read-Hall recombination) mobility models are used to give a fast runtime. **CVT** sets a general purpose mobility model including concentration, temperature, parallel field and transverse dependence and **SRH** for fixed carrier lifetimes.

We obtain the threshold voltage from a sequence of solve statements to ramp the gate when the drain bias voltage is set to 0.05V. Solutions are obtained at 0 V intervals up to 3.0V for the gate. We obtain the threshold voltage V_t =0.26 V

5.2.2 Channel Potential Profile

Figures below show the simulated SSR MOSFETs and the model calculations of the corresponding central parts of the potential distributions in the channel where threshold voltage were determined from the minimum channel potentials for a set of gate-source voltage, selecting the ones that comply with the threshold condition.

These curves clearly illustrate the lowering of the threshold voltage (DIBL-effect) related to the reduction of the energy barrier with increasing drain-source bias as in figure (5.13) and figure (5.14). Also the shift of the potential minimum in the direction of the source with increasing gate-source bias is indicated in figure (5.15) and figure (5.16)

The simulated results show a close agreement with the model in [2].

The variation observed might be attributed to the charge mobility models used in the simulation procedures. In addition to that sufficient grid density is needed for simulating short channel devices.

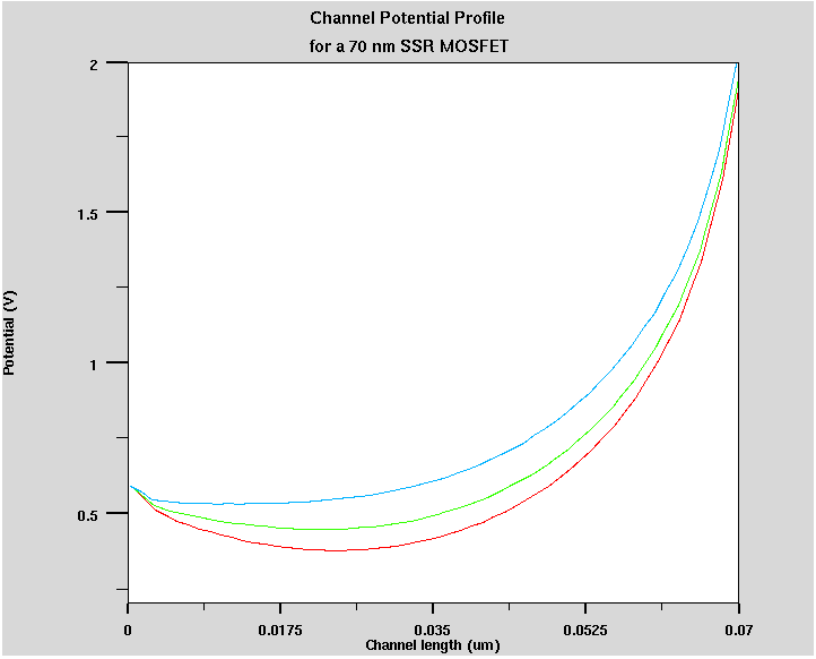

Fig. (5.13): shows the channel potential profile in 70 nm SSR MOSFET relative to the substrate for V_{DS}= 1.6 V at V_{GS}=0 V (lower curve), V_{GS}= 0.1 V (middle curve) and V_{GS}= 0.31 V (upper curve)

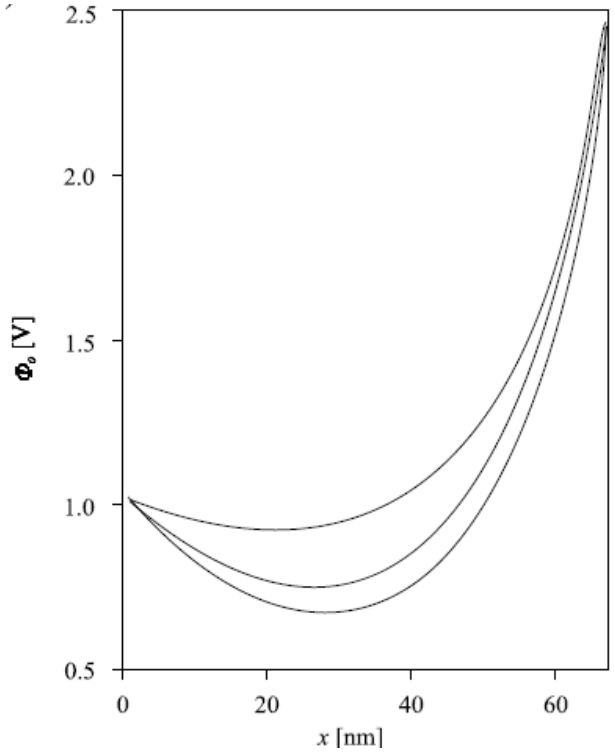

Fig. (5.14): shows the model calculations of the channel potential profile in 70 nm SSR MOSFET relative to the substrate for V_{DS}= 1.6 V at V_{GS}=0 V (lower curve) , V_{GS}= 0.1 V (middle curve), and V_{GS}= 0.31 V (upper curve)

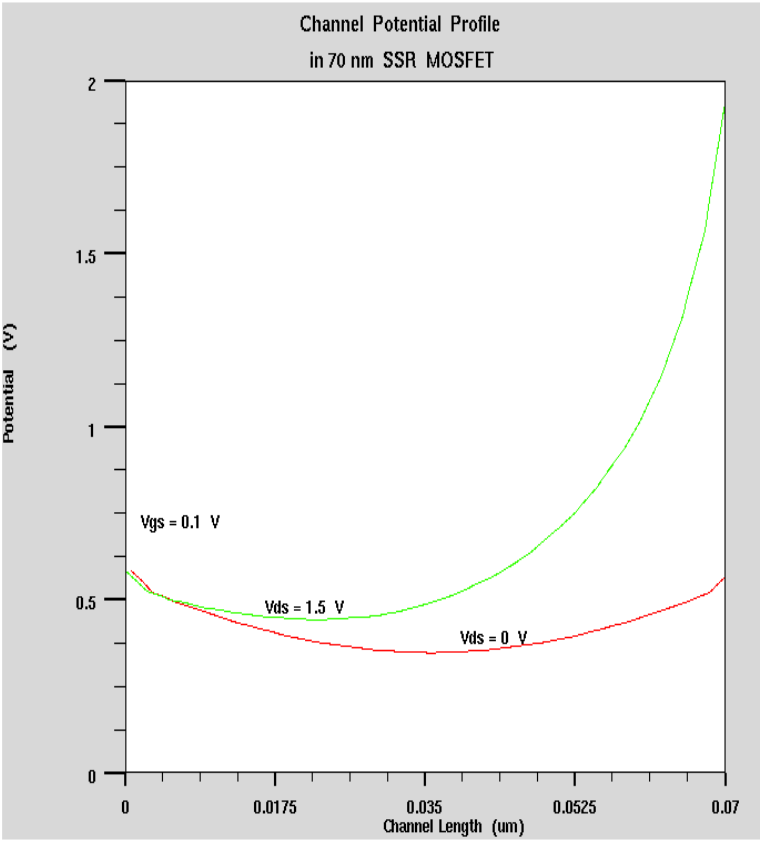

Fig. (5.15): shows the channel potential profile in 70 nm SSR MOSFET relative to the substrate for V_{GS}=0.1 V at V_{DS}= 0 V (lower curve) and V_{DS}= 1.5 V (upper curve)

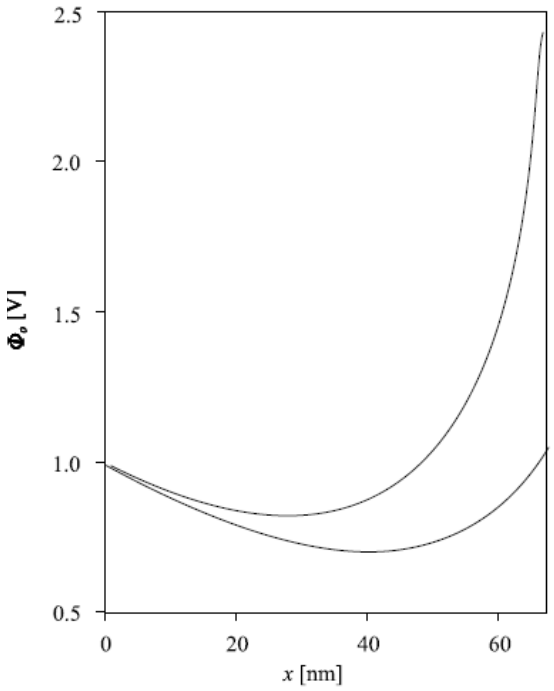

Fig. (5.16): shows the model calculation of the channel potential profile in 70 nm SSR MOSFET relative to the substrate for V_{GS}= 0.1 V at V_{DS}=0 V (lower curve) and V_{DS}= 1.5 V (upper curve)

At the meantime, the potential distribution profiles for the vertical boundaries at the source and drain interfaces can be determined by the equation (5.10) where $\varphi_{s.d}(y) = \phi_{s,d}(y) - \phi_g(y)$

From figure (5.3), five vertical intervals for *y* along the device can determined the vertical potential profiles for source/drain interfaces. The graph below shows the behavior of the potential lines which can be more or less identical with equation (5.10).

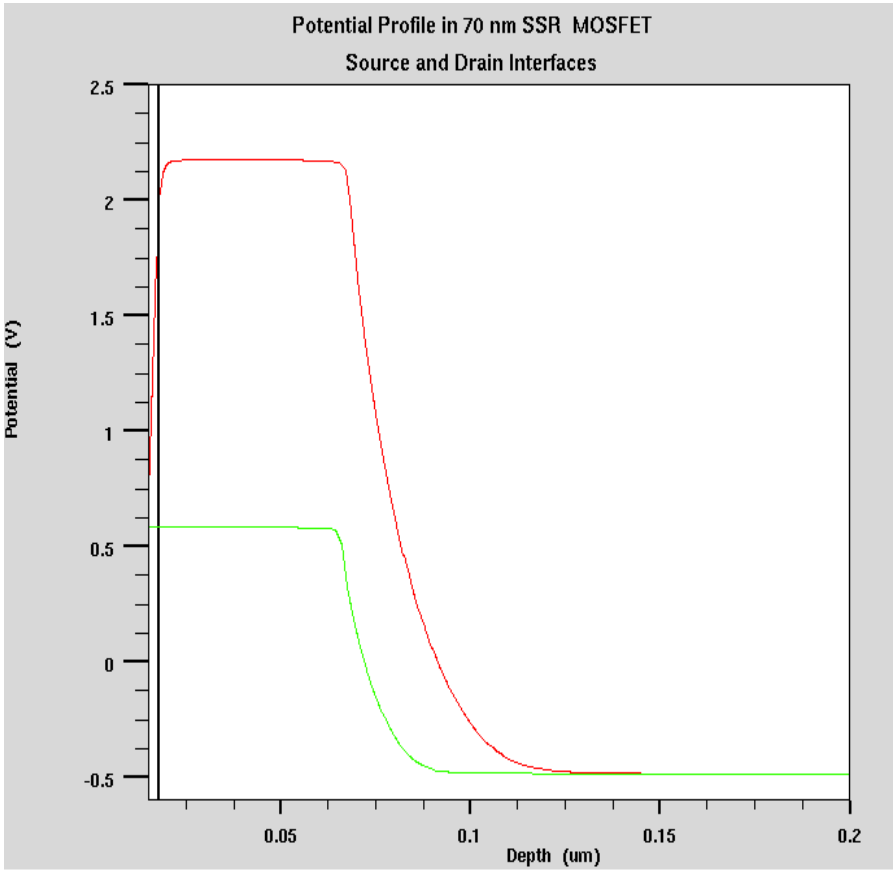

Fig. (5.17): shows the vertical potential profile at the source/Drain interfaces for a 70 nm Super-Steep-Retrograde MOSFET. The red lined for Drain side interface and the green for source.

5.2.3 DIBL-effects and Sub-threshold Extractions

Practically, drain induced barrier lowering is caused by the lowering of the potential barrier at the source of a MOSFET due to applied drain bias, figure (5.18) gives a clear description for the lowering of the potential in term of a shift in the threshold voltage when different of drain biases were applied. Therefore, DIBL effects increase with increasing junction depth of the source/drain region [13].

From figure (5.12), it can be seen that the I_{on}=925 µA/µm at V_{gs}=1.5 V. Meanwhile, figure (5.18) shows the leakage current I_{off} of the SSR MOSFET at or above 1 nA/µm at V_{ds}=1.5 V

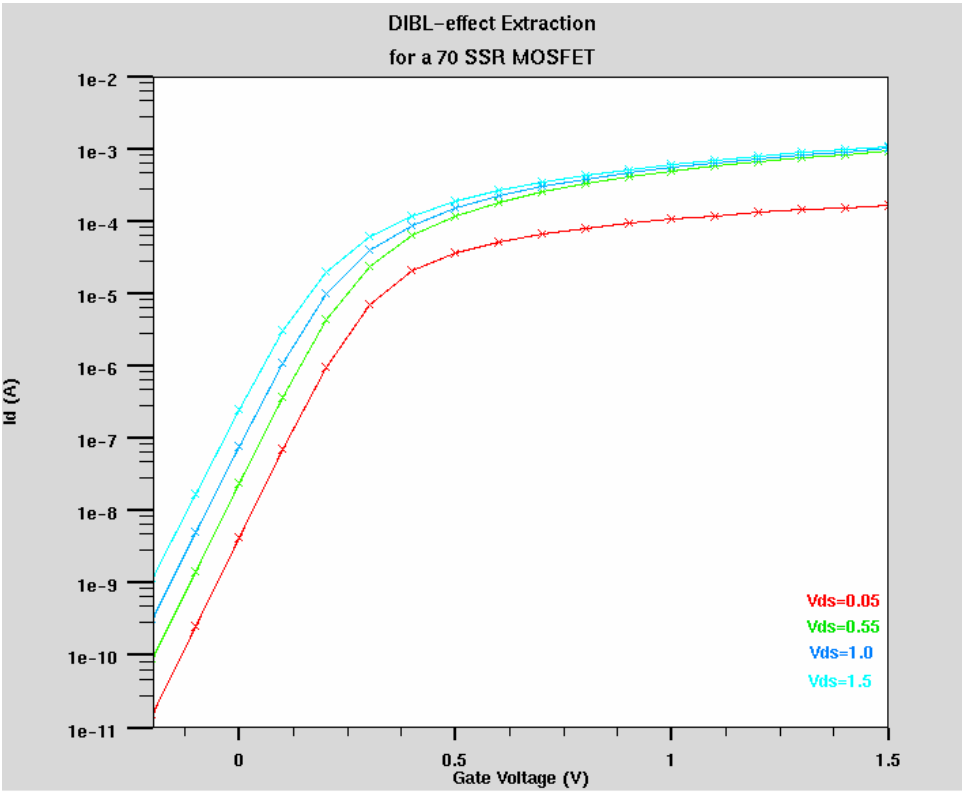

Fig. (5.18): shows a semilog plot of the extraction of DIBL effect for SSR MOSFET where the lowering of threshold voltage related with increasing the drain-source bias.

The simulation result for the SSR MOSFETs in the sub-threshold regime compare to the modelling approach in [2] shows some differences in the drain leakage current. The deviations observed can mostly be attributed to the variation of the adjustable parameters in [2] such as the effective depth source and drain contact, which accounts for the rounding of the contacts towards Region 1 and the physical models used in the simulation.

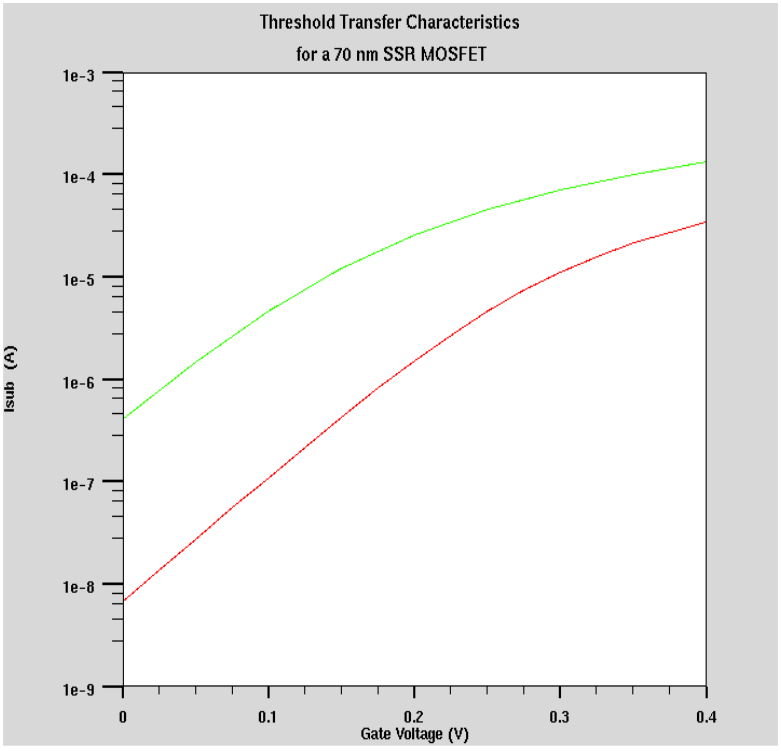

Fig. (5.19): shows the simulated sub-threshold transfer characteristics for 70 nm SSR MOSFET with t_{ox}= 3 nm. V_{DS}=0.1 V (lower curve) and V_{DS}=1.6 V (upper curve)

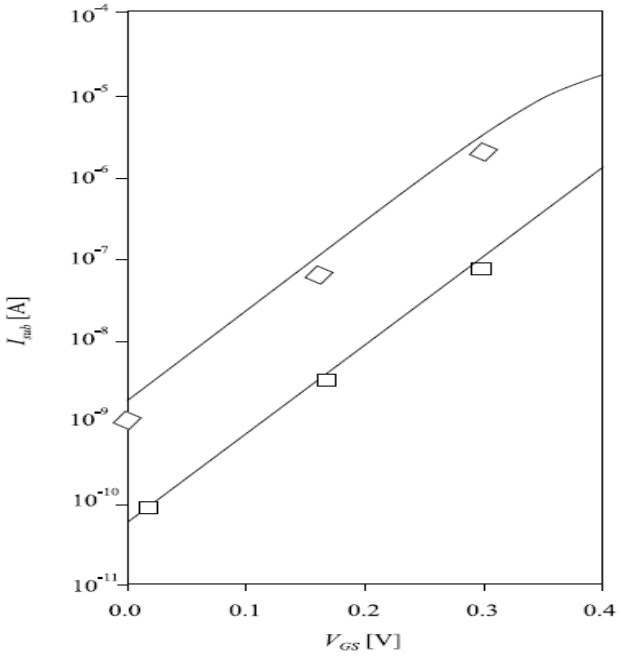

Fig. (5.20): shows the sub-threshold transfer characteristics for experimental (symbols) and the modeled (lines) for 70 nm SSR MOSFET with t_{ox} = 3 nm. V_{DS}=0.1 V (lower curve) and V_{DS}=1.6 V (upper curve)

5.3 Template Bulk MOSFET

Managing of short channel effects is predicted to have a significant impact on processes used for doping the source and drain extension. Drain and source extensions doping levels are expected to increase, driven by the need to reduce junction depth while minimizing parasitic resistance. Similarly, drain extension doping profiles, which required lateral grading for minimum hot carrier damage, will need to become more laterally abrupt to support low voltage operation.

For n-channel devices, a more abrupt source extension junction leads to a higher source injection velocity and higher resulting drive current. Therefore, for NMOS higher abruptness values are more desirable [1].

5.3.1 Current-Voltage Characteristics Curves

Figure (5.21) and (5.22) below show the current-voltage characteristics for a 25 nm Bulk device at different gate- source voltages. The method used for the simulation is the same as that followed for both classical and SSR MOSFETs, the only exception is the use of a more complicated physical model where the quantum mechanical effects are dominant, at some nanometer device dimensions. This is for example the case in the Template Bulk and DG-SOI MOSFETs where the physical gate oxide was aggressively scaled to 1.6 nm in order to achieve high drive currents and controllable short channel effects. Therefore, the need of Bohm Potential, Van Dort's and Hansch's Models are more fitting for accurate simulations of the effects of quantum mechanical effects in the channel near the gate oxide interface in MOSFETs.

Moreover, the improvement of the drive current is more obvious in the suppression of the short channel effects. Below are the simulated results when using ATLAS for the saturation and the leakage current at both above and below threshold voltages. It can be seen that Template Bulk MOSFET shows excellent I_{on}-I_{off} characteristic performance with drive current I_{on}=829 µA/µm at V_{gs}=1.5V (Fig (5.21)) and the I_{off} at or below 10 n A at a voltage of V_{ds}=1.5V.

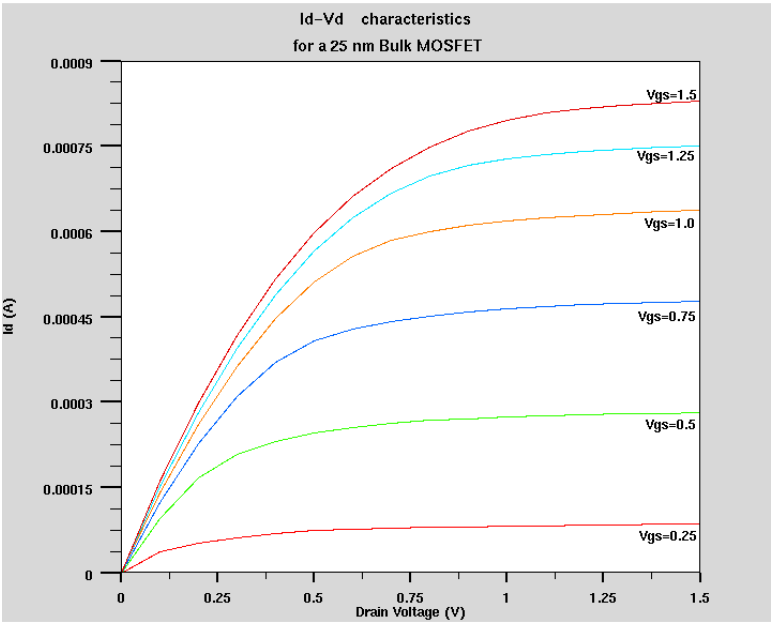

Fig. (5.21): shows the Current-voltage characteristics of n-channel Bulk MOSFET of a 25 nm gate length.

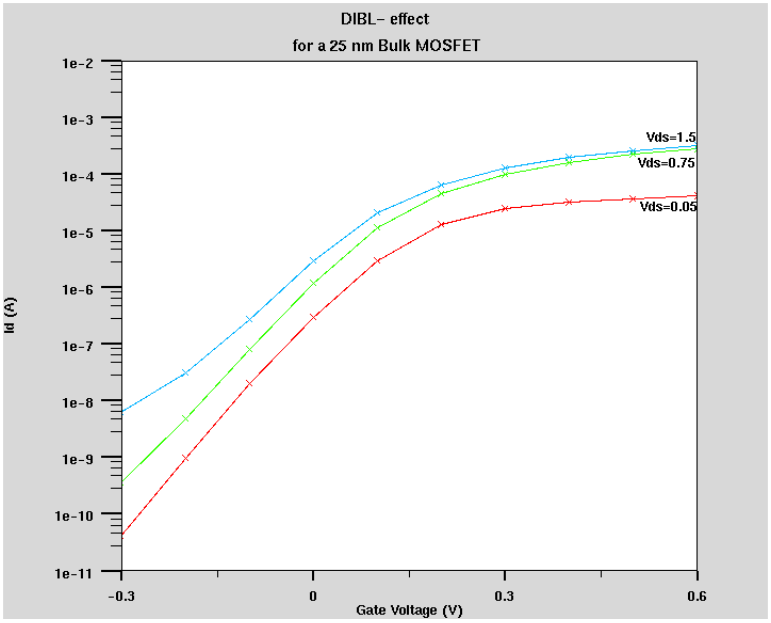

Fig. (5.22): Semilog plot of the extraction of DIBL effect for a 25 nm Bulk MOSFET where the shift of threshold voltages is related to different drain-source bias.

5.3.2 Channel Potential Profile

The figure below shows the potential profile in a 25 nm Bulk MOSFETs corresponding to central parts of the channel where threshold voltage were determined from the minimum channel potentials for a set of gate-source voltage, selecting the ones that comply with the threshold condition.

It can be seen that increasing drain-source bias lowers the threshold voltage (DIBL-effect) related to the reduction of the energy barrier.

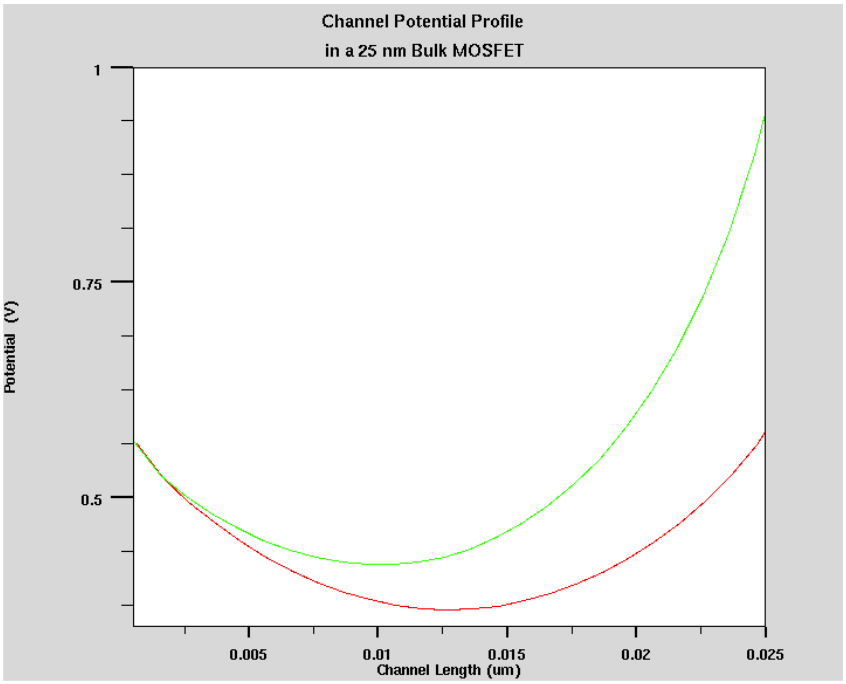

Fig. (5.23): shows the simulated result of the channel potential profile of a 25 nm Bulk MOSFET at drain voltage of 0.05 V (lowered curve) and 0.55 V (upper curve).

Since the Bulk MOSFET has a very thin gate oxide and a high substrate doping, there will be strong normal electric fields close to the Si/SiO2 interface. This will create a potential well for the mobile carriers in the inversion layer. Due to the existence of this potential well, the allowed energy states no longer form a continuous band. As a result,

the lowest allowed energy level does not remain aligned with the conduction band edge. This leads to an effective widening of the band-gap.

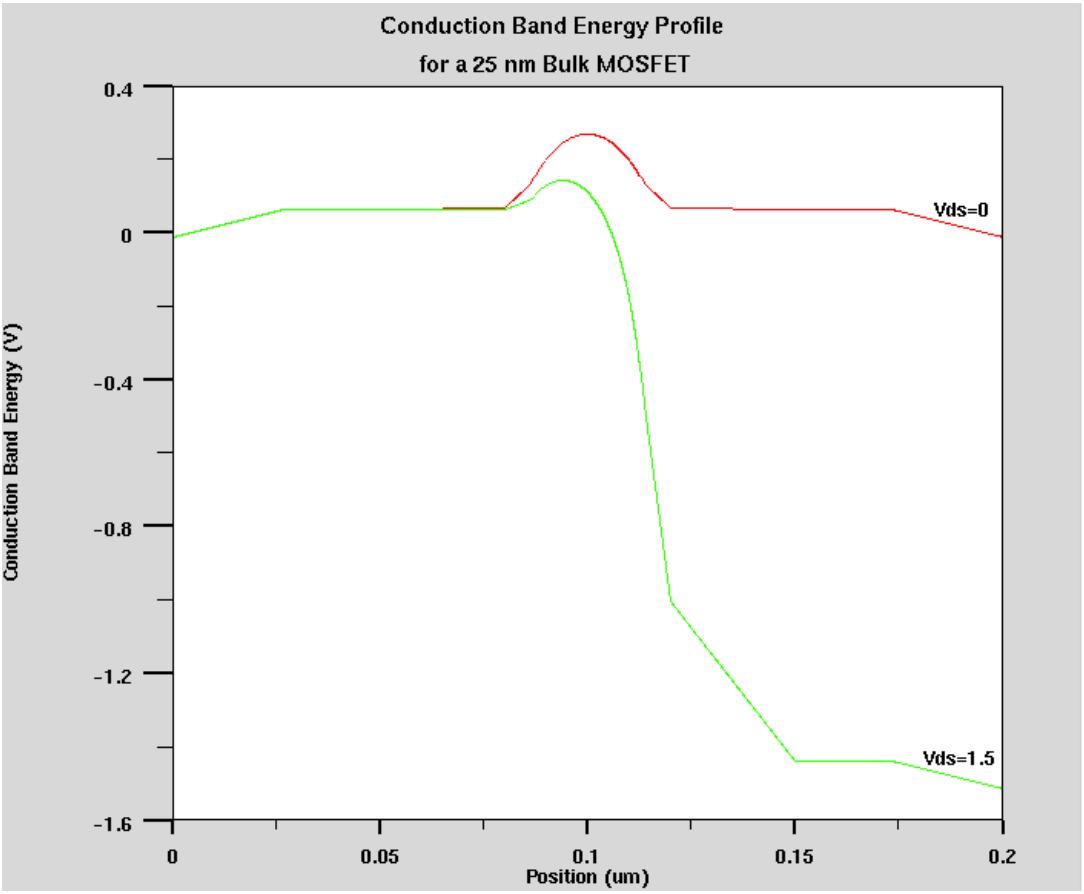

Fig. (5.24): Conduction Band Energy Profile at the Si-SiO_2 interface in a 25 nm n-channel Bulk MOSFET with V_{DS}=0V and 1.5V.

4.4 Double-Gate MOSFETs

Double-gate MOSFETs are promising devices for future high-performance CMOS circuits. As the transistor gate lengths continue to be scaled down to a few nanometres, control of channel effects becomes more and more important. Beside that, it will be increasingly difficult to control the electrostatic interaction between the source/drain that results in device current leakage. The solution to this problem is to enclose the channel area by the double-gate. The gate controls the front and the back which will offer a better control of short channel effect than does a single gate.

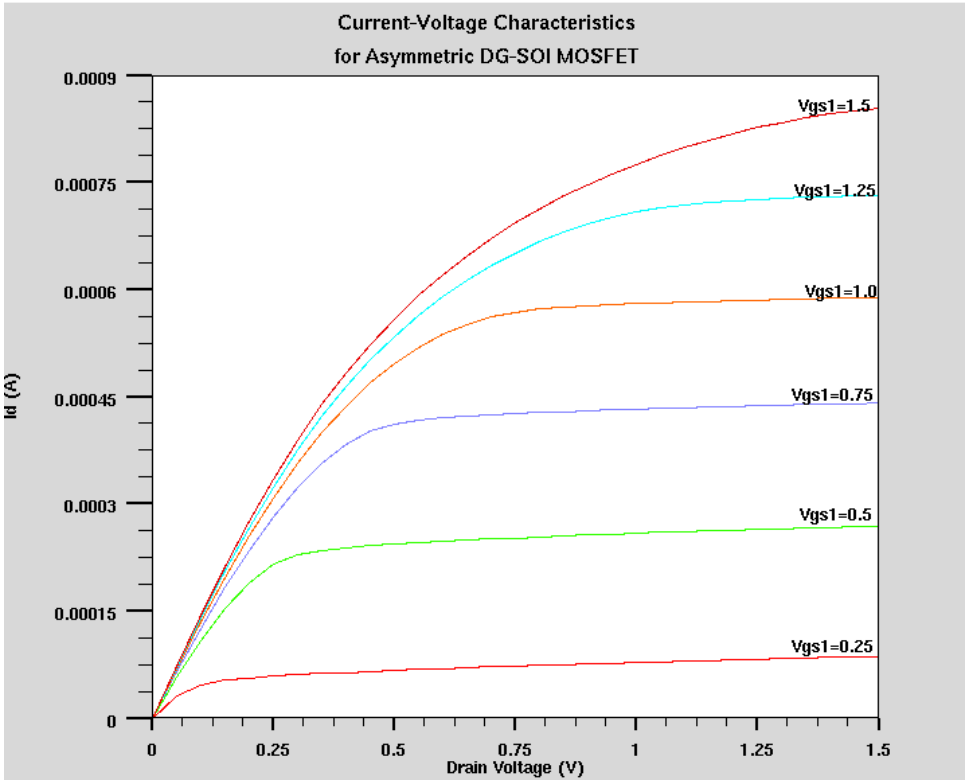

Fig. (5.25): shows the Current-voltage characteristics of Asymmetric double-gate SOI MOSFET of a 25 nm gate length at V_{gs2}=-1 V.

5.4.1 Current-voltage characteristics

First, we have considered the dual-gate DG-SOI MOSFET where the two gates are linked to a similar applied biasing. The simulation results have revealed a large negative threshold voltage which can degrade the device for the use in CMOS applications [11]. To avoid the undesirable more negative threshold voltage, we turned our effort to the asymmetric double-gate device by applying a negative bias to V_{gs2}. For this case, we have found a satisfactory threshold voltage of 0.05V. A maximum drive current which above all of its counterpart devices is reached beside; a superb saturation current is archived.

Figure (5.25) shows the current-voltage characteristics for the Asymmetric-gate (DG) SOI MOSFET. It can be seen that the drive current I_{on} equals to 850µA/µm. Meanwhile, the Bulk MOSFET shows a maximum driving current I_{on} of 829 µA/µm at Vgs=1.5V, as in figure (5.21).

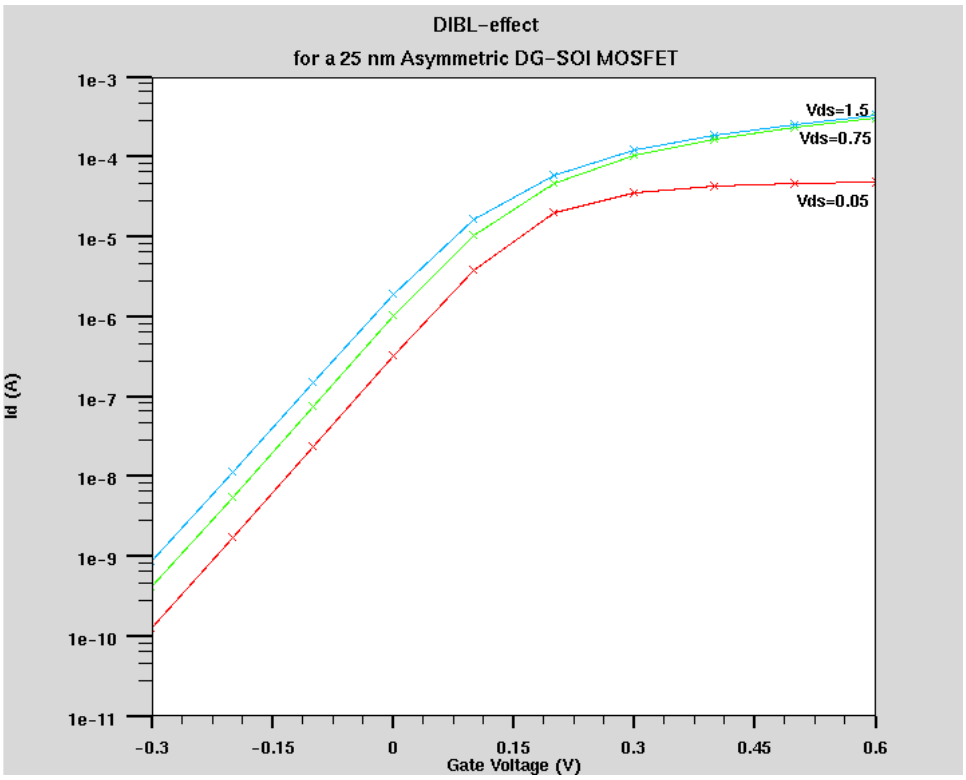

Fig. (5.26): shows the sub-threshold characteristics of Asymmetric DG-SOI MOSFET. V_{gs2}=-1V and V_{ds} at 0.05V, 0.75 and 1.5V.

In the other hand, figure (5.26) shows the I_{ds}-V_{ds} characteristics for the asymmetric DG-MOSFET (V_{gs2}=-1V) at V_{ds}= 0.05, 0.75 and 1.5 V. It can be seen that the device has exhibited an excellent off –state leakage at or below 1 nA at V_{ds} =1.5 V while the Bulk MOSFET has shown 10 nA leakage current at the same power supply of 1.5 V.

In terms of short channel control, simulations have shown that the asymmetric DG-SOI MOSFET device overcome the problem of the minimizing the Drain Induce Barrier Lowering, which has decreased from 100 mV\V in the Bulk MOSFET to 75 mV/V. In the same time, the sub-threshold swing S ($S = \frac{dV_{gs}}{d(\log I_D)}$) has decreased from 98.1mV/decade in the Bulk MOSFET to 71.5 mV/decade at the same drive current of 1 μA.

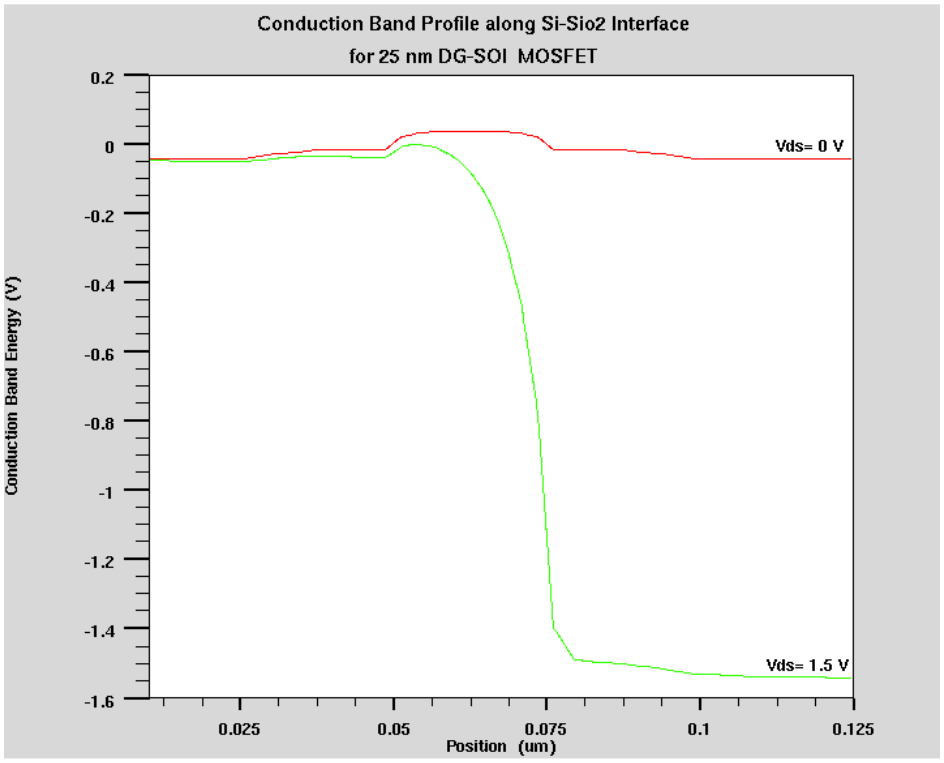

Fig. (5.27): Conduction Band Energy Profile at the Si-SiO_2 interface in a 25 nm n-channel DG-SOI MOSFET with V_{DS}=0V and 1.5V.

Figure (5.27) shows the Conduction band profile at the Si-SiO_2 interfaces where a perfect capacitive coupling between the body and the gates is reached. The potential is almost constant a cross the channel for a very thin t_{si}, thus a small threshold voltage shift is obtained when the drain voltage increased. It can be seen that the DG-SOI MOSFET has a controllable ability of suppressing DIBL-effects than in Bulk MOSFET, figure (5.24).

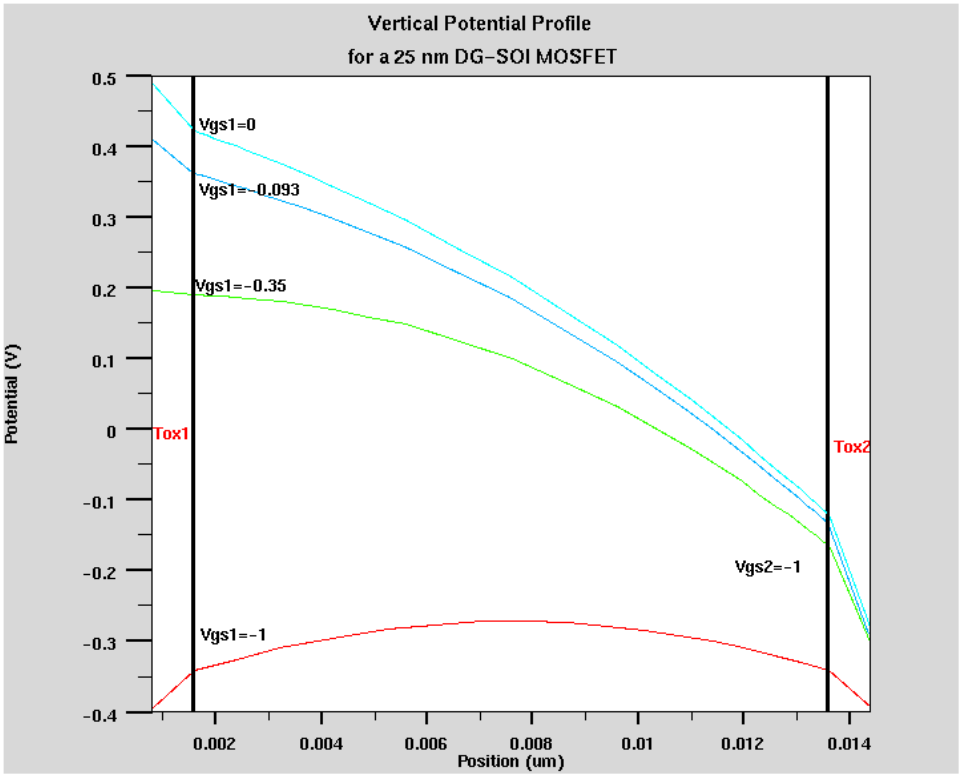

Fig. (5.28): shows the gate-to-gate potential profile at the central part of the channel for a 25 nm asymmetric DG-SOI MOSFET for different gates voltages.

The main principle of proposing the DG-SOI MOSFETs is the idea of controlling the threshold voltage through the interaction between the two gates as can be seen from figure (4.9). To be more specific, we have represented the potential distribution as dependence on the gate voltages as can be seen in figure (5.28). The vertical channel potential profile in the channel is almost constant in the sub-threshold regime, and is shifted with a very small variation according to the variation in the gates voltages. At the drain and source interfaces, first the inversion layer is formed on the inside surface of the

t_{ox1} where the potential changes linearly fixing the surface potential, and after that a parabolic potential distribution is formed where the applied voltage is sustained by the both gate oxides. However, by applying an asymmetric bias to the gates will automatically shift the channel potential from the centre to create a conducting channel at gate1 [11]. Therefore, the DG-SOI MOSFET has different threshold voltages for the two gates.

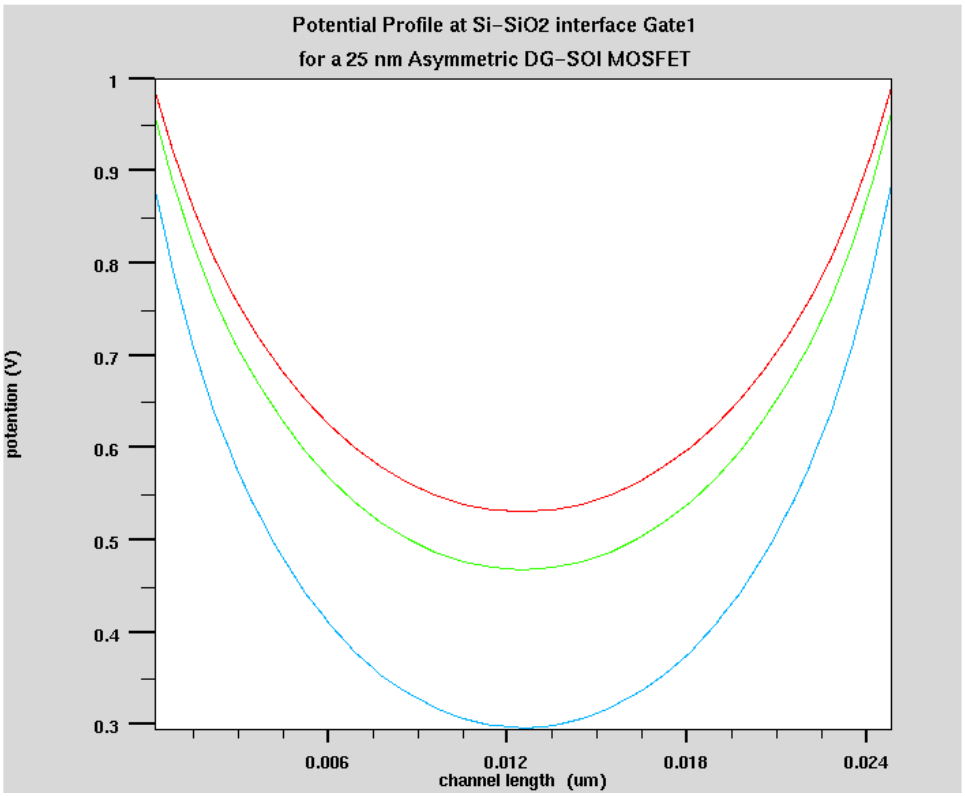

Fig. (5.29) shows channel potential profile at the interface of gate1 for a 25 nm asymmetric DG-SOI MOSFET at V_{gs2}=-1V, for V_{gs1}=-0.35V (lower curve), -0.093V (middle) and 0 V (upper curve).

Figure (5.29) shows the channel potential profile at the interface of gate1, where the effect of the negative bias on gate2 has toggled the problem of the channel transport from the centre of the channel to the silicon/silicon-dioxide interface. Hence, a minimum barrier at gate1 can be reached both above and below the threshold.

CHAPTER 6

CONCLUSION

There have been many advances by the semiconductor industry in the past three decades. Minimum feature sizes have been reduced by more than 2 orders of magnitude, while the clock speed increased by more than 4 orders of magnitude in the same time. One of the most important consequences of scaling resulting from Moore's law is to controllably scale the channel length so as to improve the circuit performance and packing density.

However, as device dimensions continue to shrink, a major challenge is to maintain a good control of short channel effect in the low threshold voltage case. Moreover, high-field effects that are related to the increased electrical field in the channel owing to the reduction of the dimensions, and also quantum mechanical effects will be dominant for very small dimensions. This is especially noticeable in the oxide thicknesses in the deep sub-micron region. As a result, quantum mechanical effects must be considered in modern device design.

In order to control these effects, the device designs needed for deep sub-micron devices are becoming more and more complex as well, involving complicated doping distributions such as super retrograde channel doping, and source/drain extension with a lateral source/drain abruptness for a 25 nm Bulk MOSFETs and for DG-SOI MOSFETs.

We present simulation –based analysis of devices with diverse gate lengths, doping pattern, and in some cases some variety in the oxide thickness (as in the classical MOSFETs where we considered the sub-threshold transfer Characteristics).

In the first task, we build up our simulations based on the model analysis reported in [2] where long channel devices with 250 nm, 210 nm and sub-100 nm are considered. However, the simulated results of the channel potential profile and sub-threshold extraction were compared to the model results in [2], the results has revealed consistency between the simulation and the model analysis.

In addition to that, we compare both drive- and leakage- currents I_{on}-I_{off} plots for both Classical and SSR MOSFETs to give a more complete picture of digital circuit performance achievable using a particular device design. The conventional I_{on}-I_{off} which are directly related to threshold voltage, can be further improved by using channel retrograded doping profile.

Moreover, we have presented a simulation of devices design at the 25 nm channel length generation. The DG-SOI MOSFET is considered to be the most promising candidate for CMOS scaled to the ultimate limit of 25 nm channel length and device structure such as the Bulk MOSFET has also been proposed as a good candidate.

The simulations are based on using a selected doping profile and oxide thickness to cope with the variable specification of the ITRS Roadmap in order to improve the device performance. The results have shown an excellent procedure in suppressing the short channel effects but on other hand, the DG-SOI MOSFET exhibits very high off-state leakage.

Furthermore, the high leakage current in the advanced MOSFETs can be overcome by adopting the alternative high-permeability (high-K) material as the gate insulator.

The goal of using higher K dielectric is to maintain a high level of inversion charge with a thicker gate insulator layer than in the SiO2 case.

These minimize gate leakage currents and at the same time allow device scaling to continue until the ultimate impact of quantum mechanical effects could be advantageous.

Considerable attention has been paid in this work to software engineering tools. While physical insight and workable device designs are the ultimate goals, by paying attention to the means to these ends, we could maximize productivity by producing software that is vigorous, extensible, maintainable and reusable.

The extra effort expended in software design and practicing a structured TCAD software development process has been repaid many times over with the effort saved, certainly in this work and hopefully by future generations of technology designers.

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