UiO : Institutt for informatikk
Det matematisk-naturvitenskapelige fakultet

Frequency $\Sigma\,\Delta$ Modulator with ultra-low power supplies towards sub-100 mV

Thesis submitted for the degree of Master in Electronics, Informatics and Technology

60 credits

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Innhold

1 Abstract

This master thesis centers on the exploration of a frequency delta-sigma modulator (FDSM) with ultra-low power supply down to 80 mV for the analog circuitry. The FDSM is configured with ring voltage controlled oscillator (RVCO) serving as the integrator, and two D-flip flops with one as a counter and the other one as a register, finally a differentiator to separate the quantization error from the signal. All components are operated in the subthreshold region as they are supplied with voltages of 80 and 100 mV. Schmitt trigger based logic gates are employed in the entire circuit as the topology is proved to be operational and robust with ultra-low power supply in several sources.

This design offers an unconventional solution to ultra-low power supply limitations, by employing an undersampling of the RVCO under an oversampling method of the overall system. Various simulation results are presented in this thesis, as well as the design choices and analysis of the output signal in both time and frequency domain.

This design has the potential for applications such as biomedical devices for monitoring heartbeats and blood pressure, as well as sensor interfaces for self-powered IoT products.

2 Acknowledgement

I would like to express my sincere gratitude to my supervisors Dag Wisland and Snorre Aunet, I wouldn't have come so far if they hadn't been so understanding of my health challenge during the study period. I developed this enormous respect for all the educators because of how my supervisors has nurtured me during these two years. I see the passion they have for this field, and they are so generous to offer help and pass down the knowledge to the generations coming.

To all the educators, to my supervisors, and to myself for making good choices.

To my grandma 钟淑娣.

3 Introduction

An Analog-to-Digital Converter (ADC) serves as a bridge between the analog world of real-world data and the digital components within a system. It transforms analog signals, such as voltage or current readings generated by sensors, into a digital format. With the advancing technology, the need for smarter and more portable electronic devices is growing rapidly. Given that ADC plays an crucial role in the electronic systems, it's important than ever to explore the power limitation of ADCs.

This growing demand is particularly visible in Internet of Things (IoT) products, which are designed to operate autonomously in collecting and transmitting data. It highlights the need for energy efficiency in these devices. Energy efficiency not only prolongs the lifespan of device batteries but also plays a crucial role in applications like biomedical implants, where continuous patient condition monitoring is essential without any interruptions. Excessive power consumption in such devices carries the risk of generating excessive heat, which can lead to tissue damage and other unwanted outcomes.

Successive approximation ADCs (SAR) have traditionally been the preferred choice for low power consumption. SAR ADCs operate by comparing the input signal to a reference voltage using a binary search algorithm to approximate the input signal's value. This approach simplifies the circuit complexity and reduces power consumption, achieving a low conversion rate that requires just one clock period per bit (plus an additional one for input sampling). However, as the power supply voltage drops to 100 mV, the sampling speed becomes as the primary limitation for the system [1].

In recent years, a SAR ADC was developed in the same 65 nm CMOS process node with a power supply voltage of 600 mV, capable of achieving a sampling rate of 6 MHz [7]. Nevertheless, achieving such a sampling rate becomes challenging as the power supply limit is pushed even lower. Therefore, this thesis aims to explore a frequency delta-sigma modulator (FDSM) designed to operate with ultra-low power supplies of 80 mV and 100 mV in the 65 nm CMOS process.

The choice of FDSM architecture is influenced by the ultra-low supply voltage. The FDSM architecture was initially proposed in [6], where all components within the system consist

of digital gates. The FDSM system was later researched more with ultra-low supply voltage of 200 mV in [22] and [23]. The all-digital gate approach helps alleviate the challenges posed by ultra-low power supplies by enabling transistors to operate in the subthreshold region.

To address the difficulties associated with ultra-low power supplies, such as increased sensitivity to parasitic capacitance, leakage current and diminished operational speed, all the digital gates in this system are employed with Schmitt trigger based circuits as the feedback mechanism of the topology reduces leakage current, which is the significant drawback in the subthreshold operation. Schmitt trigger based gates have also been proven to be robust even when dealing with ultra-low power supply voltages [12], it is also shown in Asta Skirbekk's master thesis work of "Design of SRAM for Sub-100mV Operation Using 22 nm FD-SOI" that Schmitt trigger based inverter and NAND gate are able to perform with sub-100 mV power supplies using 22 nm FD-SOI technology in a practical manner.

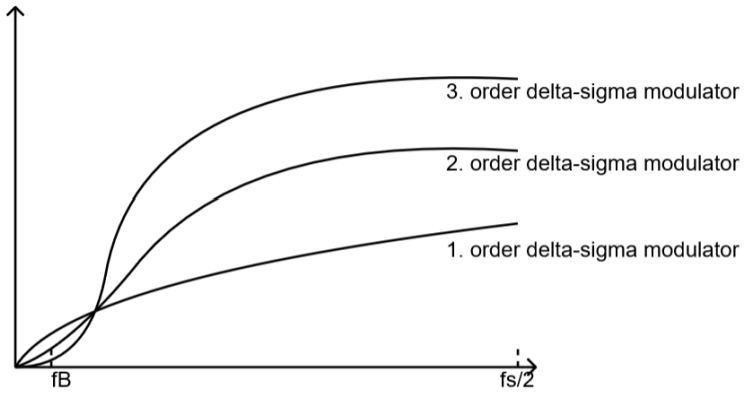
The following chapter provides a foundational understanding of the delta-sigma modulators, along with an introduction of the key constituents of this project. Moving forward, chapter five presents the implementation of the FDSM, dissecting its components in an in-depth manner. This progression leads to chapter six, wherein the results and performance of the converter is presented. The complications of both the results and design process are brought up and discussed in chapter seven. A comprehensive summation of the entire project takes place in chapter eight. Lastly, chapter nine discusses the potential of this project, discussing how the design can be further enhanced.

4 FDSM

The delta-sigma converter is one of the most common data converters used in the industry. Unlike Nyquist data converters which sample at two times the highest frequency component in the signal, delta-sigma converters rely on oversampling and noise shaping to improve resolution of the ADC. The quantization noise is reduced inside the signal band by sampling at frequency much higher than Nyquist frequency, doubling the sampling rate improves the resolution by 0.5bit. SQNR is given as

$$SQNR = 6.02N + 1.76 + 10log(OSR)$$

For every doubling of the oversampling rate (OSR), SQNR is improved by 3dB. Figure 1 demonstrates the effects from the structure of delta-sigma converters. When output of the converter is observed in the frequency domain, noise is suppressed in the signal band at the cost of amplifying the noise at out of band, in this way, the noise in the system is high-pass filtered or shaped.



Figur 1: Noise shaping slope of different orders of $\Sigma\Delta$ modulator, figure inspired by [14]

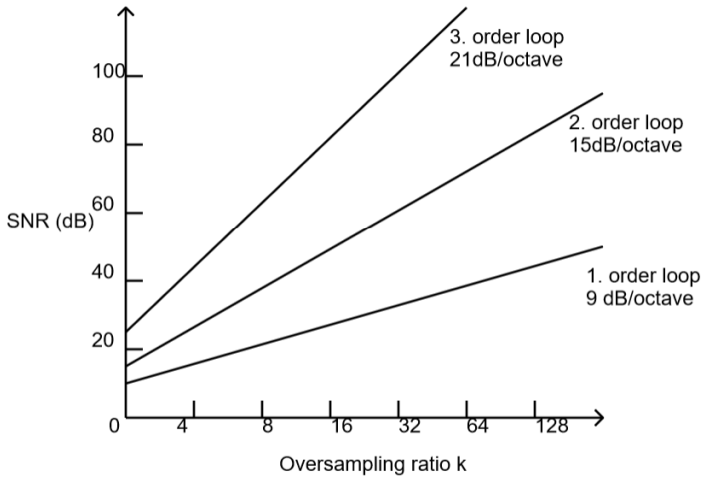
Figure 1 also shows how the noise shaping slope differs for delta-sigma modulators of varying orders when the output is observed in the signal bandwidth.

1. A first order delta-sigma modulator exhibits a noise shaping slope of -20 dB per decade.

2. For a second order delta-sigma modulator, this slope becomes steeper at -40 dB per decade.

3. A third order delta-sigma modulator has even steeper slope at -60 dB per decade.

It is also observed from 1 that as the delta-sigma modulator's order increases, the quantization error power at the baseband decreases.



Figur 2: SNR vs oversampling ratio. Illustration inspired by [3]

Signal-to-noise ratio (SNR) is improved significantly when combining oversampling with noise shaping, effect shown in figure 2:

- In the case of a first order delta-sigma modulator, SNR increases by 9 dB for every doubling of the OSR.

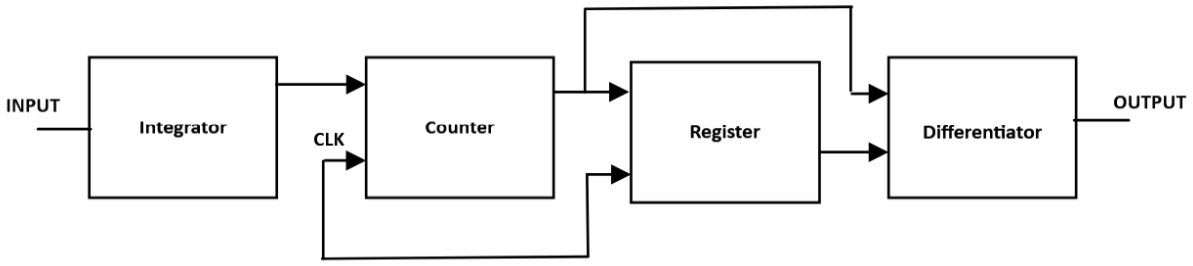
- A second order delta-sigma modulator shows more improvement with an SNR increase of 15 dB for every doubling of the OSR.

- Lastly, a third order delta-sigma modulator showcases the most significant improvement, where the SNR increases by 21 dB for every doubling of the OSR.

Conventional delta-sigma modulators rely on operational amplifier integrator with high gain to perform the integration, which in turn requires high power consumption. This project, however, seeks to investigate the use of a delta-sigma modulator in the subthreshold region, where energy consumption is significantly lower compared to the strong inversion state. Rather than opting for a traditional delta-sigma converter, the project has chosen to employ a frequency $\Sigma\Delta$ modulator (FDSM) to meet the specified requirements.

The analog input signal is first applied to an integrator, the integrator converts the ana-

log signal from voltage domain to phase domain. The phase of the integrator containing information of the modulating signal is then applied to the a counter. However, since the counter only detects integer increments of the integrator phase, quantization error is introduced in the system. The output of the counter is then sampled with a register triggered by a clock. The resulting sample sequence is differentiated in the digital domain to retrieve the frequency information from the sample phase, thereby generating the converter output.

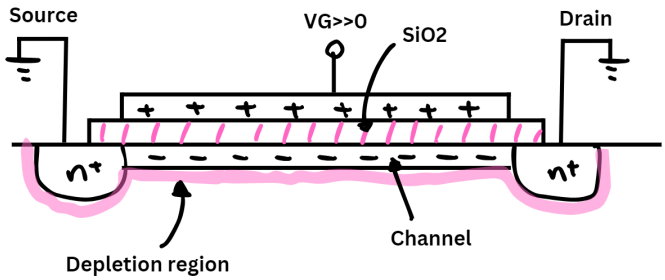


Figur 3: Block diagram of FDSM

4.1 Subthreshold operation

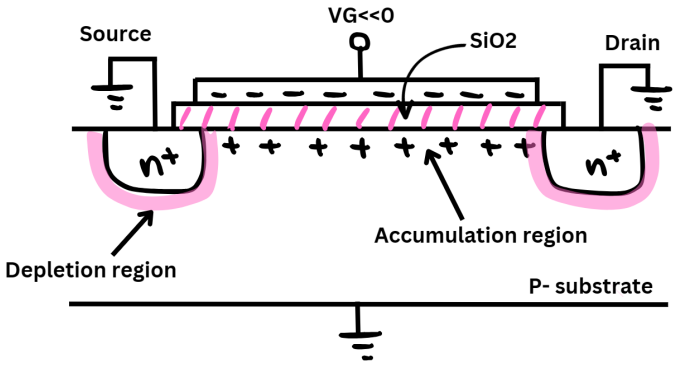
Due to the ultra-low power supply, all the transistors operate in sub-threshold region. When in sub-threshold region, the transistor operates below its threshold voltage ($V_{gs} < |V_{th}|$).

A physical structure of the NMOS transistor is shown in the figure below as the source, drain and substrate is grounded. The transistor can be consider as a capacitor with the gate that acts like one plate of the capacitor, and the surface of the silicon acting like the other plate. Now that the gate and surface of the silicon is considered as a capacitor, when a larger positive gate voltage is applied to the terminal, it attracts negative charge from the source and drain regions. A channel with n region is created right under the thin insulating $Si0_2$, where mobile electrons connects the drain and source regions, therefore creating current flow.



Figur 4: Physical configuration of a NMOS transistor where the channel is presented. Illustration inspired by [8]

For sub-threshold operation, let's first consider the case where a negative voltage is applied to the gate as shown in the figure 5. Since a very negative voltage is applied to the gate, the negative charge will appear near the gate, and positive charge will appear near the channel region. Since the substrate the p-doped, the negative gate voltage increases the channel doping to p^+, resulting in an accumulated channel. The n^+ source and drain regions are separated from the p^+ channel region by the depletion regions, resulting in the equivalent circuit of two back-to-back diodes.



Figur 5: Physical configuration of a NMOS transistor where the accumulated channel is presented. Illustration inspired by [8]

When a small positive gate voltage is applied to the gate terminal. Instead of a channel being created for current flow, a diffusion is appeared under the thin insulating $Si0_2$, as shown in the figure 5. Where the current is denoted as [12]:

$$I_{DN(P)} = I_{N(P)} \cdot e^{\frac{V_{GB(BG)}}{n_{N(P)}\phi_t}} \cdot (e^{-\frac{V_{SB(BS)}}{\phi_t}} - e^{-\frac{V_{DB(BD)}}{\phi_t}}) \quad (1)$$

where $I_{N(P)}$ is the transistor strength/current scaling factor

$$I_{N(P)} = \mu_{N(P)} \cdot n_{N(P)} \cdot C_{ox'} \cdot \phi_t^2 \cdot \frac{W}{L} \cdot e^{-\frac{|V_{TN(P)}|}{n_{N(P)}\phi_t}+1} \tag{2}$$

$V_{GB(BG)}$ = gate-bulk/bulk-gate voltage;

$V_{SB(BS)}$ = source-bulk/bulk-source voltage;

$V_{DB(BD)}$ = drain-bulk/bulk-drain voltage;

$\frac{W}{L}$ = dimension of the transistor;

$\mu_{N(P)}$ = mobility of the electrons at the surface of the channel;

$n_{N(P)}$ = slope factor of when drain current is a function of gate-source voltage;

$C_{ox'}$ = oxide capacitance per unit area;

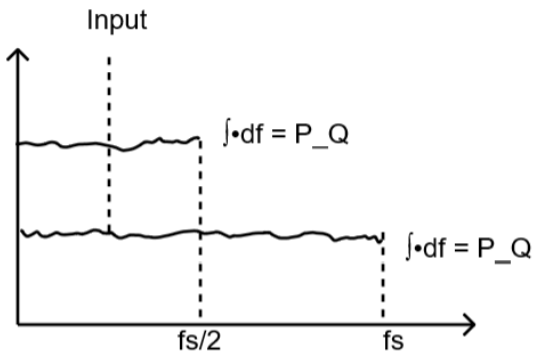
ϕ_t = thermal voltage which is also equal to $\frac{kT}{q}$;

$|V_{TN(P)}|$ = the threshold voltage.

4.2 Oversampling of input signal

Oversampling is a central topic of delta-sigma converters, the attractiveness of the oversampling method is that by oversampling the signal, the noise high pass filter and let out of the band of interest.

Unlike Nyquist sampling theorem which states that to not miss information of the sample, the sampling rate must be twice the highest frequency component in the sample ($2 \cdot f_{max}$). The oversampling implies that the sample is sampled at a frequency that is much higher the Nyquist frequency. There are a couple advantages coming out from the oversampling method. First, by sampling at a higher frequency, the amount of quantization noise is reduced as illustrated in figure 6. The quantization noise power can be calculated as the integration of the derivative of sampling frequency. Therefore the higher the sampling frequency, the smaller the outcome of the integration, thus the smaller the quantization noise.



Figur 6: Quantization noise is reduced by increasing the sampling rate

Secondly, the resolution of an oversampling can be calculated as followed:

$$P_Q = \frac{\Delta^2}{12} \cdot \frac{1}{OSR}, \Delta = V_{LSB} = \frac{V_{ref}}{2^N}$$

Where Δ is the step size, and P_Q is the quantization noise power.The oversampling rate (OSR) can be found as $OSR = \frac{F_s}{2F_b}$, and F_s is the sampling frequency and F_b is the signal bandwidth.

The signal effect of full-scale sine wave input is:

$$P_s = \frac{\Delta^2 2^{2N}}{8}$$

The relationship between signal-to-quantization-noise ratio (SQNR) and OSR shows that for every doubling of OSR, the SQNR is improved by 3dB

$$SQNR = 10log(\frac{P_s}{P_Q}) = 6.02N + 1.76 + 10log(OSR) \tag{3}$$

Moreover, the effective number of bits (ENOB) is improved by 0.5 bit.

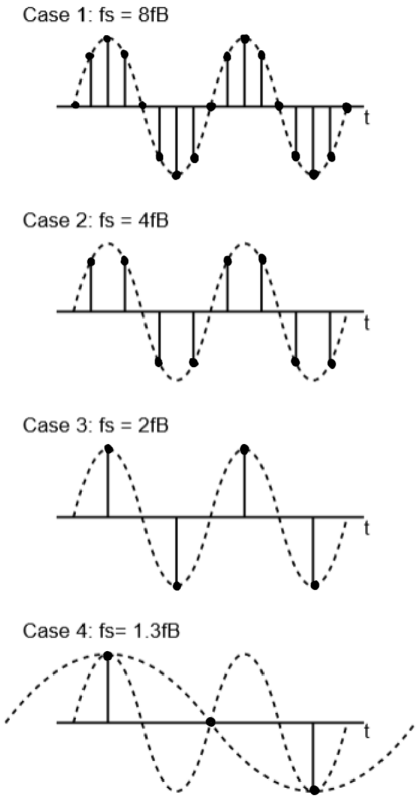
$$ENOB = \frac{SQNR - 1.76}{6.02} \tag{4}$$

The advantages of oversampling help solving the quantization noise limit at the same time improving the resolution of the data converter.

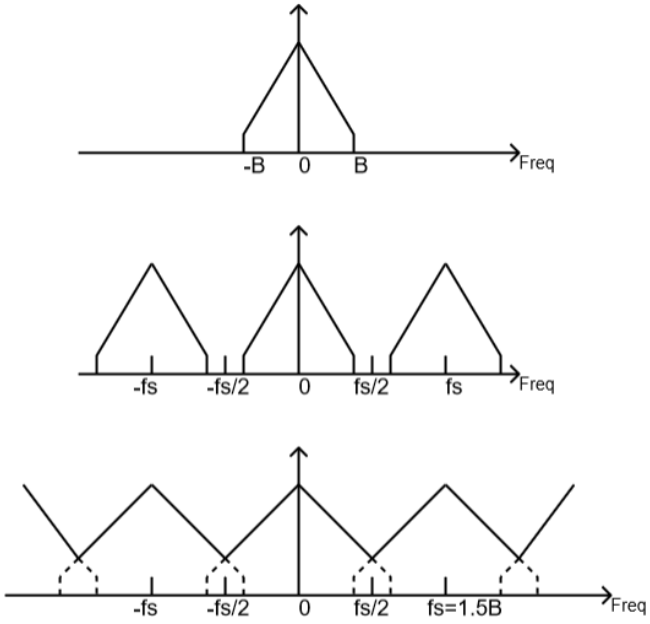
4.3 Undersampling of RVCO

As preciously stated, the undersampling method is utilized in this oversampling converter. Prior to delving deeper into the implementation of the undersampling method, it is important to understand the theoretical background of undersampling and how to undersample without loss of information.

Undersampling is a common sampling technique in signal process, where it implies that it samples less the the Nyquist sampling theorem. To be more specific, undersampling occurs when the data is sampled at less than the $2 \cdot f_{max}$. However, this doesn't necessarily mean that aliasing or lost of information will occur when the data is undersampled. Nyquist Shannon theorem is a modified version of the Nyquist sampling theorem [10], it states that if there's an analog signal with bandwidth f_B, to be able to reconstruct the original signal, the sampling frequency must be bigger than twice the signal bandwidth ($f_s \geq 2 \cdot f_B$). Figure 7 shows the relation between sampling rate and sampled signal, in case 4, when the criteria $f_s \geq 2 \cdot f_B$ is not met, the original sample of sine wave with two periods could be down-sampled as sine wave with only one period, lost of information occurs here. Figure 8 shows what no aliasing vs aliasing in the frequency domain look like. With aliasing, the frequency components overlap with each other, with the overlapping areas as aliasing.



Figur 7: Lost of information occurs when criteria $f_s \geq 2 \cdot f_B$ is not fulfilled, illustration inspired by [14]



Figur 8: Aliasing in the frequency domain

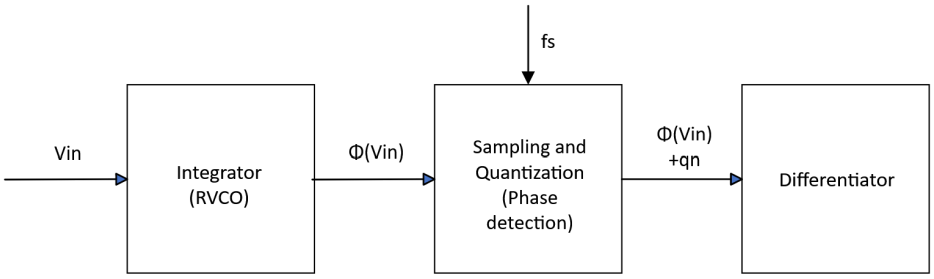
While in some cases, aliasing might be desirable in the sampling process. Undersampling is often employed in the sampling of bandlimited signal. When undersampling a bandlimited signal, the aliasing occurred in the sampled data is known as the desired sampled data. By knowing the aliasing is the desired data, reconstruction of the sampled data can be used to find the desired data. The undersampling method requires lower power consumption because of the nature of less signal is required to processed, which is greener to the environment, and reduce the cost of the overall system.

Moreover, the use of ultra-low voltages in circuits with prolonged standby periods, such as sensor nodes for the Internet of Things (IoT), can significantly reduce power consumption. This makes FDSM particularly beneficial in power-sensitive applications where energy efficiency is a critical factor.

5 Implementation

The FDSM topology is chosen in this project due to the reason that all components in FDSM are digital circuits, unlike the traditional delta sigma modulator, the integrator is implemented with an oscillator instead of operational amplifier, as oscillator is able to do the integration with power supply of 100 mV, while operational amplifier replies on high power supply to achieve high gain to do the integration. With ultra-low power supply of 100 mV, digital circuits provide good benefits of being operational in subthreshold region [5] [19]. In addition, Schmitt trigger based logic gates are utilized in the entire system, as they are proven to be operational and exceed great performance in the subthreshold region[5] [12].

Figure 9 shows a block diagram of FDSM, the integrator, as mentioned above, is implemented with a body-biased Schmitt trigger based ring voltage-controlled oscillator (RVCO), sampling and quantization is implemented with two also Schmitt trigger based D-flip flops (DFFs) and differentiator is implemented with a static XOR gate.



Figur 9: Block diagram of FDSM. Figure inspired by [22]

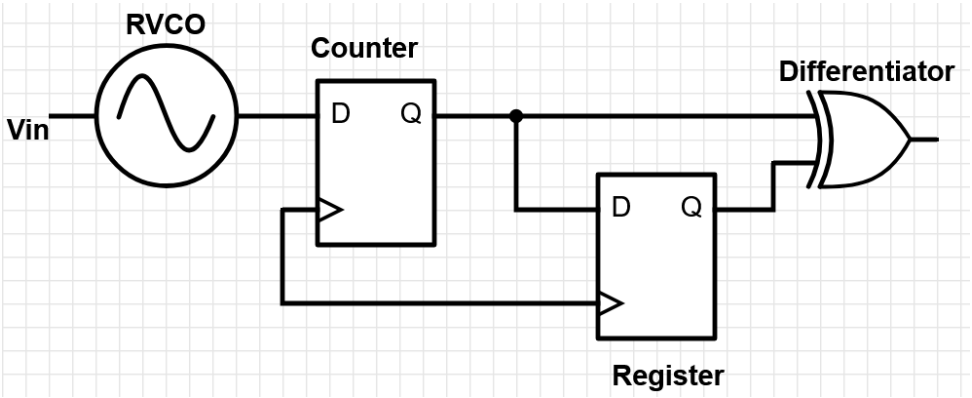
The input signal with peak to peak voltage of 0 and 80mV and frequency of 1 Hz is first applied to the bulk terminal of the RVCO, then later integrated. The output of the RVCO is then sampled and quantized in the DFFs with a sampling frequency of 295.5 Hz, however, the output of the last DFF contains both the signal itself and quantization error, so error is eventually differentiated in the XOR gate.

It's important to highlight that the chosen sigma-delta converter utilizes an undersampling method in its operation. While the overall characteristic of the converter is still oversampling with the sampling frequency (295.9 Hz) is in comparison of the input signal (1 Hz),

however, the sampling frequency is lower than the frequency of the RVCO (around 600 Hz). Consequently, when comparing the sampling frequency and the RVCO frequency, it becomes an undersampling method [6].

The decision to adopt the undersampling method is motivated by the limitations imposed by the ultra-low power supply on the speeds of the DFFs and XOR gate, the clock frequency on these components can not operate faster than the RVCO. As a result, the undersampling method becomes the preferred choice in this particular scenario to achieve the desired performance.

Still, the oversampling of the overall system allows quantization noise to be effectively pushed outside the bandwidth of interest through noise shaping, which is exactly the outcome of this converter.



Figur 10: Block diagram of FDSM

5.1 Theoretical calculation of SQNR and ENOB

SQNR and ENOB were theoretically calculated to estimate the performance of this converter, they set an expectation of how the converter should behave. As mentioned earlier, a signal of 1 Hz is applied at the input of the RVCO , the frequency in the RVCO varies from 594.3 Hz to 655.8 Hz, with it's frequency deviation (Δf = 71.5 Hz). A clock frequency of 295.9 Hz is utilized.

$$\Delta f = 655.8Hz - 584.3Hz = 71.5Hz$$

Carrier frequency f_c

$$f_c = \frac{584.3Hz + 655.8Hz}{2} = 620.05Hz$$

Maximum signal frequency $f_{max} = 1Hz$; clock frequency $f_{clk} = 295.9Hz$, the equation of SQNR for this undersampling FDSM is derived in [6]:

$$SQNR = 20log(\frac{SR_0^{'}}{2\sqrt{2}}) - 20log(\frac{\pi}{6}(2\frac{f_{max}}{f_c})^{\frac{3}{2}}) \tag{5}$$

Where

$$\frac{SR_0^{'}}{2\sqrt{2}} = \frac{2f_{clk}\Delta f}{f_c^2 - \Delta f^2} = \frac{2 \cdot 295.9Hz \cdot 71.5Hz}{(620.05Hz)^2 - (71.5Hz)^2} = 0.1115$$

Therefore

$$SQNR = 20log(\frac{0.1115}{2\sqrt{2}}) - 20log(\frac{\pi}{6}(2 \cdot \frac{1Hz}{620.5Hz})^{\frac{3}{2}}) = 52.28dB$$

$$ENOB = \frac{SQNR - 1.76}{6.02} = 8.39bits$$

5.2 RVCO

A ring oscillator consists of an odd number of inverters connected in a ring or loop configuration hence the name ring oscillator. The working principle is that say, when a high input is applied to the first inverter, the logic high will be inverted to logic low at the output of the inverter. This logic low then again inverted to logic high in the next inverter. After passing an odd number of inverters, the output of the last inverter in the ring is fed back to the input of the first inverter, completing the loop. This feedback causes the next cycle of the oscillation to occur. The continuous propagation of the inverted signal around the ring leads to oscillation, with the output signal transitioning between logic high and logic low states.

Frequency of the RVCO has a relationship with the parameters shown below:

$$f = \eta\frac{I_D}{2NC_LV_{DD}} \tag{6}$$

Where ηI_D is the mean current consumed by the oscillator, N is the number of inverter and C_L is the load capacitance seen by each inverter (gate capacitance, drain capacitance, routing capacitance and a possible additional capacitance or varactor.) While, I_D is the drain current of the pmos transistor, which is mentioned in equation (1).

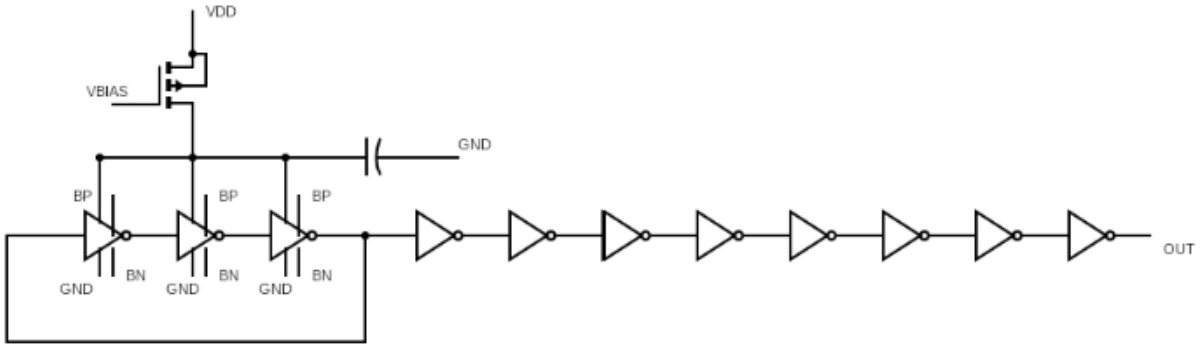
The frequency of the VCO has to be chosen so that it omits $f_{clk_min} = 4 \cdot \Delta f$ where f_{clkmin} is the minimum sampling frequency and Δf is the maximum frequency deviation of the VCO. This criteria makes sure that the undersampling doesn't result in aliasing in the frequency domain. It is worth mentioning that this is the theoretical limit of the sampling frequency where the system is made room for phase noise.

From equations 1 and 6, it is observed that $I_{DS,max}$ can be controlled by manipulating V_{BS}. By increasing V_{BS}, the threshold voltage of the transistor is decreased, ηI_D is also increased. Thereby, the frequency of the RVCO is modulated by manipulating the bulk-source voltage of the transistors (i.e, by modulating the transistor's threshold voltage V_{th}).

Equation 1 implies that $I_{DS,max}$ is exponentially dependent on V_{BS}, and the sensitivity of the RVCO will be increasing with V_{BS}. To obtain linearity, this effect will be compensated with a so-called soft rail technique. This is done by connecting a pmos transistor between VDD and the chain of inverters to improve linearity.

Ring voltage controlled oscillator is appealing to this project for several reasons. Firstly, it offers the potential for achieving high linearity during frequency tuning from the bulk terminals of the MOS transistors. Moreover the presence of multiple output nodes in the RVCO helps to increase the SQNR. Additionally, the RVCO's ability to operate under a low power supply aligns greatly with the project's power constraints. While in comparison to conventional sigma-delta modulators which typically require a high power supply to achieve a high operational amplifier gain, making RVCO more attractive to this project.

5.2.1 Architecture

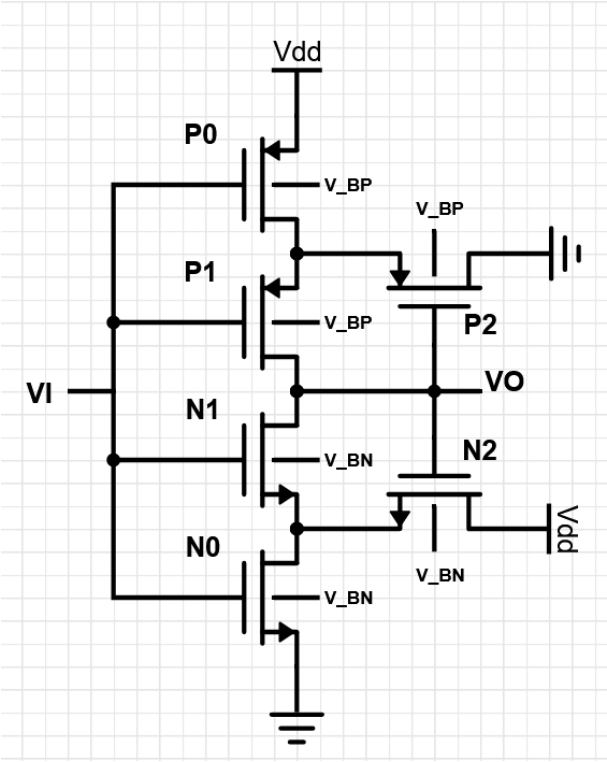


Figur 11: Architecture of the RVCO

A sinusoidal signal with 1 Hz as the input signal of the RVCO is applied to the bulk terminals of the transistors. Three inverters are chosen to match with the specific frequency range desired in the project, they are connected after each other to make a ring structure. The soft rail technique is implemented with a pmos transistor connected between VDD and the inverters to increase linearity of the oscillator. A capacitor is connected between ground and the bias transistor to remove ripples in the oscillations. Finally, eight inverters with maximum width of 2 um, and length of 60 nm are place before the output of the RVCO to boost up the amplitude of the oscillation and low-pass filter the signal to a more square like output.

Notice that single-ended RVCO is employed in this system, a weakness of single-ended RVCO is that it is sensitive to the supply voltage noise. This problem can eventually be mitigated by proper voltage regulation and/or modifying to a pseudo-differential design demonstrated in [23].

5.2.2 Schmitt trigger based inverter



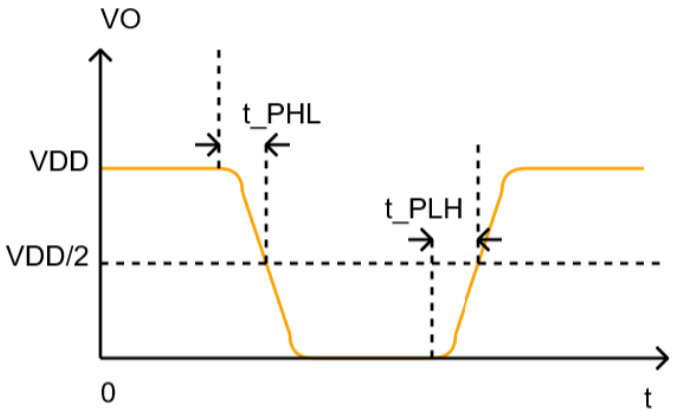
Figur 12: Schmitt Trigger based inverter

The Schmitt trigger topology was selected for its robustness in handling ultra-low power supply[12] [19]. The utilization of transistor stacking in the structure has several advantages, including a tenfold reduction in leakage current, increased voltage gain, improved noise immunity, and reduced sensitivity to process, voltage and temperature variations. Additionally, the feedback mechanism significantly diminishes one of the leakage current routes (will be more in 5.3.2).

5.2.3 Dimensions

A squared signal is desired at RVCO output for the phase detector to detect the phase information. Therefore, to take a good consideration of the rise time and fall time of the inverter is necessary when it comes to designing of the RVCO. Throughout the signal propagation, each transition of the input pulse requires a certain amount of time before the output of the inverter can respond, the moment when the output crosses $\frac{VDD}{2}$ which ideally should be the midpoint of its movement is referred as the “switching point”. The

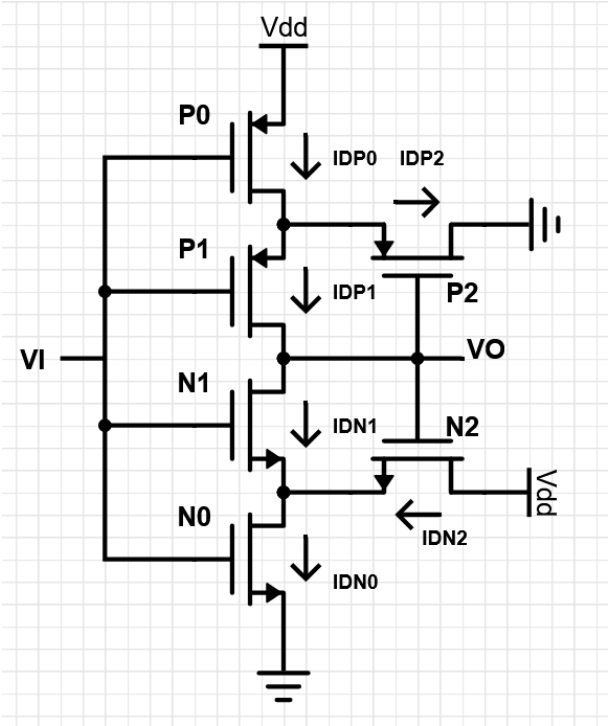
propagation delay for the output to switch from high to low (t_{PHL}) and low to high (t_{PLH})can also be found in this transfer curve characteristic as illustrated in figure 13.



Figur 13: The time delays are defined as indicated. Figure inspired by [17]

The longer the propagation delay the rounder the edges of the output are, the less of this signal is desired. Hence, the emphasis is placed on achieving a robust voltage gain for the inverter. This ensures a shorter propagation delay and leads to more squared-like outputs, as well as symmetric switching is ensured here for the equal current-driving capability in both directions.

Dimensions of the transistors are essential for the a strong gain and symmetric switching. The transistor scaling process is inspired by Luiz Alberto Pasini Melek's PhD work of "Analysis and design of a subthreshold CMOS schmitt trigger circuit"[12], where current ratios were introduced to the transistor scaling process. However, the current ratio method stays an inspiration to this project due to the PhD work was done in 180 nm process and due to the difference in fabrication process, resulting the parameters in the equation to be different. For the convenience of the readers, let's take a general look at the current ratio method that was mentioned in the PhD work.



Figur 14: Current and voltages in the ST inverter circuit, figure cited from [12]

The currents are denoted as $I_{DP0}, I_{DP1}, I_{DP2}, I_{DN0}, I_{DN1}$ and I_{D2} as they flow through transistors P_0, P_1, P_2, N_0, N_1 and N_2. Recall equation 1 for drain currents for nmos and pmos, now assume that p and nmos networks have the same strength, and slope factor to n and pmos are both equal to one ($n_N = n_P = 1$), resulting $I_{N(0,1,2)} = I_{P(0,1,2)} = I_{0,1,2}$.With lengthy algebra for finding the small voltage gain and derivation of the small voltage gain with respect to current ratio $\frac{I_2}{I_0}$ and $\frac{I_1}{I_0}$, a optimum gain is found for each current ratio.

However, the current ratios for the optimum gain mentioned in the PhD work do not apply to 65 nm process which is used in this process. Therefore the current ratios employed are the optimum results of the different tryouts of the current ratios.

$\frac{I_2}{I_0}$	$\frac{I_1}{I_0}$	Gain [V/V]
0.1	0.4	-3.95

	P_0	P_1	P_2	N_0	N_1	N_2
W[m]	2u	120n	2u	500n	250n	2u
L[m]	400n	250n	1u	100n	500n	1u

Figur 15: Dimensions of the body-biased inverter

Calculation of the dimensions is described in more detail in the later section 5.3.3. To ensure strong gain and symmetric switching, the optimum current ratios were found, as

listed in Figure 15. The dimensions were first simulated with a ST inverter without body-biasing. Once the result is satisfying, voltages are applied to both the bulk-terminals of n and pmos. To find the strongest inverter gain first will give more room to gain reduction once the body-biasing technique is applied. Even though both bulk-terminals of n and pmos transistors are utilized, only voltage of the nmos bulk-terminals is varying, while voltage of the pmos bulk-terminals remains constant.

Parasitic capacitance is a major limitation for the circuit performance, it causes delays, slow circuit speed and increased power consumption. This is primarily due to the prolonged time required for current to charge and discharge the parasitic capacitance. To mitigate this issue, one finger and one multiplier were employed to minimize the contribution of parasitic capacitance as much as possible. Multiple fingers may reduce drain capacitance, however, based on the simulation results. It seems like multiple fingers has more internal capacitance than single finger.

5.2.4 Soft rail technique

Linearity is one of the major limitation of an ADC, non-linearity from the RVCO introduces unwanted harmonic components in the frequency spectrum thus decreases the SQNR and further deteriorates the resolution of the converter. A so-called soft rail technique is proven to improve linearity in the RVCO [24]. Therefore, a soft rail transistor is employed in the RVCO to compensate the non-linearity in RVCO.

The working principle of the soft-rail technique is that when V_{BS} is raised, it causes an increase in I_D, consequently leading to a higher mean total current consumption within the RVCO which it's current that flows through the soft-rail transistor.

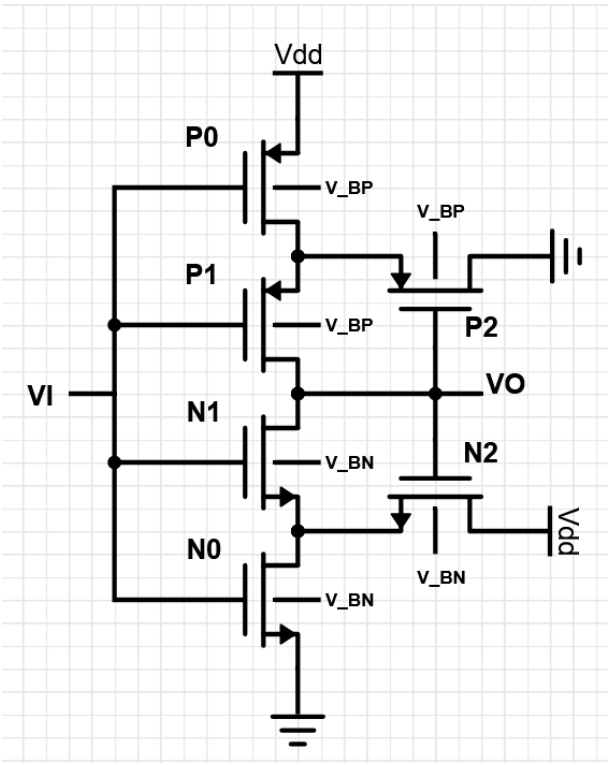
From equation 1 is observed that I_D is exponentially dependent on V_{BS}, which is not a linear relationship between the bulk voltage and the drain current, which can be causing nonlinearity when RVCO integrates the signal. The problem can be compensated by placing a pmos transistor between VDD and the chain of the inverters, since V_{SD} (source to drain voltage) is fixed (with fixed biased voltage V_G and fixed VDD/V_S), as the drain current increases, the V_{SD} also increases. However, since V_S/VDD is fixed, an increase in

V_{SD} results in an decrease in V_D. Bulk voltage changes with the drain voltage which is a soft voltage, in this way the non-linearity is compensated.

Linearity is an important topic for the RVCO and should be considered and handled carefully as nonlinearity introduces harmonic distortion to the signal and further limits SQNR, which is an important parameter to measure how well the ADC performs.

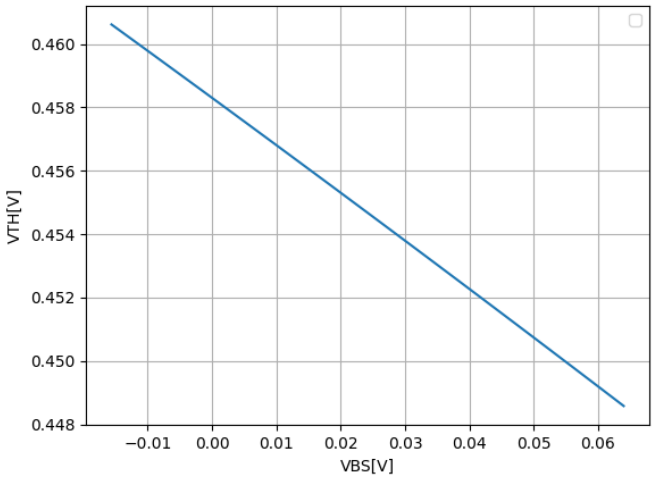
5.2.5 Body biasing

The frequency modulation of RVCO is done by biasing the terminals of the transistors. This technique is also called body biasing. Body biasing technique utilizes the bulk-to-source voltage to modulate the frequency of the RVCO.



Figur 16: Schmitt Trigger based inverter

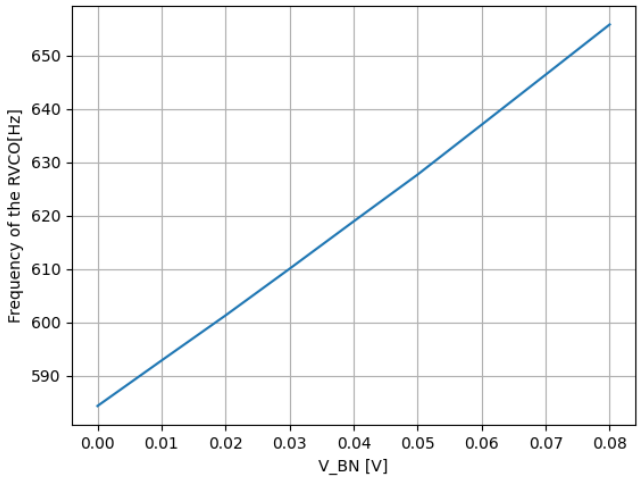
The threshold voltage and the bulk voltage of the nmos transistor have the relationship as the figure shown below:



Figur 17: Relationship between V_{BS} and V_{TH} of a nmos transistor

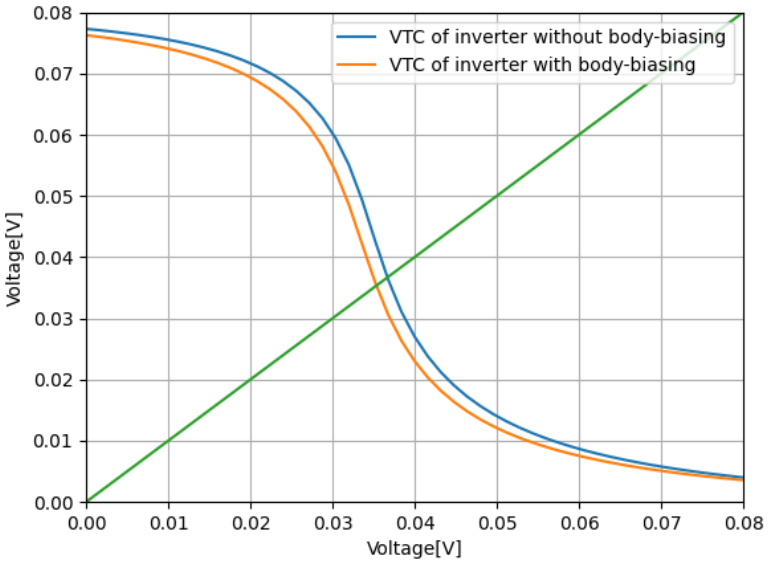
Figure 17 indicates that the threshold voltage is tune-able by adjusting the bulk-source voltage of the transistor, it also illustrates that the threshold voltage decreases as the bulk-to-source voltage increases. Body biasing also results in suppressed occurrence of random dopant fluctuation by manipulating the voltage of the substrates as the threshold voltage is no longer solely dependent on the doping levels [20].

10 mV is applied to the bulk terminal of pmos as it gives the highest frequency according to simulation results in figures 59 and 60. A sinus wave with voltage varying from 0 to 80 mV is applied to the nmos bulk terminal. Nmos bulk terminal utilized for body biasing because figure 18 indicates a linear relationship between RVCO frequency and nmos bulk terminal, as nonlinearity in RVCO introduces harmonic distortions in the frequency domain and further deteriorates SQNR and resolution of the ADC.

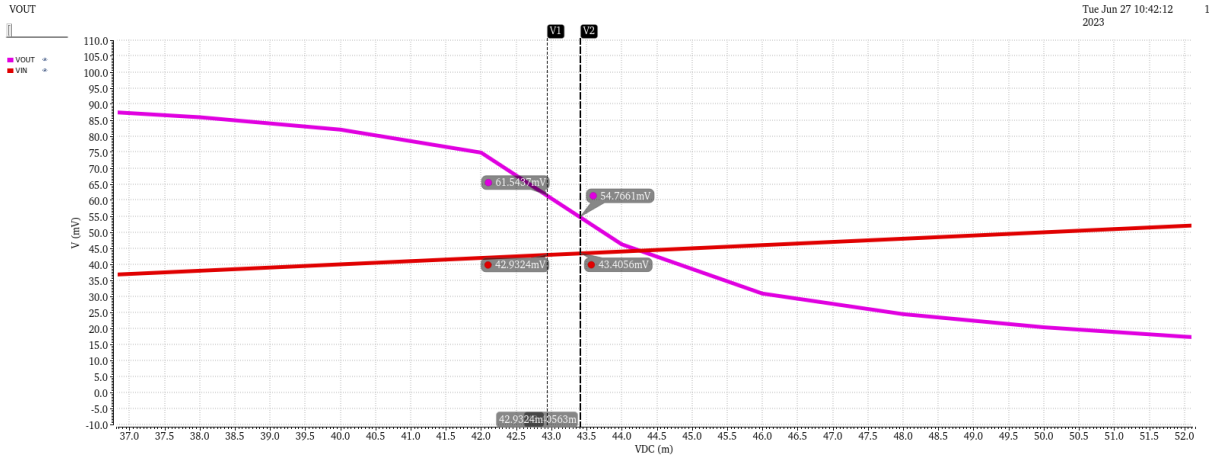


Figur 18: Frequency vs V_{BN} while V_{VBIAS} and V_{BP} stay constant

However, with the benefits of being able to tune the RVCO frequency by applying voltage on the bulk terminal, body-biasing technique comes with a priced. Figure 19 to 21 illustrates that the voltage gain deteriorated from -14.32 V/V to -3.95V/V, loss of symmetry also happens at the same time when body-biasing is technique is applied.



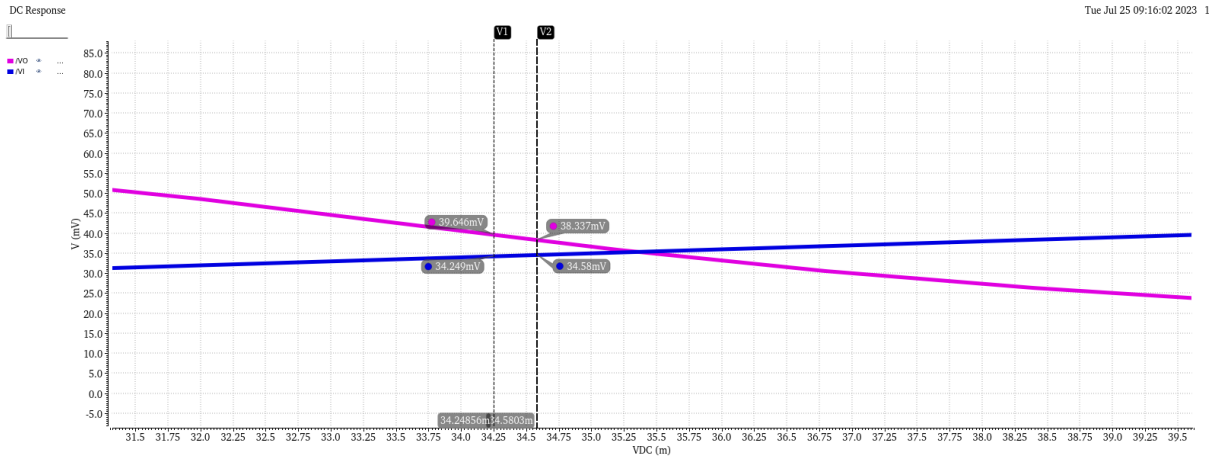
Figur 19: Comparison of VTC of inverter with and without body-biasing



Figur 20: Voltage gain of the inverter without body-biasing

The voltage gain of the inverter without body-biasing is

$$\frac{\Delta Vout}{\Delta Vin} = \frac{49.0842mV - 52.5927mV}{43.8024mV - 43.5574mV} = -14.32V/V$$



Figur 21: Voltage gain of the inverter with body biasing

The voltage gain of the inverter with body-biasing is

$$\frac{\Delta Vout}{\Delta Vin} = \frac{38.337mV - 39.646mV}{34.58mV - 34.249mV} = -3.95V/V$$

As a fixed voltage of 10 mV is applied to pmos bulk terminal and a nmos bulk terminal is applied with a sinusoidal signal with peak to peak voltage of 0 and 80 mV. As not complementary voltages are applied to the n and pmos transistors, it results in unequal

current driving strength of n and pmos transistor, further leading to loss of symmetry.

5.3 D-flip flop

The sampling and quantization part can be seen as a counter connected with a register, with one DFF acts as a counter since a counter triggered by rising edges is equivalent to a D-flip-flop, and the other DFF acts as a register. First, the counter is placed after the RVCO to track the phase, since the counter only detects integer increments of the RVCO phase, quantization error is introduced in the system. Then, the output of the counter is sampled with a register triggered by a clock.

The working principle of the D-flip flop it that it introduce a delay in the state change of their output signal, Q, until the next rising edge of the clock (CLK) signal occurs. If D is 0 and CLK experiences a rising edge, the output Q will be 0; if D is 1 and CLK has a rising edge, the output Q will be 1. Both D flip-flops share the same clock signal to ensure that bits change states simultaneously, eliminating propagation delay issues.

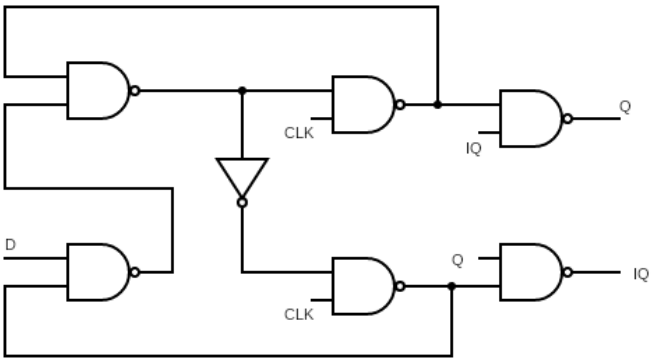
D	CLK	Q	IQ
0	1	0	1
1	1	1	0

Figur 22: Truth table of D-flip flop

Due to the introduction of additional logic gates, synchronous counters have a drawback in terms of power consumption. The power supply applied here is 100 mV, which is 20 mV higher than the RVCO.

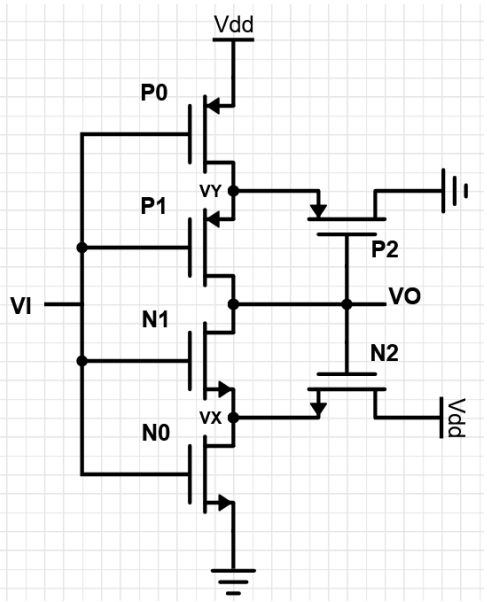
5.3.1 Architecture

Figure 23 shows the architecture of the D-flip flop, this topology is chosen because it has been proven to be robust and operational under ultra low power supply [19].

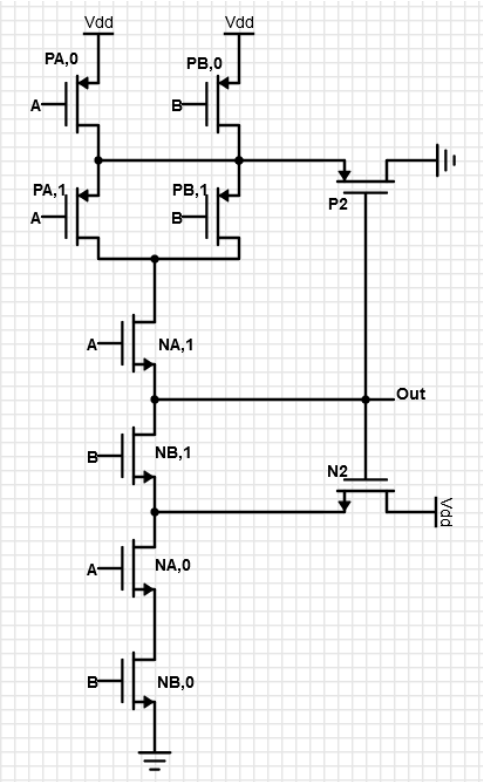


Figur 23: Architecture of the D-flip flop

5.3.2 Schmitt trigger based inverter and NAND gate



Figur 24: Schmitt Trigger based inverter



Figur 25: Schmitt Trigger based NAND gate

Schmitt trigger based inverter and NAND gate are chosen for this system because the topology has been reportedly proved that it provides robust performance with low power supply [5] [12]. The special characteristic of Schmitt trigger structure is that there are two transistor N_2 and P_2 (as illustrated in figure 25) to provide voltage controlled current feedback to the middle node. The benefits from the two feedback transistors is clear by investigating the circuit operation. Let's consider the case where the input signal is at logic high, pmos transistors P_0 and P_1 in the pull up network is turned off, while nmos transistors N_1 and N_0 in pull down network is turned on. Since the pull down network is conducting, a path to the ground is formed, the output signal is at logic low, which turning N_2 off and P_2 on. One thing worth mentioning is that even though P_2 is on, there's no current flowing through the transistor since P_0 and P_1 is off; When the input signal is at logic low, P_0 and P_1 is turned on, N_1 and N_0 is turned off. Pull up network is conducting, a path to VDD is formed, causing output signal to be at logic high. Which turning P_2 off and N_2 on. The interesting thing here is that when N_2 is on, it pulls node V_X to a high potential, which causing V_{gs1} to be negative ($V_{G1} - V_{S1} = 0 - 1 = -1$) and V_{DS1} to be 0 ($V_{D1} - V_{S1} = 1 - 1 = 0$). The fact that V_{GS1} is negative and V_{DS1} is

zero reduces the leakage current through transistor N_1. Therefore, not only that schmitt trigger based digital gates are robust to the low power supply, it also reduces the leakage current by introducing the feedback mechanism.

5.3.3 Dimensions

Sizing of the transistor is especially challenging since there isn't much literature about D-flip flop being designed in the 65 nm process node with such low power. As mentioned earlier, the sizing method used in this project is inspired of Luiz Alberto Pasini Melek's PhD work of "Analysis and design of a subthreshold CMOS schmitt trigger circuit"[12]. The optimum series transistor ratio I1/I0 and I2/I0 was found in Dr.Melek's work.

As it is evaluated in [12], the optimum gain can be found as $\frac{I1}{I0}$ gets closer to 0, and $\frac{I2}{I0}$ equals a certain value. However, since the work was done in 180 nm process node, due to the difference in fabrication process, the parameters in the equation is different in the 65 nm process node which is used in this project. Therefore the theory of the optimum transistor ratios is not accurate in this case. Still, the transistor ratios I1/I0 and I2/I0 were taken as a starting point in this project, and further examined to find the optimum gain for the logic gates.

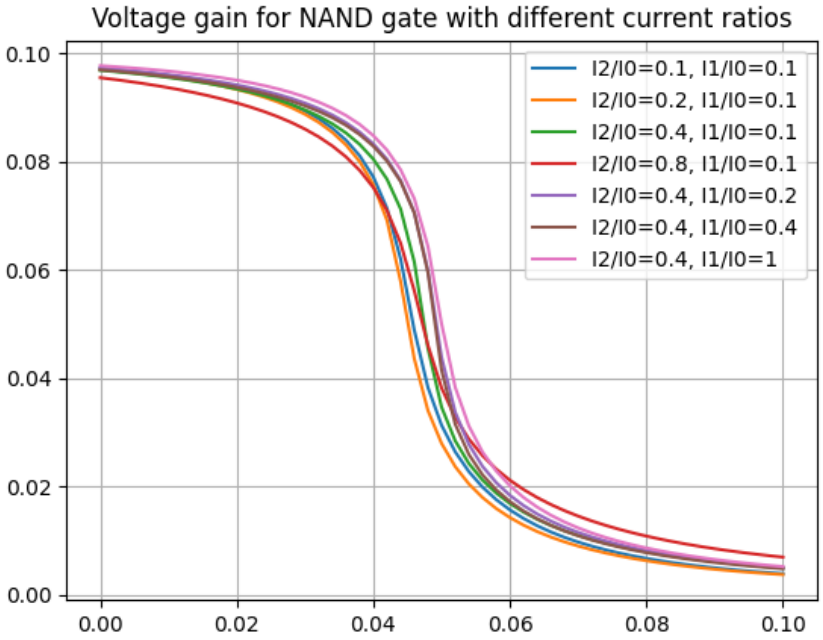
Different current ratios were tried out and tested to find the optimum result of it all. The current ratios were tested in a separate testbench that included only the digital gate itself, parameter sweep was computed, so the dimensions were not directly configured on the transistors. Therefore the gains displayed in the tables below are slightly smaller compared to the scenario where the dimensions are directly set on the transistors.

$\frac{I_2}{I_0}$	$\frac{I_1}{I_0}$	Gain [V/V]
0.1	0.1	-6.05
0.2	0.1	-7.12
0.4	0.1	-7.99
0.8	0.1	-5.13

$\frac{I_2}{I_0}$	$\frac{I_1}{I_0}$	Gain [V/V]
0.4	0.06	-11.86
0.4	0.1	-7.99
0.4	0.2	-8.04
0.4	0.4	-9.03
0.4	1	-7.16
1	0.1	-4.07
1	0.4	-4.74

Figur 26: Current ratios tryouts of NAND gate

The current ratio used for NAND gates in the system is $\frac{I_2}{I_0} = 0.4$ and $\frac{I_1}{I_0} = 0.06$.



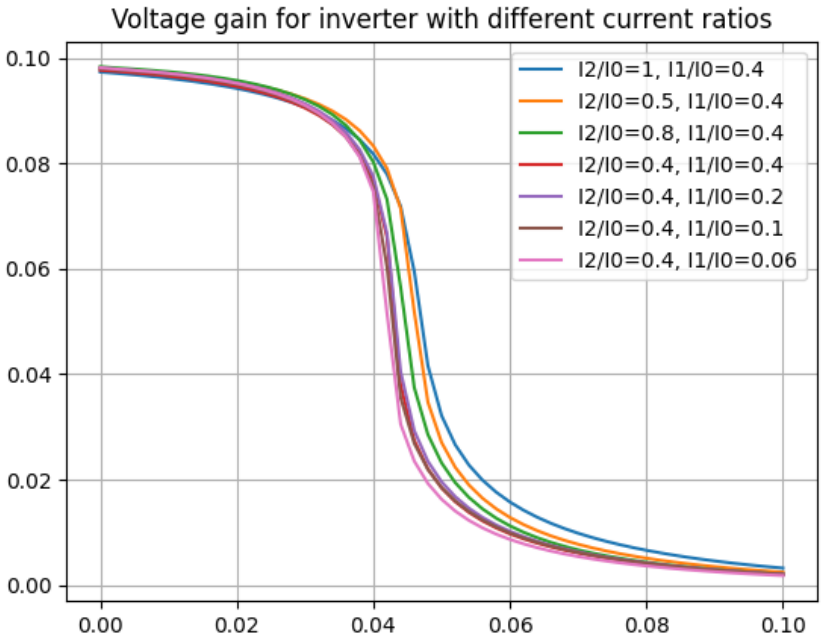
Figur 27: Voltage gain of NAND gate with different current ratios

$\frac{I_2}{I_0}$	$\frac{I_1}{I_0}$	Gain [V/V]
0.4	0.4	-14.02
0.5	0.4	-9.8
1	0.4	-8.94

$\frac{I_2}{I_0}$	$\frac{I_1}{I_0}$	Gain [V/V]
0.4	0.06	-10.5
0.4	0.1	-12.42
0.4	0.2	-13.1
0.4	0.4	-14.02
0.4	0.8	-9.54
0.4	1	-9.69
1	0.4	-8.94
1	0.5	-9.9

Figur 28: Current ratios of Inverter

The current ratio used for the inverters in the system is $\frac{I_2}{I_0} = 0.4$ and $\frac{I_1}{I_0} = 0.1$.



Figur 29: Voltage gain of inverter with different current ratios

A universal rule was applied to the scaling of the transistors: minimize gate length (L). Since larger gate length leads to larger parasitic capacitance. An example of how the parasitic capacitance is related to the gate length is:

$$C_{gs} = \frac{2}{3} W L C_{ox} + C_{ov} \tag{7}$$

where C_{ov} is the overlapping capacitance.

As the gate length has a linear relationship with the gate-to-source/parasitic capacitance, the equation over indicates that the larger the gate length, the more the parasitic capacitance. As the supply voltage going down, the circuit becomes more and more sensitive to the parasitic capacitance, too much parasitic capacitance can cause the circuit to take longer time to charge up the parasitic nodes, ultimately lower the overall speed on circuit and eventually the circuit performance. Therefore, the universal rule in digital circuits is to scale down the gate length to mitigate these issues.

The scaling of the inverter comes in 3 steps:

Step 1: Find the ratios for $\frac{I_2}{I_0}$ and $\frac{I_1}{I_0}$ and further define the relations between the lengths

and the widths:

$$\frac{I_2}{I_0} = 0.4; \frac{I_1}{I_0} = 0.06$$

Assume $I_2 = 1$; thus, $I_0 = 2.5; I_1 = 0.15$

For $I_2 = 1$:

$$\frac{W_{P2}}{L_{P2}} = 1, \frac{W_{N2}}{L_{N2}} = 1$$

$$W_{P2} = L_{P2}, W_{N2} = L_{N2}$$

For $I_0 = 2.5$:

$$\frac{W_{P0}}{L_{P0}} = 2.5, \frac{W_{N0}}{L_{N0}} = 2.5$$

$$W_{P0} = 2.5L_{P0}, W_{N0} = 2.5L_{N0}$$

For $I_1 = 0.15$:

$$\frac{W_{P1}}{L_{P1}} = 0.15, \frac{W_{N1}}{L_{N1}} = 0.15$$

$$W_{P1} = 0.15L_{P1}, W_{N1} = 0.15L_{N1}$$

Step 2: Sweep the lengths for the most symmetric results, insert the actual numbers on the lengths and widths.

Step 3: Since a smaller gate length contributes to less parasitic capacitance which results in a faster logic gate, in this step the gate length will be divided with n ($n \in N$), where the current ratio will still remains unchanged:

$$\frac{L_i}{n} \geq 60nm \wedge \frac{W_i}{n} \geq 120nm$$

where $i \in (0, 2)$, $L_i \geq 60nm$, $W_i \geq 120nm$

However, trade-off between the parasitic capacitance and symmetric switching is inevitable here. The more the length is divided here, the less parasitic capacitance there is in the system, hence stronger voltage gain of the logic gate. But the switching point will be less symmetric by cutting the lengths.

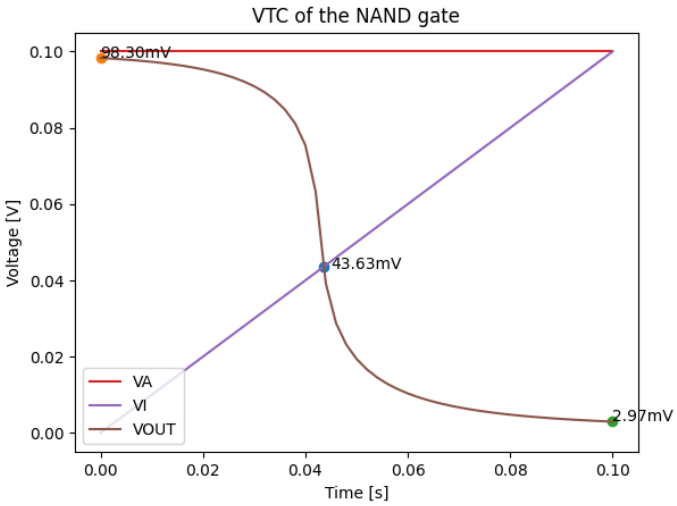
The final dimensions of the inverter and NAND gate are displayed below

Transistor	Inverter [m]	NAND gate [m]
P_0	$\frac{2u}{400n}$	$\frac{2u}{265n}$
P_1	$\frac{120n}{250n}$	$\frac{150n}{200n}$
P_2	$\frac{2u}{1u}$	$\frac{2u}{665n}$
N_0	$\frac{250n}{500n}$	$\frac{250n}{335n}$
N_1	$\frac{500n}{100n}$	$\frac{500n}{65n}$
N_2	$\frac{2u}{1u}$	$\frac{2u}{665n}$

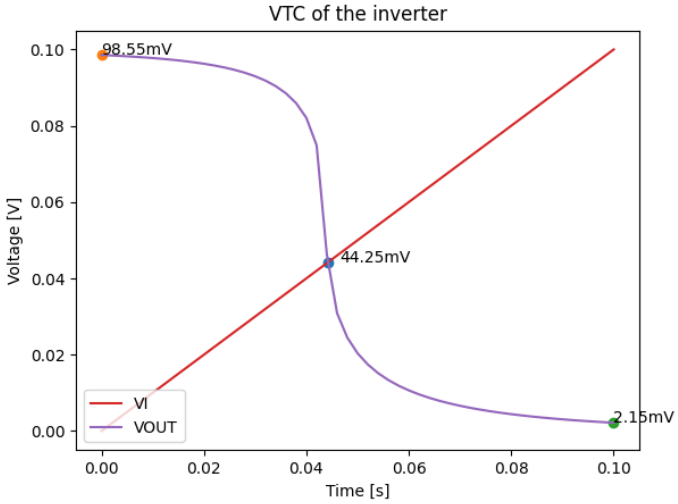
Figur 30: Final dimensions of the inverter and NAND gate

5.3.4 Symmetric switching

A symmetric switching from one logic to another is important when it comes to not only being robust the process variations, but also the ability for a logic gate to keep up with the system when it comes to relatively high system speed. The NAND gate and inverter are powered with 100 mV and the ideal switching of 50 mV is desired. However, because of the ultra low power supply, the circuit is extra sensitive to the parasitic capacitance, which makes a perfect switching difficult. Figure 31 and 32 shows a switching point at 43.63 mV for the NAND gate, and 44.25 mV for the inverter.



Figur 31: VTC characteristic of NAND gate



Figur 32: VTC characteristic of the inverter

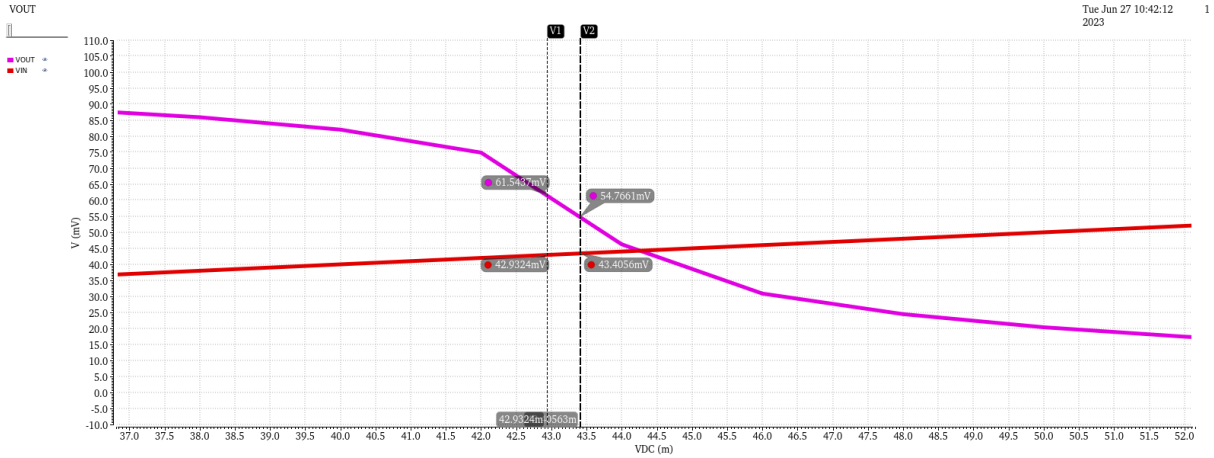
5.3.5 Voltage gain of inverter and NAND gate

Voltage gain serves as an indicator of the logic gate's ability to uphold a consistent logic level at the output. A higher voltage gain signifies that the logic gate exhibits a robust response to variations in the input signal and can sustain a stable output signal. The voltage gain of a logic gate represents the ratio between the Small difference in output voltage and the small difference in input voltage.

$$A = \frac{\Delta V_{out}}{\Delta V_{in}} \tag{8}$$

Voltage gain of the inverter was found by placing two points close to the switching point, the closer the two points the higher the outcome of the voltage gain. By reading for x and y coordinates of the two points, $\Delta Vout$ and ΔVin are found. From figure 33, the voltage gain is calculated as

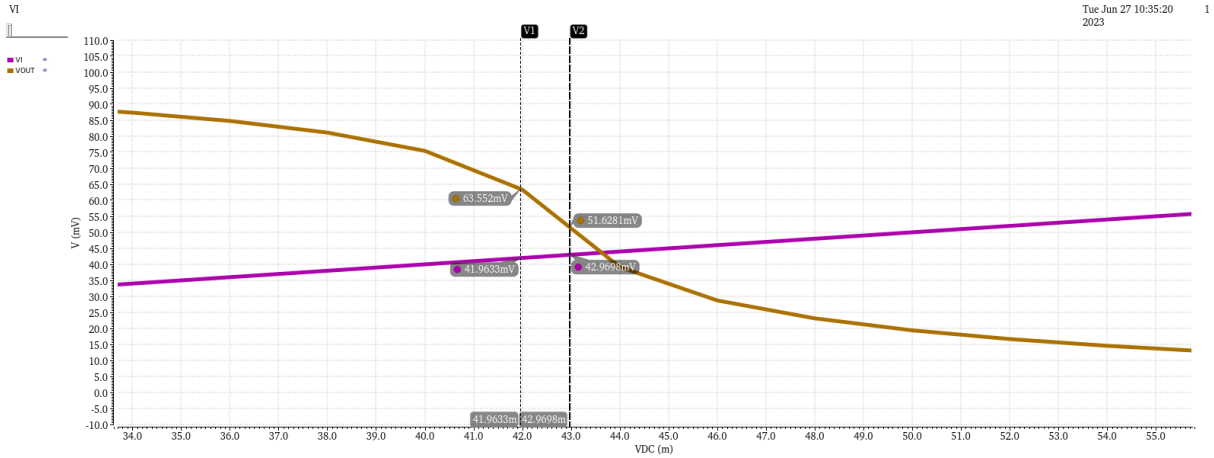
$$\frac{\Delta V_{out}}{\Delta V_{in}} = (54.7661mV - 61.5437mV)/(43.4056mV - 42.9324mV) = -14.32V/V$$



Figur 33: VTC characteristic of the inverter

Voltage gain of the NAND gate is calculated as

$$\frac{\Delta V_{out}}{\Delta V_{in}} = (51.6281mV - 65.552mV)/(42.9698mV - 41.9633mV) = -11.85V/V$$



Figur 34: VTC characteristic of the NAND gate

5.3.6 Noise margin

Noise margin is an important parameter for a logic gate due to the reason that it shows the resilience of a logic gate against noise, which has the potential to generate error at its output. The noise margin can be further specified in relation to the range of input voltage that the gate can accommodate while still producing a valid output signal. A gate with a higher noise margin can tolerate a broader range of input voltage levels without

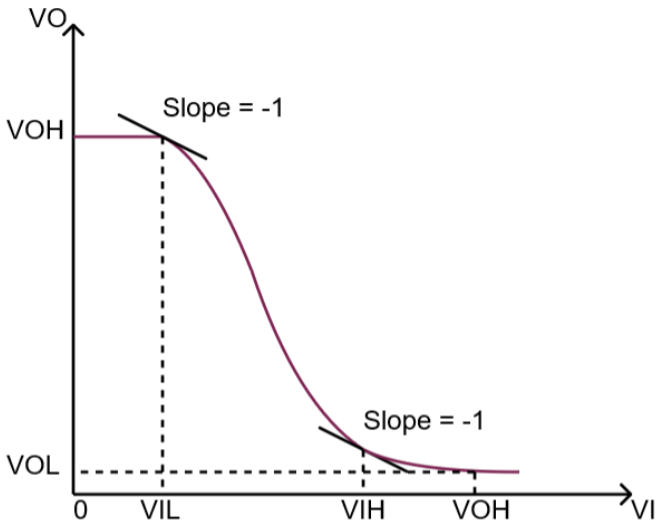
generating an incorrect output signal, in contrast to a gate with a lower noise margin.

There are two main types of noise margins when talked about: the noise margin for a logic high (NM_H) and the noise margin for a logic low (NM_L):

$$NM_L = VIL - VOL$$

$$NM_H = VOH - VIH$$

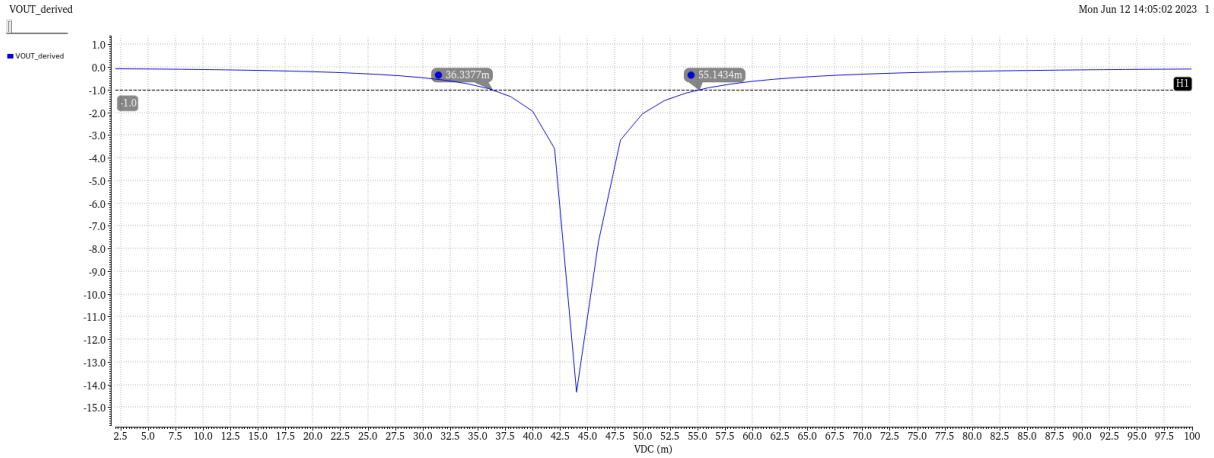
Before further examining the noise margins of the digital gates used in the DFF, it's important to understand transition curve from an output logic high to logic low:



Figur 35: Typical voltage-transfer characteristic (VTC) of a logic inverter, illustrating the definition of the critical points. Illustration inspired by [17]

The figure over shows the transition from output logic high to logic low. It indicates the relationship among the derived output voltage, low input voltage (V_{IL}) and high input voltage (V_{IH}). V_{IL} and V_{IH} can be found at which the slope is -1 V/V. When V_I surpasses V_{IL}, the inverter gain amplifies, causing the voltage-transfer characteristic to enter the transition region. Likewise, when V_I drops below V_{IH}, the inverter also enters the transition region, resulting in an increase in gain magnitude.

Figure 36 and 37 show the derived output voltage of inverter and NAND gate. VIL and VIH are found by locating the -1 slope.

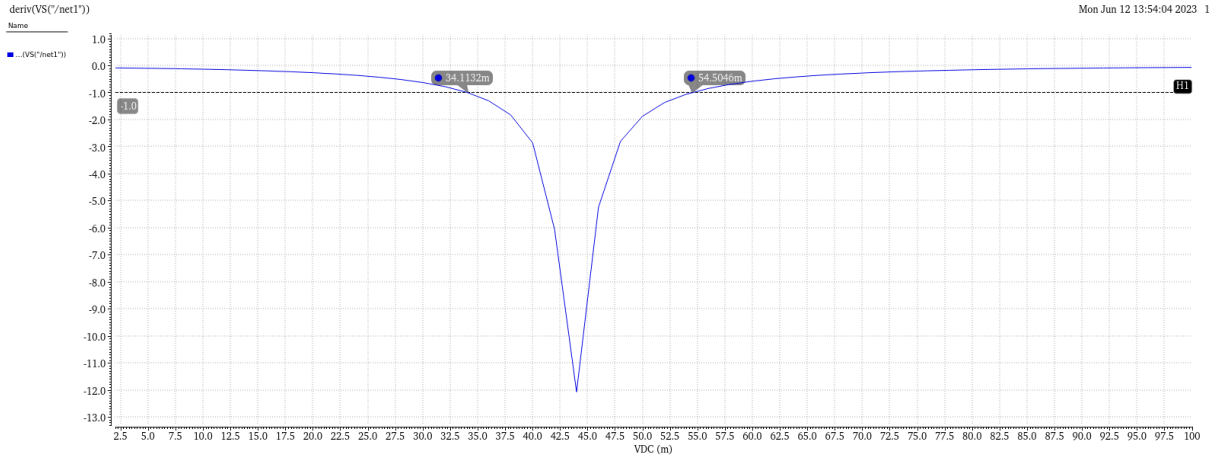


Figur 36: Derived output voltage of the inverter

Noise margins (NM) of Inverter:

$$NM_L = VIL - VOL = 36.3377mV - 2.15mV = 34.1877mV$$

$$NM_H = VOH - VIH = 98.55mV - 55.1434mV = 43.4066mV$$



Figur 37: Derived output voltage of the NAND gate

Noise margins (NM) of NAND gate:

$$NM_L = VIL - VOL = 34.1132mV - 2.97mV = 31.1432mV$$

$$NM_H = VOH - VIH = 98.30mV - 54.5046mV = 44.0464mV$$

Having good noise margins is crucial to ensure the reliability and stability of digital

circuits, which play a vital role in preventing errors resulting from noise and guaranteeing that the circuit consistently produces accurate output signals across various conditions. It is hard to judge the numbers presented in the noise margins above, if it tells us the gate has a good noise margin or a bad noise margin, but it does tell us that the circuit can tolerate that number voltage of noise when the output is producing low (NM_L) or high (NM_H). In [2], NM_L with 100 mV is around 55 mV, which is slightly higher than $NM_L = 34.1877mV$ for this system, NM_H with 100 mV in [2] is around 23 mV, which is slight below than $NM_H = 43.4066mV$ in this system. As said, it's hard to compare these two inverters since they are simulated in different process nodes, different process nodes have different process parameters and transistor current abilities.

5.4 XOR gate

The resulting sample sequence from the DFFs is differentiated by employing an XOR gate to retrieve the signal from the output consists of both the signal itself and the quantization error. While theoretically, a differentiation task could be performed by a Schmitt trigger based XOR gate, since Schmitt trigger based logic gates are proven to be robust with ultra-low power supply. However, with use a Schmitt trigger based XOR gate would involve a new round of transistor scaling, Consuming a substantial amount of time. Due to the time efficiency here, Schmitt trigger based NAND and inverter with prior completion of scaling are utilized for the construction of the XOR gate.

5.4.1 Architecture

The architecture of the XOR gate comes from the Boolean function of the XOR gate:

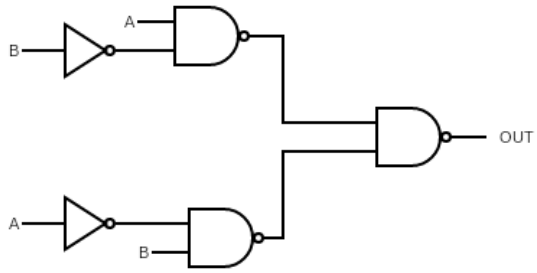
Boolean function of an XOR gate:

$$Y = A\overline{B} + \overline{A}B$$

The logic function can be further written as:

$$Y = \overline{\overline{A\overline{B} + \overline{A}B}} = \overline{\overline{A\overline{B}} \cdot \overline{\overline{A}B}}$$

The logic gates that are needed in the architecture is easily seen from the equation above:



(a) Architecture of XOR gate

A	B	C
A	B	OUT
0	0	0
0	1	1
1	0	1
1	1	0

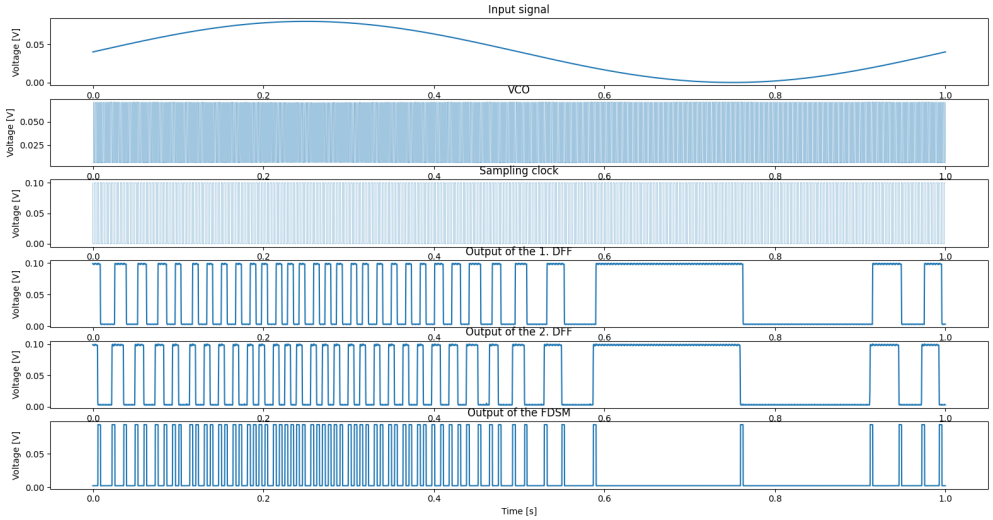
(b) Truth table of XOR gate

Figur 38: Characteristics of XOR gate

6 Results

This section presents the FDSM's performance outcomes, including both simulation results and output signals in the frequency domain. Important dynamic specifications such as SQNR and ENOB are also listed with different bands of interest. Analog signal is successfully converted to digital bit streams while maintaining ultra-low power consumption. Additionally, the design is also run with corners simulations to test its robustness under extreme process conditions.

6.1 Simulation results

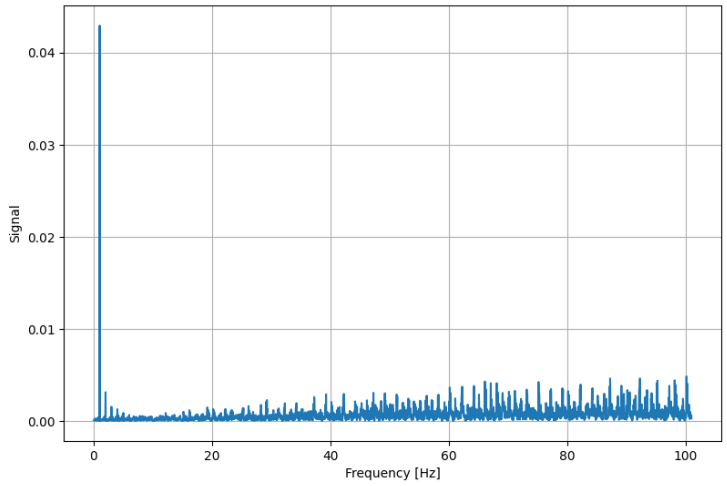


Figur 39: Simulation results of the FDSM system

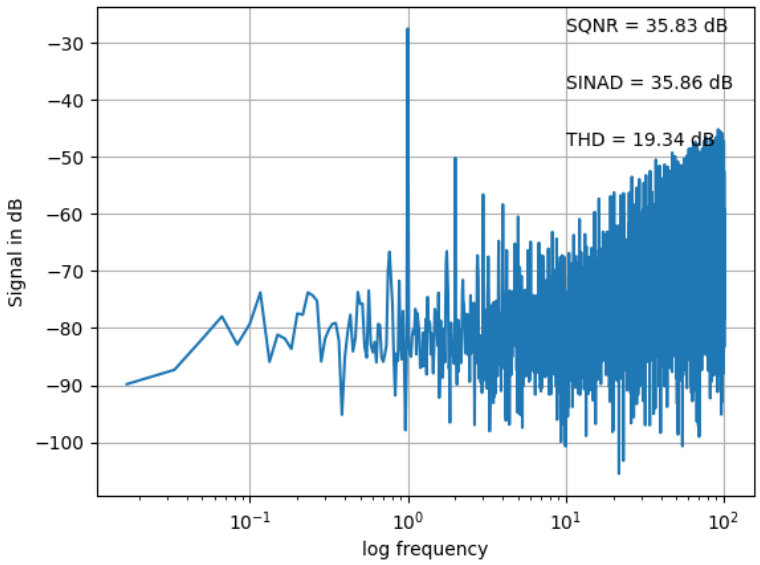
Figure 54 depicts the simulation results obtained from various output nodes of the FDSM. A sinusoidal input signal that varies from 0 to 80 mV is sent into the RVCO to modulate the RVCO frequency. The input signal is integrated in the RVCO and presented as squared like waves at the output of the RVCO. Then, the phase information of RVCO output is sampled by the clock, and presented at the output of the first DFF. The sample result (output of the first DFF) is then passed to the quantizer which is the second DFF, the signal at this point contains the input signal phase information and the quantization error. Finally, the noise is differentiated by the XOR gate at the end. The bottom part of the

figure illustrates the digital bit streams converted from the analog input signal.

6.2 Frequency spectrum



Figur 40: FFT



Figur 41: FFT in dB

FFT shows a noise shaping spectrum of a -20 dB per decade, input signal is observed at 1 Hz, together with harmonic distortions at $n \cdot 1Hz$. The harmonic distortions exist due

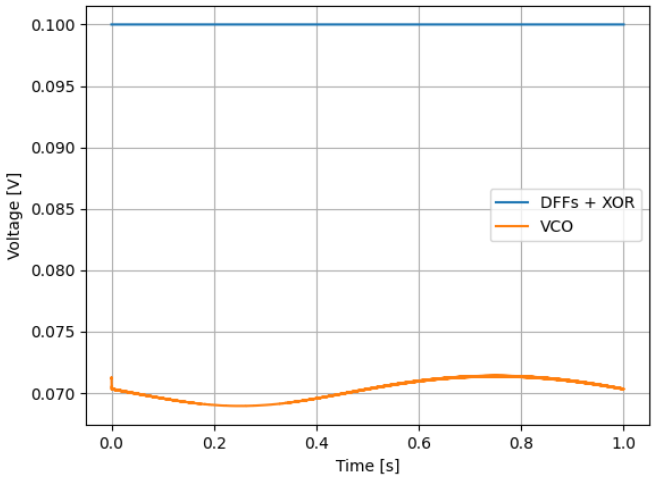
to the non-linearity in the RVCO. The RVCO's function is to integrate the signal, however, since the RVCO is nonlinear, the integration also becomes nonlinear, which results in harmonic distortions in the frequency spectrum. Even though the soft-rail technique improved the linearity, the RVCO is still not linear enough to eliminate harmonic components from appearing in the frequency spectrum. Important ADC performance parameters like SINAD is strongly deteriorated when nonlinearity is introduced in the system, as the harmonic components which are seen as a part of the noise, the ratio drops as the large peaks (beside the fundamental frequency) occur in the frequency spectrum

DC component of the frequency spectrum is manually removed due to the quantized output. FFT counts how many points the output has a constant value(i.e. expresses how long the signal is constant on or off vs how often it switches). Since the output of the FDSM is square pulses, the integrals where the signal is constant on or off appear as DC component in the frequency spectrum.

6.3 Power consumption

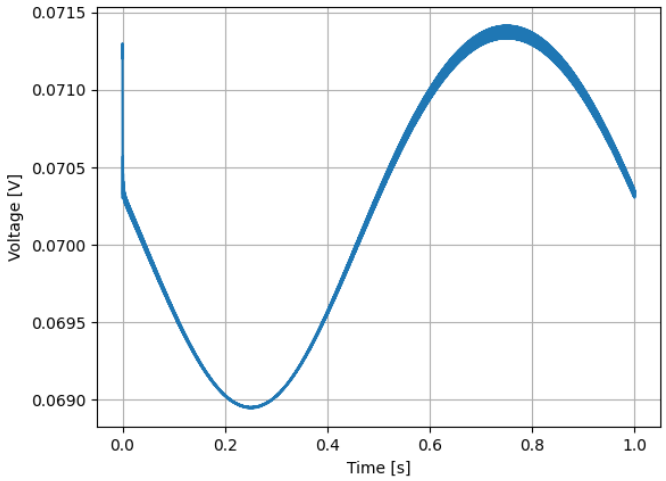
Since the driving force behind this design pertains to IoT products and biomedical implants, it becomes crucial to assess its compatibility with these applications, which typically demand low power consumption.

Power consumption of the ADC is found by finding the average currents and voltages of RVCO and the rest of the circuit, which is computed on the software program Cadence. Then multiplying average current and voltage to get the power consumption. Figures 42, 44 and 45 show the currents and VDDs of the circuit. Figure 42 shows both the constant voltage supply of the DFFs and XOR gate, and the variation in the voltage supply of RVCO.



Figur 42: VDD level of VCO and DFF + XOR gate

The voltage variation of RVCO is illustrated again in the figure below. The RVCO is supplied with a voltage at 80 mV, instead of having a supply voltage constant at 80 mV, figure 43 shows a voltage drop to around 70 mV.



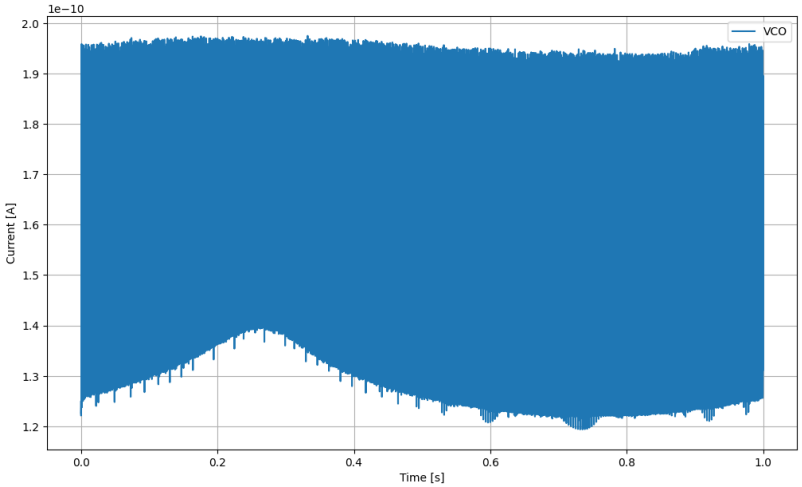
Figur 43: Voltage drop on power supply to RVCO

The relationship between voltage drop and current can be viewed as:

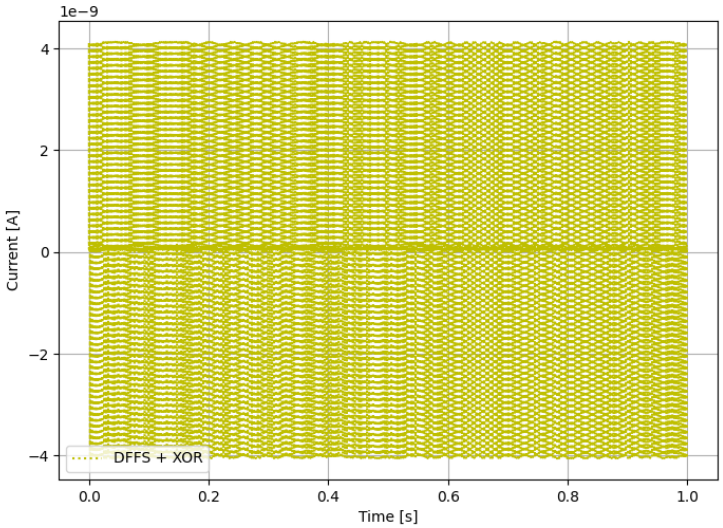
$$V_{drop} = I_{gate} \cdot R_{gate}$$

This again leads to how much current the circuit utilizes to charge up a capacitive node,

and over how long time. The observation made here is that too much current are used to charge up a capacitive node so it causes a voltage drop in the VDD.

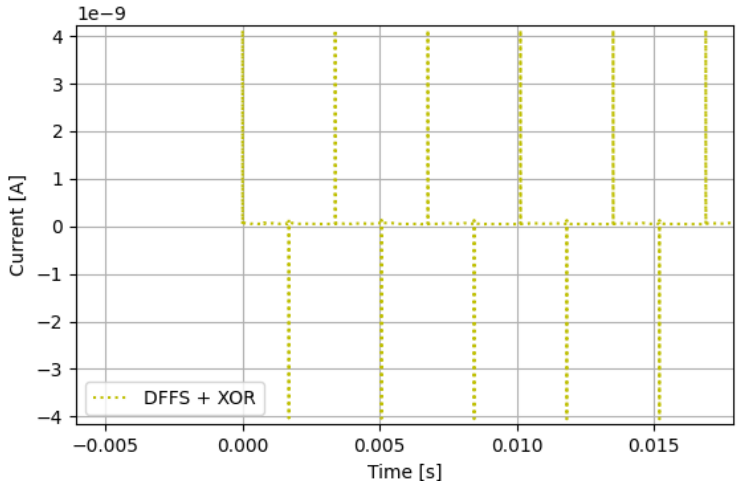


Figur 44: Current consumption of VCO



Figur 45: Current consumption of DFFs and XOR gate

To explain figure 45 further, a zoomed in version is presented below. Because the current is measured at the VDDs of the digital gates, the direction of current flow changes from positive to negative as the path is established, either from VDD to the output or from ground to the output, when the output transitions from 0 to 1 and vice versa.



Figur 46: Zoomed version of figure 45

Power consumption for the RVCO circuitry:

$$P_{VCO} = V_{VCO} \cdot I_{VCO} = 80mV \cdot 137.5pA = 11pW$$

Power consumption for the DFF and XOR gate circuitry:

$$P_{DFF+XOR} = V_{DFF+XOR} \cdot I_{DFF+XOR} = 100mV \cdot 52.64pA = 5.264pW$$

The total power consumption of the ADC is:

$$P_{total} = P_{VCO} + P_{DFF+XOR} = 11pW + 5.264pW = 16.264pW$$

The calculations above shows the design has minimal power consumption, which means it's a great potential for extending battery life. With such low power consumption, heat generation is also low which makes it a good candidate for biomedical implants where heat generation of the chip is a major concern. Last and not least, a product with low power usage is great for the environment, it contributes to reduce energy consumption on a larger sale, leading to a greener and more sustainable world.

6.4 Dynamic specifications

Within this segment, the computation of dynamic specifications, including SQNR, ENOB, SINAD, THD and FoM takes place across various frequency bands of interest. The purpose of these calculations is to provide a comprehensive assessment of the ADC's performance.

Firstly, the Signal-to-quantization-noise ratio (SQNR) is computed as it reflects the relationship between the signal strength and the quantization error introduced in the ADC.

$$SQNR_{dB} = 10\log_{10}(\frac{P_{signal}}{P_{noise}}) = 10\log_{10} P_{signal} - 10\log_{10} P_{noise} \tag{9}$$

Furthermore, an examination is conducted into the Signal-to-noise and distortion ratio (SINAD), which is the ratio of the signal power to the total power in all noise and harmonic distortions.

$$SINAD_{dB} = 10\log_{10}(\frac{P_{signal}}{P_{noise+harmonic}}) = 10\log_{10} P_{signal} - 10\log_{10} P_{noise+harmonic} \tag{10}$$

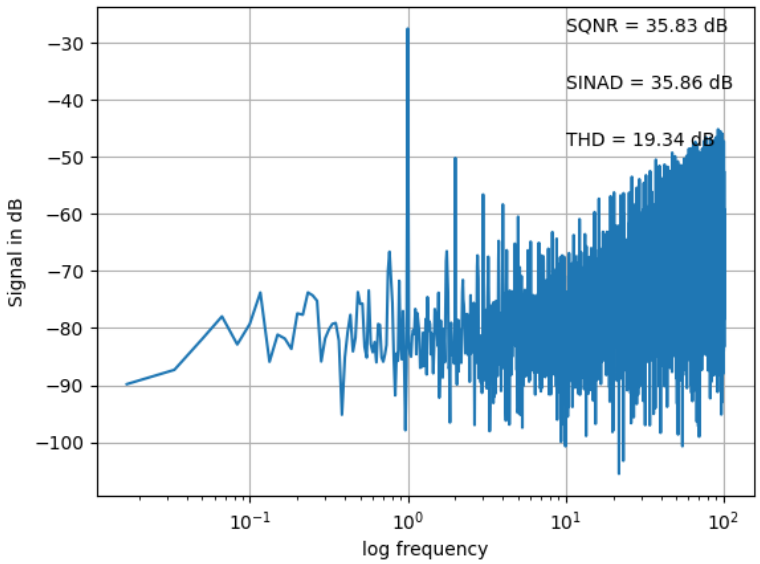
Total harmonic distortion (THD) is also computed as it is the ratio of the total power of all second and higher harmonic components to the power of the fundamental frequency.

$$THD = 10\log_{10} \frac{P_{signal}}{P_{harmonic}} \tag{11}$$

At last, Figure-of-merits (FoM) are calculated to assess the competitiveness of this ADC in comparison to other ADCs. The Walden FoM formula is chosen [9][21] as it relates the ADC power consumption to its performance, considering the factors such as conversion rate and error amplitude.

$$FOM = \frac{P}{2^{ENOB} \cdot f_s} \tag{12}$$

6.4.1 Dynamic specifications with band of interest as 100 Hz



Figur 47: FFT in dB

$$SQNR_{dB} = -27.51999101689828 - (-63.35225074593771) \approx 35.83dB$$

$$SINAD_{dB} = -27.339842531159864 - (-63.37762431059965) \approx 35.86dB$$

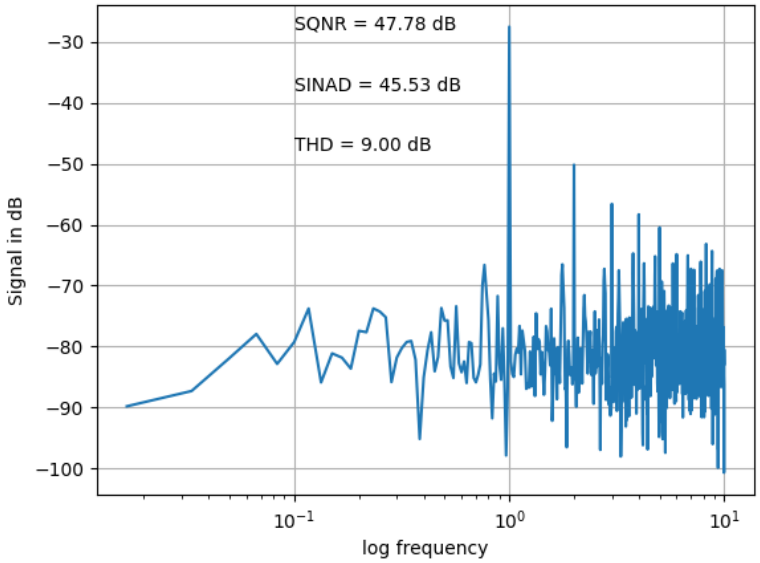
$$THD \approx 19.34dB$$

$$ENOB = \frac{SQNR - 1.76}{6.02} = \frac{35.83dB - 1.76}{6.02} \approx 5.66bits$$

$$FoM = \frac{P}{2^{ENOB} \cdot f_s} = \frac{16.264pW}{2^{5.66} \cdot 295.5Hz} = 1.09fJ/conversion$$

ENOB dropped from 8.39 bits (the theoretical calculation of ENOB) to 5.66 bits, however, the theoretical calculation of ENOB is calculated with band of interest equals to 1 Hz. The results has a bigger application area as it is able to accept higher input frequency up to 100 Hz. This converter shows a competitive power consumption and FoM of 1.09 fJ/conversion based on the simulations.

6.4.2 Dynamic specification with band of interest as 10 Hz



Figur 48: FFT in dB with band of interest as 10 Hz

$$ENOB = \frac{SQNR - 1.76}{6.02} = \frac{47.78dB - 1.76}{6.02} \approx 7.64bits$$

$$SINAD_{dB} \approx 45.54dB$$

$$THD \approx 9.00dB$$

$$FoM = \frac{P}{2^{ENOB} \cdot f_s} = \frac{16.264pW}{2^{7.64} \cdot 295.5Hz} = 0.276fJ/conversion$$

The resolution of the converter is increased as more noise is cut due to the shorten band of interest. FoM shows a even more competitive result with 0.276 fJ/conversion. Notice that THD decreases to 9 dB, this is because as the band of interest cut out more noise, it also cut out the smaller noise components that contribute to the $P_{harmonic}$, as $P_{harmonic}$ is the total power of the harmonic components.

The two types of results presented above show potential applications for heartbeat monitoring, as human heartbeats have a frequency range of 0.6 – 2 Hz, and blood pressure measuring, as the blood pressure has a frequency of less than 100 Hz. Possible application products could include biomedical devices, chest-band devices, and even self-powered IoT products.

Literature [1] displays an ADC performance survey where the conversion energy and SINAD of numbers of ADCs are plotted together for comparison. The lowest conversion energy of an ADC is around 0.1 pJ having a SINAD between 40 to 60 dB. Some other ADCs with conversion energy around 0.1 - 1 pJ even have SINADs around 20 to 40 dB. The dynamic specifications of this system show exciting results of how close this design is to the cutting edge ADCs. Even though these are the simulation results, and doesn't represent the system performance in a practical manner, it still shows the potential this system carries.

6.5 Corners simulations

It is important to ensure the design demonstrates the required performance across manufacturing variability of advanced node processes. Normally, process FET corner combinations are combined with parasitic RC corners, along with variability on voltage and temperature, to ensure robustness of the design. For example, a SS(slow nmos and slow pmos) corner is simulated along with a maxiRC(maximum resistance and capacitance) parasitic corner and an FF(fast nmos and fast pmos) corner is simulated with a minRC(minimum resistance and capacitance) parasitic corner. However, since layout is not made for this design, parasitic corner simulations were not able to be run, but a thorough examination is conducted regarding the influence exerted by temperatures and corner variations on the circuit. Typical Typical (TT), Fast Fast (Fast Fast), Slow Slow (SS), Slow Fast (SF), and Fast Slow (FS) corners are run and evaluated alongside its respective maximum temperature range.

	TT	FF	SS	SF	FS
Temperature range (celcius)	20°- 42°	-22°- 46°	-	-	-

Figur 49: Temperature range of the corner simulations

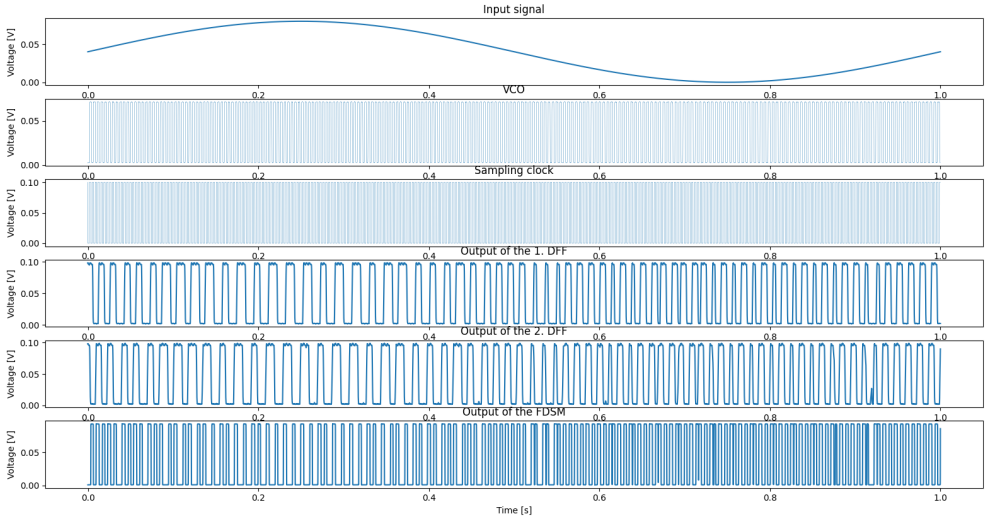
Observed from the table above that the system does not function in SS(slow nmos and slow pmos), SF(slow nmos and fast nmos) and FS(fast nmos and slow pmos) corner. Recall that corner simulation reflects the speed and the ability of the transistor to supply current under extreme circumstances, altering the current delivery capacity of a transistor holds a

similar impact to modifying its dimensions. This design tries to push the limits in typical simulations, but differences in the strength of the pmos and nmos networks impact the voltage gain of the digital gate,, further influencing the circuit speed. Similarly, for the SS corner, if both pmos and nmos have decreased current abilities, the voltage gain goes down, making it harder for the signal to travel through the system.

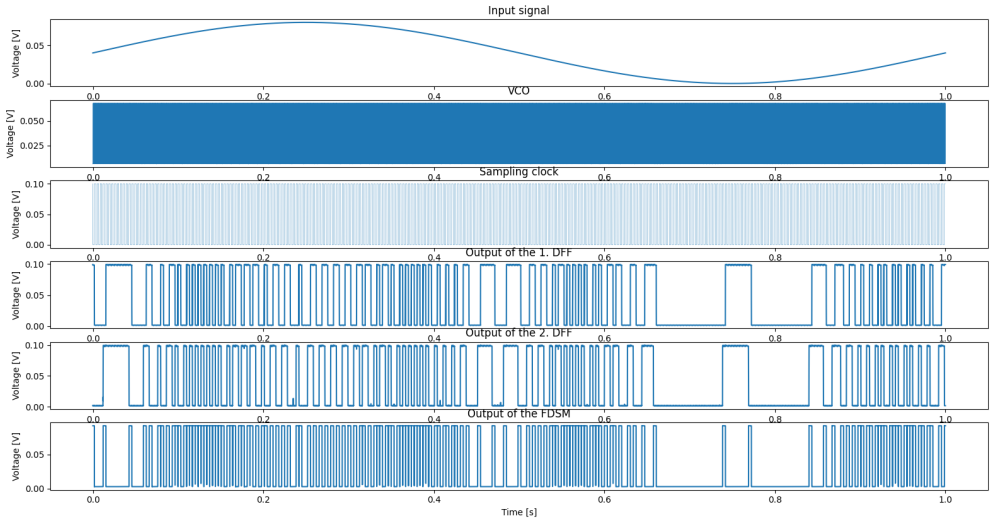
Voltage of the pmos bulk terminal was tuned up for the hope to increase the current capability in pmos for FS corner, and tuned down for the SF corner. Recall equation 1, that an increase in bulk voltage results an increase in drain current of the transistor. However, this method didn't give the desired pmos strength in these scenarios. Even though bulk terminal til pmos was either tuned all the way up to the maximum value or the minimum value, the system was still not able to operate under these corners. Recall equation 6 that with increasing drain current, frequency of RVCO also increases. The increase in bulk voltage results in an increase in drain current and further gives visible change in frequency of the RVCO.

6.5.1 Temperature impact on circuit performance

Figure 50 and 53 are both run under the FF corner variation but with different temperature environments, they illustrate the impact a reduction in temperature has on the circuit.



Figur 50: Fast fast corner simulation result with temperature -22 °



Figur 51: Fast fast corner simulation result with temperature 27 °

Recall equation 1 and 2, now reproduced here:

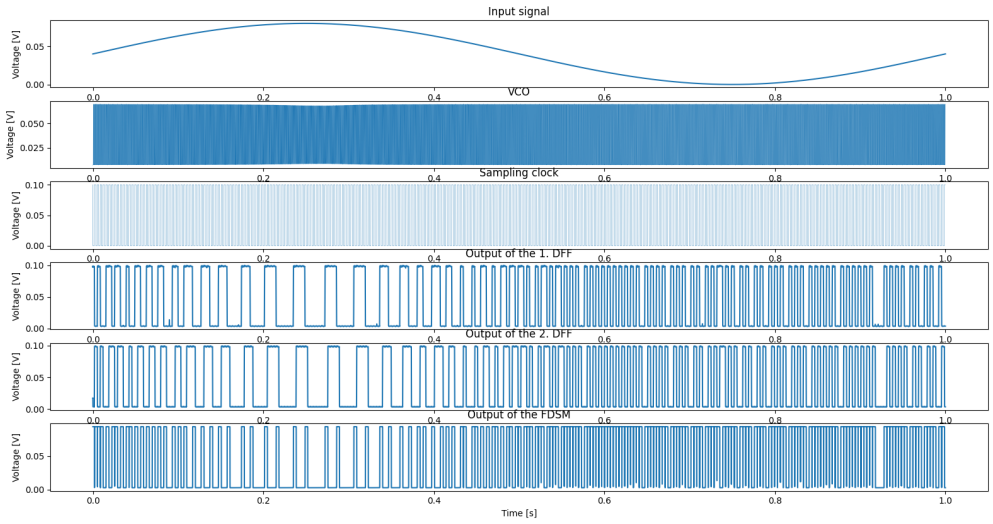
$$I_{DN(P)} = I_{N(P)} \cdot e^{\frac{V_{GB(BG)}}{n_{N(P)}\phi_t}} \cdot (e^{-\frac{V_{SB(BS)}}{\phi_t}} - e^{-\frac{V_{DB(BD)}}{\phi_t}})$$

$$I_{N(P)} = \mu_{N(P)} \cdot n_{N(P)} \cdot C_{ox'} \cdot \phi_t^2 \cdot \frac{W}{L} \cdot e^{-\frac{|V_{TN(P)}|}{n_{N(P)}\phi_t}+1}$$

As the thermal voltage $\Phi_t = \frac{kT}{q}$ has a linear relationship with temperature T, and ϕ_t is

directly related to the transistor strength, a reduction in the temperature will directly reduce the transistor strength, resulting in less current flowing through the transistor. At extremely low temperatures such as -22 °, the RVCO's frequency is evidently reduced when compared to FF corner simulation with 27 °. The combination of sampling clock remains unchanged and the reduction in RVCO frequency, causes the frequencies in the DFFs to be larger, resulting in bit streams being produced more often. However, due to the reason that RVCO frequencies being slowed down, the frequencies of the RVCO and sampling clock do not perfectly match, leading to uncertain bit streams, which can be observed in the time interval between 0.4 s and 0.6 s. It shows that the output cannot reliably produce a certain bit stream when it momentarily drops to logic low and then quickly rises back to logic high. This uncertainty will eventually pose a significant challenge to the converter's performance.

Figure 52 illustrates the impact of the increase in temperature has on the circuit.

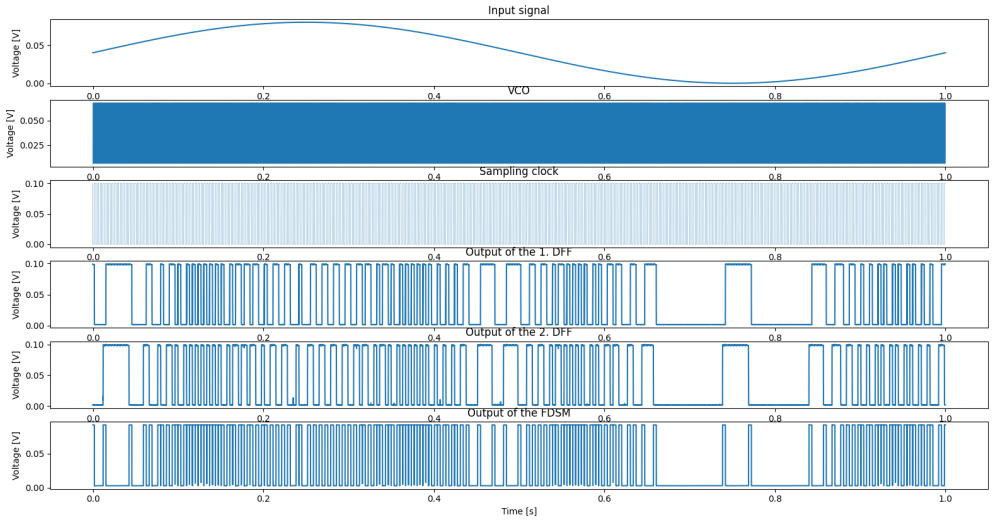


Figur 52: Typical typical corner simulation result with temperature 42 °

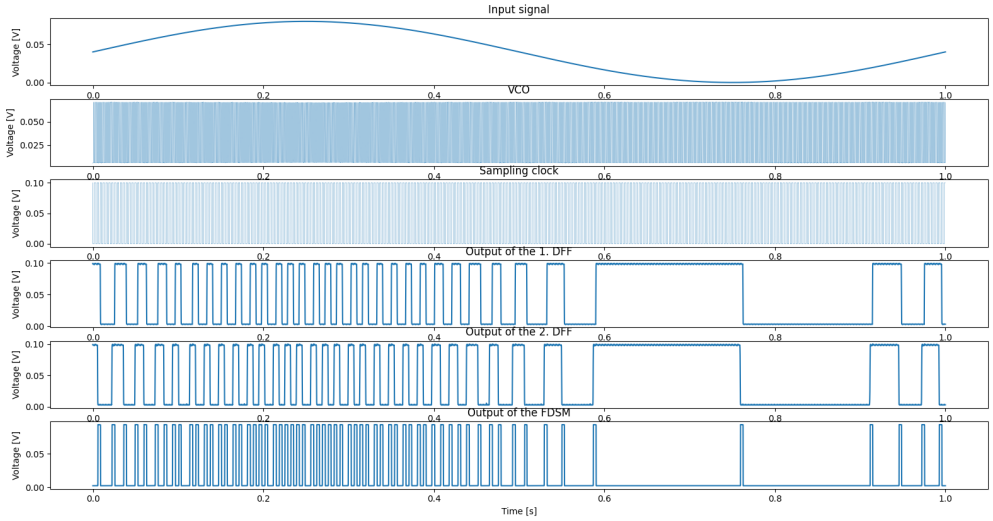
On the other side, with the increase in temperature, there's more current flowing through the transistors, causing the frequency of the RVCO to arise, resulting in an overall increase in system speed. Glitching is observed at the output due to the unmatched RVCO and clock frequency. Additionally, jittering is observed at the outputs of the both DFFs, especially for the second DFF, it indicates that the second DFF struggles to keep up with

the speed of the system. It also means that more noise is present at the system output in this case.

6.5.2 Process corner impact on circuit performance



Figur 53: Fast fast corner simulation result with temperature 27 °



Figur 54: Typical typical corner simulation result with temperature 27 °

Figures above show the impact of process corner has on the circuit. Both simulations were run with 27 °, while figure 53 was run with fast fast corner with both n and pmos

transistors exhibit higher carrier mobilities and figure 54 was run with typical typical with both n and pmos transistors exhibit normal carrier mobilities. As current delivering ability increases in both nmos and pmos in FF corner, causing the RVCO to oscillate more. While the sampling frequency stays the same, the increase in the RVCO frequency results in an increase in frequencies in both the first DFF and the second DFF. However, this increase in the frequencies of the DFFs causes the time interval where the DFFs have different logic values to be very little, causing the output bit streams to be very undefined.

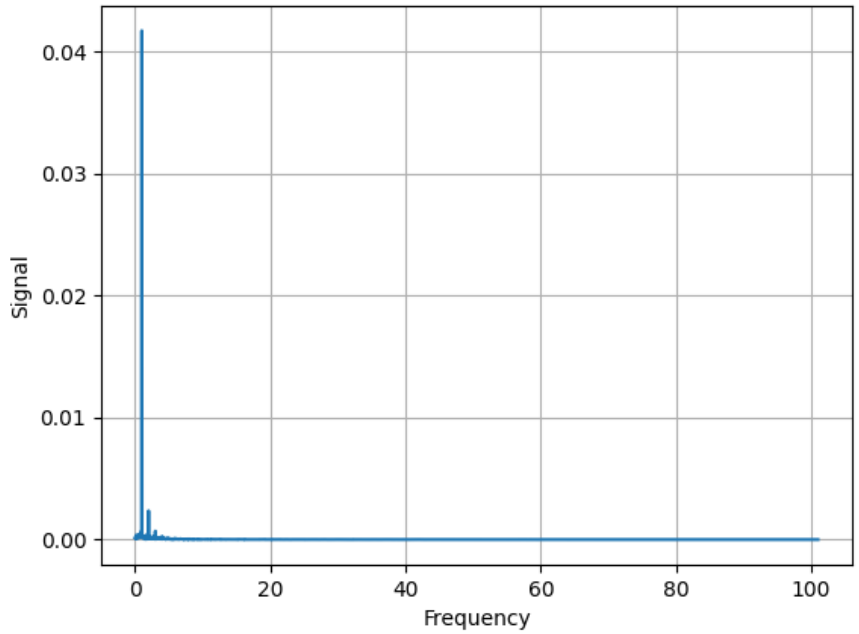
6.6 Signal processing techniques for SQNR improvement

This section proposes IIR filter and Blackman window at the FDSM output for the attempt to improve SQNR of the output as well as further exploring the potential of this ADC.

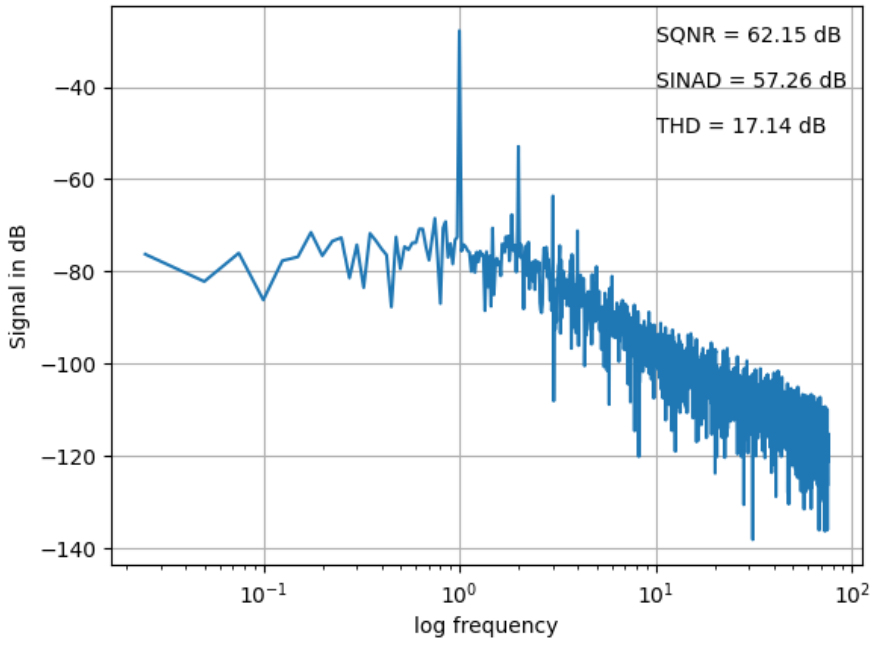
6.6.1 IIR filter

A second order Butterworth lowpass filter is applied at the output of the ADC. Butterworth filter was utilized mainly because its characteristics of flat frequency response in the pass-band. Cut-off frequency with 2 Hz was chosen since the input signal has frequency of 1 Hz. A second order filter was chosen since the noise and harmonic components are significantly lower than the signal itself, with an order of two should improve SQNR significantly in this case. And also with the consideration of the higher the order of the filter, the more cost it is for building the filter. Therefore, a second order with a more relaxed transition band is chosen here.

Upon observing the frequency spectrum, the application of the low-pass filter significantly diminishes noise. The presence of harmonic components is reduced, any remaining harmonic components exhibit smaller spikes compared to those present without the implementation of the low-pass filter.



Figur 55: FFT of the low-pass filtered signal



Figur 56: FFT of the low-pass filtered signal

SQNR and ENOB below are calculated with band of interest of 100 Hz:

$$SQNR_{dB} = -27.798132422498213 - (-88.94006160226152) \approx 61.14dB$$

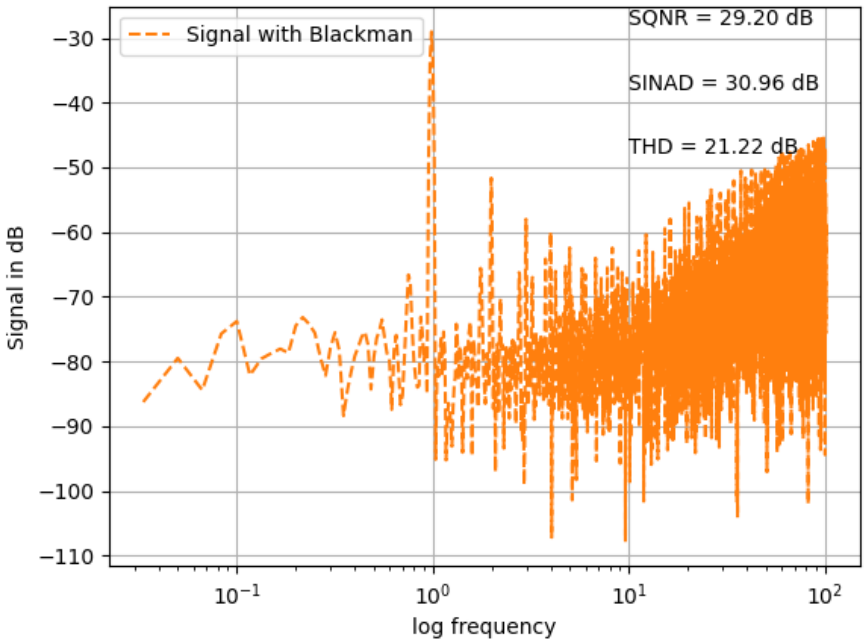
$$ENOB = \frac{61.14 - 1.76}{6.02} \approx 9.86bits$$

As it's presented above, the lowpass filter passes the signal at 1 Hz and attenuates the noise that are higher than the cut-off frequency, SQNR is improved 25.31 dB.

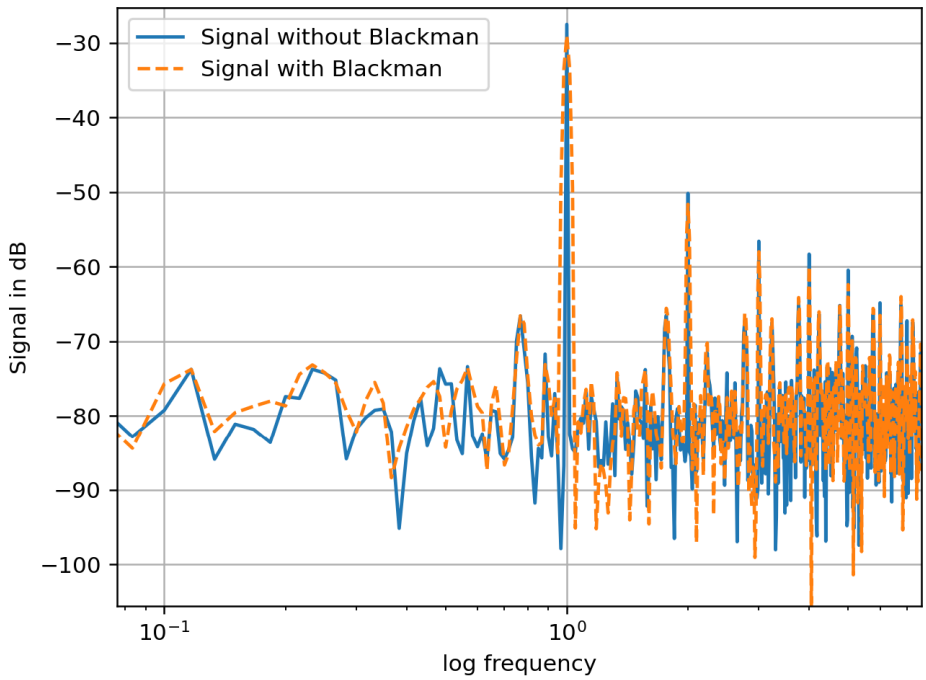
6.6.2 Blackman window

Blackman window was computed here because FFT of the original output shows clear harmonic components, and since it tends to smooth out the peaks of the frequency components. Blackman window has the highest side lobe level compared to other typical windows, which means that the side lobes are greatly reduced in amplitude. Therefore, the Blackman window was computed with the initial thought of smoothing the noise area of the frequency spectrum and further increase SQNR.

As it is observed in figure 58, as the window function smooths out the peaks in the noise floor, it also smooths out the fundamental frequency, further decreasing the SQNR. Therefore, window function was not chosen to improve SQNR in the system.



Figur 57: Output signal with Blackman window



Figur 58: Comparison between the original signal and signal with Blackman window

7 Discussion

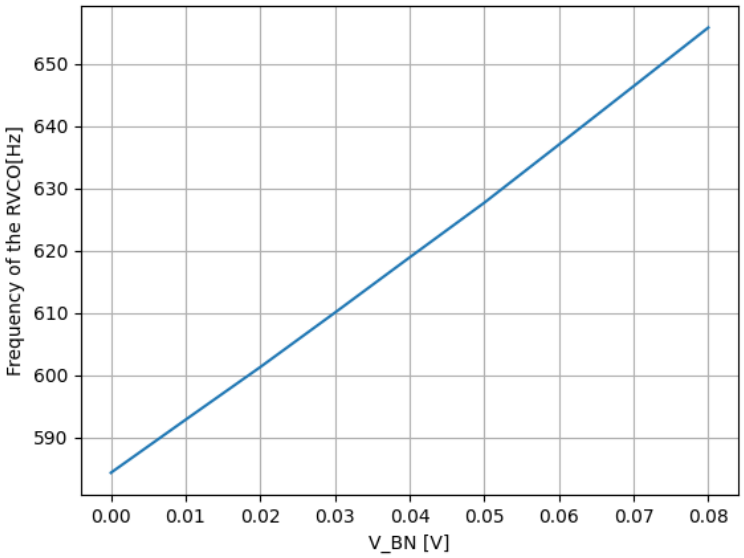
This section goes further into examining and explaining the results from the previous chapter. By critically examining the results and complications of the project, this section intends to dig deeper to gain more understanding, explore implications and further addressing complexities that have come up in the design process, and discuss the variables that have influenced the performance of the converter.

7.1 RVCO frequency tunabitiy

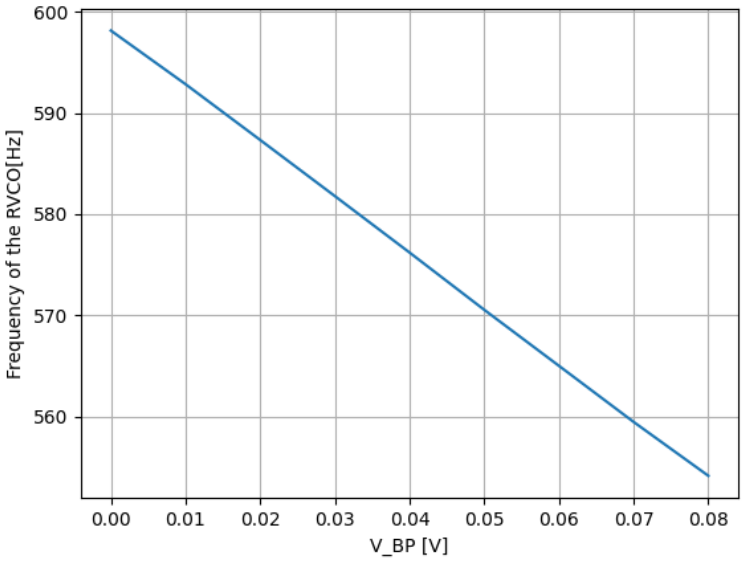
Even though the frequency modulation of the RVCO is done by applying a sine wave varying from 0 to 80 mV in this system, it's however interesting to investigate the parameters that can vary the frequency of the RVCO in this design.

Once the optimum dimensions are found for the inverters, there are four parameters left that can change the frequency of RVCO: the amounts of inverters in the ring (N), V_{BN}, V_{BP}, V_{BIAS}. Recall equation 3 and 4, the frequency of the RVCO has a significant influence on ENOB, where both maximum frequency deviation and the carrier frequency of the RVCO are involved. The higher the frequency, the better resolution; the wider the frequency range, the better the resolution. Therefore, an optimal frequency tuning is important to achieve a higher resolution on the ADC.

The relationship between current and frequency is observed from equation 6, where it indicates that the more the drain current flowing through the transistors, the higher the frequency. It is also observed that drain current has a relationship with V_{BS} (for nmos) and V_{SB} (for pmos), that is the higher the nmos bulk voltage, the higher the frequency; the higher the pmos bulk voltage the smaller the frequency, since in this case V_{SB} will be smaller and smaller. The same behavior is also observed by plotting frequency as a function of V_{BN} and V_{BP}, shown in figure 59 and 60



Figur 59: Frequency vs V_{BN} while V_{VBIAS} and V_{BP} stay constant



Figur 60: Frequency vs V_{BP} while V_{BIAS} and V_{BN} stay constant

While frequency tuning can be done by adjusting the bulk-terminals of the transistors, the bias transistor also has an impact on frequency of RVCO. Drain current of the transistor in sub-threshold region was discussed in 1, and frequency of the RVCO was discussed in equation 6 are now reproduced here for the convenience for the readers.

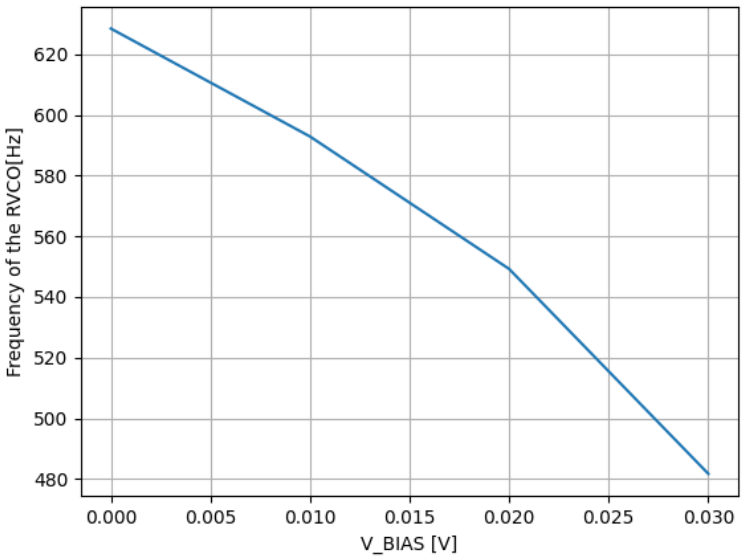
$$f = \eta \frac{I_D}{2NC_L V_{DD}}$$

$$I_{DN(P)} = I_{N(P)} \cdot e^{\frac{V_{GB(BG)}}{n_{N(P)}\phi_t}} \cdot (e^{-\frac{V_{SB(BS)}}{\phi_t}} - e^{-\frac{V_{DB(BD)}}{\phi_t}})$$

where

$$I_{N(P)} = \mu_{N(P)} \cdot n_{N(P)} \cdot C_{ox'} \cdot \phi_t^2 \cdot \frac{W}{L} \cdot e^{-\frac{|V_{TN(P)}|}{n_{N(P)}\phi_t}+1}$$

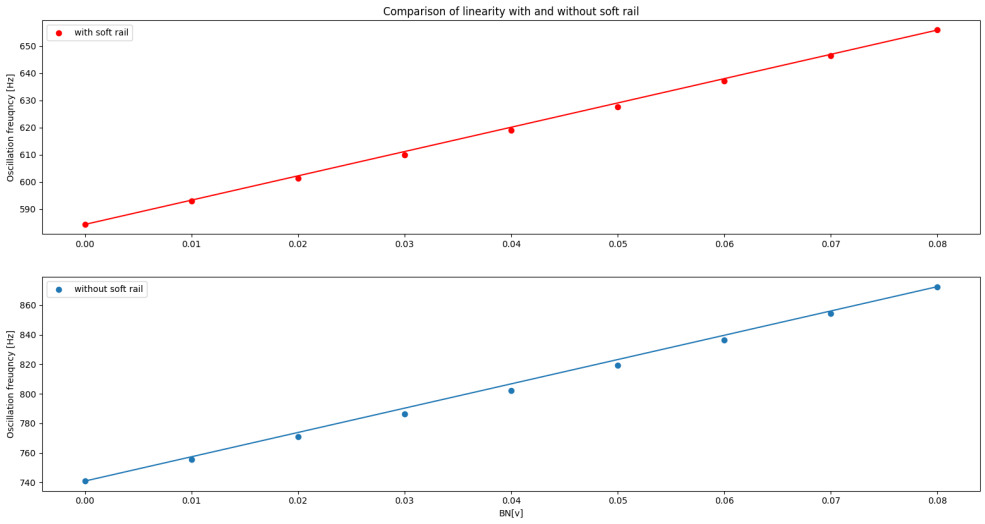
The equations above implies that both the dimensions of the bias transistor and the bias voltage has a linear relationship the frequency of the RVCO. When a smaller width is employed on the transistor, the drain current decreases, causing the frequency of the RVCO decreases and vice versa. When the bias voltage (V_{bias}, also the gate voltage of the bias transistor) decreases, causing V_{GB} to be bigger, further increasing the drain current resulting in an increase in the RVCO frequency. The relationship is also illustrated in figure 61.



Figur 61: Frequency vs V_{BIAS} while V_{BN} and V_{BP} stay constant

With this detail investigation of frequency modulation with bulk terminal voltages and V_{BIAS}, reasons behind the choices of V_{BIAS}, V_{BP} and V_{BN} become clear. V_{BIAS} and V_{BP} are set to 10 mV to get maximum frequency, input voltage is injected to nmos bulk terminal because it shows good linearity from figure 59.

7.2 Linearity of RVCO

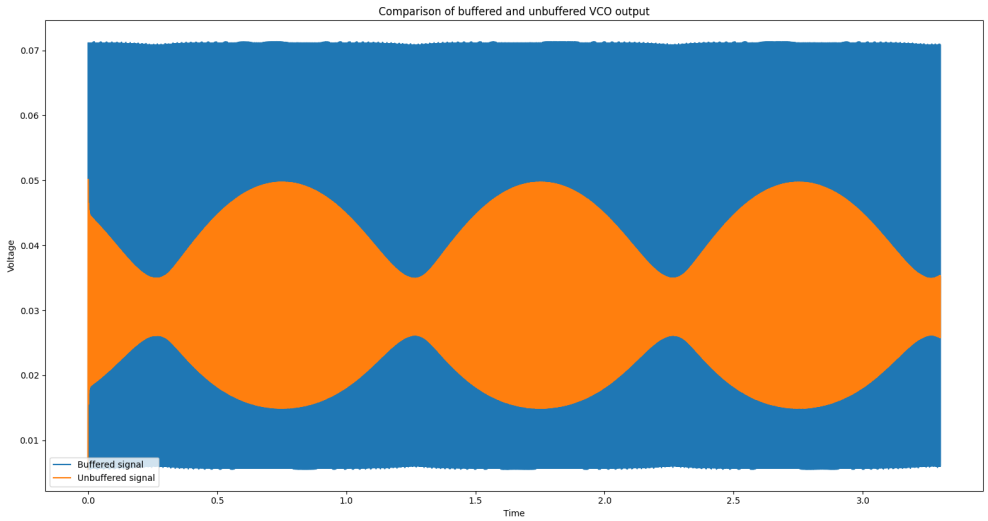


Figur 62: Comparison of linearity with and without soft rail solution

Since nonlinearity opposes harmonic components in the frequency spectrum of the output signal, and will further deteriorate SQNR, a soft-rail technique is used to improved the nonlinearity of the RVCO.

The impact of the soft-rail technique is illustrated in figure 62. The red dots represent the linearity with soft rail solution and blue dots represent the linearity without soft rail solution. A better linearity is observed as the red dots are closer to the straight line.

7.3 RVCO output buffering



Figur 63: Comparison of unbuffered and buffered VCO output

The output signal of the RVCO is not ideal pulses, rather, it has rather rounded edges as the orange line in figure 63. This is due to the time it takes for output to rise and fall. The time it takes for the inverter to rise and fall has something to do with its current driving capability and this again affect the time needed to charge and discharge the various capacitance in the circuit. The relationship among the parameters can be expressed as:

$$I\Delta t = \Delta = C\Delta V \tag{13}$$

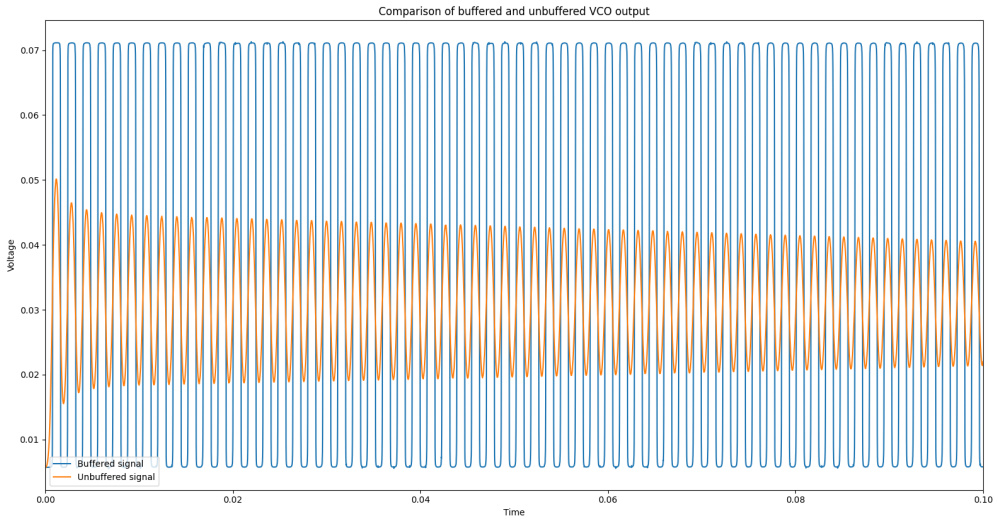
It states that current I passes through a capacitance C for a duration of Δt, results in the accumulation of a charge of ΔQ on the capacitor. This accumulation of charges causes the voltage across the capacitor to increase by ΔV.

The RVCO is extra sensitive to the parasitic capacitance due to the reason that it's operating in the sub-threshold region. The orange line in figure 63 is a good example of this challenge, the signal struggles to have a full output swing as it can not swing from VDD to ground and vice versa because there's too much capacitance that the inverter in the chain can drive.

There are two common ways to settle the problem. The first one is to increase the widths

of the transistors in the RVCO chain so that the inverter chain can drive the node better. On the other side, the result of the increased width increases the parasitic capacitance and causes the frequency range to change. This solution will be difficult to balance when the current ratio method is used for scaling the transistor, where the width and length are strictly determined and related to each other in order to achieve the optimal gain.

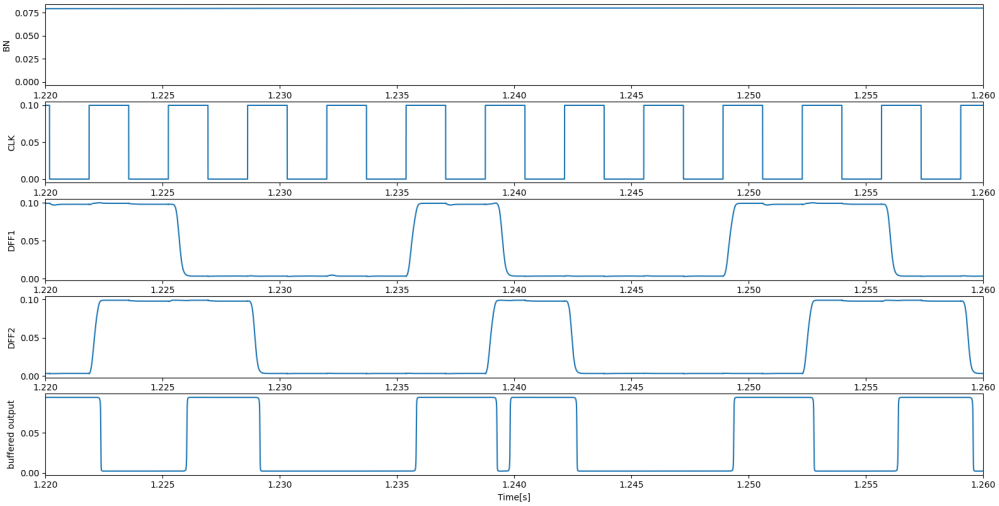
The second solution to the problem is to put a buffer after the inverter chain. The buffer consists of two inverters where the second inverter is x times bigger than the first inverter, therefore charging up and out the capacitance without using acceptably large time and resulting driving signal to VDD/ground. This solution is more desirable due to the reason that the problem can be settle without causing an overall system change.



Figur 64: Comparison of unbuffered and buffered VCO output with simulation time 0.1s

Two inverter with the second one is 1.5 times bigger than the first one is placed behind the inverter chain. Observe figure 63 and 64, where the orange line represents the signal before buffer and the blue line represents the signal after the buffer. The desired signal presents after the buffer where it swings to VDD/ground with a squared form.

7.4 FDSM output

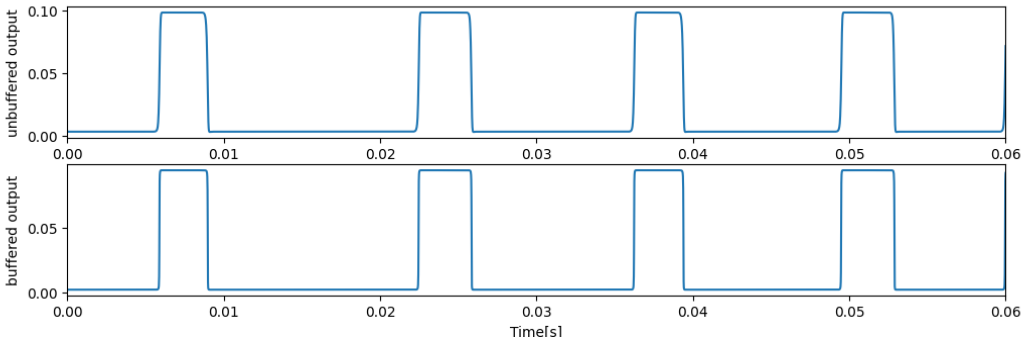


Figur 65: Output of the FDSM (zoomed in)

Unfortunately, glitching is observed at the FDSM output as undefined bit streams are observed when the input signal reaches 80 mV. Figure 65 zooms inn to the time interval where the undefined bit stream happens. Between 1.235s to 1.245 in figure 65, output of the system drops quickly down to logic low level from a logic high level then rise back up to logic high just as quick. This is due to the DFFs goes quickly high right after each other, XOR gate produces logic high when the logic levels of the DFFs are different, otherwise producing a logic low. When DFFs rise up quickly after each other, leaving behind a small time window where they are at the same logic level, making XOR gate to drop quickly down to logic low in the small time window, then rise up again when the DFFs have different logic levels.

During the sampling of the RVCO output, the first DFF generates a logic high output when the clock samples a high value from the RVCO output. However, over time, the phase of the RVCO output experiences a shift. This phase shift results in a scenario where, during clock sampling of the RVCO, the duration in which the clock samples a logic high from the RVCO output becomes shorter. As a consequence, the pulse width of the output from the first DFF becomes narrower, subsequently leading to the second DFF to go high shortly after.

The extreme small time window where the first DFF and the second DFF has different logic level introduce undefined bit stream at the XOR gate output. What is really desired here, is that the phase shift in the RVCO is such that it maintains the pulses from the DFFs wide enough for the XOR gate to produce a well-defined bit stream. With further investigation of the connection between RVCO output and the sampling clock within this system, it becomes evident that the clock must at least sample three logic high values in a row from the RVCO. This specific condition ensures that the pulses of the DFFs to be wide enough for XOR to produce a bit stream output.



Figur 66: Output of the FDSM (zoomed in)

To reduce noise at the output and also reduce the rise and fall time of the output, two inverters are placed behind the output to make the output more square like. From figure 66, it is observed that the output is more square like after the two inverters, which also means the the propagation delay is smaller in this case.

7.5 Sampling frequency criteria

To further analyze how the relationship between the sampling frequency and RVCO frequency impacts the system. Low-pass filters are computed on the different outcomes of FDSM, sampling frequency criteria based on [6] is also analyzed and discussed.

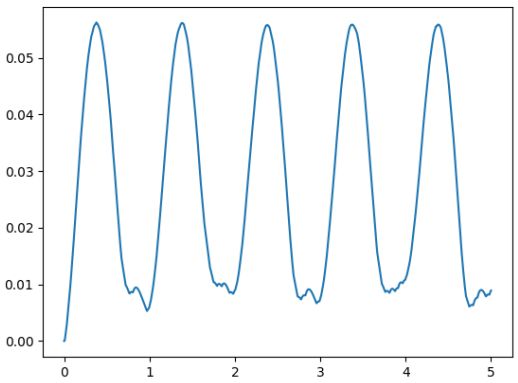
As mentioned above, a criteria for the sampling frequency (f_{clk}) was developed in [6]: To avoid signal distortion, the relationship below must be satisfied:

$$f_{clk} \approx 4 \cdot \Delta f \tag{14}$$

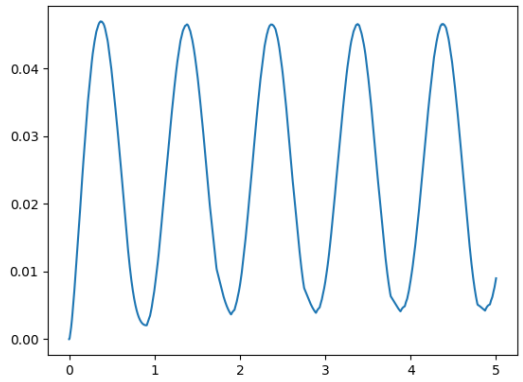
When put in the frequency deviation, the value of clock frequency becomes:

$$f_{clk} = 4 \cdot 71.5Hz = 286Hz$$

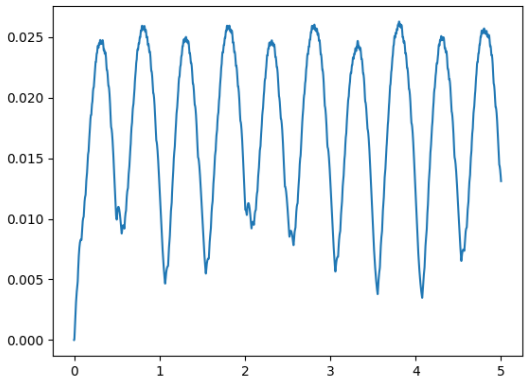
Literature [6] also states that this is the theoretical limit, in the practical manner, it should also make room for phase noise. In this design, through experiments results, the practical value turns out to be 295.9 Hz, which is also the sampling frequency used in this system. In [6], a minimum sampling frequency criteria is developed, which states that $4 \cdot \Delta f$ is the minimum sampling frequency in the undersampling FDSM system. However, through observation of experiment results, $4 \cdot \Delta f$ is surprisingly the maximum sampling frequency allowed in this design. Figures 67 to 69 display the low-pass filtered FDSM output signals. In figure 67 where the sampling frequency is set at 200 Hz (lower than the 295.9 Hz limit), a sine wave with 5 periods and no distortion is observed, which closely resembling the input signal. Moving on to figure 68 which represents the maximum allowable sampling frequency of 295.9 Hz, it also presents a sine wave with 5 periods and no distortion. Lastly, figure 69 depicts a scenario with a sampling frequency of 312.5 Hz, exceeding the system's maximum allowable sampling frequency. The distorted signal no longer resembles the input signal here.



Figur 67: Low-pass filtered output signal without distortion (5ms)



Figur 68: Low-pass filtered output signal without distortion (3.38ms)



Figur 69: Low-pass filtered signal with distortion (3.2ms)

To investigate more about why $4 \cdot \Delta f$ is the maximum sampling frequency in this system, let's come back to literature [6], where the sampling frequency is shown with a given m $\in$ N:

$$f_{clk} \in < \frac{2(f_c + \Delta f)}{m+1}, \frac{2(f_c - \Delta f)}{m} > \tag{15}$$

To give a further insight of what m or m+1 is, for low input signal deviations, the number of counted edges during $\frac{1}{f_{clk}}$ will be limited to two adjacent integers m and m+1.

Equation 15 shows the upper and lower limit of the sampling frequency, however, [6] also states that the upper and lower limit of the sampling frequency range will flip for a certain m. Let's consider the case where the upper and lower limit of the sampling range is flipped

in equation 15. Equation 15 can be rewritten as:

$$f_{clk} \in < \frac{2(f_c - \Delta f)}{m}, \frac{2(f_c + \Delta f)}{m+1} > \tag{16}$$

For equation 16 to be true, the following statement must be satisfied:

$$\frac{2(f_c - \Delta f)}{m} < \frac{2(f_c + \Delta f)}{m+1} \tag{17}$$

With length algebra (shown in Appendix figure 81), equation 17 results in:

$$m > \frac{f_c - \Delta f}{2\Delta f} \tag{18}$$

Integer m has therefore a minimum value equals $\frac{f_c - \Delta f}{2\Delta f}$.

To further investigate if $4 \cdot \Delta f$ is the maximum sampling frequency allowed, the minimum value of m is set into the upper limit of equation 16:

$$f_{clk} = \frac{2(f_c - \Delta f)}{m_{min}}$$

With rough assumption: $f_c >> \Delta f$, there is a theoretical maximum limit of the sampling frequency:

$$f_{clkmax} = 4 \cdot \Delta f \tag{19}$$

To check if equations 19 and 16 are true in the practical manner, values of f_c and Δf are set into $\frac{2(f_c - \Delta f)}{m}$ and $\frac{2(f_c + \Delta f)}{m+1}$:

$$m = \frac{6210.05Hz + 71.5Hz}{2 \cdot 71.5Hz} = 4.84$$

$$\frac{2(f_c - \Delta f)}{m} = \frac{2 \cdot (620.05Hz - 71.5Hz)}{4.84} = 226.67$$

$$\frac{2(f_c + \Delta f)}{m+1} = \frac{2 \cdot (620.05Hz + 71.5Hz)}{4.84 + 1} = 236.83$$

As the results above show that $226.69 < 236.83 = \frac{2(f_c - \Delta f)}{m} < \frac{2(f_c + \Delta f)}{m+1}$. Equations 16 and 19 are in fact true in this system.

8 Future Work

Simulation results from schematic is not the final answer even though is necessary and a good indication. In the context of future work, an important continuation of this project would be to create layout of the circuit. As parasitics and non-ideal effects will appear after layout, therefore, it is important to consider how to draw layout for critical/sensitive parts of the circuit to get robust and predictable performance. Once layout is created, the next step is to fabricate a chip and perform measurements on the chip to validate the results shown in this thesis.

The thesis began some algebra work but couldn't complete it due to time constraints, therefore, the sections below discuss the specific plan for the beginning steps of some of the future work can be as well as an outline of the algebra work.

8.1 Corner simulations

An important task for the future is revisiting the design to optimize the functionality of SF, FS, and SS corners. Passing these corner simulations is crucial for circuit's proper operation against process variations.

One of many thing that can be done for making the corners work is to resize the dimensions of the transistors. For SF, FS and SS corners, the simulation already fails at RVCO not being able to oscillate. RVCO oscillation relies on the inverter outputs being pulled up to VDD or down to ground, but in this scenario, it's obvious that this operation is not taking place due to excessive capacitance coming from the change of process corner. To make RVCO more robust against process variations, and to produce square wave output of itself without the inverter buffers, more research can be done to ensure that the body biasing doesn't deteriorate the voltage gain of the inverter as much as it is in this project.

8.2 Optimum current ratios for subthreshold region in 65nm process

Since no formula has been derived for optimizing the voltage gain of logic gates in the subthreshold region in the 65 nm process, therefore the transistor dimensions used in this design are the optimal results of many tryouts. This method doesn't have a theoretical calculation as a foundation and relies on sweeping of the transistor dimensions which consumed a lot of time. It would be convenient to have a mathematical and scientific based method for finding the most fitted transistor dimensions for any system operating in subthreshold region for 65 nm process. In [12], optimum current ratios $\frac{I2}{I0}$ and $\frac{I1}{I0}$ were found by producing the best voltage gains of the Schmitt trigger inverter. However, the work was done in a different process node therefore doesn't apply to this system. Therefore, an algebra work was partially done for this project for finding the optimum current ratios further for the best voltage gain. This remains a future work due to the reason that it lacks enough data to support the theory.

Refer again to 1 here, in this algebra we consider p and nmos has same current strength: $I_N = I_P; I_{DN} = I_{DP} = I_D$ We can first modify equation 1 this way:

$$I_D = I_N \cdot e^{\frac{V_{GB}}{n_N \cdot \phi_t}} (e^{\frac{-(V_S - V_B)}{\phi_t}} - e^{-\frac{-V_{DB}}{\phi_t}}) \tag{20}$$

According to [16]:

$$g_{ms} = -\frac{\partial I_D}{\partial V_S}; g_{md} = -\frac{\partial I_D}{\partial V_D}; g_m = -\frac{g_{ms} - g_{md}}{n}$$

To find g_{ms} we can consider I_N as a constant A, $e^{\frac{V_{GB}}{n_N \cdot \phi_t}}$ as a constant B, therefore equation 20 can be written as:

$$I_D = A \cdot B \cdot (e^{\frac{-V_S + V_B}{\phi_t}} - e^{\frac{-V_{DB}}{\phi_t}})$$

$$I_D = ABe^{\frac{V_B}{\phi_t}} \cdot e^{-\frac{V_S}{\phi_t}} - AB \cdot e^{-\frac{V_{DB}}{\phi_t}}$$

we consider $e^{\frac{V_B}{\phi_t}}$ as a constant C, $e^{-\frac{V_{DB}}{\phi_t}}$

$$I_D = ABC \cdot e^{\frac{-V_S}{\phi_t}} - ABD$$

Derive I_D with respect to V_S:

$$\frac{\partial I_D}{\partial V_S} = g_{ms} = ABC \cdot (-V_S \cdot e^{\frac{-V_S}{\phi_t}})$$

Set in constants A, B og C

$$g_{ms} = -I_N \cdot e^{\frac{V_{GB}}{n_N \phi_t}} e^{\frac{V_B}{\Phi_t}} V_S \cdot e^{-\frac{V_S}{\phi_t}}$$

for the convenience of the calculation, we write all other variables that are not I_N as A'. Therefore the equation above becomes:

$$g_{ms} = -I_N \cdot A'$$

Find g_{md}: Note that equation 20 in this case, since I_D is derived with respect to V_D, then equation 20 can be further modified with constants A, B and C as:

$$I_D = A \cdot B(C - e^{\frac{-(V_D - V_B)}{\phi_t}})$$

$$I_D = ABC - ABe^{\frac{-V_D + V_B}{\phi_t}}$$

$$I_D = ABC - ABe^{-\frac{V_D}{\phi_t}} e^{\frac{V_B}{\phi_t}}$$

$$\frac{\partial I_D}{\partial V_D} = ABV_D \cdot e^{-\frac{V_D}{\phi_t}} e^{\frac{V_B}{\phi_t}}$$

$$\frac{\partial I_D}{\partial V_D} = g_{md} = I_N \cdot e^{\frac{V_{GS}}{n_N \phi_t}} \cdot V_D \cdot e^{\frac{-V_D}{\phi_t}} \cdot e^{\frac{V_B}{\phi_t}}$$

Again, all variables that are not with current strength are noted as B':

$$g_{md} = I_N \cdot B'$$

Finding g_m, according to [16], g_m is written as:

$$g_m = \frac{g_{ms} - g_{md}}{n}$$

Since g_{ms} and g_{md} are found above, the equation can be further calculated as:

$$g_m = \frac{g_{ms} - g_{md}}{n} = \frac{I_N(-e^{\frac{V_{GB}}{n_N\phi_t}} \cdot V_S \cdot e^{\frac{V_{BS}}{\phi_t}} - e^{\frac{V_{GS}}{n_N\phi_t}} \cdot V_D \cdot e^{-\frac{V_{DB}}{\phi_t}})}{n_N}$$

Again, all variables that are not relevant to current strength in the equation above are written as C', equation above becomes:

$$g_m = I_N \cdot C'$$

Equation for voltage gain of ST based inverter is found in [12]:

$$\frac{V_O}{V_I} = \frac{-g_{m1}}{g_{md2}} \cdot \frac{1 + \frac{g_{ms1}g_{m0}}{g_{m1}(g_{ms2}+g_{md0})}}{1 - \frac{g_{ms1}g_{m2}}{g_{md1}(g_{ms2}+g_{md0})}}$$

Replace g_{ms}, g_{md} and g_m with what we've found above

$$\frac{V_O}{V_I} = \frac{-I_1 \cdot C'}{I_2 \cdot B'} \cdot \frac{1 + (\frac{-I_1A'I_0C'}{I_1C'C' - I_2A' + I_0B'})}{1 - (\frac{-I_1A'I_2C'}{I_1B'(-I_2A' + I_0B')})}$$

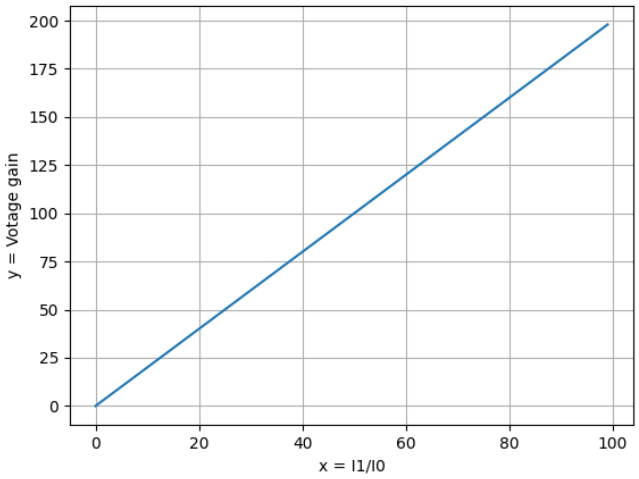
$$\frac{V_O}{V_I} = -\frac{C'I_1(-I_2A' + I_0B' - I_0A')}{I_2(-I_2A'B' + I_0B'^2 - I_2A'C')}$$

Multiple right side of the equation with $\frac{1}{I_0}$ on both the numerator and denominator. The equation can be further modified as:

$$\frac{V_O}{V_I} = \frac{\frac{I_1}{I_0}(I_2A'C' - I_0B'C' + I_0A'C')}{\frac{I_2}{I_0}(-I_2A'B' + I_0B'^2 - I_2A'C')} \tag{21}$$

8.2.1 Optimum transistor ratio for I1/I0

When it comes to finding the optimum ratio for $\frac{I_1}{I_0}$ to achieve the biggest voltage gain, equation 21 can be considered as a linear function y = kx where y is a function of x. k = variables that are not associated with $\frac{I_1}{I_0}$; x = $\frac{I_1}{I_0}$.



Figur 70: linear function of x and y, this figure only demonstrates the relationship between x and y values, it doesn't represent the actual voltage gain and transistor ratio

Figure 70 shows that $y \to \infty$ when x $\to \infty$. The optimum y value will be found as x grows bigger, which means that voltage gain value grows bigger as the transistor ratio $\frac{I_1}{I_0}$ grows bigger.

Recall table 29, on the right side of the table presents the results of when $\frac{I_2}{I_0}$ stays constant and $\frac{I_1}{I_0}$ acts like a variable. When $\frac{I_1}{I_0} = [0.06, 0.4]$, the behavior of voltage gain and $\frac{I_1}{I_0}$ does act like a linear relationship, however, voltage gain starts to deteriorate when $\frac{I_1}{I_0}$ gets bigger than 0.8. This observation does not match with the equation that's been derived over. There are a couple reasons that could cause this:

1) Equation 21 with small voltage gain as a function of $\frac{I_1}{I_0}$ could be a discontinuous function, then constants A', B', C' should be investigated more to check if there's any possible cause for discontinuity to happen.

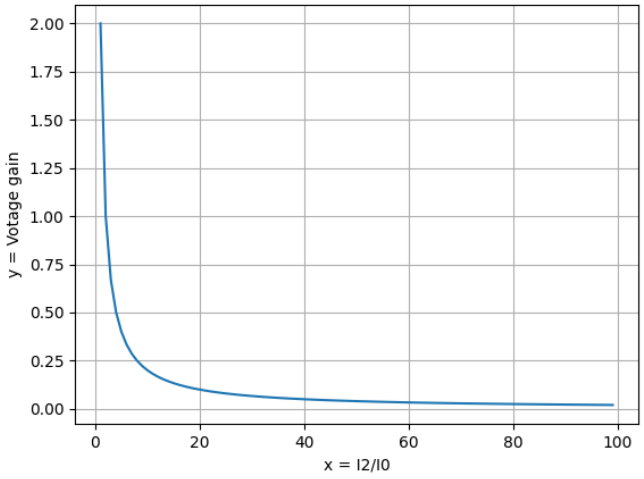
2) Calculation error - calculation could be fatal somewhere in the algebra.

3) Simulation setup - How the simulation is set up influences the precision of the result, there could too little step size between each sampled data, causing the results to be imprecise.

Unfortunately, there was enough time left to investigate any of the assumption. More experiments can be done if more time is allowed.

8.2.2 Optimum transistor ratio for I2/I0

When it comes to finding the optimum ratio for $\frac{I_2}{I_0}$ to achieve the biggest voltage gain, equation 21 can be considered as a linear function $y = k \cdot \frac{1}{x}$ where y is a inverse function of x. k = variables that are not associated with $\frac{I_2}{I_0}$; $\frac{1}{x} = \frac{I_2}{I_0}$.



Figur 71: Inverse function of x and y, this figure only demonstrates the relationship between x and y values, it doesn't represent the actual voltage gain and transistor ratio

y reaches maximum value as $x \to \infty$. This relationship means that the voltage gain gets bigger as the transistor ratio $\frac{I_2}{I_0}$ gets smaller.

Recall the left side of table 28, where $\frac{I_1}{I_0}$ stays constant and $\frac{I_2}{I_0}$ varies from 0.4 to 1. The result pattern does behave as an inverse function, where the voltage gain deteriorates with bigger $\frac{I_2}{I_0}$. However, the experiment data is too little to support that this equation is the theory to a optimum ratio of $\frac{I_2}{I_0}$.

9 Conclusion

This master project started with the initial thought of exploring analog/digital building blocks in subthreshold region to optimize their power efficiency. As the concept evolved, the project transitioned towards the development of an ADC tailored for self-powered IoT devices and biomedical applications.

Achieved through simulations, this thesis demonstrates the successful implementation of a frequency delta-sigma modulator with signal bandwidth of 1 Hz, capable of operating on a supply voltages on 80 and 100 mV using 65 nm CMOS process. The FDSM has an power consumption of 16.264 pW. It achieved an SQNR of 35.83 dB and a FoM of 1.09 fJ/conversion for a band of interest of 100 Hz. When the band of interest was reduced to 10 Hz, it delivered an SQNR of 47.78 dB and a FoM of 0.276 fJ/conversion. Notice that the numbers given above are the simulation results, more work such as fabrication and measurement of the chip should be done to validate the simulation results and eventually present the system performance in the real world.

Oversampling of the input signal was utilized to reduce the quantization noise in band, undersampling of RVCO was also utilized due to the supply voltage limitation opposed on the system speed. All transistors operated in the subthreshold region not only to accommodate the ultra-low power supplies but also to minimize the data converter's energy consumption. Schmitt trigger based logic gates were employed to reduce the leakage current which is a major limitation of the subthreshold operation.

In the time domain, the results show a process where the input signal is initially sampled and quantized, followed by differentiation of the quantization error from the signal at a later stage. In the frequency domain, it shows shows the input signal at 1 Hz following its harmonic components as well as noise shaping with a slop of -20dB/decade which comes from the oversampling method. Two signal processing techniques were explored in an effort to enhance SQNR. The challenges encountered during the project's design and the complexity of the results are thoroughly examined. While not all aspects of the project yielded successful outcomes, the difficulties were analyzed and discussed, which helps guide future research.

This project shows that the limit of the energy consumption of data converters can be pushed even further, offering the exciting prospect that with continued efforts, data converters could operate at such low energy levels in a practical manner.

10 Appendix

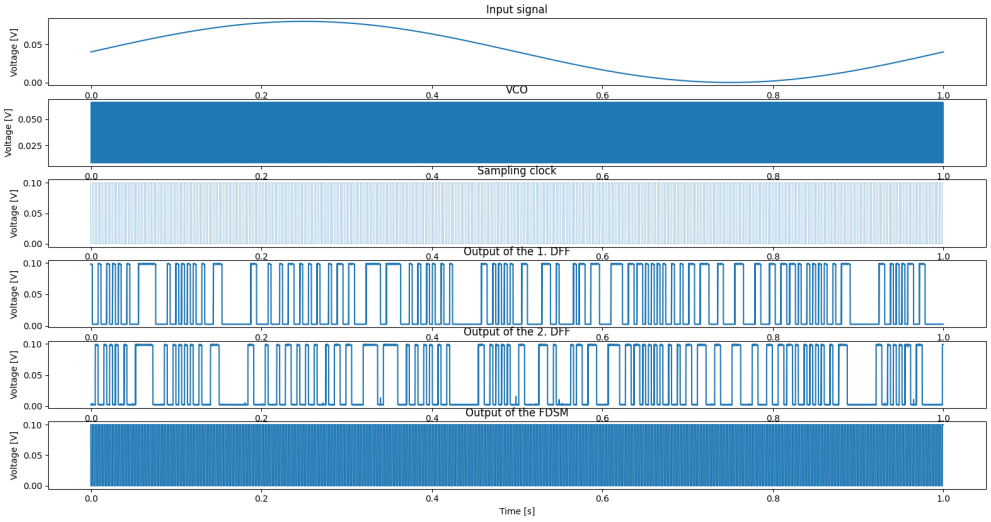
```
import numpy as np
import matplotlib.pyplot as plt
import csv

BN_biased = []
f_biased = []
BN_unbiased = []
f_unbiased = []

with open('VCO_biased.csv', 'r') as csvfile_1:
    heading = next(csvfile_1)
    VCO_biased_csv = csv.reader(csvfile_1, delimiter = ',')

    for row in VCO_biased_csv:
        f_biased.append(float(row[1]))
        BN_biased.append(float(row[0]))

with open('VCO_no_biased.csv', 'r') as csvfile_2:
    heading = next(csvfile_2)
    VCO_no_biased_csv = csv.reader(csvfile_2, delimiter = ',')

    for row in VCO_no_biased_csv:
        f_unbiased.append(float(row[1]))
        BN_unbiased.append(float(row[0]))

line_1x = [BN_biased[0], BN_biased[-1]]
line_1y = [f_biased[0], f_biased[-1]]
line_2x = [BN_unbiased[0], BN_unbiased[-1]]
line_2y = [f_unbiased[0], f_unbiased[-1]]

plt.subplot(2,1,1)
plt.plot(line_1x, line_1y, color = 'r')
plt.title('Comparison of linearity with and without soft rail')
plt.ylabel('Oscillation freuqncy [Hz]')
plt.scatter(BN_biased, f_biased, label ='with soft rail', color = 'r')
plt.legend(loc="upper left")

plt.subplot(2,1,2)
plt.plot(line_2x, line_2y)
plt.ylabel('Oscillation freuqncy [Hz]')
plt.xlabel('BN[v]')
plt.scatter(BN_unbiased, f_unbiased, label ='without soft rail')
plt.legend(loc="upper left")
plt.show()



import numpy as np
import matplotlib.pyplot as plt
import csv
from shapely.geometry import LineString

time = []
VA =[]
VI = []
```

```
VOUT = []

with open('NAND_SP.csv', 'r') as csvfile:
    heading = next(csvfile)
    NAND_SP = csv.reader(csvfile, delimiter = ',')

    for row in NAND_SP:
        time.append(float(row[0]))
        VA.append(float(row[1]))
        VI.append(float(row[3]))
        VOUT.append(float(row[5]))


x = np.array(time)
f = np.array(VOUT)
g = np.array(VI)

print(f[0])
print(f[-1])
print(x[0])
print(x[-1])

first_line = LineString(np.column_stack((x, f)))
second_line = LineString(np.column_stack((x, g)))
intersection = first_line.intersection(second_line)

if intersection.geom_type == 'MultiPoint':
    plt.plot(*LineString(intersection).xy, 'o')
elif intersection.geom_type == 'Point':
    plt.plot(*intersection.xy, 'o')

x, y = intersection.xy
print(x, y)

marker_x1 = [0]
marker_y1 = [0.09830]
marker_x2 = [0.1]
marker_y2 = [0.00297]

plt.plot(marker_x1, marker_y1, marker='o')
plt.plot(marker_x2, marker_y2, marker='o')
plt.text(0, 0.09830, '98.30mV')
plt.text(0.1, 0.00297, '2.97mV')

plt.plot(time, VA, label = 'VA')
plt.plot(time, VI, label = 'VI')
plt.plot(time, VOUT, label = 'VOUT')
plt.legend(loc="lower left")
plt.text(0.045, 0.043, '43.63mV')
plt.xlabel('Time [s]')
plt.ylabel('Voltage [V]')
plt.title('VTC of the NAND gate')
plt.show()

Codes for low-pass filtered FFT and SQNR:

import numpy as np
import matplotlib.pyplot as plt
```

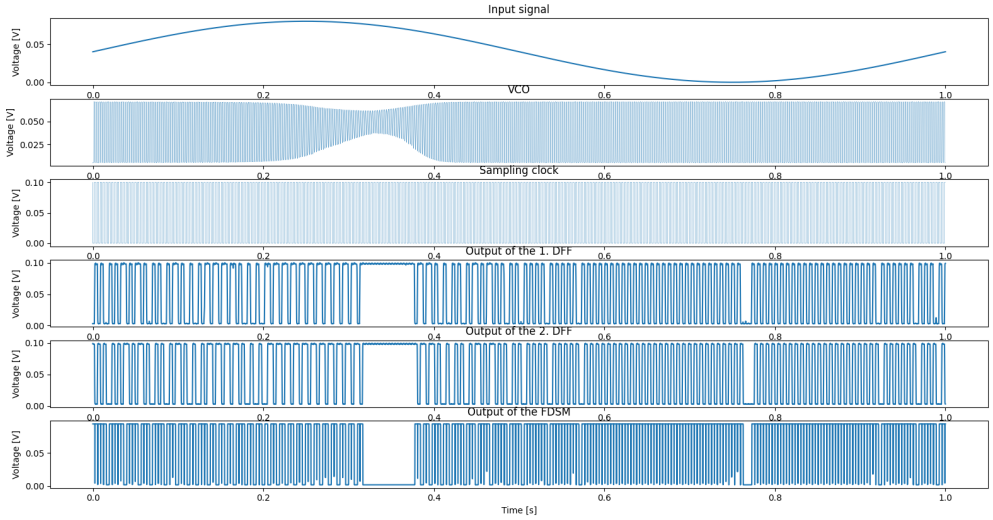
```
from scipy.fftpack import fft, fftfreq
import csv
from scipy import signal
from scipy.signal import blackman
from scipy.signal import butter, lfilter
from array import *

Time = []
Voltage = []


with open('FDSM_out_40s_3.38ms.csv', 'r') as csvfile:
    heading = next(csvfile)
    FDSM_out_dff_unbuffered = csv.reader(csvfile, delimiter = ',')

    for row in FDSM_out_dff_unbuffered:
        #klippe bort dataen f r systemet starter
        if row[0] >= '0.0001':
            Time.append(float(row[0]))
            Voltage.append(float(row[1]))

y = np.array(Voltage)
x = np.array(Time)
#print(y.shape)

timestep = x[1] - x[0]
#print(timestep)

N = int(y.shape[0])
T = timestep

xf = fftfreq(N, T)[:N//2]
#Remove DC component
xf = xf[1:]
#Limit to band of interest
xf = xf[0:3030]

yf = fft(y)
#only positive frequency
FFT_yf = yf[0:N//2]
FFT_yf = FFT_yf[1:]
FFT_yf = FFT_yf[0:3030]
#scaling of y axies of the FFT
FFT_yf1 = (2/N * np.abs(FFT_yf))*2

#sos = signal.butter(2, 4, 'lp', fs=1/T, output='sos')
sos = signal.butter(2, 2, 'lp', fs=1/T, output='sos')
filtered = signal.sosfilt(sos, y)
plt.plot(Time, filtered)
plt.show()


filtered_yf = fft(filtered)
FFT_filtered = filtered_yf[0:N//2]
FFT_filtered = filtered_yf[1:3031]
FFT_filtered_1 = (2/N * np.abs(FFT_filtered))*2


```

```
173
174
175 #calculate power of the signal
176 def power_of_signal(x):
177     N = x.shape[0]
178     return np.sum(np.power(x, 2)) / N
179
180
181
182 #Distinguish input signal with the rest
183 f_signal = []
184 signal_signal = []
185 f_noise = []
186 signal_noise = []
187 for x, y in zip(xf, FFT_filtered_1):
188     if y >= 0.005:
189         f_signal.append(x)
190         signal_signal.append(y)
191     else:
192         f_noise.append(x)
193         signal_noise.append(y)
194
195 s_signal_signal = np.array(signal_signal)
196
197 print('the length of the x coordinates of the freq is', len(f_noise))
198 print('the length of the y coordinates of the freq is', len(signal_noise
    ))
199 print(f_signal, signal_signal)
200
201
202 #calculation of SQNR with all hamonics
203 FFT_filtered_list = FFT_filtered_1.tolist()
204 all_harmonics_y = []
205 all_harmonics_x = []
206
207 #find harmonics
208 for n in range(101):
209     for x,y in zip(xf, FFT_filtered_1):
210         if x == n*f_signal[0]:
211             all_harmonics_y.append(y)
212             all_harmonics_x.append(x)
213
214 print('harmonics are', all_harmonics_y)
215
216 #remove fundamental signal and harmonic signals from the sample
217 noise = []
218 for i in FFT_filtered_list:
219     noise.append(i)
220
221 for k in all_harmonics_y:
222     noise.remove(k)
223
224 print('length of the noise is',len(noise))
225 a_noise = np.array(noise)
226
227 SQNR_allharmonics =10*np.log10(power_of_signal(s_signal_signal) /
    power_of_signal(a_noise))
228 print(10*np.log10(power_of_signal(s_signal_signal)), 10*np.log10(
```

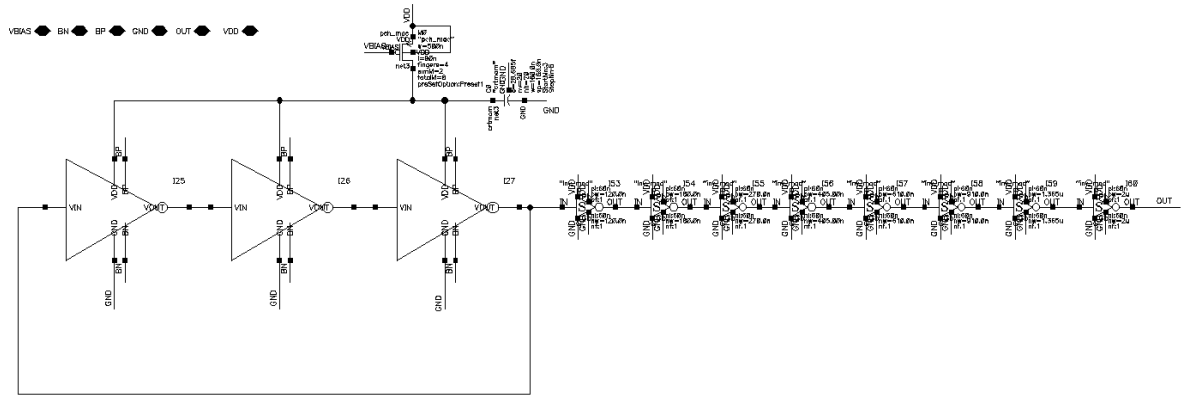
```
    power_of_signal(a_noise)))
print('SQNR is', SQNR_allharmonics,'dB')
print('Amplitude of the signal is', s_signal_signal)


plt.plot(xf, FFT_filtered_1)
plt.xlabel('Frequency')
plt.ylabel('Signal')
plt.grid()
plt.show()

plt.semilogx(xf, 20*np.log10(FFT_filtered_1))
plt.xlabel('log frequency')
plt.ylabel('Signal in dB')
plt.grid()
plt.show()
```



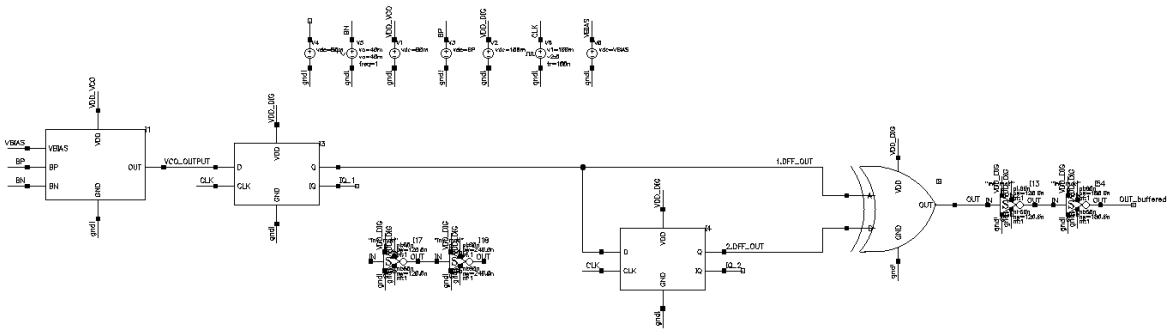
Figur 72: Fast fast corner simulation result with temperature 46 Celsius



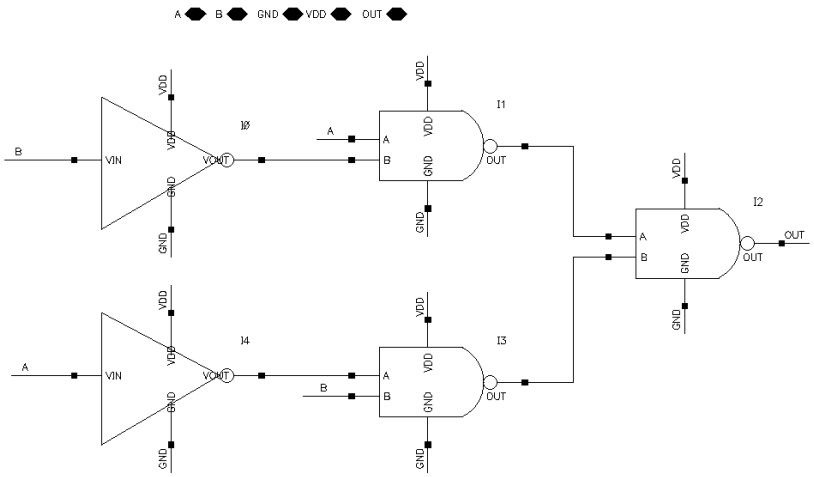
Figur 73: Typical typical corner simulation result with temperature 20 Celsius



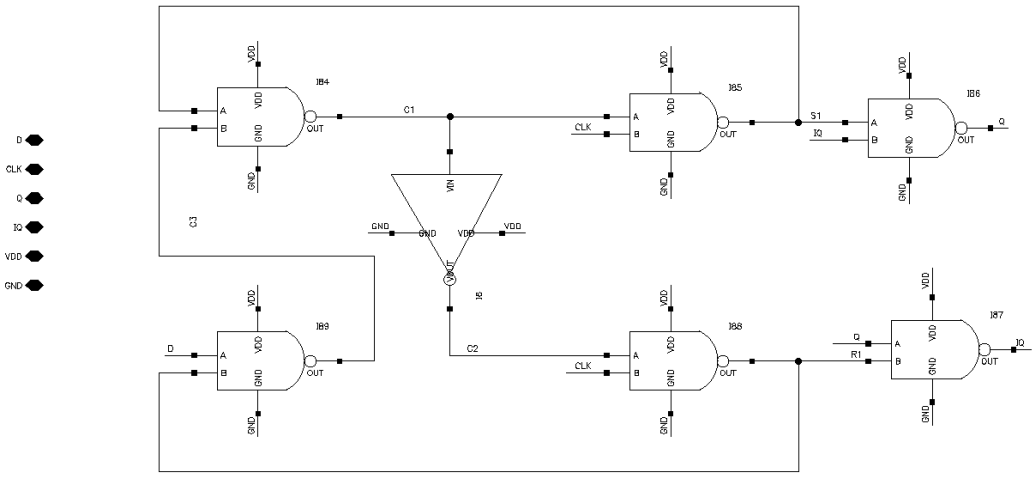
Figur 74: RVCO circuit on Cadence



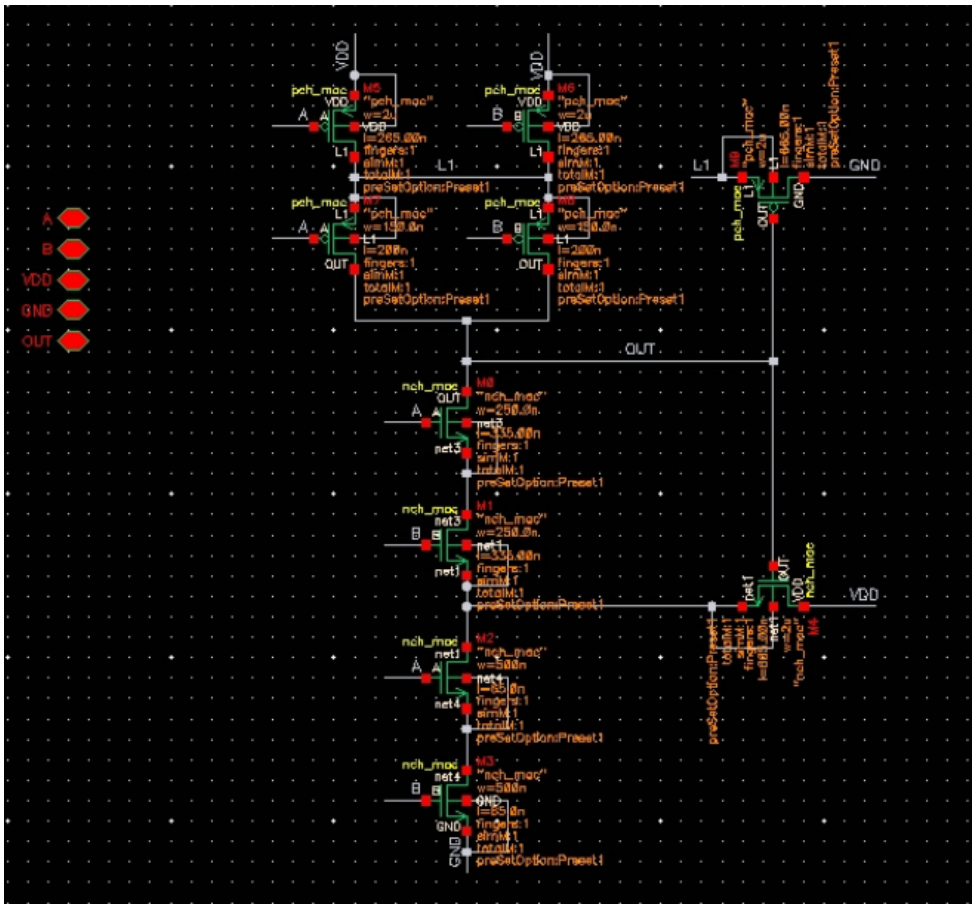
Figur 75: FDSM circuit on Cadence



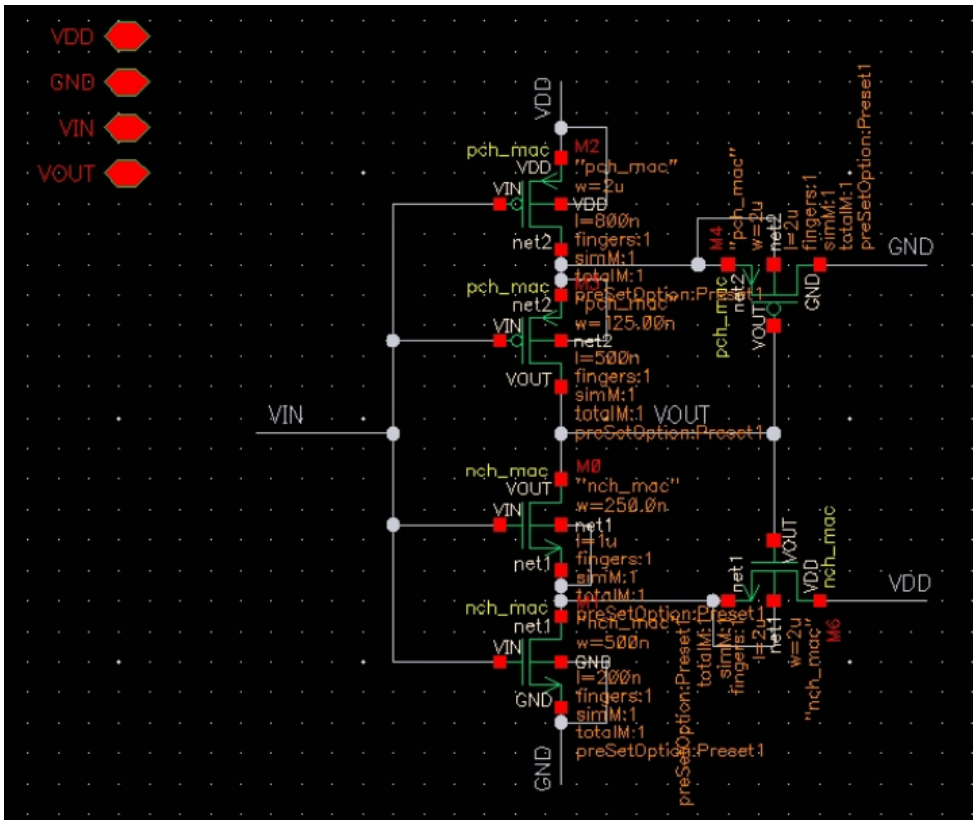
Figur 76: XOR gate circuit on Cadence



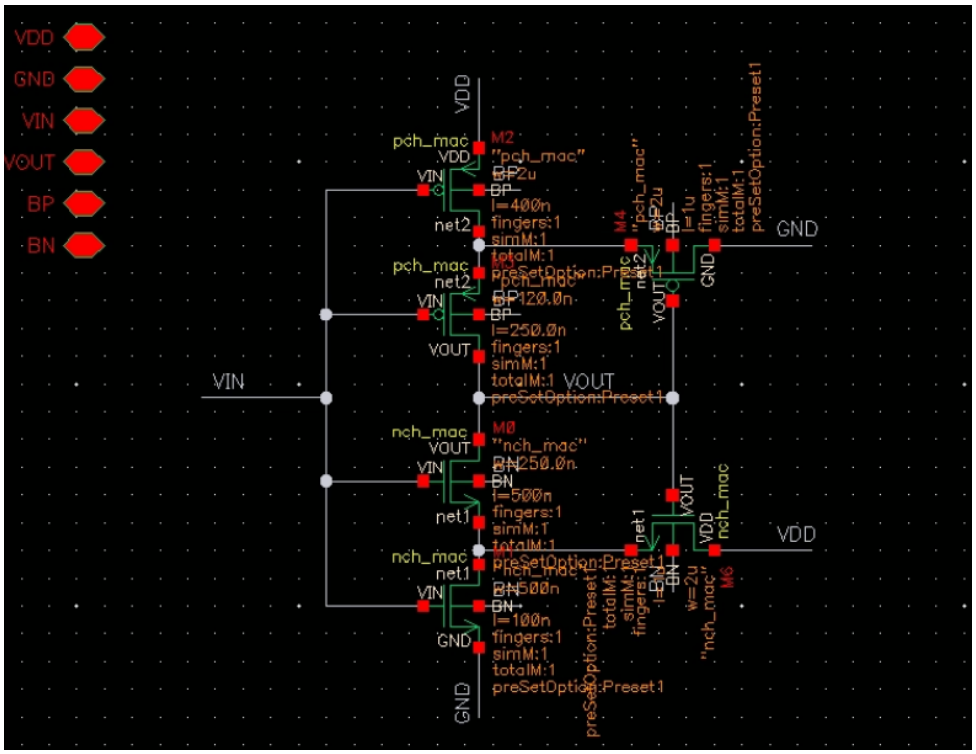
Figur 77: DFF circuit on Cadence



Figur 78: NAND gate on Cadence



Figur 79: ST inverter on Cadence



Figur 80: Body biased inverter on Cadence

$$\frac{2(f_c - \Delta f)}{m} < \frac{2(f_c + \Delta f)}{m+1}$$

$$2(f_c - \Delta f)(m+1) < 2(f_c + \Delta f)m$$

$$(2f_c - 2\Delta f)(m+1) < (2f_c + 2\Delta f)m$$

$$\cancel{2f_c m} + 2f_c - 2\Delta f\, m - 2\Delta f < \cancel{2f_c m} + 2\Delta f\, m$$

$$-2\Delta f\, m - 2\Delta f\, m < 2\Delta f - 2f_c$$

$$-4\Delta f\, m < 2\Delta f - 2f_c$$

$$-m < \frac{2\Delta f - 2f_c}{4\Delta f}$$

$$m > \frac{2f_c - 2\Delta f}{4\Delta f}$$

$$m > \frac{\frac{1}{2}(f_c - \Delta f)}{2\Delta f}$$

$$m > \frac{f_c - \Delta f}{2\Delta f}$$

$$m_{\_min} = \frac{f_c - \Delta f}{2\Delta f}$$

$$f_{clk} = \frac{2(f_c - \Delta f)}{m_{\_min}} = \frac{2(f_c - \Delta f)}{\frac{f_c - \Delta f}{2\Delta f}}$$

when $f_c \gg \Delta f$

$$f_{clk} = \frac{2\cancel{f_c}}{\frac{\cancel{f_c}}{2\Delta f}} = 4 \cdot \Delta f$$

Figur 81: Calculation of m and f_{clk}

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