Fabrication and characterisation of 4H-SiC diodes for particle detectors

Daniil Panfilov

Thesis submitted for the degree of
Master in Materials Science and Nanotechnology
60 credits

Semiconductor physics
Faculty of mathematics and natural sciences

UNIVERSITY OF OSLO

Spring 2023

Fabrication and characterisation of SiC-4H diodes for particles detectors

Daniil Panfilov

Fabrication and characterisation of SiC-4H diodes for particles detectors

http://www.duo.uio.no/

Printing: Reprosentralen, Universitetet i Oslo

Abstract

Silicon Carbide (SiC) radiation detectors are increasingly gaining recognition for their enhanced performance in diverse applications including nuclear radiation detection, functioning under high-temperature environments, x-ray detection, neutron detection and dosimetry. SiC comes out on top with its ability to operate efficiently in challenging environments. Compared to its primary competitor silicon (Si), 4H-SiC polytype has higher thermal conductivity, superior temperature stability, and a wider bandgap. In this thesis a scalable fabrication technique for n-type 4H-SiC Schottky diodes is proposed, serving as a stepping stone for the future fabrication of 4H-SiC-based detectors. The work encompasses the development and fine-tuning of photolithography processes, fabrication of 4H-SiC Schottky diodes, and their characterization.

The photolithography process is based on the lift-off method. It involves two layers: (i) positive resist and (ii) a so-called lift-off layer to provide an undercut for easier removal of the resist. Such parameters as the exposure and development times were optimized. Optical microscopy and cross-sectional scanning electron microscopy were employed for optimizing the lithography process. Nickel, deposited by e-beam evaporation, was used for formation of Schottky diodes.

Current-Voltage (IV) measurements show that the reverse-bias leakage current for most of the diodes is below the detection limit of the instruments used. The reverse saturation currents and the ideality factors are deduced from the fitting of the diode equation to the measurements for the forward bias. The lowest ideality factor and saturation current are 1.14 and $3.24 * 10^{-21} A$, respectively. The highest breakdown voltage obtained is 350 V. Capacitance-Voltage (CV) measurements have revealed the doping concentration in the epi-layer to be $1.2 - 1.3 * 10^{16}\ cm^{-3}$. The depletion width at 100 V is deduced to be around 3 μm. The highest built-in voltage is found to be 1.6 V for 200 μm diodes, which is comparable with a theoretic value of 1.7 V [3, 4]. It is observed that smaller diodes (200 μm) demonstrate better characteristics, such as ideality factor, breakdown voltage and build-in voltage, compared to larger ones (2000 μm). We hypothesise that this is due to surface imperfections in the SiC epi-layer or dust particles from poor sample handling: As the diode size increases, there is a higher probability of a surface imperfection or a dust particle to occur between SiC and the metal, which will be detrimental for the Schottky diode.

CV characterization of metal-oxide-semiconductor (MOS) structures is used to examine thermally grown silicon oxide (SiO_2) and aluminium oxide (Al_2O_3), deposited by atomic layer deposition (ALD). MOS with thermally grown SiO_2 reveal CV curves typical for a high-quality MOS structure, validating the insulating and passivating properties of the oxide.

In comparison, ALD-grown $Al_2\ O_3$ did not manifest reproducible and consistent CV characteristics.

Acknowledgements

First and foremost, I would like to express my heartfelt gratitude to my supervisors Prof. Eduard Monakhov, Dr Angela Kok, Dr Marco Povoli and Dr Michael Getz, for their patience and guidance throughout this thesis. I would also like to extend my sincere appreciation to Viktor Bobal for helping me out in the cleanroom and showing me the ins and outs of the lithography process. In addition, thank you to all LENS employees and Mena students for the company and council. Special thanks to my fellow master students Lars, Marie and Alireza. It was fun studying with you guys!

I want to also thank Veronika for her love and encouragement, and my family for their unwavering support.

The Research Council of Norway is acknowledged for the support to the Norwegian Micro- and Nano-Fabrication Facility, NorFab, project number 295864.

Contents

Introduction **1**

1 Theory **2**

1.1 Semiconductors 3

1.1.1 Electrons around the single atom 3

1.1.2 Band gap 4

1.1.3 Direct and indirect semiconductors 5

1.1.4 The Fermi Dirac distribution 6

1.1.5 Charge carriers 7

1.1.6 Doping 8

1.1.7 Conductivity and mobility 9

1.1.8 Optical absorption 11

1.1.9 Recombination of electrons and holes 11

1.2 Diodes 12

1.2.1 PN-diode 12

1.2.2 Depletion region 13

1.2.3 PN-junction under a bias 14

1.2.4 Schottky junction diodes 16

1.3 MOS-capacitors 18

2 Fabrication and characterization methods **21**

2.1 Fabrication 21

2.1.1 Photo lithography 21

2.1.2 Physical vapor deposition 24

2.1.3 Thermal oxidation 26

2.2 Characterization 28

2.2.1 Current-voltage characterization 28

2.2.2 Capacitance voltage characterization 31

2.2.3 Metal-oxide-semiconductor capacitance characterization 31

3 Fabrication details & experimental results **34**

3.1 Test Pattern 34

3.1.1 Lithography 34

3.1.2 Lift of layer 38

3.1.3 Diode pattern & metallization 38

3.2 Sample preparation 40

3.2.1 Schottky fabrication 40
3.2.2 MOS fabrication 42
4 Characterization results **45**
4.1 Current Voltage results 45
4.2 Capacitance Voltage results 49
4.3 Metal-oxide-semiconductor capacitance characterization results 51
5 Conclusion **54**
5.1 Future work 55
References **56**

Introduction

The active area of the detector consists of a configuration of reverse-biased planar diodes, varied in shape and size, and connected in a specific circuit arrangement to suit the intended application. Central to this thesis, is a Schottky diode, an electronic rectifier formed from a junction between a metal and a doped semiconductor. In close proximity to the junction forms a region devoid of charges, known as the depletion region. When ionizing radiation provides sufficient energy to an electron in the valence band, the electrons jump to the conduction band to the valence band, creating an electron-hole pair. The induced charge carriers can be separated by the electric field within the depletion region and collected on the diode electrodes [5].

The performance of solid-state detectors hinges significantly on the materials used to create their components, including Schottky diodes. Silicon Carbide (SiC) is an increasingly noteworthy material in the technological sphere and is experiencing a surge in popularity due to its unique properties. It is compatible with high-energy radiation detectors designed to operate in extreme environments [6-10]. The several SiC key characteristics:

High thermal conductivity. Specific SiC polytypes exhibit significantly elevated levels of thermal conductivity. For instance, 4H-SiC, a premier commercially available SiC polytype, exhibits a thermal conductivity of $4.9 W/(cmK)$ significantly outpacing its primary competitor, Silicon (Si), which stands at $1.5 W/(cmK)$[8]. High thermal conductivity improves the heat dissipation [8] and the ability to manage the operational temperature of devices [9].

High atomic displacement energy. An impinging energetic particle can knock atoms from the crystalline lattice sites. The atomic displacement energy, E_d, also known as threshold displacement energy, determines the minimum kinetic energy needed for a permanent displacement of atom from is lattice site. The atomic displacement value for SiC is high, $E_{dSi} = 35\ eV$ and $E_{dC} = 22\ eV$ compared to Si`s $E_d \approx 13 - 20 eV$ [9]. In theory, this should make SiC devices more durable in radiation environments [8, 9].

Large band gap. At room temperature (300K), the three most prevalent SiC politypes: 3C-SiC, 6H-SiC, and 4H-SiC, have band gaps of approximately 2.36 eV, 3.02 eV, and 3.26 eV, respectively [8]. This is considerably higher than Si: 1.12 eV [8]. A wide band gap is considered to cause low noise in detectors due to low leakage currents [8, 9]. Additionally, the band gap width effectively prevents the absorption of visible and infrared light, which could otherwise introduce noise when detecting highly energetic radiation particles [8, 9].

The thesis consists of five parts. Part I describes the theoretical fundamentals essential to understand concepts discussed in this thesis. It includes some of the fundamentals in semiconductor physics, pn-junction, Schottky and metal- on semiconductor (MOS). Part II describes the experimental methods used for fabrication and characterization of the devices made. It entails some of the theory behind photolithography, physical vapour deposition (PVD) and thermal oxidation Part III lists fabrication procedures and their immediate experimental results. Part IV encompasses characterization results and provides current voltage measurements (IV) and capacitance voltage measurements (CV). The final chapter provides main conclusions of the work and suggests topics for future research.

Part I Theory

This chapter introduces the theoretical concepts relevant to this thesis. The chapter will cover several essential topics: Semiconductor physics, pn-junction, Schottky junction and MOSCAP junction. The theory is based on the following books: Griffiths [11], Streetman [2] and Sze [12].

1.1 Semiconductor

Electrical conductivity can classify materials into metals, insulators, and semiconductors. Among these, semiconductors play a crucial role in modern electronics, serving as a critical component in many devices. They can be found in everything from rectifying diodes to complex programmable devices.

Some of the more known semiconducting materials are silicon, germanium, and gallium arsenide [12]. Silicon and Germanium are examples of so-called elemental semiconductors. They can be primarily found in the 14th group in the periodic table. Silicon, in its primary form, is widely used in all electronics. It is cheap and, in most cases, relatively easy to work with. Elemental germanium is not as popular as at the dawn of the semiconductor industry. Nowadays, germanium compounds with other elements found in the 14th group are much more common [12, 13]. Gallium arsenide is a primary example of a binary semiconductor. This type of compound originates from groups: 13th and 15th. GaAs is currently used in lasers, transistors, light-emitting devices, and other types of electronics.

1.1.1 Electrons around the single atom

Before going into the ins and outs of what exactly makes a semiconductor a semiconductor, it is beneficial to briefly go through how electrons behave around a single atom. In the 1920s, it was shown through a series of experiments, such as the photoelectric effect by Einstein and the double split experiment by Davisson and Germer, that electrons do not obey Newtonian mechanics. A new set of equations and rules was developed into a new theory that later became a new physics field called quantum mechanics.

As a result of this development, it was established that electrons can only exist at certain energy levels around the atom. These states can take different geometric shapes and are referred to as orbitals. The shape of the orbital and the characteristics of an electron can be found by solving the Schrodinger equation, which can be written as:

$$\hat{H}\boldsymbol{\psi} = E\boldsymbol{\psi}, \tag{1.1.1}$$

where the Hamiltonian operator, $\hat{H}$, encapsulates kinetic and potential operators, E is the eigenvalue for energy and $\boldsymbol{\psi}$ is the wave function of the particle in question (in this case electrons). The $\boldsymbol{\psi}$ alone does not have a clearly defined physical meaning (or this meaning is not yet found). However, the absolute value of it, $|\boldsymbol{\psi}|^2$, describes the probability of the particle existing in a specific region. A set of quantum numbers defines the electron wave functions: n, l, m and s.

The principal quantum number *n* describes the energy level, as the number increases, the energy and the distance between the electron and the atomic core increase. For each , there are *n* amount *l* numbers. Azimuthal quantum number *l* describes electrons' orbital angular momentum and geometric shape of the orbital. The third quantum number, the magnetic quantum number, m_l, describes the orientation of the orbital. These quantum numbers span from -*l* to *l*. Finally, the last quantum number, m_s , describes the spin of the electron, and it can be either: $+\frac{1}{2}$ or $-\frac{1}{2}$.

1.1.2 Band gap

In a solid, many atoms are brought close together. Consequently, the electronic orbitals overlap. According to the Pauli exclusion principle, two electrons cannot occupy the same orbital. Thus, when two electrons in the same state are brought close enough together, their electron levels are split into two. Similarly, if an n number of atoms are brought close enough together, their levels split into n states. These states form continuous energy bands that electrons may occupy. Band gaps, i.e., regions without states, may separate these bands.

The valence electrons occupy the highest energy band, known as the valence band. If there is a band gap between the valence band and the subsequent energy band, called the conduction band, it will remain empty unless energy is transferred to the electrons. This energy is provided at room temperature, and electrons are excited from the valence band to the conduction band.

The band gap between the valence and conduction bands is a characteristic property of semiconductors and insulators. In insulators, the band gap is large enough to hinder electron excitation. In semiconductors, the band gap is small enough to make this excitation possible at room temperature. Metals, on the other hand, either have no band gap or a substantial number of electrons in the conduction band, as is shown in Figure 1.

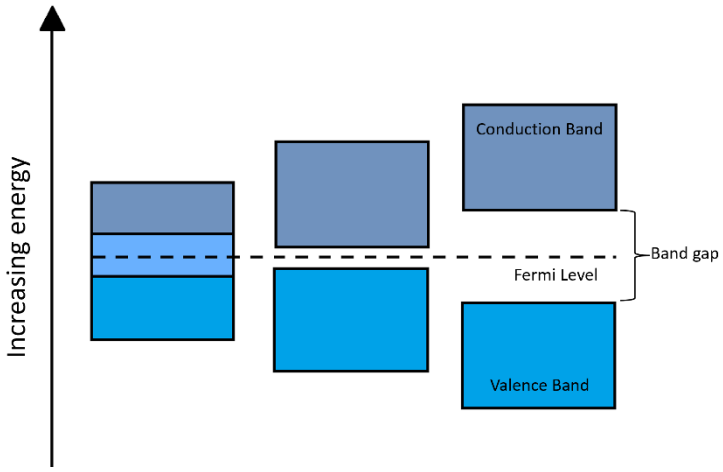

Figure 1 The band gap of metals, semiconductors and insulators. The figure is inspired by Streetman, page 91,[2].

1.1.3 Direct and indirect semiconductors

To better understand the behaviour of electrons in energy bands, it is helpful to analyse the electron function in a periodic potential. This function can be determined by solving the Schrodinger equation, which can be rewritten from (1.1.1) in the form:

$$\left[-\frac{\hbar}{2m^*}\nabla^2 + V(\boldsymbol{r})\right]\psi(\boldsymbol{r},\boldsymbol{k}) = E(\boldsymbol{k})\psi(\boldsymbol{r},\boldsymbol{k}), \tag{1.1.2}$$

where $\hbar$ denotes the Planck's constant, m^* is the effective mass of the electron, $V(\boldsymbol{r})$ is the approximated periodic potential as a function of real space vector $\boldsymbol{r}$, $\psi(\boldsymbol{r},\boldsymbol{k})$ is the electron wave defined as a function of both real and momentum vectors r, k and $E(\boldsymbol{k})$ is the energy that only depends on the momentum vectors k.

The solution to the equation (1.1.2) takes the form of a wave function, also known as the Bloch function:

$$\psi(\boldsymbol{r},\boldsymbol{k}) = U(\boldsymbol{r},\boldsymbol{k})e^{-i\boldsymbol{r}\boldsymbol{k}}, \tag{1.1.3}$$

where $U(\boldsymbol{r},\boldsymbol{k})$ is a periodic function. The corresponding wave energy $\boldsymbol{E_k}$ can be then written as:

$$\boldsymbol{E_k} = \frac{\hbar}{\boldsymbol{2m^*}}|\boldsymbol{k}|^2. \tag{1.1.4}$$

The plot of energy against different directions in $\boldsymbol{k}$ space can provide valuable insights into material properties. For example, the presence of the bandgap and its width can be determent. If there is a difference between the highest energy point in the valence band and the lowest point in the conduction band the gap energy E_g can be calculated.

The other property that can be determined is the band gap type. The material is considered to have a direct bandgap if the highest point in the valence band and the lowest point in the conduction band have the same momentum and, consequently, equivalent ***k***. Electrons in materials with direct band gap can easily transition from the conduction band to the valence band by emitting a photon. In contrast, materials with indirect band gap require a change in momentum and cannot easily facilitate this process.

These characteristics make direct band gap material preferable in light-emitting diodes. In fact, direct band gap materials can often be found in lasers and light emitters. Figure 2 provides a dispersion relation for SiC-4H, an indirect band gap material, and Indium Nitride (InN), a direct band gap material.

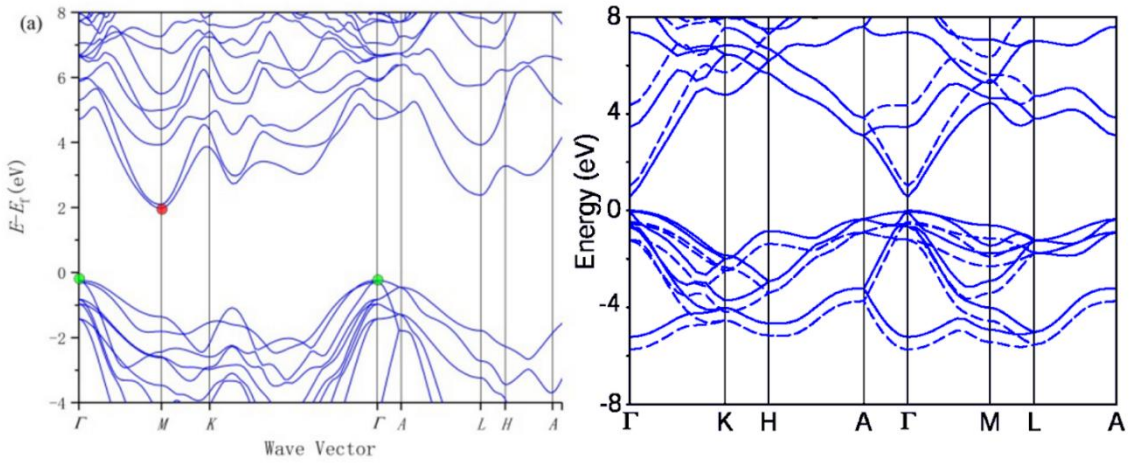

Figure 2 Picture on the left shows the dispersion relation for SiC-4H with wide indirect. band gap. The picture on the right shows InN with a narrow direct band gap. Taken from[14] and [15]:

1.1.4 The Fermi Dirac distribution

The probability of electrons to occupy a certain energy level is described by Fermi Dirac function. It is represented by the equation:

$$f(E) = \left[1 + e^{\frac{E-E_F}{kT}}\right]^{-1}, \tag{1.1.5}$$

where $f(E)$ is the probability of the electron occupying the energy level E. The temperature is denoted by T, and k is the Boltzmann constant. The Fermi level, E_F, represents the energy at which the probability of finding the electron is mathematically fifty percent.

Since the value for $f(E)$ have value between 0 and 1, the probability for not finding electrons can be written as:

$$1 - f(E) = \left[1 + e^{\frac{E_F - E}{kT}}\right]^{-1}, \tag{1.1.6}$$

When the temperature is at absolute zero, the probability for electron to occupy the energy below the fermi level, $f(E < E_F)$, becomes equal to one, and the probability for electron to occupy the energy level above the fermi level, $f(E > E_F)$, becomes zero. Consequently, the probability distribution looks like a step function at $T = 0K$. At temperatures greater than absolute zero, the likelihood of electrons being present above E_F increases. This coincides with the electron's ability to jump between the valence and the conduction band.

1.1.5 Charge carriers

There are two types of charge carriers. Firstly, there are electrons, which, once excited to the conduction band, can transport negative charge throughout the material, given the abundance of empty states surrounding them. Secondly, there are holes. Essentially, they are empty states in the valence band. As holes denote an electron deficiency, they are considered to carry positive charges.

When an electron is excited to the conduction band in a semiconductor, it leaves behind a vacant state in the valence band. Semiconductors that have an equal number of electrons and holes are called intrinsic. Semiconductors that display an imbalance in the number of electrons and holes, having either an excess of electrons or holes due to the presence of defects or impurities, are called extrinsic semiconductors.

The equilibrium electron charge carrier concentration, n_0, can be found by integrating the Fermi Dirac distribution from (1.1.5) and the electron density of states $N(E)dE$ over energy dE.

$$n_0 = \int_{E_C}^{\infty} f(E)N(E)dE, \tag{1.1.7}$$

where E_C is the energy for the conduction band. A similar expression for the concentration of holes, h_0 , can be written from (1.1.6):

$$h_0 = \int_{-\infty}^{E_V} [1 - f(E)]N(E)dE \tag{1.1.8}$$

where E_V is the energy for the valence band. In cases where temperatures and carrier density are adequately low, the density of states N(E) can be approximated to density near the bottom of the conduction band:

$$N(E) = M_C \frac{\sqrt{2}}{\pi^2} \frac{m_{de}^{3/2}(E - E_C)}{\hbar^3} \tag{1.1.9}$$

where M_C is the number of minima in the conduction band and m_{de} is the product of density states along the principal axes n: $m_{de} = (m_1^* m_2^* m_3^*)^{1/3}$, where m_1^*, m_2^* and m_3^*

are the effective masses along the principle axes. For non-degenerate semiconductors, the doping concentration is smaller than N_C, then Boltzmann`s statistics can be used instead of Fermi-Dirac statistics, and integral (1.1.7) becomes:

$$n_0 = N_C exp\left(-\frac{E_C - E_F}{kT}\right), \tag{1.1.10}$$

where N_C is the effective density of states in the conduction band and can be expressed as:

$$N_C = 2\left(\frac{2\pi m_{de} kT}{\hbar^2}\right)^{3/2} M_C, \tag{1.1.11}$$

by similar argumentation the hole concentration (1.1.8) can be evaluated to be:

$$p_0 = N_V exp\left(-\frac{E_F - E_V}{kT}\right), \tag{1.1.12}$$

where N_V can be written as:

$$N_C = 2\left(\frac{2\pi m_{de} kT}{\hbar^2}\right)^{3/2} M_C \tag{1.1.13}$$

is the effective density of states in the valence band. These equations are valid for both intrinsic and extrinsic materials. For intrinsic material E_F is usually in the middle and can be denoted by E_i . By rewriting (1.1.10) and (1.1.12) intrinsic carrier concentrations, n_i and p_i can be found:

$$p_i = N_V exp\left(-\frac{E_i - E_V}{kT}\right) = n_i = N_C exp\left(-\frac{E_C - E_i}{kT}\right) \tag{1.1.14}$$

By multiplying (1.1.10) with (1.1.11) the law of mass action can be derived:

$$n_0 p_0 = n_i^2 = p_i^2 \tag{1.1.15}$$

1.1.6 Doping

Doping refers to the controlled introduction of defects into a material. This process can be categorized into two types: p doping and n doping. In an ideal semiconductor, EHP is the only type of carrier, meaning the number of holes and electron is equal. The inclusion of atoms with extra charges leads to an uneven ratio between electrons and holes. If most of the carriers are electrons, the material is classified as an n type semiconductor. Likewise, if most of the carriers are holes, the material is referred to as a p type semiconductor.

Additional electron states are introduced with the new atoms. They lie between the valence band, E_V and the conduction band, E_C. In p type material, these states are located closer to

the E_V. If the fermi level is above, these states will be filled with electrons from the valence band, forming holes. In n-type material, the introduced states lie closer to the E_C. If the fermi level is below these levels, the introduced atoms will donate electrons to the conduction band, making electrons the majority of charge carriers. This process is often called donor ionization because the introduced atom either gives away or receives electrons.

The majority of charge carriers in extrinsic semiconductors can be approximated to be:

$$n_0 \approx N_D; p_0 \approx N_A, \tag{1.1.16}$$

where N_D represents the number of donor impurities that provide extra electrons to the lattice, while N_a represents the number of acceptor impurities that can accept an electron from the lattice.

In semiconductors with donors and acceptors simultaneously, the relationship between the electrons, holes, acceptors, and donors can be determined by the charge neutrality equation:

$$p_0 + N_D^+ = n_0 + N_A^-, \tag{1.1.17}$$

where N_D^+ is ionized donors and N_A^- is occupied acceptors.

1.1.7 Conductivity and mobility

In the absence of an external electric field, electrons move randomly. There is no net motion. Even though, individually, each electron has a direction, the material remains electronically neutral. However, when an electric field is applied, the net motion of the group becomes directionally oriented. The average velocity of electrons, also known as the net drift velocity, can be written as:

$$< \boldsymbol{v} \geq \frac{-q^2 \hat{t}}{m_n^*} \boldsymbol{E}, \tag{1.1.18}$$

where E is the electric field, $\hat{t}$ is the mean time between the collisions, q is the electron charge, and $m_n^*$is the effective mass.

The density of the current J can be calculated by multiplying the drift speed of charges with the total amount of charges present q:

$$\boldsymbol{J} = -qn < \boldsymbol{v} >, \tag{1.1.19}$$

by inserting (1.1.18) in (1.1.19) the density current becomes:

$$\boldsymbol{J} = -qn \frac{-q^2 \hat{t}}{m_n^*} \boldsymbol{E}. \tag{1.1.20}$$

This is another form of ohm's law and can be rewritten to:

$$\boldsymbol{J} = -\sigma \boldsymbol{E}, \tag{1.1.21}$$

where conductance, σ, can be rewritten to:

$$\sigma = n\frac{-q^2\hat{t}}{m_n^*} = qn\mu_n, \tag{1.1.22}$$

where, μ_n ,denotes the electron's ability to migrate through the material in an electric field. It is proportional to the mean free time divided by the mobility effective mass:

$$\mu_n = \frac{q\hat{t}}{m^*}. \tag{1.1.23}$$

The equation labelled (1.1.22) is suitable only for materials with electrons as the sole charge carriers. Nonetheless, considering the contribution of hole charges, the overall conductivity in materials that have both electrons and holes can be altered as follows:

$$\sigma = q\left(n\mu_n + p\mu_p\right). \tag{1.1.24}$$

In practicality, mobility is affected by several factors. Generally, mobility can be also expressed by Matthiessen`s rule:

$$\mu = \sum_i \left(\frac{1}{\mu_i}\right)^{-1}, \tag{1.1.25}$$

where μ_i are mobilities from different contributing factors.

Temperature impacts the mobility and conductivity of materials. When the temperature rises, the lattice's thermal vibrations become more noticeable, resulting in more collisions between the phonons and charge carriers, lowering their mobility. This effect has proportionality with $T^{3/2}$ and the mobility from this interaction μ_i can be expressed as:

$$\mu_i \propto \frac{T^{3/2}}{N_I m^{*1/2}}, \tag{1.1.26}$$

where N_i is ionized impurity density. Conversely, ionized impurities significantly impact the carriers at lower temperatures. Resulting in mobility contribution μ_l that has inverse proportionality with $T^{3/2}$ this proportionality can be expressed as:

$$\mu_l \propto \frac{1}{m^{5/2}T^{3/2}}. \tag{1.1.27}$$

Other scattering mechanisms impact mobility, but their effect is negligible in this context. Thus, mobility can be written as:

$$\mu(T) = \left(\frac{1}{\mu_l} + \frac{1}{\mu_i}\right)^{-1} \propto \left(\frac{a}{T^{\frac{3}{2}}} + \frac{b}{T^{-\frac{3}{2}}}\right). \tag{1.1.28}$$

1.1.8 Optical absorption

A semiconductor can absorb some amount of radiation particles whose energy matches or exceeds the width of its band gap ($E_{photon} \geq E_g$). This photon energy pushes the electron from the valence band to the conduction band, thus generating excess electrons and holes. Contrarily, a photon with energy less than the band gap ($E_{photon} < E_g$) lacks sufficient energy for the excitation process and, thus, cannot be absorbed. Consequently, materials absorb some amount of light and let through others.

The intensity of the transmitted light through a material, I_t , can be expressed as:

$$I_t = I_0 e^{\alpha l}, \tag{1.1.29}$$

where I_0 signifies the initial beam's intensity and '*l*' represents the thickness of the material. The absorption coefficient, denoted by \alpha, is reliant on the photon's wavelength. Given that the energy of the photon is inversely related to its wavelengths, semiconductors possessing large E_g are not capable of absorbing the visible spectrum, which is characterized by relatively long wavelengths. This concept accounts for why silicon, known for its narrow band gap, is capable of absorbing visible light. Conversely, Silicon Carbide, distinguished by its wider band gap, fails to absorb the same spectrum, rendering it transparent.

1.1.9 Recombination of electrons and holes

Excess electrons can recombine with holes in the valence band by falling back to the conduction band. A photon discharge compensates for the loss of energy. In the case of a direct band gap, this process does not require a change of momentum. The net rate of electron concentration can directly be expressed by subtraction of the recombination rate $\alpha_r n(t)p(t)$ from the thermal generation $\alpha_r\, n_i^2$:

$$\frac{dn(t)}{dt} = \alpha_r n_i^2 - \alpha_r n(t)p(t), \tag{1.1.30}$$

,

where $n(t)$ and $p(t)$ are the electron and a hole concentration as the function of time, n_i denotes intrinsic carrier concentration and α_r is some recombination rate constant.

If the presence of excess electrons is solely due to the absorption of light, their quantity will be equivalent to the number of holes present. If the number of excess carriers is relatively small and by accounting that the excess carrier concentrations and their recombination are equal, $\delta n(t) = \delta p(t)$, (1.1.30) can be rewritten as:

$$\frac{d\delta n(t)}{dt} = \alpha_r n_i^2 - \alpha_r\big(n_0 + \delta n(t)\big)\big(p_0 + \delta p(t)\big) = -\alpha_r[(n_0 + p_0)\delta n(t) + \delta n^2(t)], \tag{1.1.31}$$

which in the case of p-type, ($p_0 \gg n_0$), can be simplified to:

$$\frac{d\delta n(t)}{dt} = -\alpha_r p_0 \delta n(t) \tag{1.1.32}$$

and the solution to this equation can be written as follows:

$$\delta n(t) = \Delta n e^{-\alpha_r p_0 t} = \Delta n e^{\frac{-t}{\tau_n}} \ \ where \ \ \tau_n = 1/p_0\alpha_r \tag{1.1.33}$$

where, the parameter τ_n, known as the recombination lifetime, represents the average time it takes for carriers to recombine. A more general expression for low-level injection carriers, valid for both p-type and n-type, can be described as:

$$\tau_n = \frac{1}{\alpha_r(n_0 + p_0)} \tag{1.1.34}$$

1.2 Diodes

A diode, an important component in numerous electronic devices, is essentially a two-terminal rectifier. Its primary function is to allow an electric current to flow in a single direction while impeding it in the reverse direction. For the purposes of this project, we will specifically focus on the physics of the pn-junction and the Schottky junction diodes.

1.2.1 PN-diode

The pn junction diode derives its unique properties from the boundary between the conjunction of p type and n type semiconductors. At the intersecting point, electrons within the n-region diffuse into the p region, subsequently recombining with the existing holes. Likewise, holes originating from the p region traverse and combine with electrons in the n-region.

On the edge of the n side forms a layer of positive charges due to the presence of uncompensated donors. Conversely, the p-side manifests a layer with negative charges due

to the uncompensated acceptors present. As a direct consequence, an opposing electric field is generated, a deterrent to further carrier diffusion.

With no net charge, this opposing electric field, i.e., drift current, intensifies until it effectively counteracts the diffusion current reaching the equilibrium condition:

$$\boldsymbol{J_{drift} + J_{diff} = 0} \tag{1.2.1}$$

When the system reaches equilibrium, built-in potential V_0 naturally occurs gradually over the depleted region, W. The value of the electric field can be found by derivating the potential $\xi(x) = \frac{-dV(x)}{dx}$. The built-in potential and band diagram of pn junction is depicted in Figure 3

Another important equilibrium condition is that the fermi level remains constant across a pn-junction, resulting in a bend in the band diagram, shown figure c):

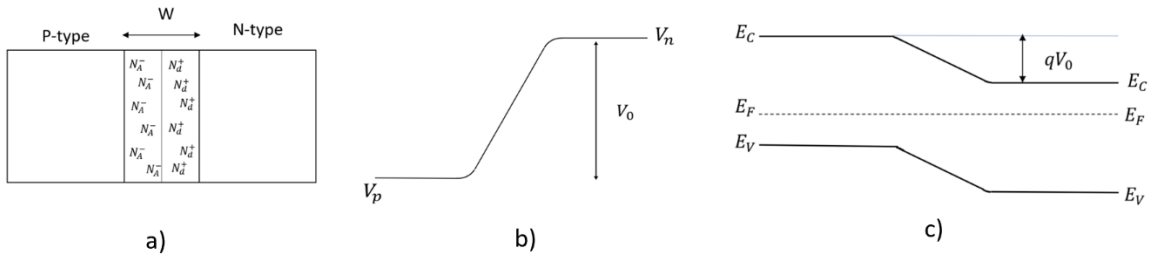

Figure 3 Properties of PN-junction in equilibrium. a) Schematically drawn PN-junction with depletion region W. b) Electrostatic potential between p- and n-type. c) The energy band diagram of PN-junction. The figure is inspired by Streetman [2]

1.2.2 Depletion region

Before recombination, the carrier density within the space charge region can be approximated as the product of the impurity ion concentration, $N_{A/D}$, and the fundamental charge, $\pm q$. Bearing in mind the need for the charge on the p-side to cancel out that on the n side, the resulting condition can be set forth:

$$|\pm Q| = qAx_{p0}N_A = qAx_{n0}N_D \tag{1.2.2}$$

where $\pm Q$ signifies the charge on each side, x_{p0} is the penetration length on the p-side, x_{n0} is the penetration length on the n side, and A is the cross-section area.

The electric field points from the n side to the p side. Its distribution within the depletion region can be calculated by using the Poisson equation:

$$\frac{d\xi}{dx} = \frac{q}{\epsilon}(p - n + N_d^+ - N_a^-). \tag{1.2.3}$$

where ϵ is the permittivity. This equation can be simplified by applying the depletion approximation, i.e., neglecting the carriers' contribution. Two regions of constant space charge become:

$$\frac{d\xi}{dx} = \frac{q}{\epsilon} N_d x_{n0} \quad for \quad 0 < x < x_{n0} \ . \tag{1.2.4}$$

Upon integrating the given equation, the maximal value of the electric field can be represented as follows:

$$\xi_0 = -\frac{q}{\epsilon} N_d x_{n0} = -\frac{q}{\epsilon} N_a x_{p0} \ . \tag{1.2.5}$$

By integrating and accounting for the fact that the electric field must be zero at the edges of the depletion region, the built-in voltage V_0 can be expressed as:

$$-V_0 = \int_{-x_{p0}}^{x_{n0}} \xi(x) dx \ . \tag{1.2.6}$$

The function ξ exhibits a triangular shape, reaching its maximum value at ξ_0. Consequently, the integral can be computed as follows:

$$-V_0 = -\frac{1}{2}\xi_0 W = \frac{1}{2}\frac{q}{\epsilon} N_d x_{n0} W \ . \tag{1.2.7}$$

Equation (1.2.2) provides that $x_{n0}N_d = x_{p0}N_a$, thus the depletion region can be written as $W = x_{n0} + x_{p0}$. When these two expressions are combined: $x_{n0} = W\frac{N_a}{N_a+N_d}$. This result, when inserted into equation (1.2.7), enables the built-in voltage V_0 to be expressed as:

$$V_0 = \frac{q}{2\epsilon}\frac{N_a N_d}{N_a + N_d} W^2 \ . \tag{1.2.9}$$

When the equation is solved for W, the following is obtained:

$$W = \sqrt{\frac{2\epsilon V_0}{q}\left(\frac{1}{N_a} + \frac{1}{N_d}\right)} \ . \tag{1.2.10}$$

1.2.3 PN junction under a bias

By applying an electrical potential to a junction, state equilibrium is disturbed. Depending on the polarity of the bias, the resulting potential barrier can either rise or diminish. Depending on the polarity of the bias, the barrier can either increase or decrease. In the case

of positive bias V_F, the applied voltage opposes the drift current. Thus, initial built-in barrier V_0 gradually decreases to $V_0 - V_F$. For the reverse bias V_R, the opposite is true, i.e. barrier becomes $V_0 + V_R$, as is shown on Figure 4.The majority of charge carriers are supplied under the influence of a forward bias, which results in a decrease in the width of the depletion region. Conversely, when a reverse bias is applied, the depletion region expands as it absorbs the supplied minority charges. Thus, the equation (1.2.10) can be rewritten to represent the bias depletion width W_B:

$$W_B = \sqrt{\frac{2\epsilon(V_0 - V)}{q}\left(\frac{1}{N_a} + \frac{1}{N_d}\right)} \tag{1.2.11}$$

where V is the applied bias.

The minority carrier concentration at the edge of the depletion zone will vary due to the applied bias The equilibrium ratio between the concentration of holes at n and p side can be described as:

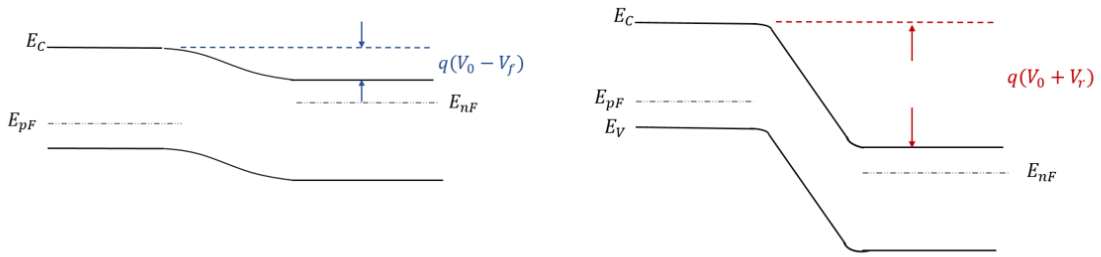

Figure 4 Effects of positive and negative bias on the left and right, respectively. The figure is inspired by page 196 Streetman [2].

$$\frac{p_p}{p_n} = e^{\frac{qV_0}{kT}} \tag{1.2.12}$$

where p_n and p_p are the hole concentrations at n and p side, becomes:

$$\frac{p(-x_{p_0})}{p(x_{n_0})} = e^{\frac{q(V_0 - V)}{kT}}, \tag{1.2.13}$$

where $p(-x_{p_0})$ and $p(x_{n_0})$ is the hole concentration at the edges of W_B $(W_B \equiv x_{n_0} + x_{p_0})$. At low-level injection, the change in majority carrier concentration can be negligible relative to the equilibrium: $p(-x_{p0}) = p_p$. Thus, by inserting (1.2.12), (1.2.13) becomes:

$$\frac{p(-x_{n_0})}{p_n} = e^{\frac{q(V)}{kT}}. \tag{1.2.14}$$

The excess hole concentration at the edge of the n-region, Δp_n and, by similar arguments, the excess electron concentration Δn_pcan then be calculated:

$$\Delta p_n = p(x_{n0}) - p_n = p_n\left(e^{\frac{qV}{kT}} - 1\right), \qquad (1.2.15)$$
$$\Delta n_p = n(-x_{p0}) - n_p = n_p\left(e^{\frac{qV}{kT}} - 1\right).$$

The excess minority carriers will recombine with the majority carriers as they migrate away from the edge of the depletion region. As they diffuse further, a higher proportion of them will recombine. The resulting distribution of excess carriers $\delta p(x)$ as the function of distance $x_{n/p}$ from the depletion edge exhibits an exponential decay pattern and can be represented by the following equations:

$$\delta p(x_n) = \Delta p_n e^{\frac{-x_n}{L_p}} = p_n\left(e^{\frac{qV}{kT}} - 1\right)e^{\frac{-x_n}{L_p}}, \qquad (1.2.16)$$
$$\delta n(x_p) = \Delta n_p e^{\frac{-x_p}{L_n}} = n_p\left(e^{\frac{qV}{kT}} - 1\right)e^{\frac{-x_p}{L_n}},$$

where L_p and L_n denote the diffusion distances for holes and electrons, respectively.

The total diode current as the function of the applied voltage can be derived as the sum of the p-side current I_p and n-side current I_n,

$$I = \frac{qAD_p}{L_p}\Delta p_n + \frac{qAD_n}{L_n}\Delta n_p = I_0\left(e^{\frac{qV}{kT}} - 1\right), \qquad (1.2.17)$$

where A is the area of the diode, the $D_{n/p}$ is the diffusion coefficient for electron/holes and $L_{n/p}$ is the diffusion lengths for electrons/holes. The saturation current I_0 can be expressed as:

$$I_0 = qA\left(\frac{D_p}{L_p}p_n + \frac{D_n}{L_n}n_p\right). \qquad (1.2.18)$$

The expression finalized in (1.2.18) is commonly known as the *ideal diode equation*.

1.2.4 Schottky junction diodes

Another form of diode is a Schottky diode. This diode consists of a metal and a semiconductor. Not every metal and semiconductor can form a Schottky diode. The work function of the metal, which represents the energy required to remove an electron from the Fermi level and is denoted by $q\Phi_m$, must meet specific criteria. In the case of an n-type Schottky junction, $q\Phi_m$ must be higher than the work function of the semiconductor $q\Phi_s$. Conversely, for a p-type junction, the opposite condition must hold; otherwise, the junction will form an ohmic contact.

As depicted in the Figure 5, in the ideal n-type Schottky a potential barrier is established as $q\Phi_B = q(\Phi_m - \chi)$, which, under reverse bias, increases and obstructs the path for carriers originating from the metal. Conversely, during forward bias, the barrier diminishes analogous to a pn junction until it facilitates the passage of majority carriers across the junction. The equilibrium contact potential, also known as built voltage, can be calculated as the difference between the metal and semiconductors work functions: $qV_0 = q(\Phi_m - \Phi_s)$. The electron affinity, denoted as χ, is the energy required to remove an electron from the valence band E_V.

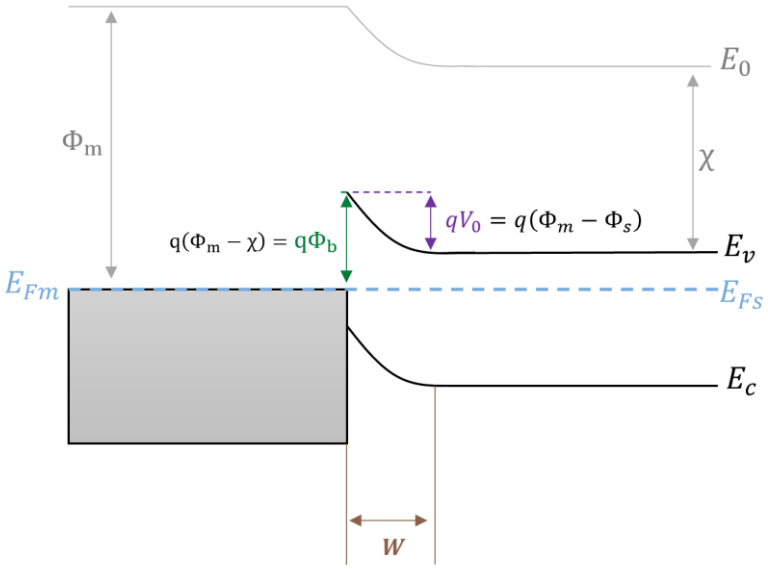

Figure 5 Schematic representation of n-type Schottky. The figure is inspired by Streetman [2], page 229.

The Schottky depletion, $W_{Shottky}$, is quite similar to the W from (1.2.10). If it is assumed an abrupt (for instance n^+p) junction, with $\boldsymbol{N_D} \gg \boldsymbol{N_A}$ the (1.2.10) can be rewritten to:

$$W_{Schottky} = \sqrt{\frac{2\epsilon V_0}{qN_D}\left(V_0 - V - \frac{kT}{q}\right)}. \tag{1.2.19}$$

The ideal Schottky diode equation can be derived from the thermionic-Emission-Diffusion theory [12]:

$$I_{Schottky} = A^{**}T^2 e^{-\frac{q\Phi_B}{kT}}\left(e^{\frac{qV}{kT}} - 1\right). \tag{1.2.20}$$

where A^{**} is a Richardson constant [12]. It is important to note that in practice these expressions are never realized completely, due to surface contaminations and other imperfections [12].

1.3 MOS capacitors

Metal-Oxide-Semiconductor (MOS) capacitors play an important role in the technological world. They are most recognized for being a part of MOS field-effect transistors, the cornerstone of many modern electronic systems. But they are also used in other electronics, such as analogue circuits, sensors, and Charge-coupled devices CCDs. Notably, within the context of this thesis, they can be used to characterize semiconductors.

The MOS structure consists of three layers: a metal, an oxide and a semiconductor. In an ideal case, the work function of the metal is assumed to be equal to the work function of the semiconductor, i.e., $\Phi_m = \Phi_s$ and it is assumed no carrier transport through the insulator under dc biasing conditions (i.e., the resistivity in insulator is assumed to be indefinite). Ideal conditions put into equations for n- type and p-type yields:

$$\Phi_{\mathrm{m}} - \Phi_s = \Phi_m - \left(\chi + \frac{E_g}{2q} - \psi_B\right) = \Phi_m - (\chi + \phi_n) = 0\,, \tag{1.2.21}$$

$$\Phi_{\mathrm{m}} - \Phi_s = \Phi_m - \left(\chi + \frac{E_g}{2q} - \psi_B\right) = \Phi_m - \left(\chi + \frac{E_g}{2q} - \phi_p\right) = 0\,, \tag{1.2.22}$$

respectively, where ϕ_n , ϕ_p and ψ_B are the Fermi potentials with respect to the mid gap and band edges.

Figure 6 illustrates the band structure for n-type (a) and p-type (b) ideal MOS capacitor. In the figure: the semiconductor's Fermi level is denoted by E_F, E_i is the intrinsic level, and $q\phi_B$ signifies the potential barrier height that can be derived as $E_C^I - E_V^I$, where E_C^I is the insulator band energy and E_V^I is the conduction band energy. As is shown on the figure the Fermi potential ψ_B can be found as the distance between the fermi level and intrinsic level, ($q\psi_B = |E_F - E_i|$).

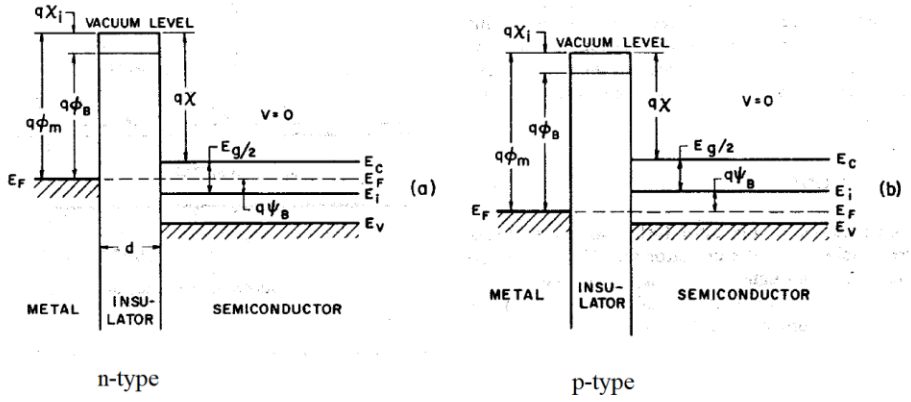

Figure 6 Energy-band diagram for an ideal MOS. Picture is taken from Sze [16] page 364.

If the voltage is applied three cases may happen:

Accumulation

When a negative voltage is applied to the metal layer in a p-type MOS, the charges accumulate on the semiconductor-oxide boundary so that:

$$|Q_m| = |Q_s|, \tag{1.2.23}$$

where Q_m is the charge on the metal, and Q_s is the charge on the semiconductor. The Gauss law becomes:

$$E = \int \frac{\rho}{\epsilon} dx \tag{1.2.24}$$

causes a constant electric field across the oxide that gradually decays in the semiconductor. The potential:

$$V = -\int \boldsymbol{E} \cdot \boldsymbol{dl}, \tag{1.2.25}$$

then increases linearly from the metal side to the semiconductor side. The semiconductors Fermi level shifts below the metal's Fermi level by qV. Since the work functions cannot change, this causes the tilt in the oxide conduction energy as is depicted in Figure 7 a). This operational state is commonly designated as accumulation.

Depletion

During small positive voltages, the potential of the metal is raised compared to the semiconductor, and, as shown in Figure 7 b), the bands experience the shift in the opposite direction. This is called depletion since the number of charges at the semiconductor-oxide interface steadily decreases.

Inversion

After a while, when E_f grows considerably above E_i, the material starts to build up electron concentration near the surface. This mode of operation is called inversion, shown on Figure 7 c).

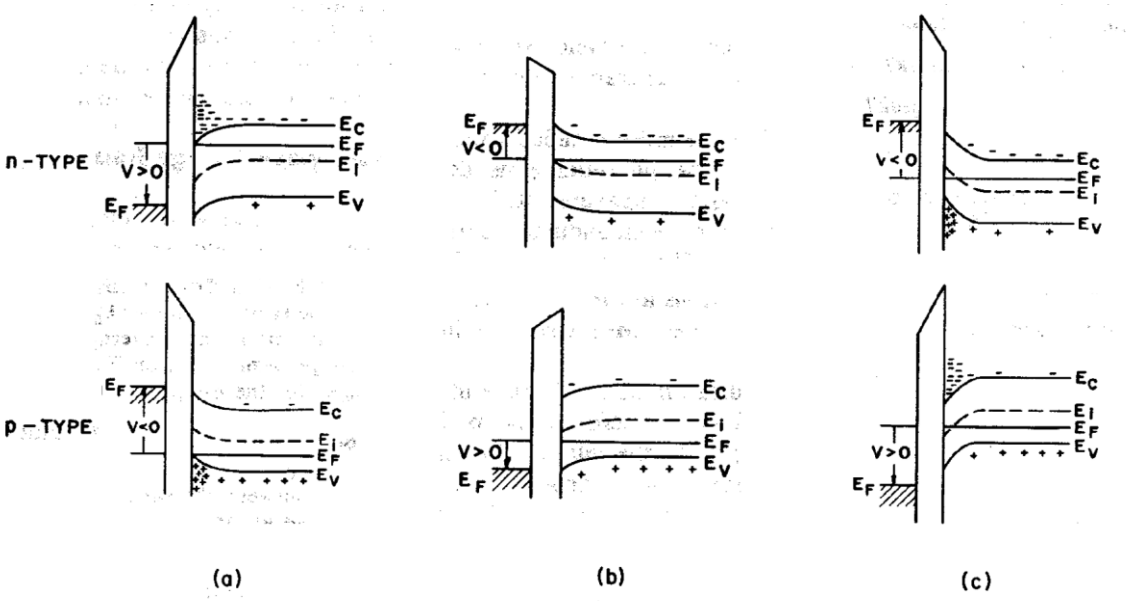

Figure 7 Band diagram of MOS modes of operation. Picture is taken from Sze [16], page 365.

Part II Fabrication and characterization methods.

2.1 Fabrication

In this chapter, the use of several techniques required for the fabrication will be covered. A detailed description of the experimental process will be provided in the results part.

2.1.1 Photo lithography

Lithography is a widely used fabrication method in manufacturing of microelectronics. It involves the selective removal of specific parts of a thin photosensitive film, known as photoresist, which is applied to a substrate [17]. The process can be divided into two main parts. Firstly, there is the optical part, where the focus is on the optical means to transfer a pattern onto the photoresist. Secondly, there is the chemical processes that occur within the photoresist after it is exposed to light [1].

Areal image

To initiate the lithography process, an optical source emits light or electrons onto a substrate that is coated with photoresist. The source can be light that typically falls within the range of visible light (400 nm) to deep ultraviolet (200 nm), [1]. In optical projection lithography (OPL), the design is projected through a physical mask, which typically consists of transparent and opaque parts made of materials like silica and chromium, commonly used in the silicon industry [1]. It is crucial to ensure the mask is defect-free since any defects will be transferred to the final product.

In contrast, maskless photo lithography (MPL) projects the optical beam into a focal spot and scans it across the photoresist [18]. One significant advantage of MPL is that it eliminates the need for a physical mask. Instead, the design can be directly uploaded to the machine, resulting in potential cost and time savings during the fabrication process.

The desired pattern is initially created using computer software. For complex devices, deposition multiple layers of different materials with various shapes and sizes may be required. Thus, the lithography process often involves the use of multiple masks for different layers. The equipment utilized in lithography must not only imprint the design but also align the layers, hence these instruments are often called *alligners* [1].

An aligner's performance can be evaluated based on several measures, with one of them being the alignment overlay accuracy. This metric reflects the instrument's ability to precisely detect and align with the alignment marks. Another important parameter is the throughput, which, roughly put, measures the speed at which the sample is exposed. Lastly, is the resolution. The resolution, denoted as R, represents the smallest feature size on the pattern. The resolution is primarily influenced by the diffraction phenomenon of light. This dependence can be expressed through the equation:

$$R = \frac{k\lambda}{NA}, \tag{2.1.1}$$

where k is a constant specific to the application, typically ranging between 0.6 and 0.8, λ is the wavelength of the radiation source, and NA is the numerical aperture of the lens [17]. According to this equation, the resolution can be enhanced by reducing the wavelength (λ) or increasing the numerical aperture (NA). It is important to note that the quality of the photoresist also has an impact on the resolution.

Photoresist

Once the photoresist is exposed to light, the substrate is dipped into a developer solution. Based on the reaction, photoresist can be classified into two categories: positive and negative. Positive photoresist exhibits a reaction to light that causes the exposed areas to dissolve more rapidly during the etching process. Provided that the development time is optimal, the unexposed areas must remain unchanged. The response of the negative photoresist is opposite from that of the positive photoresist. The unexposed areas will dissolve quicker during the development. [1]

Chemically, the photoresist is an organic compound that consist of three essential components: a resin serving as the foundational material, a photoreactive compound (PAC) that modulates the dissolution rate based on light exposure, and a solvent that governs mechanical properties, such as the viscosity of the solution [1].

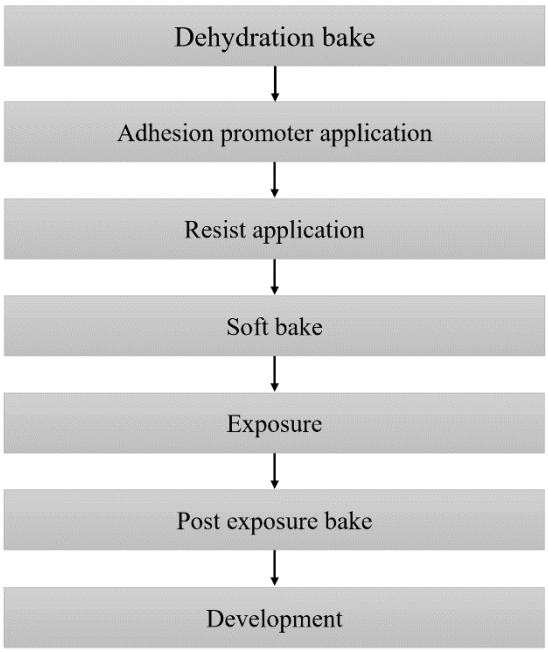

Figure 8 illustrates a typical photoresist application process. It begins with a dehydration bake, followed by the application of a primer, typically hexamethyldisilane (HMDS), which

functions as an adhesion promoter [1]. Next, the photoresist is applied in liquid form onto the surface of the substrate. Uniform distribution is achieved by employing a resist spinner, which accelerates the substrate to a predetermined rotational speed. The sample then undergoes a soft bake and is subsequently prepared for exposure and development.

There are several parameters that must be tuned. Firstly, the process must be optimized to the photoresist's sensitivity, which is measured by the amount of energy it is required to create a chemical change in the photoresist. In practicality, the intensity of the beam will be relatively fixed so the exposure time and then, the development time must be tuned through a trial-and-error approach.

Lithography can be an expensive and time-consuming process that some even argue that it can account for more than one-third of the manufacturing costs [1]. Nevertheless, its unparalleled flexibility in creating intricate shapes at the micro/nanoscale makes lithography an indispensable technique.

An example of a complete lithography process is illustrated on the Figure 9

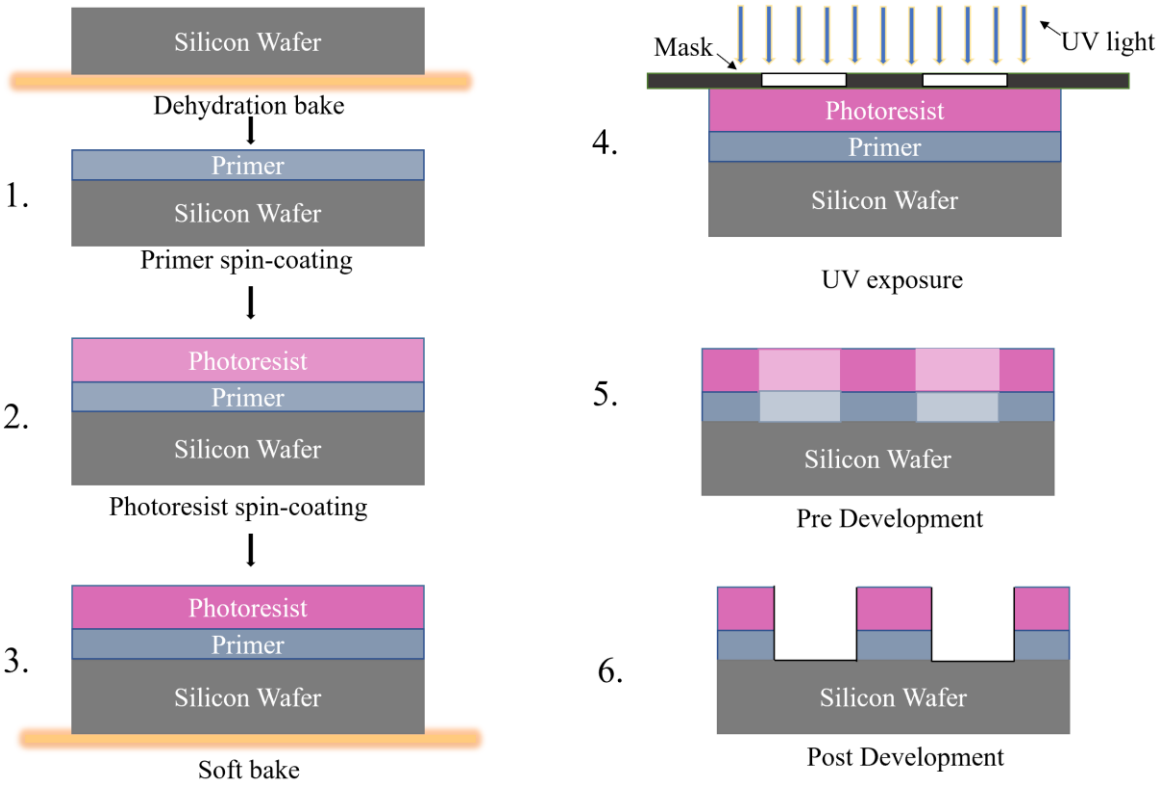

Figure 9 Schematic representation for the lithography process step by step (with positive photoresist).

2.1.2 Physical vapour deposition

Physical vapour deposition (PVD) is an umbrella term for techniques that involves a vaporization of some material from a charged or solid/liquid source, that is physically deposited onto a substrate. The film can have thickness in the range of a few nanometres up to several thousand [19]. Various types of PVD methods exist, including sputtering, arc vapor deposition, and ion plating. However, for the purpose of relevance to this thesis, the primary emphasis in this section will be on the vacuum evaporation deposition (VD).

In the process of vacuum deposition, a sample is placed inside a chamber, followed by the pumping of the vacuum, typically to a pressure lower than 1 mtorr [1]. The material to be deposited, referred to as the charge, is loaded into a container situated within the chamber. Subsequently, the container is heated to a point where the charge begins to vaporize. As a result of the reduced pressure, the vaporized particles travel in straight trajectories until they accumulate as a thin film on the surface of the sample. The figure illustrates a simplified representation of a VD system.

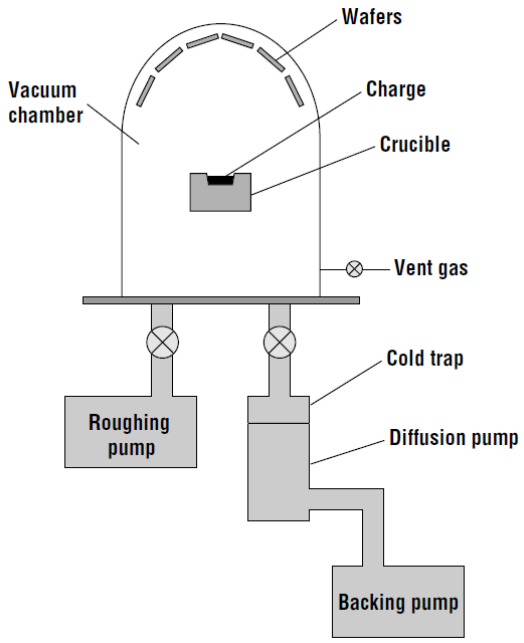

Figure 10 Schematic representation of the VD system. Taken from Campbell [1]

To obtain good deposition rates the vapor from the charge must be at least 10 mtorr [1]. The vapor pressure P_e from the liquid charge can be expressed in terms of temperature T as [20]:

$$P_e = 3 * 10^{12} \sigma^{\frac{3}{2}} T^{-\frac{1}{2}} e^{\frac{\Delta H_V}{N k_b T}}, \quad (2.1.2)$$

where, σ represents the surface tension of the metal, N is Avogadro's number, and ΔH_V is the enthalpy of evaporation. The relationship between pressure and temperature is influenced by the specific material under consideration. Thus, certain materials must be heated to much higher temperature to achieve reasonable deposition rates, than others. For instance, the required temperature for Aluminium (Al) is around 1250℃ and the required temperature for Tungsten (W) is above 3000℃ [1].

The deposition rate can be derived from the number of gas molecules crossing a plane per unit time J_n [1]

$$J_n = \sqrt{\frac{{P_e}^2}{2\pi kTm}}, \tag{2.1.3}$$

where m is the atomic mass. By multiplying this expression with the mass of the molecule, the expression for the mass evaporation rate R_{Ml} can be obtained [21]:

$$R_{Me} = \sqrt{\frac{m}{2\pi kT}} P_e \, . \tag{2.1.4}$$

The mass loss of the crucible R_{Ml} can be found by taking the integral of the area dA of the crucible:

$$R_{ML} = \int R_{Me} dA = \sqrt{\frac{m}{2\pi k}} \int \frac{P_e}{\sqrt{T}} \, dA \, , \tag{2.1.5}$$

If it is assumed that the vaporized particles travel in straight lines and that all of the material that arrives at sample sticks to the sample, the constant of proportionality k can be expressed as [22] :

$$k = \frac{sin\,\theta\, cos\,\phi}{\pi R^2} \, . \tag{2.1.6}$$

where R is the distance between the crucible and the wafer. The θ and ϕ are the angles between R and the surface normal of the crucible. If the crucible with the charge and the wafers are placed inside a spherical surface:

$$\cos\theta = cos\,\phi = \frac{R}{2r} \, . \tag{2.1.7}$$

where r is the radius of the sphere. By combining the equations (2.1.5), (2.1.6) and (2.1.7) the deposition rate R_d becomes:

$$R_d = \sqrt{\frac{M}{2\pi l \rho^2}} \, \frac{P_e}{\sqrt{T}} \frac{A}{4\pi r^2} \, . \tag{2.1.8}$$

In comparison to other vaporization methods, VD generally offers higher deposition rates [19]. However, it has one notable limitation, and it is its ability to adequately cover surface topology, commonly referred to as step coverage [1]. As the deposition process progresses, the topology can create shadows on the sample, posing a challenge. To address this issue, rotating and heating the wafer during deposition has been employed as a partial solution [1].

In contemporary applications, VD is utilized for various purposes, including the formation of optical interference coatings, permeation barrier films, mirror coatings, electrically conductive films, and corrosion protective coatings. Within the scope of this thesis, VD is primarily employed to deposit metals onto Schottky diodes and to create contacts on MOS capacitors.

2.1.3 Thermal oxidation

Thermal oxidation (TO) is a process that involves the formation of silicon oxide (SiO_2) film on a silicon (*Si*) substrate. To initiate this process, a wafer is placed on a silica crucible, that is then placed into a chamber. The chamber is enriched with an oxidation agent. The formation of the oxide begins at room temperature but quickly halts at a thickness of 25 Å.

The growth of SiO_2 occurs at the interface between the silicon (*Si*) substrate and the formed oxide layer. This is because the diffusivity of *Si* in SiO_2 is typically significantly lower than that of oxidation agents. Consequently, as the oxide film becomes thicker, the diffusion path for the oxidation agents lengthens. Therefore, to promote the reaction and enable the formation of a thicker oxide film, increased temperature is required. As a result, thermal oxidation on Silicon is typically carried out at relatively high temperatures, usually around 800 - 1000℃ [2].

There are essentially two types of thermal oxidation: dry and wet oxidation. Dry thermal oxidation involves the use of oxygen (O_2) as the oxidizing agent and wet thermal oxidation employs water vapour (H_2O). The corresponding chemical equations for these reactions can be represented as follows:

Dry Thermal Oxidation:

$$Si(s) + O_2(g) \rightarrow SiO_2(s) \tag{2.1.9}$$

Wet Thermal Oxidation:

$$Si(s) + 2H_2O(aq) \rightarrow SiO_2(s) + 2H_2(g) \quad (2.1.10)$$

In both cases, approximately 44% of the silicon is consumed, i.e., for every micron of oxide growth, around 0.44 microns of silicon are consumed [2].

The growth rate of the oxide can be deduced from the oxygen concentration at the *Si*/ SiO_2interface C_i according to the Deal-Grove model [1]:

$$C_i = \frac{HkTC_s}{1 + \frac{k_s}{(\frac{h_g}{HkT})} + \frac{k_s t_{ox}}{D}} \quad , \quad (2.1.11)$$

where, H is henrys gas constant, h_g is mass transport coefficient, the k_s is the is the chemical rate constant for the reaction, C_s is the concentration of oxygen at the surface of the substrate, D is the diffusivity, T is the temperature and t_{ox} is the oxide thickness. The total flux J of oxygen molecules reacting with the silicon is given by:

$$J = k_s C_i \quad . \quad (2.1.12)$$

The growth rate R can be obtained by dividing the flux by the number of oxygen molecules per unit volume of SiO_2 N_I

$$R = \frac{J}{N_I} = \frac{dt_{ox}}{dt} = \frac{k_s HkTC_s}{N_I\left[1 + \frac{k_s}{\left(\frac{h_g}{HkT}\right)} + \frac{k_s t_{ox}}{D}\right]} \quad . \quad (2.1.13)$$

An important relationship can be derived between the oxidation time t and the oxide layer thickness t_{ox} [1, 23]:

$$t_{ox}^2 + At_{ox} = B(t + \tau), \quad (2.1.14)$$

where A, B and τ are constants depending on the oxidation conditions. For thin oxides this condition can be simplified to:

$$t_{ox} \approx \frac{B}{A}(t + \tau). \quad (2.1.15)$$

Hence, the oxidation rate should approach a constant near 0 thickness:

$$lim_{t \to 0} \frac{dt_{ox}}{dt} = \frac{B}{A} \quad . \quad (2.1.16)$$

This, however, contradicts empirical measurements which indicate an increase by a factor of 4 or more at low thicknesses [1].

For thick oxides the condition (2.1.14) can be simplified to:

$$t_{ox}^2 \approx B(t + \tau). \quad (2.1.17)$$

In terms of structure, thermally grown SiO_2 showcases short-range order, consisting primarily of a randomly oriented network of polyhedral as depicted in the figure. Electronically, it behaves as an insulator, with its conductivity ranging from 10^{-9} Ω^(-1) to 10^{-16} Ω^(-1) over a temperature range of 25℃ to 960℃ [24].

For the scope of this thesis, it is noteworthy that TO can be performed on SiC as well [23]. Though the process is analogous, the growth requires an extended duration or elevated temperatures. TO on SiC obeys (2.1.13) at the Carbon (C) interface, but not at the Si interface [23].

2.2 Characterization

2.2.1 Current-voltage measurement

A helpful approach for evaluating the diode's quality is to measure the current I through the device while varying the applied voltage V. An optimal diode exhibits minimal resistance under forward current and maximal resistance under reverse current. The intent of I-V measurements is to evaluate the degree to which the diode adheres to the ideal scenario, and to determine important figures of merit such as the ideality factor, the saturation current, and the break-through voltage.

As illustrated in Figure 11 a), the I-V curve for an n-type Schottky measures forward bias by applying a positive potential to the n-type semiconductor, with the reverse scenario depicted in Figure 11 b).

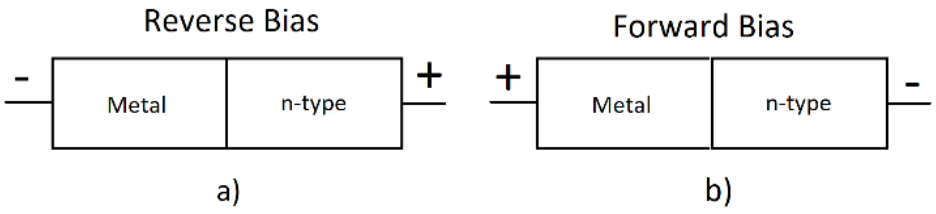

Figure 11 Illustration of forward and reverse bias contact polarities.

Forward bias measurements

For moderately doped semiconductors, the current-voltage relationship can be expressed as [25]:

$$I = AA^{**}T^2 e^{\left(-\frac{q\phi_B}{kT}\right)}\left[e^{\frac{qV}{\eta k_B T}} - 1\right] = I_S\left[e^{\frac{qV}{\eta k_B T}} - 1\right], \tag{2.2.1}$$

where I_S is the saturation defined as current and η is the ideality factor (additional parameters are defined in the referenced Schottky paper). When forward voltages exceed 3kT/q, equation (2.2.1) is normally simplified to [12]:

$$I = I_S\, e^{\frac{qV}{\eta k_b T}}. \tag{2.2.3}$$

Applying the natural logarithm to equation (2.2.2) yields a practical linear function:

$$\ln I = \ln I_s + \frac{qV}{\eta k_b T}. \tag{2.2.4}$$

Subsequently, the ideality factor η can be deduced:

$$\eta = \frac{1}{kT}\left(\frac{d(\ln I)}{dV}\right)^{-1}. \tag{2.2.5}$$

The logarithmic plot might deviate from linearity due to several factors. The series resistance starts dominating at high positive voltages (Figure 12 d)) and at high currents, the injected minority carriers may reach majority concentration levels (i.e., high current injection) (Figure 12 c)). Consequently, the current becomes approximately proportional to $exp\,(qV/2k_BT)$ [12].

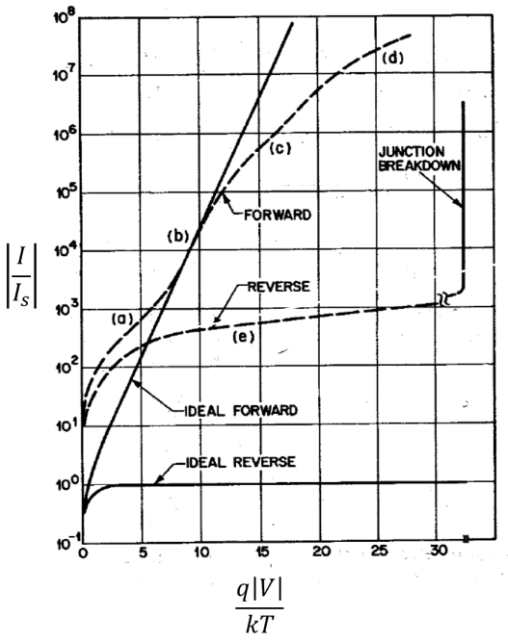

Figure 12 The dashed line represents the real case, while the solid line represents the ideal case. Figure is taken from Sze [12].

Extrapolating the linear fit from the logarithmic plot at zero voltage allows the saturation current I_s to be determined. With this value, the barrier height ϕ_B can be deduced:

$$\phi_B = \frac{kT}{q}\ln(\frac{A^{**}AT^2}{I_s}). \tag{2.2.6}$$

In practical situations, the barrier height Φ_B deviates from the ideal value (defined on page 16) due to factors such as interface states acting as charge traps and the presence of a thin interfacial layer of atomic dimensions between the metal and the semiconductor. These factors are accounted for in the barrier height Φ_B^{tr} [12]:

$$\Phi_B^{tr} = \frac{\epsilon_i}{\epsilon_i + q^2\delta D_{it}}(\Phi_m - \chi) + \left(1 - \frac{\epsilon_i}{\epsilon_i + q^2\delta D_{it}}\right)\left(\frac{E_g}{q} - \phi_0\right), \tag{2.2.7}$$

where ϕ_0 is the neutral level($\phi_0 = qE_{Fs} - qE_{Vj}$, where E_{Vj} is the bent valence band at the junction), ϵ_i is the permittivity of the interfacial layer, δ is the thickness of the interfacial layer and D_{it} is the interface trap density. Additionally, the barrier height ϕ_B will also experience image force lowering due to the external electric field in the applied bias [12].

Reverse bias measurements

Ideally, the resistance in reverse current should be infinitely high. However, in practice, reverse bias experiences leakage current as illustrated in Figure 12 e). The primary component of reverse current in Schottky diodes is attributed to edge leakage current [12], a phenomenon triggered by the sharp edge of the diode. This issue can be partially mitigated by diffused guard rings [12].

At high voltages, the diode may experience breakdown as illustrated in Figure 12. The two most common diode breakdown mechanisms are considered to be avalanche multiplication and Zener breakdown [2]. Avalanche breakdown is caused by impact ionization; if the electric field resulting from the applied bias is substantial, a charge entering from the metal side may be accelerated to a high enough energy to create an electron-hole pair (EHP) via an ionizing collision. The generated carriers may have sufficient energy to induce further ionizing collisions, resulting in cascade called *carrier multiplication*. Zener breakdown, on the other hand, is driven by the tunnelling of electrons through the depletion barrier [2].

2.2.2 Capacitance-voltage measurements

An alternative approach to characterizing diodes involves utilizing capacitance-voltage (CV) measurements. This approach determines barrier height (analogous to IV measurements), doping concentration of the semiconductor, and the built-in potential.

By combining (1.2.2) and (1.2.9) the voltage variable capacitance $\boldsymbol{C_{pn}}$ for regular diodes can be written as:

$$C_{pn} = \left|\frac{dQ}{d(V - V_0)}\right| = \frac{A}{2}\left[\frac{2q\epsilon N_d}{V_0 - V}\frac{N_d N_a}{N_d + N_a}\right]^{\frac{1}{2}}. \tag{2.2.8}$$

For an n-type Schottky diode, this equation can be likened to an asymmetrical pn^+junction. Thus, the capacitance of the n-type Schottky, denoted as C_{Sc} becomes:

$$C_{Sc} = \frac{A}{2}\left[\frac{2q\epsilon N_d}{V_0 - V}\right]^{\frac{1}{2}}. \tag{2.2.9}$$

The built-in potential and the doping concentration can be found from $\frac{1}{C^2}$ curve:

$$\frac{1}{C^2} = -\frac{2}{A^2\epsilon q N_d}V + \frac{2}{A^2\epsilon q N_d}V_0\,. \tag{2.2.10}$$

The barrier height can be found from the built-in potential as:

$$\Phi_B = V_0 + \xi + \frac{kT}{q}, \tag{2.2.11}$$

where $\boldsymbol{\xi} = E_C - E_F$ (for n-type). The doping concentration can be derived from the slope of $\frac{1}{C^2}$:

2.2.3 Capacitance-voltage measurements for MOS

Capacitance-Voltage (C-V) measurements in Metal-Oxide-Semiconductor (MOS) structures can offer valuable insights into the properties and performance of the oxide layer. The CV curve itself can be an indicator of whether the oxide layer is functioning correctly as an insulator. Secondly, CV measurements can determent important parameters that describe the MOS, including the doping concentration, threshold voltage and flat band

voltage. Lastly, deviation from the ideal case can be found from the work function difference, the interface trap density and fixed oxide charges.

If the CV curve shows an expected MOS shape, the accumulation capacitance C_i can be extracted directly from the accumulation region. During the accumulation, the MOS structure behaves as a parallel- plate capacitor, so the oxide's thickness t_{ox} can be extracted as:

$$t_{ox} = C_i \epsilon_i \ , \tag{2.2.12}$$

where $\boldsymbol{\epsilon_i}$ is the permittivity of the oxide.

The minimum point on the capacitance curve, C_{min}, is in series with the C_i and the depletion layer capacitance C_{dmin}, which van be expressed as:

$$C_{min} = \frac{\boldsymbol{C_i C_{dmin}}}{\boldsymbol{C_i + C_{dmin}}} \ , \ , \tag{2.2.13}$$

By rearranging for C_{dmin}, eq (2.2.13) becomes:

$$C_{dmin} = \frac{C_i C_{min}}{C_i - C_{min}} . \tag{2.2.14}$$

The maximum depletion width W_m is achieved at minimum capacitance, hence W_m can be extracted as:

$$W_m = C_{dmin} \epsilon_s \ , \tag{2.2.15}$$

where $\boldsymbol{\epsilon_s}$ is the permittivity of the semiconductor. W_m can be expressed in terms of doping concentration N_d:

$$W_m = 2 \left[\frac{\epsilon_s k_B T ln\left(\frac{N_d}{n_i}\right)}{q N_d} \right]^{\frac{1}{2}} . \tag{2.2.16}$$

This cannot be solved for N_d analytically. However, there exist several numerical methods that can do it. From which an approximate numerical iterative method in terms of C_{dmin}, given by Streetman is expressed as:

$$N_d = 10^{[30.388 + 1.683 \ log(C_{dmin}) - 0.03177 \ (log(C_{dmin}))^2]} \ , \tag{2.2.17}$$

where C_{dmin} is in $\frac{F}{cm^2}$.

From N_d estimate it is possible to determine the Debye screening length that can be approximated as:

$$L_D \approx \sqrt{\frac{\epsilon_s k T}{q^2 N_d}} \ . \tag{2.2.18}$$

This parameter is valuable as it presents an estimation of the extent to which charge imbalances are screened. Moreover, from it, Debye capacitance, C_{debye} , can be deduced,

which in turn gives an estimate of the flat band capacitance, C_{Fb},with its corresponding flat band voltage V_{Fb}.

$$C_{debye} = \frac{\epsilon_s}{L_D}, \tag{2.2.19}$$

$$C_{Fb} = \frac{C_i C_{debye}}{C_i + C_{debye}} \ . \tag{2.2.20}$$

The threshold voltage (for n-substrate) can be now extracted as:

$$V_{Th} = V_{Fb} - \frac{Q_d}{C_i} + 2\phi_F = \Phi_{ms} - \frac{Q_i}{C_i} - \frac{Q_d}{C_i} + 2\phi_F \ , \tag{2.2.21}$$

where the Q_i is interface charge, and the fermi potential ϕ_F can be expressed as:

$$\phi_F = \frac{kT}{q} ln\left(\frac{N_d}{n_i}\right) \ , \tag{2.2.22}$$

and the depletion charge Q_d is:

$$Q_d = qN_d W_m = 2(\epsilon q N_d \phi_F)^{\frac{1}{2}} \ . \tag{2.2.23}$$

The typical MOS curve for n-type semiconductor exhibits shape shown on the figure Figure 13. The accumulation region measures C_i at the maximum value on the right side of the curve. V_{fb} is the voltage, in the ideal case, the energy level of the semiconductor (E_{FS}) aligns with the fermi energy level of the metal (E_{FM}), as is illustrated on band diagram shown on the Figure 6.

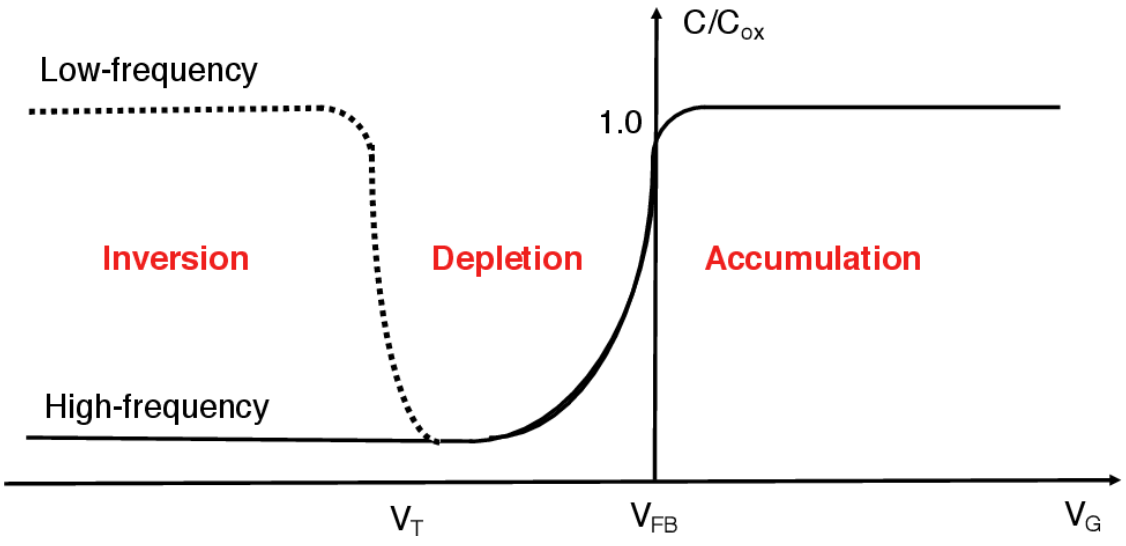

Figure 13 Shows a theoretical MOS curve. The picture is taken from [26].

Part III Experimental details & results.

The scope of this thesis is aimed towards the development of radiation detectors, focusing on fabrication and characterization of Silicon Carbide based diodes and MOS-capacitors. This chapter outlines the process of diode fabrication.

3.1 Test Pattern

This section of the thesis discusses the use of a test pattern for refining fabrication methods and adjusting lithography parameters, ultimately aiding future diode fabrication. The fabrication was performed in the cleanroom facility Mina lab UiO.

3.1.1 Lithography

Figure 13 presents the test pattern employed to assess the fabrication methods and adjust lithography parameters for prospective diode fabrication. This pattern was utilized to fabricate a series of wafers, the objective of which was to fine-tune the exposure and development times. For this experimental stage, a number of 2-inch silicon wafers were chosen as test substrates. The methodology for this process is outlined in the following steps:

1. A liquid primer (HDMS) was applied to approximately 2/3 of the silicon wafer, which was then uniformly distributed with a process spinner (Model WS-650 MZ-23 NPP/LITE).
2. After allowing a minute for the primer to dry at room temperature, a positive photoresist (S1813) was applied and spun to uniformity (RPS 3000).
3. The wafer was then heated on a hotplate at 115℃ for a 2-minute soft bake.
4. The pattern was exposed using a tabletop maskless aligner (Heidelberg instruments µPG501), with exposure time varying across wafers.
5. The exposed wafers were introduced to a developer solution (MF328) and observed under an optical microscope at various development times, as presented in Table 1.

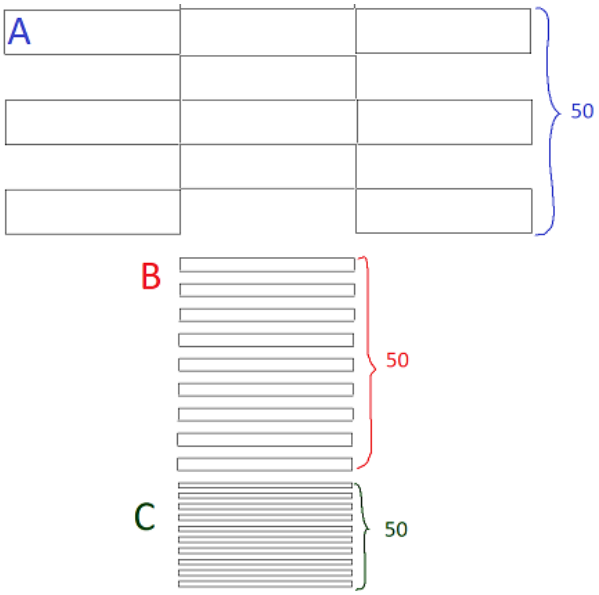

Figure 14 Pattern consisted of tree types of boxes. ” A ” boxes had 20 µm width, ”B” boxes has 5 µm width and ” C” boxes had 2 µm width. There were 50 boxes of each type placed similar to what is shown in the picture. The width of boxes and space between boxes were even.

6. For cross-sectional examination, the samples were halved by a laser cutter (ELAS) and inspected with a scanning electron microscope (SEM).

Table 1: Overview of the samples with different exposure and development times. The first numbers are initial developer time that were not enough to fully expose the pattern.

Exp. Time	10 ms	15 ms	22 ms	30 ms	100 ms
Dev. Time	30 s 90 s 120 s 180 s	60 s	96 s 126 s	30 s 60 s	30 60
Final	**210 s**	**105 s**	**156 s**	**90 s**	**120 s**

Results

The patterns that were developed under shorter exposure times lacked clarity, despite extended development durations. Figures 14 and 15 display the outcomes of 10 ms and 22 ms exposure times, respectively. Both instances yielded poorly defined patterns. The smaller boxes are barely perceptible even under extended development times, and the larger boxes never fully materialize.

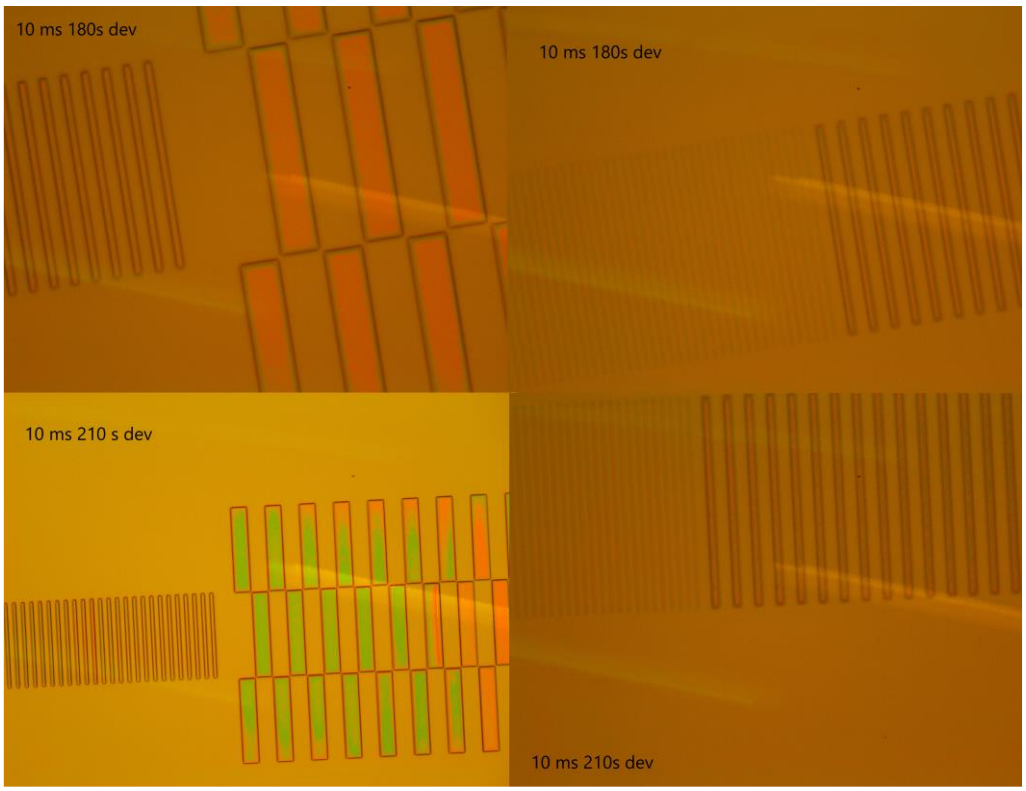

Figure 15 The sample exposed for 10 ms after different development times. Pictures on the left shows A and B boxes, and pictures on the right shows B and C boxes.

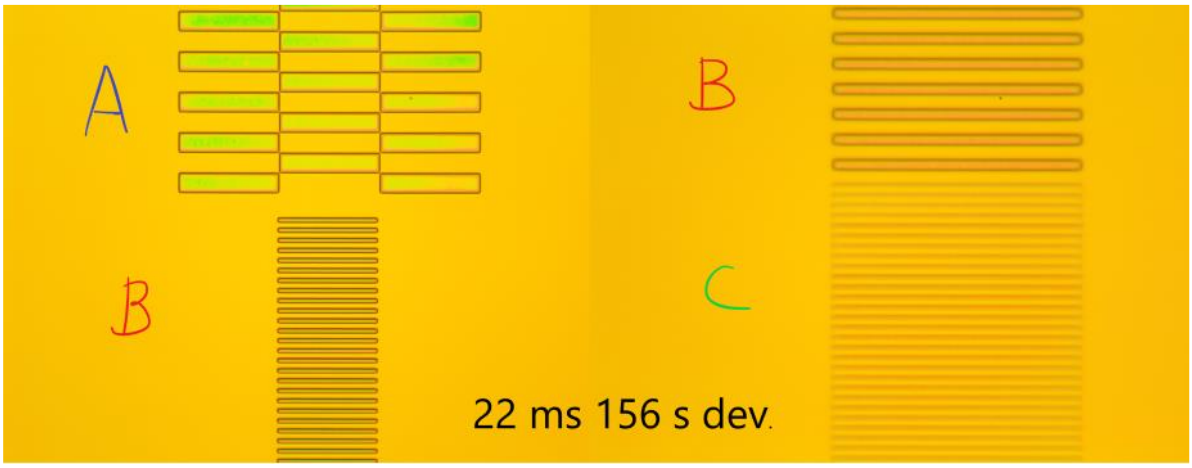

Figure 16 Exposed for 22 ms after 156 s development time

As illustrated in the top two images of Figure 16, patterns exposed for 30 ms developed satisfactory. With a development duration of 1 minute, the larger patterns exhibited minor overlap, while the smaller patterns remained underdeveloped. However, after a 2-minute development, the smaller geometric forms fully emerged, but the larger ones became somewhat overdeveloped.

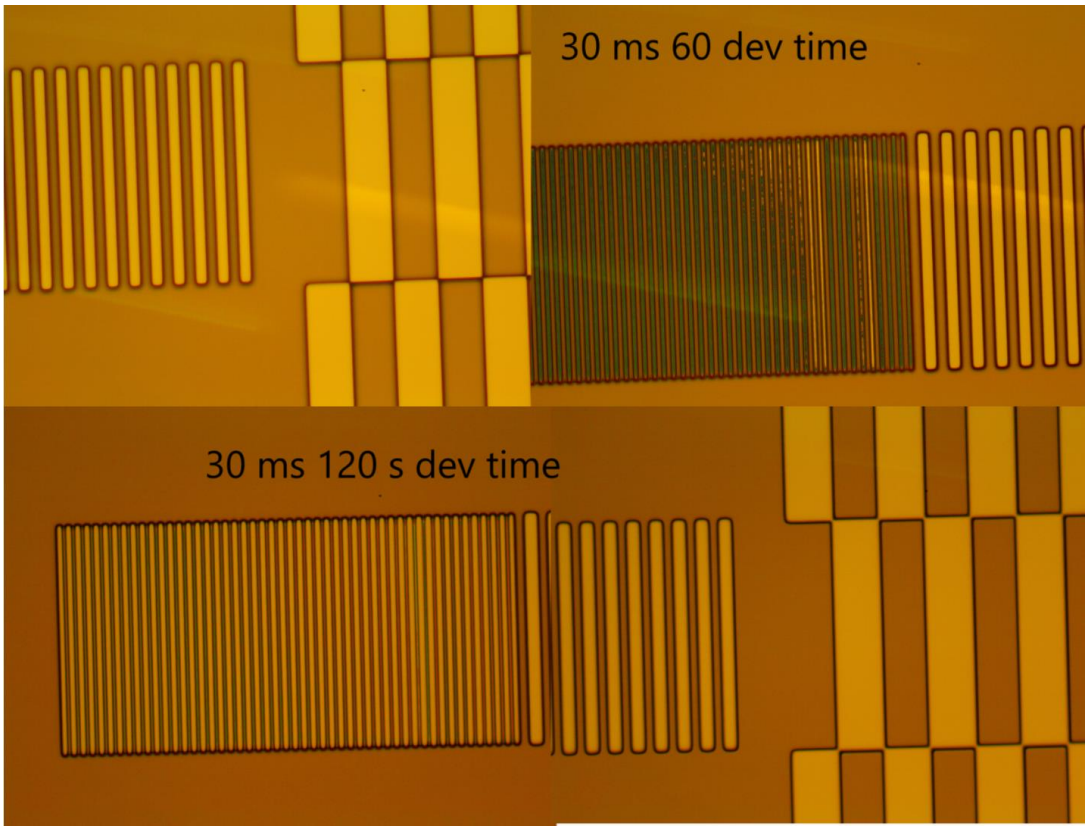

Figure 17 The three types of boxes are fully developed during different development time.

As depicted in Figure 17, longer exposure times lead to swift overdevelopment. It was observed that merely 30 seconds of development time caused the smallest boxes to blend into one large box.

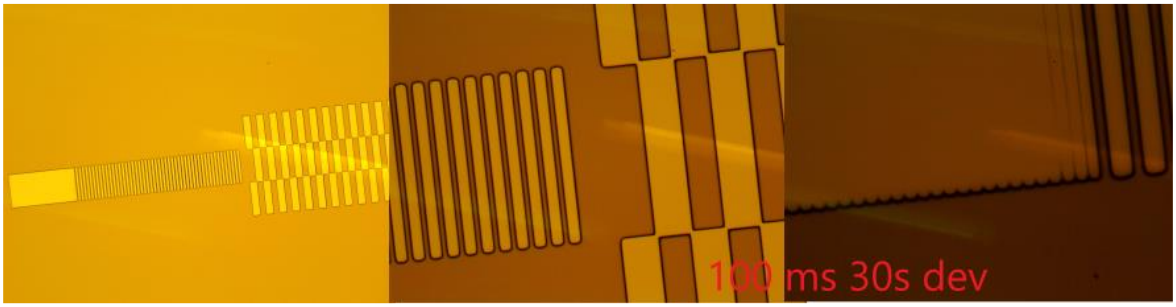

Figure 18 The exposed sample for 100 ms after 30s development time.

Upon examination using SEM, the pattern clarity was also found to be inadequate for 10 ms and 22 ms exposures with given development time, while 30 ms exposure offered clear patterns. The wall of the boxes has a wide angle of $\sim 120 - 130°$, as is shown on the Figure 18, which could be attributed to overdevelopment.

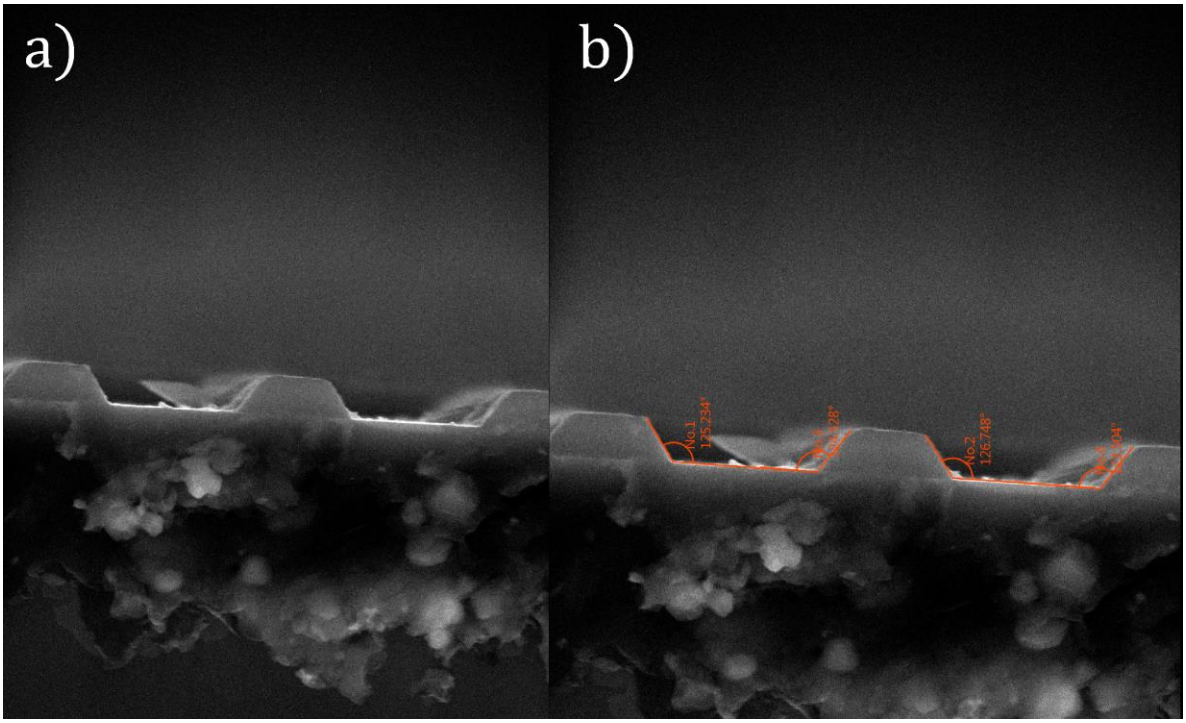

Figure 19 SEM cross section of a sample with 30 ms exposure and development time of 120 seconds. (Area B, 5 µm boxes)

In conclusion 30 ms exposure with development time between 60 and 120 min can be adequate for the given pattern dimensions. The less exposure time could be adequate if longer development time is used, given it is a Si wafer, and procedure is performed using named instruments and materials.

3.1.2 Lift of layer

Due to the wide high angle, shown on the Figure 19, it was concluded that a Lift-Off Layer (LOL) should be incorporated to aid the "lift off" process. The procedure was the same as in section 3.1.1, with two modifications: the substitution of the primer with a LOL-layer (PMGI SF8), and the substitution of the (MICROPROSIT s1813) with (MICROPROSIT 1805). Second change was done to improve compatibility with LOL layer. The same tests performed in 3.1.1, showed best expectation time at 15ms for this photoresist and the pattern dimension. In addition, an extra soft bake has been added after the LOL-layer had been spun into uniformity (190 ℃ for 90 s).

LOL layer resulted in an undercut beneath the photoresist, as demonstrated in Figure 20 a). SEM cross-sectional image, Figure 20 b), clearly depict the anticipated undercuts in the fabricated test sample.

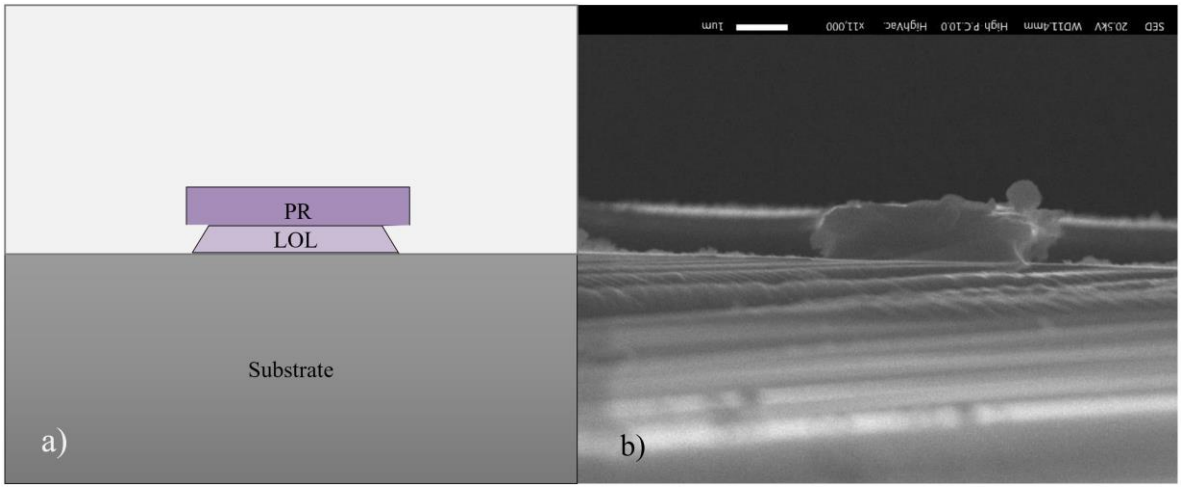

Figure 20 a) The schematic representation of the lift-off layer. b) The Scanning Electron Microscope (SEM) cross-sectional image, with the undercut created by the lift-off layer (exposure time 15 ms and development time 90 s).

3.1.3 Diode pattern & metallization

The next phase entailed applying the established fabrication procedure to the pattern, depicted in the Figure 21. Schottky pads of three varying dimensions were incorporated into the design. To mitigate the leakage current often associated with sharp edges [12] the Schottky pads' edges were designed with a rounded contour. Each diode dimension was conceived in two variations: with a protective guard ring and without one.

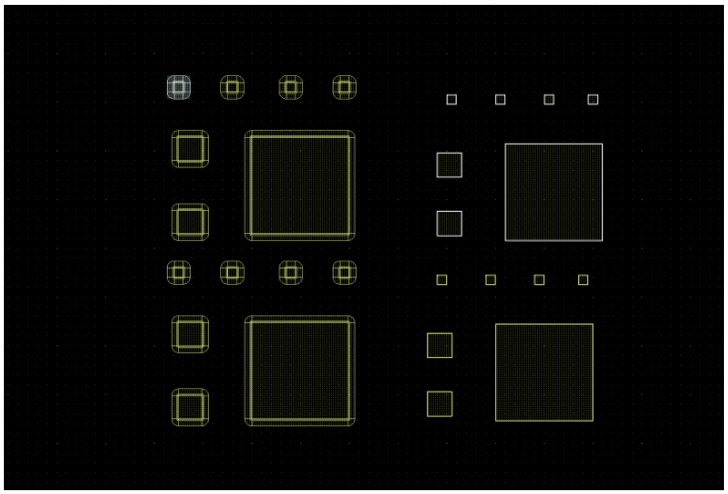

Figure 21 Big, medium and Small Schottky pad (drawn on Layout editor)

The exposure time and development was 15 ms and 90 seconds, respectively. Otherwise, the procedure remained the same with following additional steps for the metallization and lift-off:

1. After the wafer development, rinsing and drying, the wafer was put into E-beam PVD (Polyteknik Tornado 406E E-beam PVD system). Then, an aluminium layer of 110 nm thickness is deposited.

2. Lift-off: Wafer is then put into ultrasonic bath filled with acetone for approximately 10 min.

3. To remove the LOL-layered and resist residue, the wafer was put into developer solutions once more in the end of the procedure.

Figure 22 shows the resulting metallic patterns on silicon wafer. The pattern is clearly defined with sharp counters.

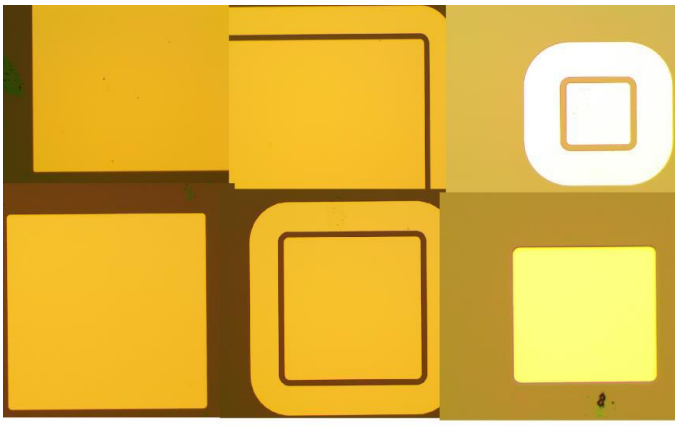

Figure 22 Schottky pads post metallization

3.2 Sample preparation

3.2.1 Fabrication of 4H-SiC Schottky diodes

The final fabrication procedure is shown schematically on Figure 23. The procedure was performed on a 1x1 cm SiC chip. The sample consisted of two epitaxial layers. The upper layer (Carbon face) was marked by manufacturer (CREE) to be 10um ($\pm 10\%$) wide, with doping concentration of $1 * 10^{16} cm^{-3} (\pm 25\%)$, while the substrate (the silicon face) had doping of $1 * 10^{18} cm^{-3} (\pm 25\%)$. The structure of the sample is depicted on the Figure 23(step 1).

The sample was first treated with standard RCA cleaning procedure [27]. This procedure consists of three steps. First step, designated to remove the organic contaminants, entailed mixing, and then heating up to 80 ℃ a mixture of deionized (DI) water, hydrogen peroxide (H_2O_2), and ammonia (NH_4OH), with the he solution ratio of 1:1:5. The sample was then held in the mixture for 10 min. After that it was rinsed in DI water for 5 min. The second step was incorporated to remove the native oxide. It involves dipping the SiC bit into a diluted (2%) hydrofluoric acid for 2 min. The sample is then rinsed once more time. The third step is designed to remove metallic ions and particles. It is essentially the same procedure as in the step one, except hydrochloric acid (*HCl*) is used instead of (NH_4OH). After the processing the wafer was rinsed and dried.

The lithography and lift off consisted of the same steps that are covered in sections 3.0.1, 3.1.2 and 3.1.3 with exposure time at 15 ms and increased development at 4 min (due to increase in pattern dimensions).

In addition, the metal deposited was nickel (Ni), not aluminium and the thickness was changed to 200 nm. Also, Hf dip was performed one more time directly before PVD, to remove the native oxide and ensure a direct metal on semiconductor contact. At first silver paste was applied for back contacts. The sample was characterized. Then, the paste was removed, and Al contacts were deposited on the backside. The Figure 23 presents overall procedure in a step-by-step schematic. The Figure 24 presents the finished Schottky diodes.

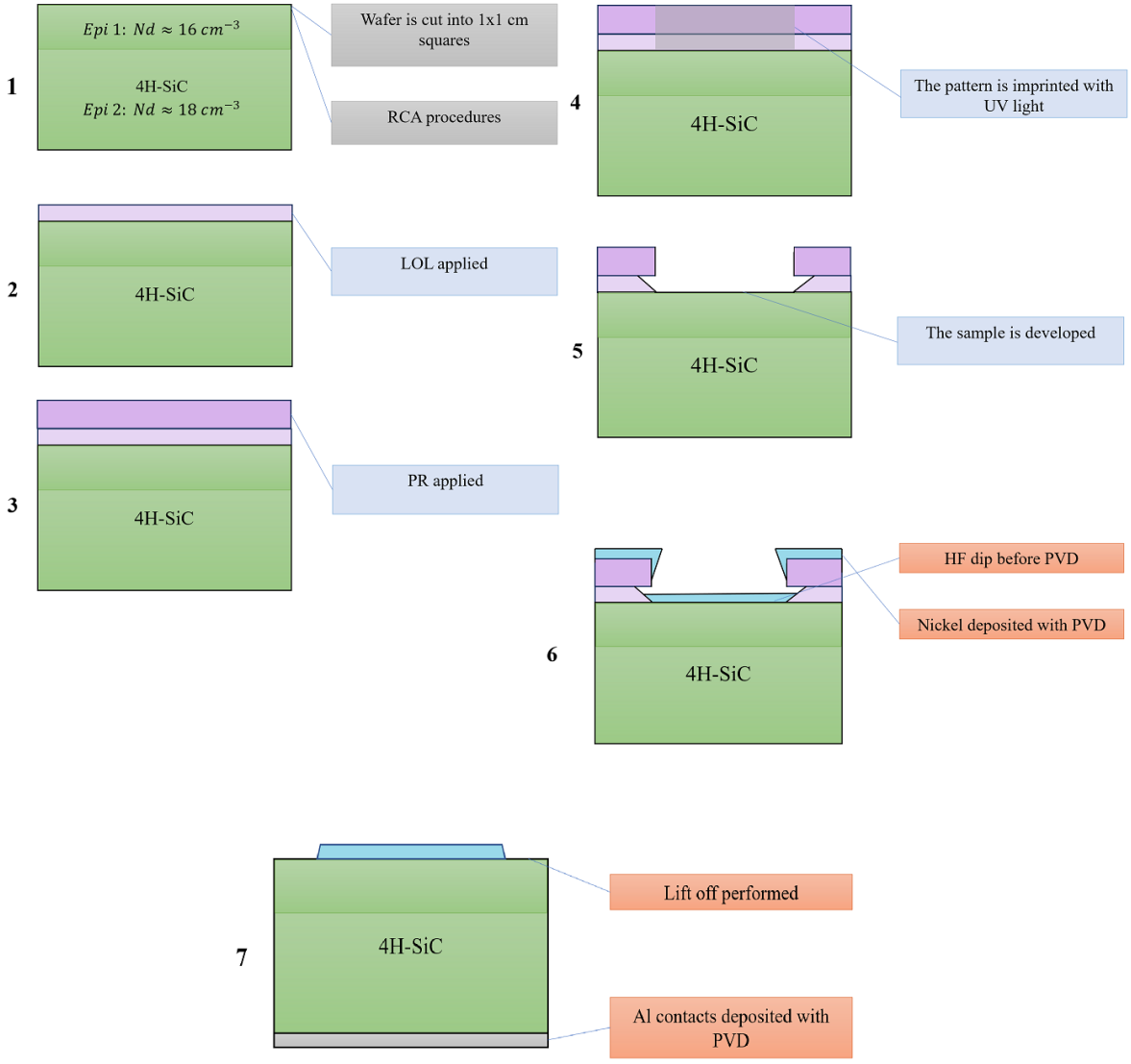

Figure 23 4H-SiC Schottky diode fabrication schematic.

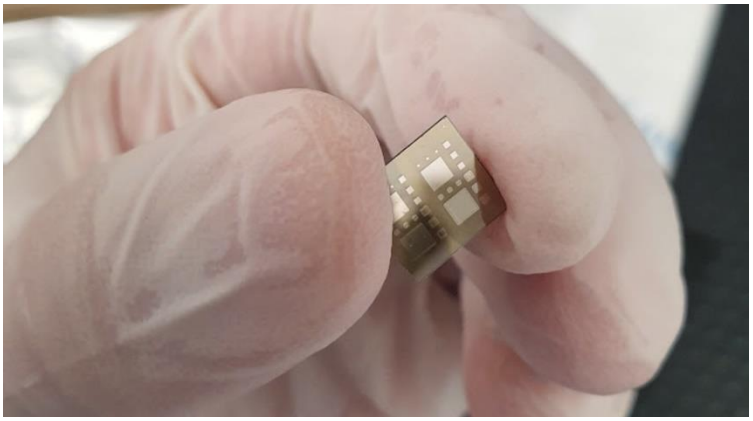

Figure 24 Picture of the final product.

3.2.2 Fabrication of 4H-SiC MOS diodes

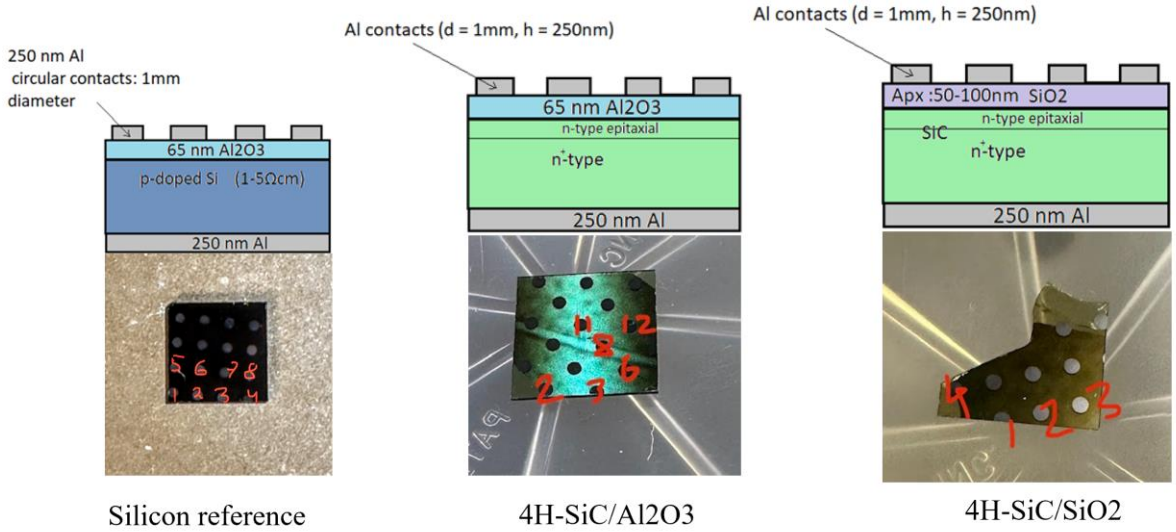

Figure 25 The schematic structure of MOS-capacitors (above). The picture of fabricated MOS (below).

As demonstrated in Figure 24, three MOS structures have been fabricated. The pair of structures on the right side showcases two different oxides on a SiC substrate. The first illustrates a silicon oxide (SiO_2) layer that has been thermally grown, while the second portrays an aluminium oxide (Al_2O_3) layer. Meanwhile, the image on the left provides a reference to silicon.

4H-SiC/ Al_2O_3

The SiC chips, each measuring 1x1 cm, were initially subjected to the RCA cleaning procedure as outlined in the previous section. Subsequently, a 250 am thick, Al contact was established on the backside using PVD. This was followed by deposition of a thin film of Al_2O_3 on the SiC substrate using Chemical Vapor Deposition (Al-CVD). This step was performed by Dr. Michael Getz, SINTEF. The resulting thickness film was approximately 65 nm. The final step in the process involved the utilization of a mask with 1 mm circular openings, permitting the creation of Al contacts atop the oxide layer via PVD. In addition, post the capacitance-voltage (CV) characterization, the samples were subjected to an annealing process in a tube furnace, maintaining a temperature of 432℃ in a forming gas (mixture of 5% H2 and 95% N2).

The silicon reference had exact same fabrication, except it was done on p-type silicon. The procedure shown on Figure 26.

4H-SiC/ SiO_2

The SiC chip was first rinsed in de-ionized water (DI) ultra-sonic bath. Then the samples were dipped in HF diluted solution (RCA: step 2). Then the sample was placed in alumina crucible and put in a tube furnace at 1300 ℃ for 1 hour in oxygen gas. After TO, during the extraction the sample broke into two pieces. One of the pieces is shown in the Figure 25. The next step consisted of removal of the oxide from the backside. This was done to apply backside contacts directly to the substrate. This process entailed application of primer (HDMS) and then photoresist (s1813) to the backside of the SiC piece and removal of the oxide from the backside with HF dip 2% that was performed in 3 min. Consequently, the photoresist was removed with acetone and backside was covered with 250 nm aluminium film via PVD. The schematic of the fabrication of two different MOS structures is depicted on the figure Figure 27

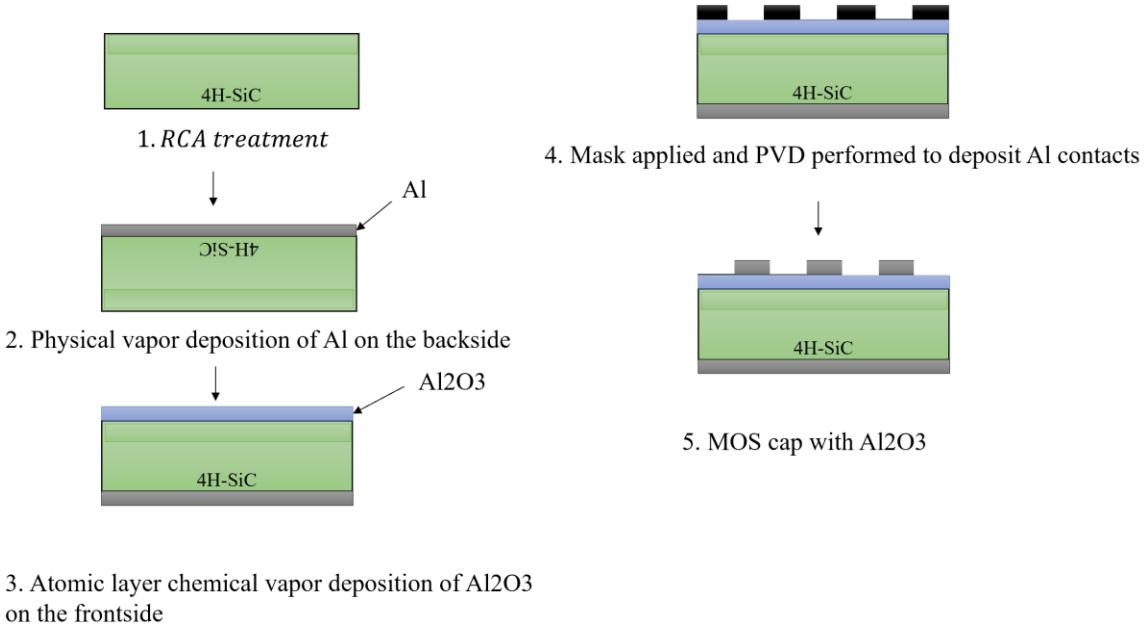

Figure 26 The schematic representation of Aluminium-Aluminium Oxide-Silicon Carbide MOS structure fabrication.

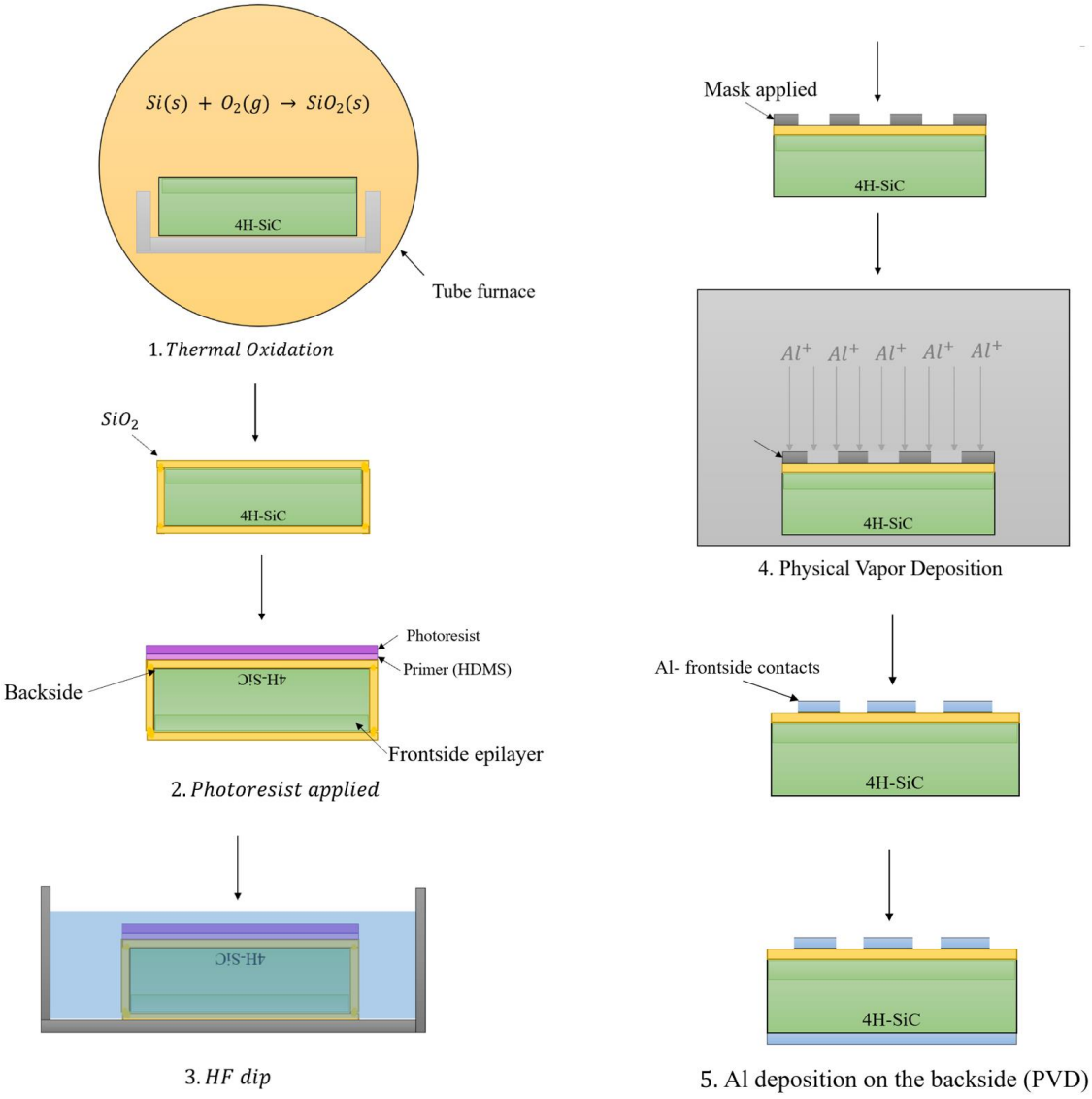

Figure 27 The schematic representation of Aluminium-Silicon Oxide-Silicon Carbide MOS structure fabrication.

Part IV Characterization results.

4.1 Current Voltage

Several diodes of each size were measured, using. The forward bias was measured with small voltage increment. The reverse bias was measured to breakdown with large voltage increment.

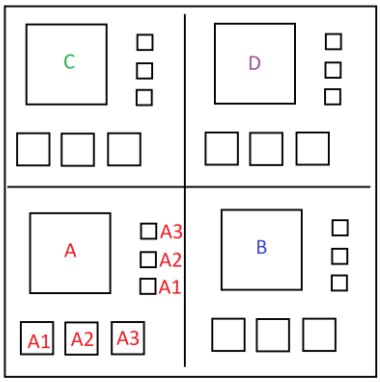

Figure 28 A schematic representation detailing the enumeration methodology used for the diodes.

The measurement was performed at the probe station in Mina Lab. To keep track, the samples were assigned number and a letter as it is shown on the Figure 28. The setup of the measurement is shown on figure. The measurements were performed at room temperature and closed lid on the setup shown on Figure 29.

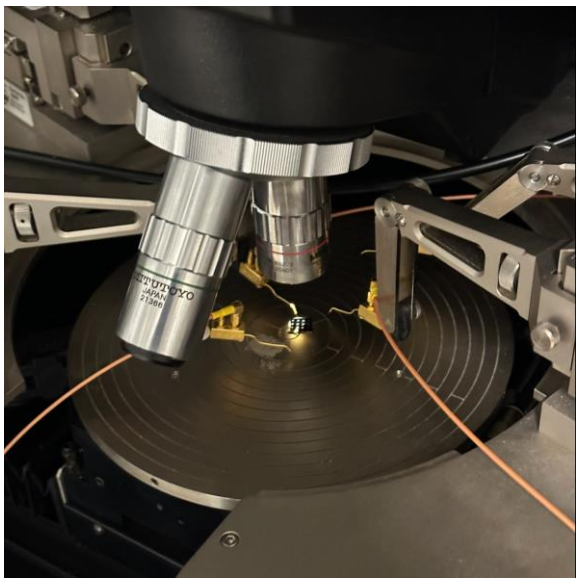

Figure 29 Picture shows the diode characterization setup at the Probe station (Minalab).

Forward Bias

The guard rings did not have noticeable effect on the forward bias. However, the decrease in size showed a general improvement in ideality factor (η) and decrease in the saturation current (I_s). The best 2000 µm diode had ideality factor η =1.58 and saturation current $I_s = 7.71 * 10^{-13}$, 500 µm measured $\eta = 1.58$ and $I_s = 2.07 * 10^{-13}$ and for 200 µm $I_s = 3.24E * 10^{-21}$. This tendency did also occur on the samples fabricated by Viktor Bobal as is showed on the Figure 30 (right). The parameters are extracted via linear regression from the region marked with red stripes. The measurements were performed on ammeter with detection limit lower than the saturation current.

This tendency might encompass the increased chance of the defect to interact with the junction with the increase of the diode area. The defects themselves can be structural defects in the material, the photoresists bits and/or other debris in between metal and semiconductor.

As is shown on the Figure 31, diode showed generally the same characteristics. Curves for 200A2 and 500A2 may stand out from the rest due to mistakes in the fabrication that either caused scratches on the resist/metal or something similar.

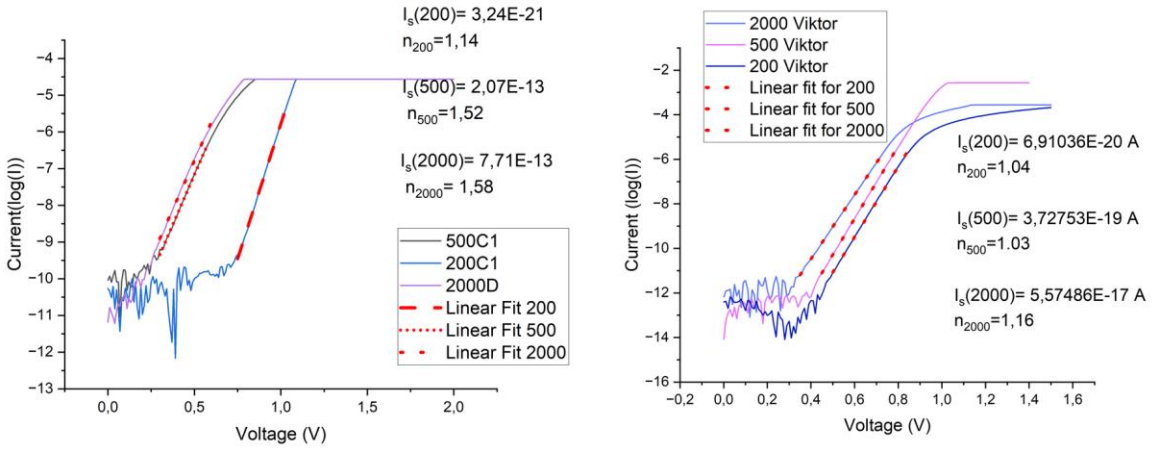

Figure 30 On the left are forward measurements performed on the different sizes. On the right measurements performed on the samples made by Viktor Bobal. The measurements were taken between 0V and 2V with (dV=0.01V) on the Keithley 6482. The reverse currents are so low on the right, due to instrument being run in another setup with better detection limit than on the left.

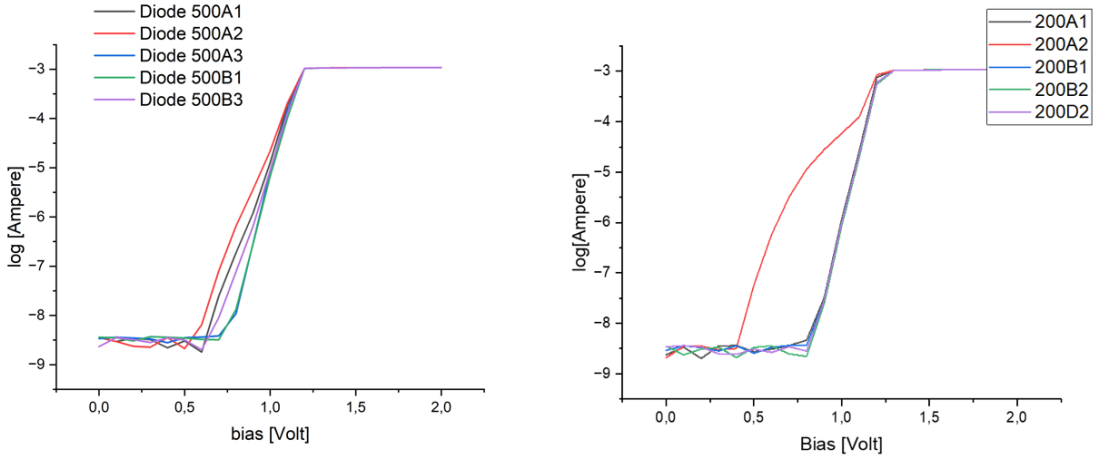

Figure 31 IV curves for multiple diodes.500 μm on the left and 200 μm on the right. Measurements were performed between 0 and 2V, with 0.1 V step. Instrumentation used: 6517B.

Reverse bias

The guard rings did not show any effect on the leakage current or the breakdown stability. The backside contacts, on the other hand, had a clear effect on the stability of the device after high reverse voltages. The silver paste (Ag) proved to decrease the quality of the Schottky device. As the Figure 32 may suggest, after breakdown the leakage current increase is higher for Ag paste contacts than for deposited Al contacts.

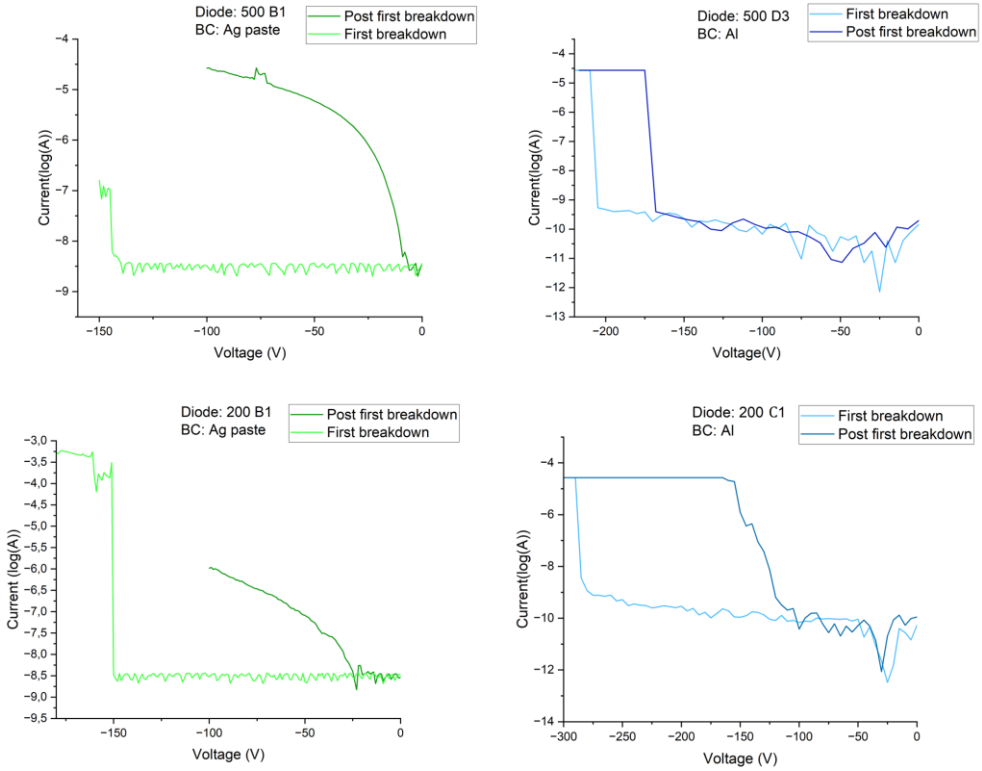

Figure 32 Thesis figure includes plots showcases Al vs Ag contacts after breakdown. Measurements performed on: Keithley 6487 for figures on the left and Keithley 6517B, note different detection limit.

After the first breakdown, the following breakdowns occurred at different voltages. They went up from about -300 V to around -150 V for the 200 µm pads, and from about -200 V to roughly -150 V for the 500 µm squares. This can be seen in Figure 33. It's worth noting that these later breakdowns stayed stable for both the 200 µm and 500 µm pads.

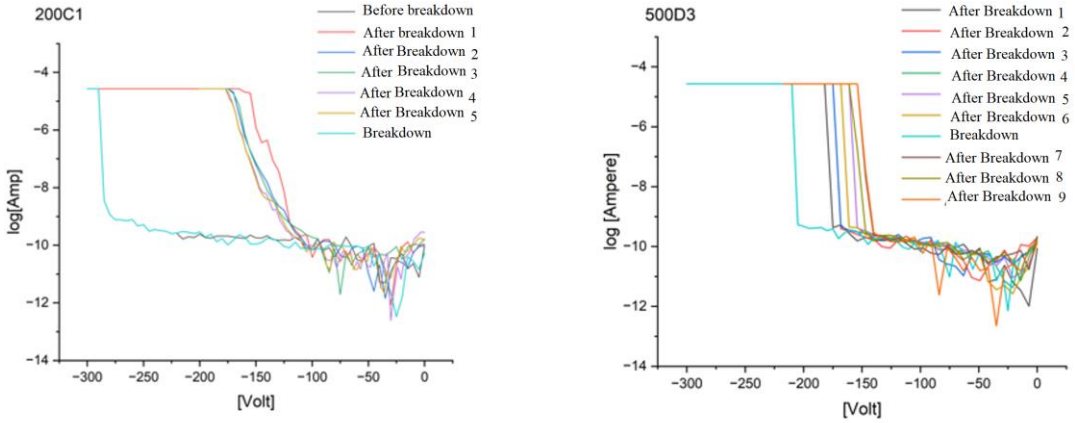

Figure 33 IV curves for 200-µm (left) and 500-µm (right). Diodes measured to several breakdowns. Measurements performed on Measurements performed on Keitley picoammeter 6487:

The devices fabricated by Viktor Bobal through a process displayed comparable breakdown characteristics, as illustrated in Figure 31. It's noteworthy that Viktor's devices generally demonstrated an improvement in breakdown values and exhibited marginally lower leakage currents in the low voltage region.

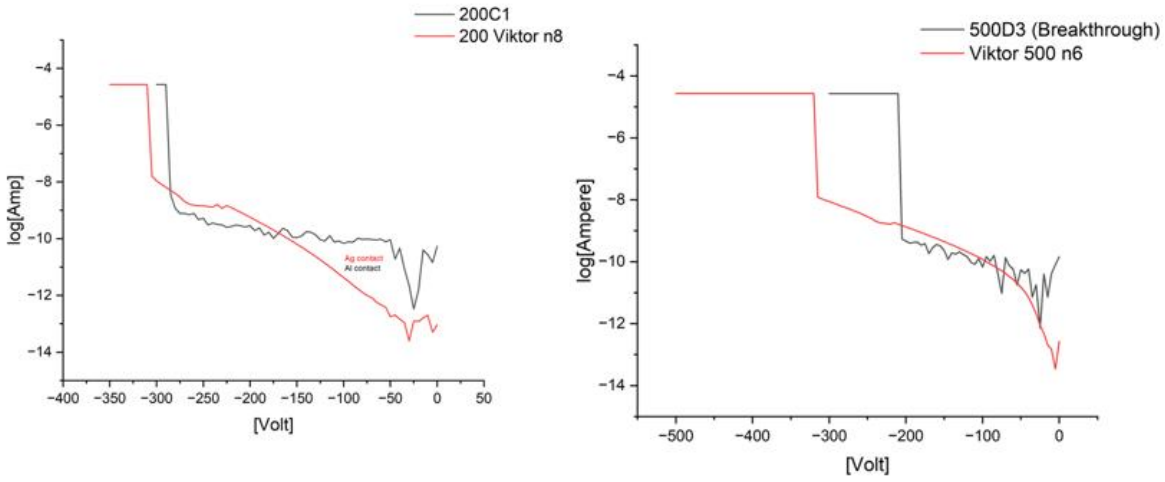

Figure 34 The plot compares the 200C and 500D to equivalent Schottky diodes made by Viktor Bobal. Measurements performed on Keitley picoammeter 6487:

The biggest pads appeared to be very sensitive to breakdown. After the first breakdown, all of them showed a considerable leakage current despite the deposition of aluminium

backside contacts. Even the cleaner diodes, produced by Viktor, exhibited the same behaviour, as it is shown on the Figure 35.

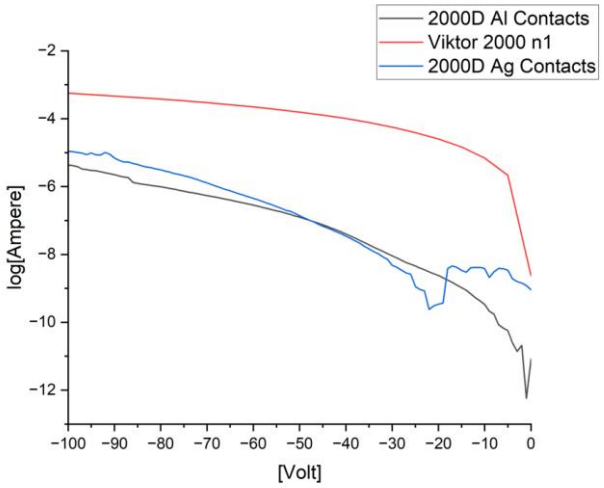

Figure 35 The reverse bias IV characteristics between 0V and 100V. The measurements are taken after initial breakdown. Measurements performed on Keitley picoammeter 6487.

4.2 Capacitance voltage results

The capacitance curves for voltages between 0 and -100V for different sizes are compared on the Figure 37. The capacitance decreases as the size of the diodes decreases, at 0 Volt diodes 2000 μm diodes have the capacitance of 1.2 nF, 500 μm has 70 pF and 200 μm has 10 pF. This observation confirms that the capacitance scales with the area of the diodes, as it should do.

To determine the built-in voltage, a linear regression analysis is performed for $1/C^2$ the region between 0 and -20 V. For the small diodes, the built-in voltage falls within the range of 1.61 to 1.66 V, while the medium-sized pads exhibit values around 1.51 V. The largest pads yield a built-in voltage of 0.44 V. In comparison to the theoretical value calculated as $(q(\Phi_m - \Phi_s) = 5.05\ eV - 3.35\ eV = 1.7\ eV)$ [3, 4], it is evident that the smallest diodes demonstrate the closest match to the theoretical value. This may indicate that larger area might encompass increased amount of microscopic clusters of metal-semiconductor phases or other similar effects that decrease the voltage barrier.

The Figure 33 displays the depletion width, as a function of bias deduced from CV measurements for 500 μm diodes. The curves suggest that at 100 V, the depletion width is

approximately 3 µm. Similarly, the doping concentration can be determined from the $1/C^2$ values for 2000D, which indicates a doping concentration of around $1.25 * 10^{16}\ cm^{-3}$ (with an uncertainty of ± 20%). This value closely aligns with the manufacturer's specified doping concentration.

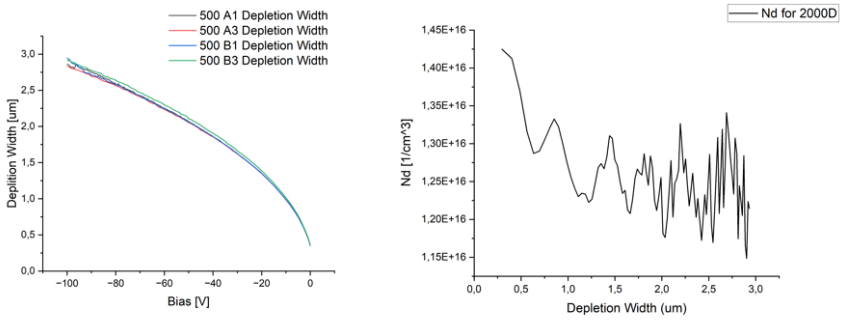

Figure 36 On the left: the depletion width as a function of bias, on the right: the doping concentration as the function of depletion width.

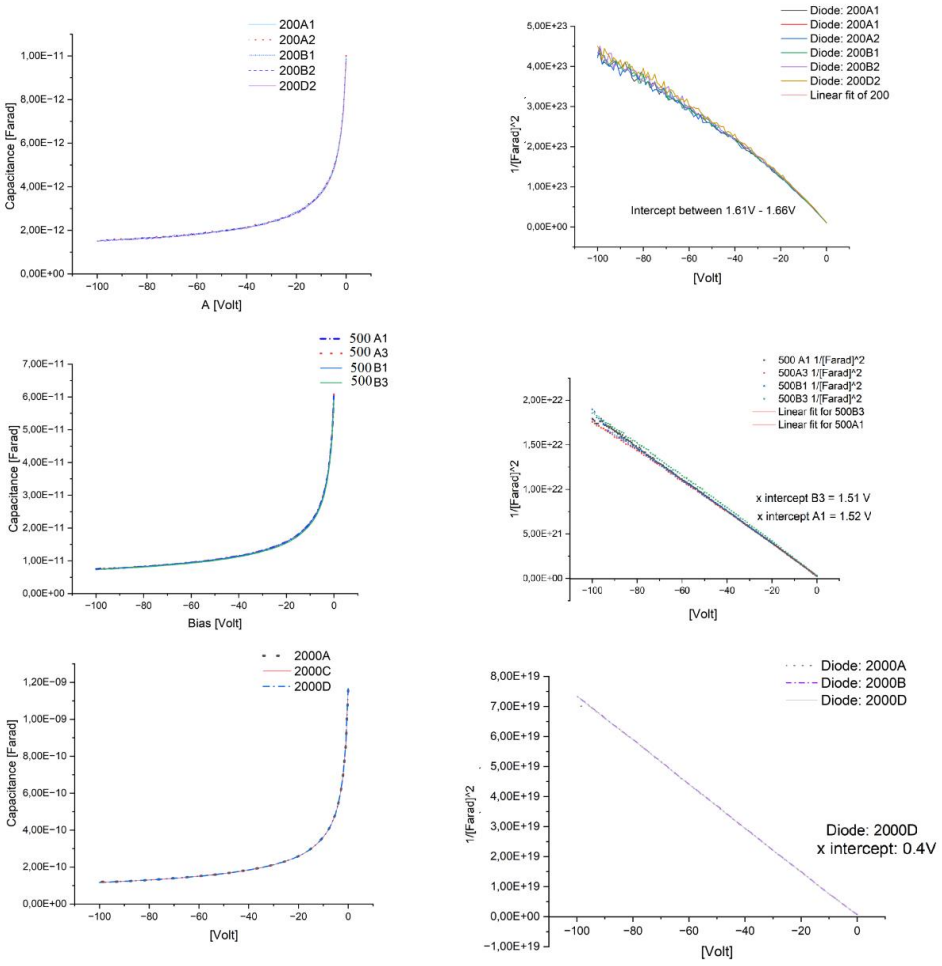

Figure 37 CV characterization curves for the three different sizes on the left and their 1/C^2 curves on the right. The linear regression is based on the region between 0 and 20 V. Measurements performed on: HP 4280 A

4.3 MOS

Silicon oxide

The Figure 38 presents MOS measurements for 3 different frequencies. The values are extracted from as an average from three different contacts. The Capacitance Voltage curves on the Figure 38 are measured for multiple contacts. They show a clear MOS shape, similar to Figure 13. The measurements were repeatable, which may be an indicator of good insulating properties. The table 2. depicts the data extracted from the samples n3, n5 and n7, depicted on Figure 38. The thickness of the silicon oxide, $t_{ox} = 80\ nm$, is extracted from the oxide capacitance, stored during the accumulation as $C_i = 337pF$. The work function difference is 0.77 eV. The threshold voltage, $V_{fb} = 4.28\ V$,may indicate the voltage at which the MOS device is in a neutral state with no charge carriers stored at either side of the oxide. The spread in the frequencies on the plots, may indicate the presence of defects at the interface surface, in the oxide or in the semiconductor.

Table 2 The table precents values extracted from the MOS curves. The data presented is average of samples: n3,n5 and n7

	$C_i(F)$	$t_{ox}(nm)$	$\Phi_{ms}(eV)$	$V_{fb}(V)$
$1MHz$	$3.36 * 10^{-10}$	81	0,78	4.83
$60\ kHz$	$3.23 * 10^{-10}$	84	0,77	4.28
1kHz	$3,37 * 10^{-10}$	80	0,77	4.28

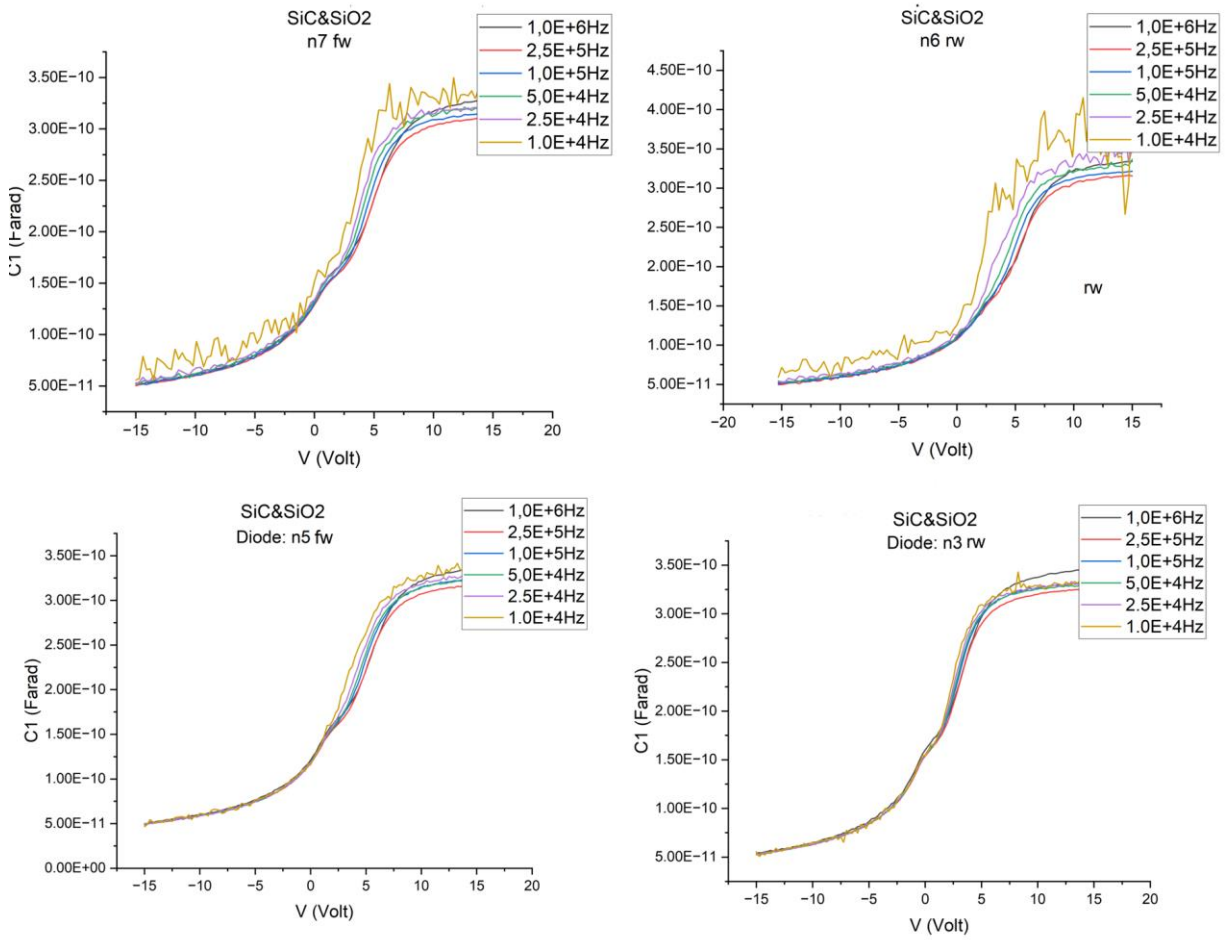

Figure 38 CV plots for SiO on SiC MOS. The figure shows four measurements on 4 separate samples. The capacitors on the left measured in forward, from -15V to 15V, the plots on the right was measured in reverse, from 15 to -15. The measurements were taken on the multifrequency CV- measurement equipment, model Agilent 4284A:

Aluminium oxide

Before annealing some measurements had some indication of MOS behavior first time they were measured, as Figure 39 suggests. However, the measurements were non-repeatable. In addition, the capacitance instrumentation limit of 40 V did not permit to measure the accumulation capacitance, which is supposed to be around $8.5 * 10^{-10}$ according to the accumulation capacitance measured on the reference, shown on Figure 40.

The annealing process for the reference sample notably reduced the quantity of impurities influencing the Metal-Oxide-Semiconductor (MOS), as evidenced by the reduction in the frequency spread,Figure 40. the annealing of Silicon Carbide (SiC) didn't enhance the ease of measurements or the quality of the resulting curves.

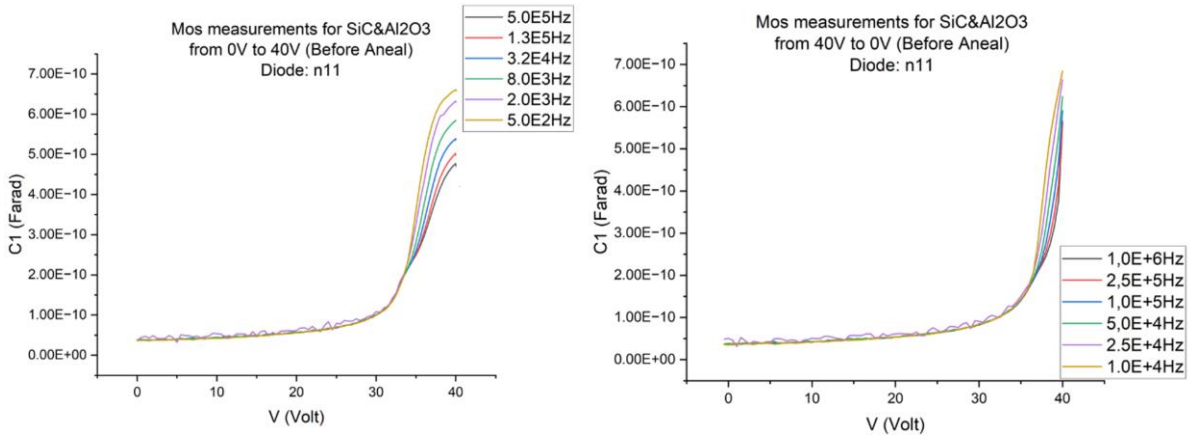

Figure 39 Two pre-anneal CV plots of MOS with Alumium Oxide (Al_2O_3) on SiC. On the right the measurement was taken from 0V to 40V. On the left the measurements was taken from 40V to 0V. Measurements performed on: 4284A

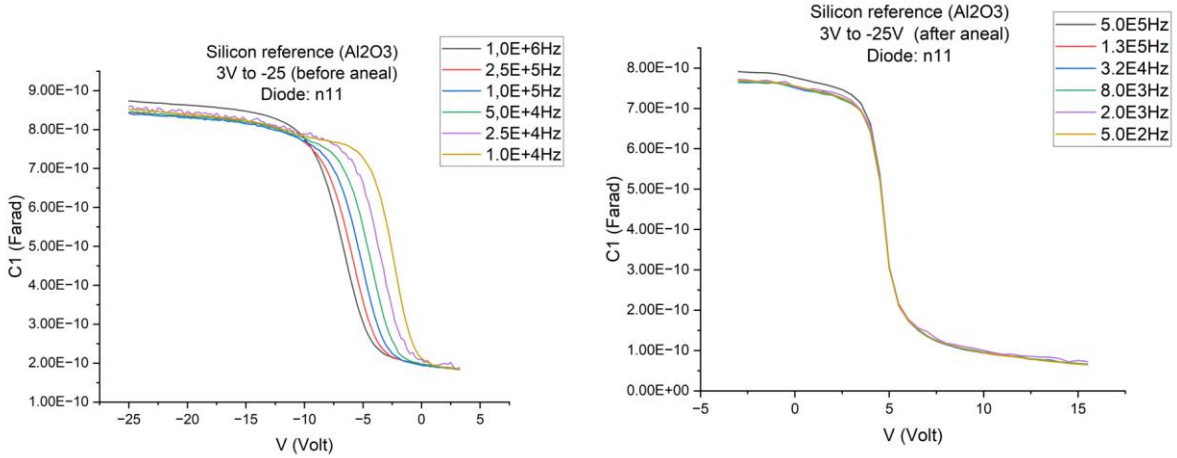

Figure 40 Pre anneal, and post anneal CV plots of MOS with Al_2O_3 on p-type Silicon. Measure on Agilent 4284A.

Part V Conclusion

A photolithography process has been developed for fabrication of Schottky diodes on n-type Silicon Carbide (*SiC*) diode. This process is based on the lift-off method. It involves using a so-called lift off layer (LOL) and a positive photoresist. The LOL and resist used were MICROPOSIT S1805 and PMGSF8, respectively. The photolithographic exposure was performed by Heidelberg μPG-501 Maskless Lithography aligner. The exposure time was tuned to be 15 ms with a development of approx. 4 min using MICROPOSIT MF-21A developer. The process was monitored with optical microscopy, and the resulting structures were examined with scanning electron microscopy (SEM) along the cross section. After the development of the lithography patterns, deposition of Ni with a thickness of around 250 nm was performed using e-beam evaporation. The lift-off step was carried out by submersing the samples in acetone in an ultra-sound bath, which resulted in removal of the resist. The samples were then submersed in the developer again in order to remove the remaining LOL. 1x1 cm^2 chips with multiple square shaped SiC diodes were fabricated with three dimensions: 200 μm, 500 μm and 1000 μm. Each size of the diodes was fabricated with and without guard-rings. The process can be scaled up for processing of entire wafers and large-scale fabrication of detectors.

The fabricated devices underwent characterization through Current-Voltage (IV) measurements and Capacitance-Voltage (CV). It is observed that the reverse-bias leakage current for most of the diodes is below the detection limit of the picoammeters used (< 25 pA, Keithley 6487). The reverse saturation current was thus deduced from the fitting of the diode equation to the measurements for the forward bias. The saturation current is found to vary between ($3.24E*10^{-21}\ A$) and ($7.71*10^{-13}\ A$). The ideality factors vary from (η =1.14) to (η =1.58). Normally, the breakdown for the as-fabricated diodes occurred at 250-350 V for 200 μm, 150-250 V for 500 μm and less than 100 V for 2000 μm. After the first breakdown, the properties of the diodes deteriorate: the leakage current increases and the breakdown voltage decreases. Both silver paste and a PVD-deposited Al layer were tested as the back-side contacts, with the latter demonstrating improved stability of the measurements.

The CV measurements have revealed the doping concentration in the epi-layer to be 1.2 - 1.3*$10^{16}\ cm^{-3}$. The depletion width at 100 V is deduced to be around 3 μm. The built-in voltage is found to be 0.41 V for 2000 μm, 1.5 V for 500 μm and 1.6 V for 200 μm, where the latter is comparable with a theoretic value of 1.7 V [3, 4]. Generally, we have observed

that the smaller diode demonstrates better properties with respect to breakdown voltage, ideality factor, build-in voltage etc.

For the sake of future device improvements, preliminary tests of two different oxides were performed: silicon oxide (SiO_2) thermally grown with dry oxidation in O_2 atmosphere (TO), and aluminium oxide (Al_2O_3) deposited with atomic layer deposition (ALD). Oxide characterization was performed by CV measurements of the metal-oxide-semiconductor (MOS) structures, where Al was used as the metal layer. The thermal oxide proved to have good insulating qualities, as the CV plots showed dependencies expected for MOS. The oxide thickness, deduced from the plot, is 80-85 nm (TO with O_2 gas for 1h at 1300 ℃). Based on three different contacts, the average flat band voltage (V_{fb}) was measured to be 4.28 V at 1 kHz and 4.83 V for 1 MHz. The average work function difference between Al and the semiconductor (Φ_{ms}) is estimated as 0.77. The CV curves for Al_2O_3 showed some indication of MOS shape with increase in capacitance at around 30 V. However, the measurements were not repeatable, and the results on Al_2O_3 layer were inconclusive.

5.1 Future work

The reported study has identified several issues that can be addressed in future studies.

Firstly, the poor diode characteristics of the larger diodes. It can be suggested that the reason is surface imperfections in the SiC epi-layer or dust particles from poor sample handling. As the diode size increases, there is a higher probability of a surface imperfection or a dust particle to occur between SiC and the metal, which will be detrimental for the Schottky diode.

Secondly, the degradation of the diodes after the breakdown or exposure to high current. One hypothesis can be that the diode experiences heating due to high current density. This can cause chemical reaction between SiC and Ni that is known to easily form nickel silicides. One can propose using Ti/Ni layers for Schottky diodes, where 5-10 nm of Ti is deposited on SiC prior to Ni deposition. Preliminary test with Ti/Ni layers, performed by Viktor Bobal and researchers at SINTEF, have indicated improvement in the stability of the diodes. However, more systematic studies are needed.

Thirdly, the studies of Al_2O_3 on SiC should be performed more detailed and systematically. One should investigate the effect of annealing in different atmospheres and at different temperatures.

References

[1] S.A. Campbell, Fabrication engineering at the micro- and nanoscale, Fourth edition. ed., Oxford University Press, New York, 2013.
[2] B.G. Streetman, Solid state electronic devices, 6th ed., Pearson/Prentice-Hall, Upper Saddle River, N.J, 2006.
[3] A.B. Cardwell, Photoelectric and Thermionic Properties of Nickel, Physical Review 76 (1949) 125-127.
[4] H.-K. Kim, S.I. Kim, S. Kim, N.-S. Lee, H.-K. Shin, C.W. Lee, Relation between work function and structural properties of triangular defects in 4H-SiC epitaxial layer: Kelvin probe force microscopic and spectroscopic analyses, Nanoscale 12 (2020) 8216-8229.
[5] G. Lutz, R. Klanner, Solid State Detectors, 2020, pp. 137-200.
[6] M. Hodgson, A. Lohstroh, P. Sellin, D. Thomas, Characterization of silicon carbide and diamond detectors for neutron applications, Measurement science & technology 28 (2017) 105501.
[7] S. Metzger, H. Henschel, O. Kohn, W. Lennartz, Silicon carbide radiation detector for harsh environments, IEEE transactions on nuclear science 49 (2002) 1351-1355.
[8] M.D. Napoli, SiC detectors: A review on the use of silicon carbide as radiation detection material, Frontiers in physics 10 (2022).
[9] F. Nava, G. Bertuccio, A. Cavallini, E. Vittone, Silicon carbide and its use as a radiation detector material, Measurement science & technology 19 (2008) 102001-102001 (102025).
[10] P.J. Sellin, J. Vaitkus, New materials for radiation hard semiconductor dectectors, Nuclear instruments & methods in physics research. Section A, Accelerators, spectrometers, detectors and associated equipment 557 (2006) 479-489.
[11] D.J. Griffiths, Introduction to quantum mechanics, Third edition. ed., Cambridge University Press, Cambridge, 2018.
[12] S.M. Sze, Physics of semiconductor devices, 3rd ed., Wiley-Interscience, Hoboken, N.J, 2007.
[13] K. Washio, SiGe HBT and BiCMOS technologies for optical transmission and wireless communication systems, IEEE Transactions on Electron Devices 50 (2003) 656-668.
[14] X. Wang, J. Zhao, Z. Xu, F. Djurabekova, M. Rommel, Y. Song, F. Fang, Density functional theory calculation of the properties of carbon vacancy defects in silicon carbide, Na mi ji shu yu jing mi gong cheng 3 (2020) 211-217.
[15] F. Bechstedt, J. Furthmüller, M. Ferhat, L.K. Teles, L.M.R. Scolfaro, J.R. Leite, V.Y. Davydov, O. Ambacher, R. Goldhahn, Energy gap and optical properties of InxGa1-xN, phys. stat. sol. (a) 195 (2003) 628-633.
[16] S.M. Sze, Physics of semiconductor devices, 2nd ed., Wiley, New York, 1981.
[17] W. Zhou, Nanoimprint Lithography: An Enabling Process for Nanofabrication, Springer Berlin Heidelberg : Imprint: Springer, Berlin, Heidelberg, 2013.
[18] M.E. Walsh, F. Zhang, R. Menon, H.I. Smith, 6 - Maskless photolithography, in: M. Feldman (Ed.), Nanolithography, Woodhead Publishing2014, pp. 179-193.
[19] D.M. Mattox, Handbook of physical vapor deposition (PVD) processing, Elsevier, Amsterdam, 2010, pp. 2-4.
[20] T. Iida, Y. Kita, I. Katayama, T. Tanaka, H. Okano, Equation for the vapor pressure of liquid metals and calculation of their enthalpies of evaporation, High temperature materials and processes 10 (1992) 199-207.

[21] R. Glang, L.I. Maissel, Handbook of thin film technology, McGraw-Hill, New York, 1970.
[22] L. Holland, Vacuum deposition of thin films, Chapman and Hall, London, 1956.
[23] A. Suzuki, H. Ashida, N. Furui, K. Mameno, H. Matsunami, THERMAL OXIDATION OF SIC AND ELECTRICAL PROPERTIES OF AL-SIO//2-SIC MOS STRUCTURE, Japanese Journal of Applied Physics 21 (1982) 579-585.
[24] J.K. Srivastava, M. Prasad, J.B. Wagner, Electrical Conductivity of Silicon Dioxide Thermally Grown on Silicon, Journal of The Electrochemical Society 132 (1985) 955.
[25] F. Roccaforte, F. La Via, V. Raineri, R. Pierobon, E. Zanoni, Richardson's constant in inhomogeneous silicon carbide Schottky contacts, Journal of applied physics 93 (2003) 9137-9144.
[26] S.E. Zhao, R. Jiang, E.X. Zhang, W. Liao, C. Liang, D.M. Fleetwood, p. zhao, R.A. Reed, D. Linten, J. Mitard, N. Collaert, S. Sioncke, N. Waldron, Capacitance–Frequency Estimates of Border-Trap Densities in Multifin MOS Capacitors, IEEE Transactions on Nuclear Science 65 (2018) 175-183.
[27] W. Kern, The Evolution of Silicon Wafer Cleaning Technology, Journal of The Electrochemical Society 137 (1990) 1887.