Designing Analog to Digital Converter for a multi-needle Langmuir-probe

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Abstract

Langmuir probes are used to measure electron densities in plasma and are deployed on research satellites, generating data for space weather monitoring and prediction services. This information, providing e.g., warning of approaching solar storms, is critical for the management of satellite communication networks, global positioning systems, and power grids.

This thesis describes the design of a multiplexed 14-bit Analog to Digital Converter (ADC) capable of operating at 20 kilo samples per second and intended for use in a Langmuir probe data acquisition system. The delta-sigma architecture chosen for this work is discussed in the context of the pros and cons of different types of ADCs. Cadence software was used for the design and simulation of the modulator, details of which are presented together with measurements from a prototype Application Specific Integrated Circuit (ASIC) assembled on a custom Printed Circuit Board (PCB), using a Field Programmable Gate Array (FPGA) for input/output logic.

Cadence simulations are compared with physical device measurements, and recommendations made for future improvements to the design.

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Acronyms

$\Delta\Sigma$ Delta Sigma.

ADC Analog to Digital Converter.

CMFB Common Mode Feedback.

CMOS Complementary Metal-Oxide Semiconductor.

CT Continuous time.

DAC Digital to Analog Converter.

DNL Differential Nonlinearity.

DRC Design Rule Check.

DSM Delta Sigma Modulator.

DT Discrete time.

ENOB Effective Number of Bits.

FFT Fast Fourier Transformation.

INL Integral Nonlinearity.

LSB Least significant bit.

LVS Layout Versus Schematic.

MDAC Multiplying digital to analog converter.

OPAMP Operational amplifier.

OSR Over-Sampling Ratio.

PCB Printed Circuit Board.

S/H Sample-and-hold.

SAR Successive Approximation.

SNDR Signal to Noise and distortion Ratio.

SNR Signal to Noise Ratio.

SQNR Signal-to-Quantization-Noise Ratio.

TSMC Taiwan Semiconductor Manufacturing Company.

UGF Unity Gain frequency.

Chapter 1

Introduction

Space weather can cause disturbances in communication and navigation devices which will lead to problems in air traffic and transpolar flights. The multi-needle Langmuir probe is designed for high resolution measurements of electron density in plasma clouds which can help forecast space weather [2]. The fig. 1.1 is showing a use of the Multi-needle Langmuir probe. This thesis will design an Analog to Digital Converter (ADC) with a 14 bit resolution for this application.

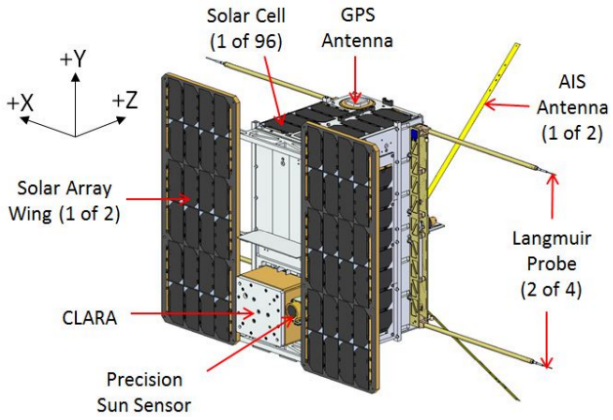

Figure 1.1: Schematic drawing of the Nor-Sat-1 satelite which uses four Langmuir probes [9]

1.1 Motivation

For 13 years the University of Oslo has developed a new Langmuir probe system with high resolution to measure electron density. The system consists of four cylindrical probes and this is where the Multi-needle Langmuir probe name comes from [2].

This system has been tested on six sounding rockets from 2003-2012 and there are more missions comming in the future where the Langmuir probe will be used. The advantage of the Multi-needle Langmuir probe is the high sample rate and the on-board processing of electron density with low computational power requirements [2]. To read this data the ADC will be integrated to this project which is the reasoning for the high resolution of 14 bits and the sample speed of (20kS/s)$\times$4 or 80 kS/s, which comes from the four Langmuir sensors with a multiplexing system.

1.2 Objective

The objective for this thesis is deciding what topology to use for the ADC in the Multi-needle Langmuir probe shown in the block diagram fig. 1.2, and designing this ADC. The ADC should have a 14 bit resolution with a sample speed of either 20kS/s$\times$4 or 80 kS/s. Making a schematic, simulations, layout and post layout simulation will be done in the program Cadence which also has more useful tools. This will ensure that the final product will work as intended, but this will also be tested physically on chip to verify that the ADC works as intended. To make a good testbench, a Printed Circuit Board will be designed and made with the combination of a FPGA which can be programmed to do different type of tests.

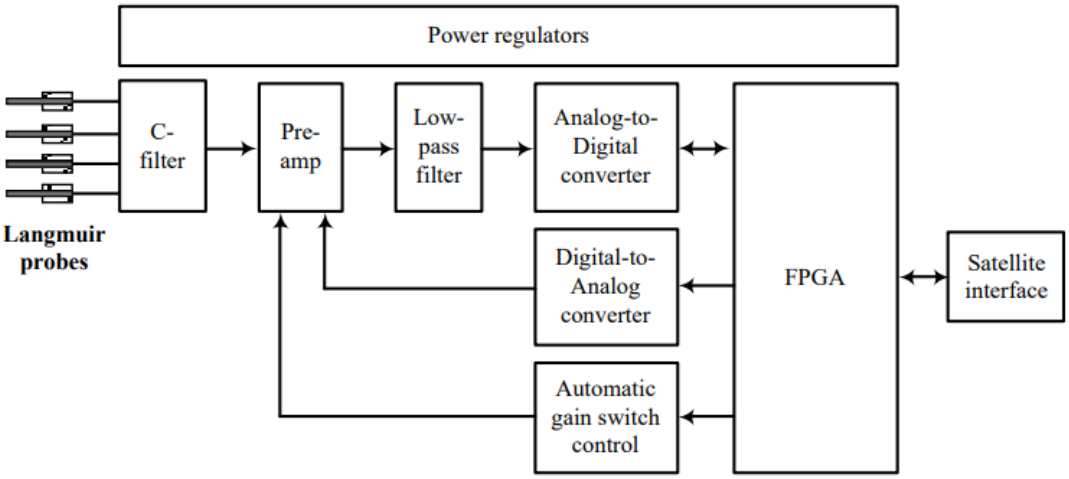

Figure 1.2: Electronic block diagram of the Multi-needle Langmuir probe instrument [9]

1.3 Thesis outline

Given below are an overview of the thesis's structure and contents:

- **Chapter 2: Analog to Digital converters** looks into the different topologies for analog to digital converters and looks into the working process of different structures and goes in detail about pros and cons.
- **Chapter 3: Delta Sigma Modulator** will go into detail about the chosen topology and describe how each component is designed and put together to meet the specifications.
- **Chapter 4: Results** Will look at the final simulation and chip results. Go into some detail how it was tested, discuss the results and compare chip vs simulation results.
- **Chapter 5: Discussion and future work** is where different topics are discussed to possibly improve the design and some future work.
- **Chapter 6: Conclusion** Is a conclusion of all the work done in this thesis.

Chapter 2

Analog to Digital converters

There are multiple Analog to Digital converters topologies. However there are a few which cover a big spectrum: Flash, Successive Approximation (SAR), Delta Sigma Modulator ($\Delta\Sigma$) and pipeline ADC's. Therefore, a basic understanding of these four will help to be able to choose the right ADC topology for its respective assignment [16]. As the name suggests, an Analog to Digital Converter converts an analog value which varies among a theoretically infinite number of values, to a digital value which has a finite number of values [18].

2.1 Flash ADC

Flash ADC is the fastest way to convert analog to digital with a large bandwidth. The downside to the flash ADC is the large power consumption, and the area used doubles for each bit added. It will need a 2^n comparators which are connected in parallel also shown in fig. 2.1. Because of these downsides, the application of the flash ADC is usually in satellite communication, radar processing, sampling oscilloscopes, and high-density disk drives [24].

From fig. 2.1 there is a resistive divider with 2^n resistors where the first and last resistor are R/2 to create a 0.5 Least significant bit (LSB) offset. The input of the positive node of the first comparator will be $V_{ref} - \frac{V_R}{2}$, the next one will be $V_{ref} - \frac{V_R}{2} - V_R$, the next is $V_{ref} - \frac{V_R}{2} - 2V_R$, and so on untill the last one $V_{ref} - \frac{V_R}{2} - 7V_R$. The input voltage will be subtracted from this value: $Vcomp^+ - V_{in}$, if the positive is higher than the negative $Vcomp^+ - V_{in} > 0$ the comparator will give a logic '1'. The comparator output is then connected to two NAND gates, all the NAND gates will output a logic '1', but where the bit order goes from '1' to '0' the NAND gate will output a logic '0' which can be used for error correction. Finally the encoder will convert $2^N - 1$ bit to N digital outputs [5, Chapter 17.5].

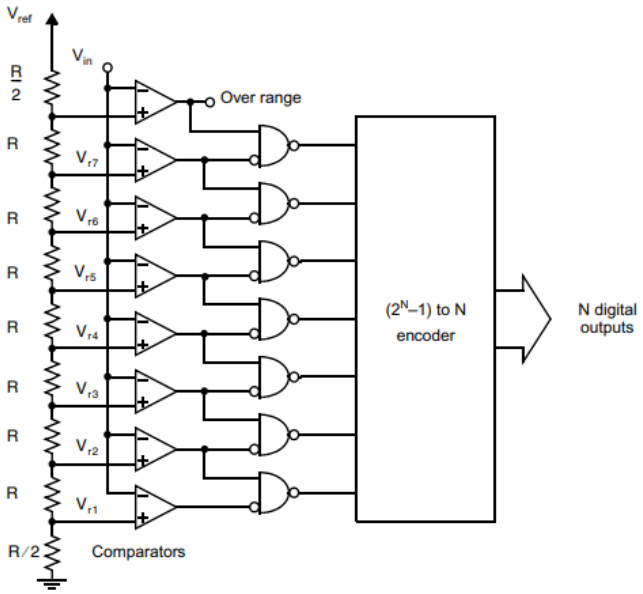

Figure 2.1: A 3 bit flash ADC [5, fig.17.24]

2.2 Successive Approximation ADC

SAR ADC is one of the most popular ADC choice due to their versatility. The SAR ADC has a modest circuit complexity which uses relatively low power. It can be made using switching capacitors, a comparator and some digital circuits. One of its few negatives is that it uses N clock cycles to complete an N-bit conversion [5, p.652].

The name Successive Approximation ADC comes from the working method of the ADC, as it suggests it takes a value in which the answer is higher or lower giving a logic '1' if it is higher and a logic '0' if it is lower. After guessing correctly you end up with the right ammount of 1's and 0's. Figure 2.2 shows how the algorithm works.

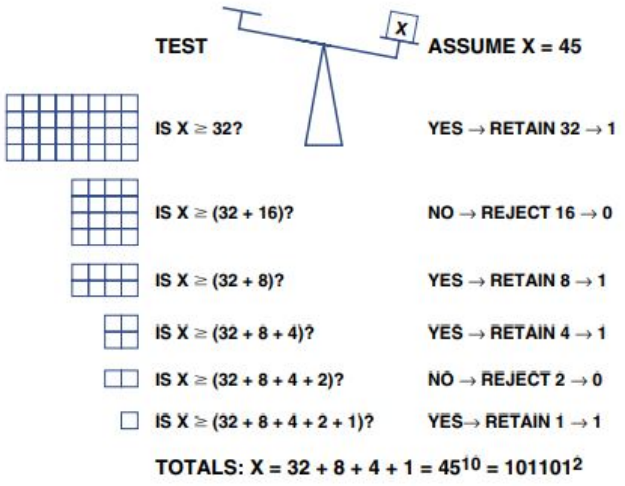

Figure 2.2: Successive-approximation ADC algorithm [16]

The block diagram for the SAR ADC is shown in fig. 2.3, it contains a Sample-and-hold circuit(S/H, or SHA in fig. 2.3), a comparator, a DAC, a timer and a register. The input goes in the S/H circuit to keep the signal constant during the conversion cycle. The comparator gives either a 0 or a 1 comparing the S/H output with the DAC, then the 0 or 1 is stored in the register. The DAC is then calibrated depending if the last bit was either a 1 or a 0 and this process repeats until all the bits are stored in the register which is at the end of the conversion process with a logic "DONE" signal. The timing diagram for this simplified process is shown in fig. 2.4 [16].

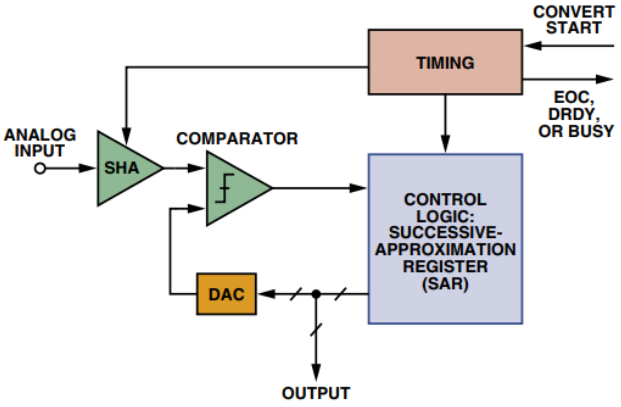

Figure 2.3: Basic successive-approximation ADC block diagram [16]

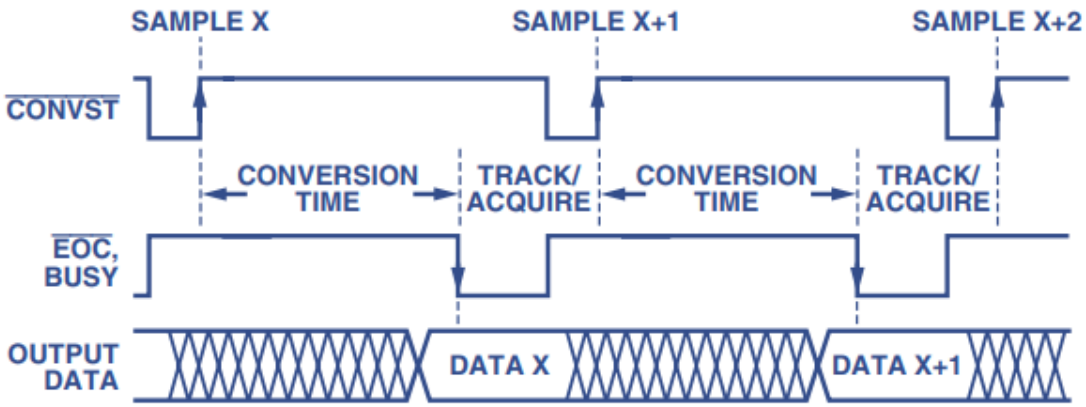

Figure 2.4: Simplified timing diagram for the SAR ADC [16]

2.3 Delta Sigma ADC

Today's Delta Sigma (ΔΣ) ADCs is used when high resolution is needed and uses oversampling to achieve this. The working principle of the ΔΣ ADC is oversampling, noise shaping and filtering. The signal is passed through a low pass filter, while the noise is moved to a higher frequency with a high pass filter. There, the high pass filtered noise can be easily removed, this will yield a high Signal to Noise (SNR) ratio within the sample frequency which again gives a high bit resolution [16].

The output of the ΔΣ modulator is a bit stream of 1's and 0's where the average of the bit stream is proportional to the DC value of the input signal [16].

The ΔΣ modulator can be built with a summing node, an integrator, comparator and a Digital to Analog converter as shown in figure 2.5.

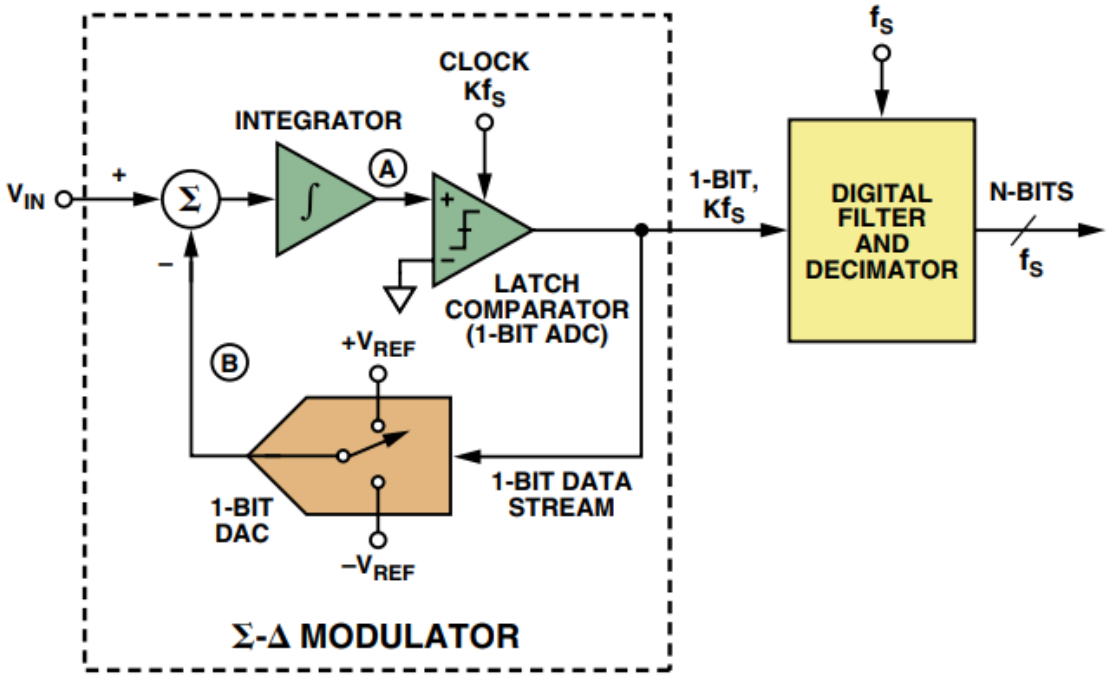

Figure 2.5: Basic first order Delta Sigma ADC [16]

In fig. 2.6 the noise spectrum is illustrated using oversampling, decimation and noise shaping. Figure A is the usual Nyquist sampling where all the quantization noise is uniformly spread within dc and $f_s/2$. Figure B is with oversampling where sample frequency is K times f_s, a decimation and a digital filter. With this the bandwidth for the signal is remaining the same, but the noise is now evenly spread withing DC and Kf_s. Figure C contains oversampling, decimation, digital filtering and noise shaping. The noise is now not evenly spread, but rather shaped so the noise is mostly in higher frequency [16].

The explanation so far is all first order delta-sigma where there is only one summing node and one integrator, however to get a better noise shaping and SNR, a higher order $\Delta\Sigma$ can be implemented. Usually a second order is used due to that any higher order than three can be difficult to stabilize. The difference in the noise shape of first and second order is shown in fig. 2.7 [16]. The noise transfer function for n^{th} order $\Delta\Sigma$ [19]:

$$NTF(Z) = (1 - Z^{-1})^n \tag{2.1}$$

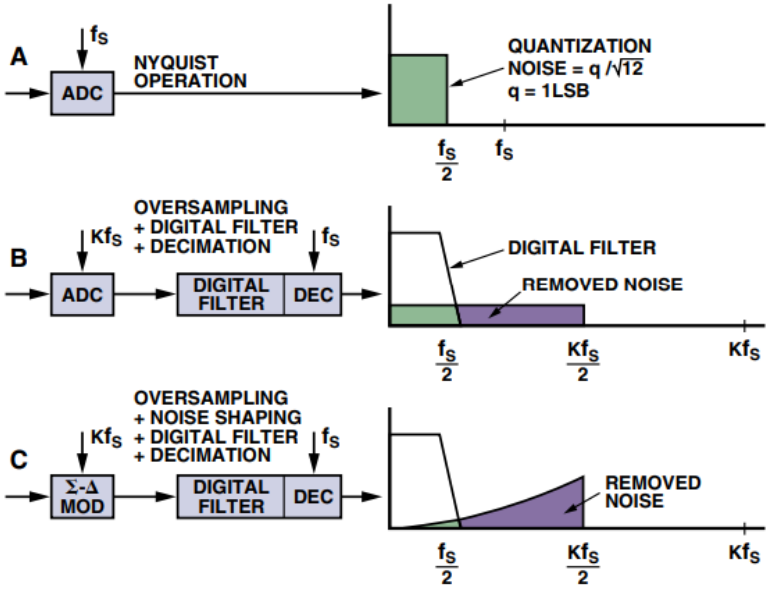

Figure 2.6: Noise spectrum of different operations for Delta Sigma ADC [16]

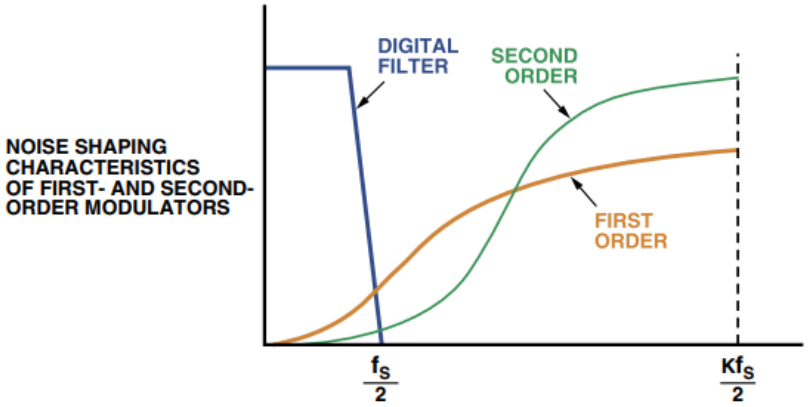

Figure 2.7: noise shape for first order vs second order $\Delta\Sigma$ [16]

2.4 Pipeline ADC

Pipeline ADCs today are made with resolution up to 14 bits with sample rates over 100MHz. Its main feature is its high resolution at higher frequencies, which means some good applications are medical instruments and telephone base stations [16].

All the analog stages operate on every clock cycle with a different sample value. This means that there is one conversion every clock cycle as shown in figure 2.8, but there is a latency as well for every clock cycle [5, p. 665].

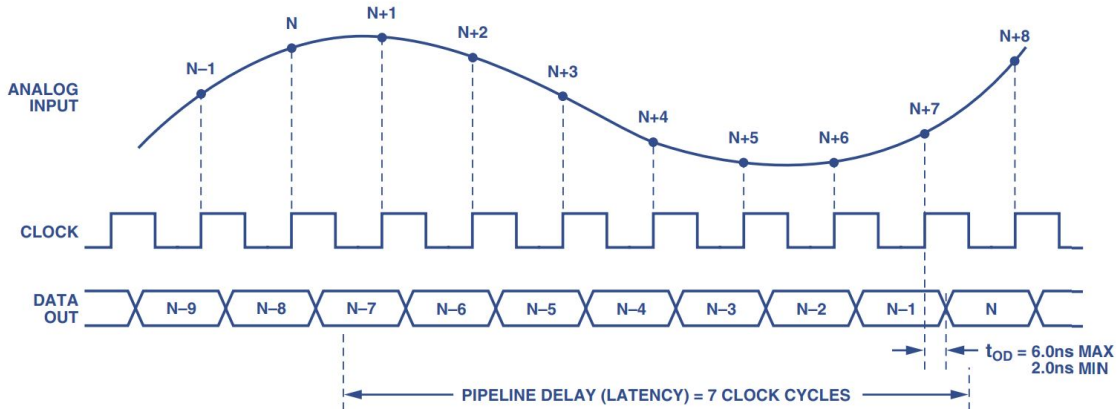

Figure 2.8: Timing of the AD9235 pipeline ADC [16]

Each step from fig. 2.9 takes an input from the previous stage, compares it to a reference voltage, and uses a MDAC to make a residue signal. The residue signal can be calculated using [5, eq. 17.39]:

$$V_{i+1} = 2[V_i + (\bar{b_i} - 0.5)V_{ref}/2] \tag{2.2}$$

The first bit is $b_1 = 1$ if $V_{in} > 0$ and $b_1 = 0$ if $V_{in} < 0$

second bit depends on the previous bit, if it was a 1 then $V_{ref}/4$ is subtracted from the input, then multiplied by two and this is checked again to be more or less than 0, which gives the new bit b_2. If the output of the previous bit was a 0 then $V_{ref}/4$ is added to the input instead, then multiplied by two and checked if it is less than or bigger than 0 to give the next bit b_2. This algorithm continues until all the bits are generated and this will create signals as shown in fig. 2.10. From fig. 2.9 each step has a decreasing number of shift registers, this is due to each stage operates at different sample inputs which needs shift registers at varying lengths. The last residue signal V_{N+1} is not used so the last stage is simply a comparator [5, p.667].

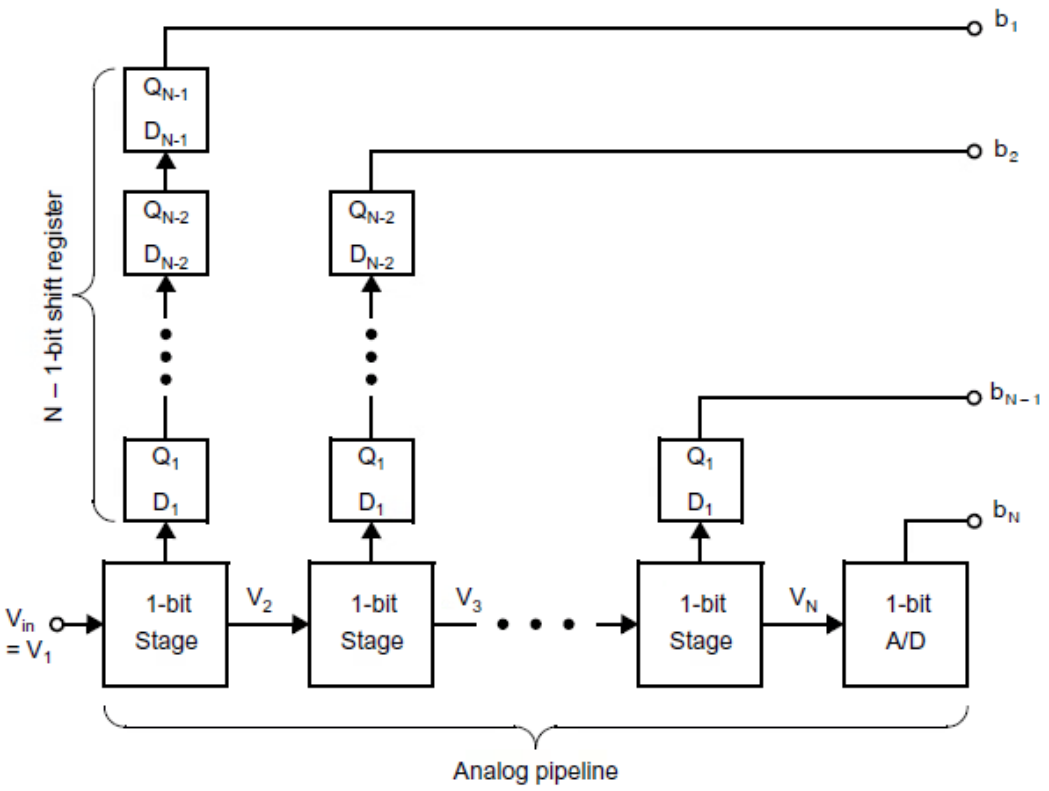

Figure 2.9: Block diagram for one bit per stage pipeline converter [5, fig. 17.19]

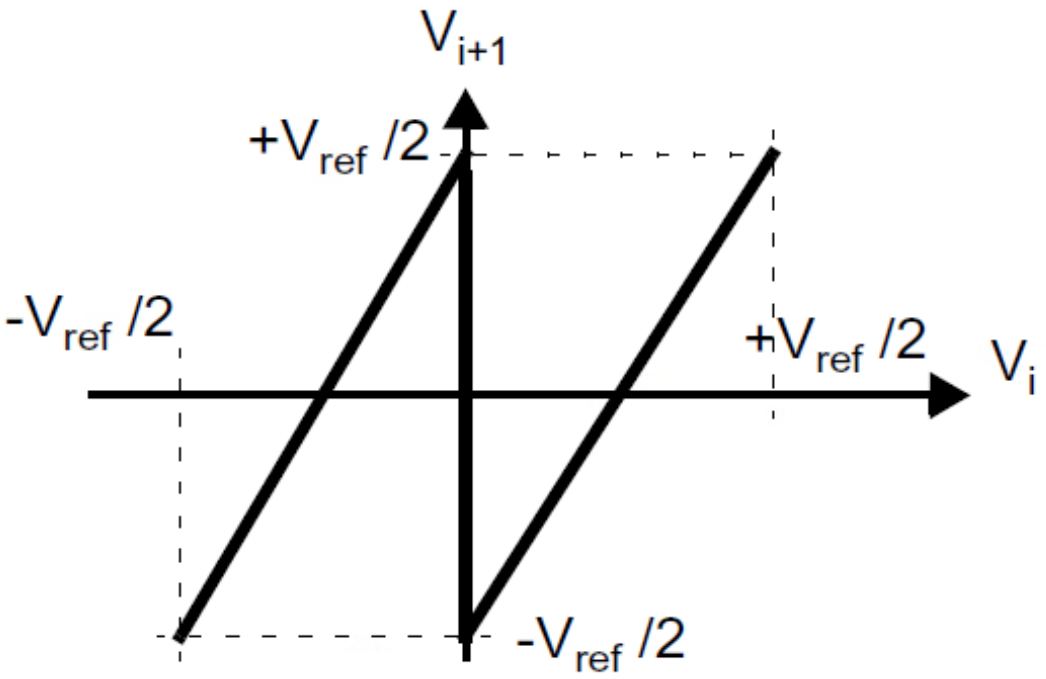

Figure 2.10: one bit pipeline signal [5, fig. 17.18]

2.5 Performance limitations

2.5.1 Resolution

The bit resolution of an ADC is the number of analog intervals which can be read in digital values. An N-bit resolution ADC have 2^N different analog intervals. The bit resolution is not necessarily the accuracy of the ADC, but it tells the number of values on the digital output [5, p. 638].

2.5.2 Offset and gain error

Offset error is the deviation of the first bit value ($V_{0...01}$) from $\frac{LSB}{2}$ or mathematically [5, eq. 15.23]:

$$E_{off} = (\frac{V_{0...01}}{V_{LSB}} - \frac{LSB}{2}) \tag{2.3}$$

where the unit calculated is in LSBs [5, p. 615] and shown graphically in fig. 2.11.

The difference of the ideal and actual values at the full scale-value where offset error has been reduced to zero is the gain error. It can be calculated as [5, eq. 15.25]:

$$E_{Gain} = (\frac{V_{1...1}}{V_{LSB}} - \frac{V_{0...01}}{V_{LSB}}) - (2^N - 2) \tag{2.4}$$

where E_{Gain} is calculated in the units of LSBs [5, p. 615]. It is explained graphically in fig. 2.11.

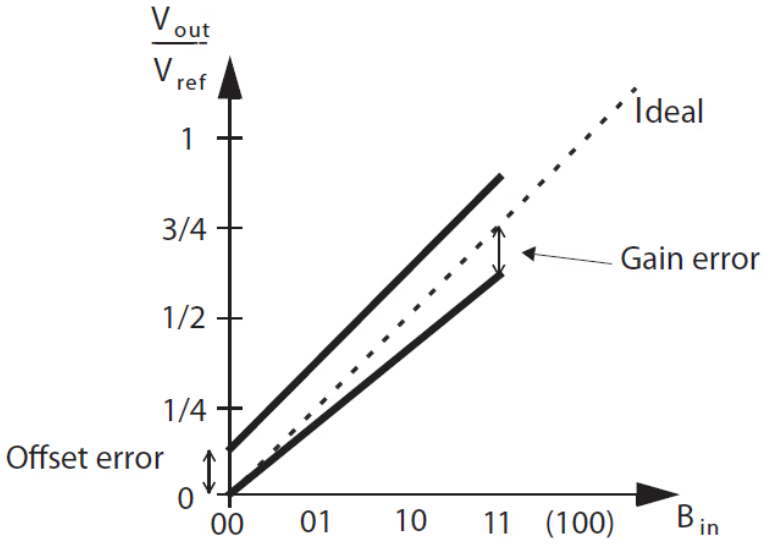

Figure 2.11: Offset and Gain error for a two bit Digital to Analog converter [5, fig. 15.9]

2.5.3 Integral nonlinearity error (INL)

After the offset and gain errors have been removed, the Integral Nonlinearity is the deviation from a straight line. The straight line is the line between the two endpoints in the transfer response of the system. There are more ways to define this line, but it's all after what is chosen to define this line. Normally INL is measured by sweeping the input, which again will measure the converters accuracy on lower input frequencies [5, p. 616].

2.5.4 Differential nonlinearity error (DNL)

The ideal converter has each analog step size equal to 1 LSB, Differential Nonlinearity Error is therefore defined to be the maximum step size deviation from 1 LSB. Optimally the DNL is equal to zero for all step sizes, if the DNL is equal to 0.5 means that the step sizes are varying from 0.5 LSB to 1.5 LSB. Like INL the DNL is low frequency accuracy, usually called static nonlinearities [5, p. 616].

2.5.5 Dynamic range

The Dynamic range is the minimum to maximum signal amplitude which the converter can meaningfully process. A good way to quantify this value is the maximum Signal to Noise and distortion Ratio (SNDR). The SNDR value is the ratio of the root mean square value of the input compared to the output plus the distortion [5, eq. 9.150]:

$$SNDR = 10\log(\frac{V_f^2}{N_o + V_{h2}^2 + V_{h3}^2 + ...}) \tag{2.5}$$

To do this the input signal must be removed from the measured output which can be done using a FFT and analyze it [5, p. 617].

Another way of measuring Dynamic Range is to calculate the Effective Number of Bits in an ideal converter with SNDR present which can be calculated as [5, eq. 15.29]:

$$ENOB = \frac{SNDR - 1.76\,\text{dB}}{6.02} \tag{2.6}$$

Where the equation for SNR is used: $SNR = 6.02N + 1.76\,\text{dB}$ and solved for N bits and SNDR is used instead of SNR [17].

2.5.6 Sampling rate and conversion time

In an ADC, the sample rate is how often it takes a input signal which is continuous and converts it into a discrete signal. The amplitude value at specific points in time is stored which again is called sample speed or in units Samples/second (S/s or usually in KS/s) [21].

This sampling speed has a lower limit which is called the Nyquist frequency, and is double of the highest frequency in the system ($\frac{f_s}{2} > f$) to avoid aliasing. Aliasing can cause the loss of information in the signal which makes the reconstruction of the signal impossible [25].

Conversion time is the time it takes the converter to complete a single measurement including the acquisition time of the input signal. Some converters have large latency due to multiple modules being used like a multiplexer or pipelining, yet have a high sample rate. An example a 12-Bit pipeline converter have a conversion time of 2 ns, but have a latency of 24 ns [5, p.617].

2.6 Sample-and-hold circuits

One of the important analog blocks in data converters is the S/H circuit which is used to sample an analog signal and store this value over some time. The use of the S/H can reduce errors due to slightly different delay times from different components inside the data converter. [5, p. 444]

The working principle is shown in fig. 2.12, where an analog input is sampled at different points usually with a clock frequency. This value is then stored (example is stored in a capacitor), which is the "sample" part of the S/H. This stored value is held in the capacitor until a new value is sampled which is the "hold" part of the S/H. An example of a Sample-and-hold circuit is shown in fig. 2.13. [23]

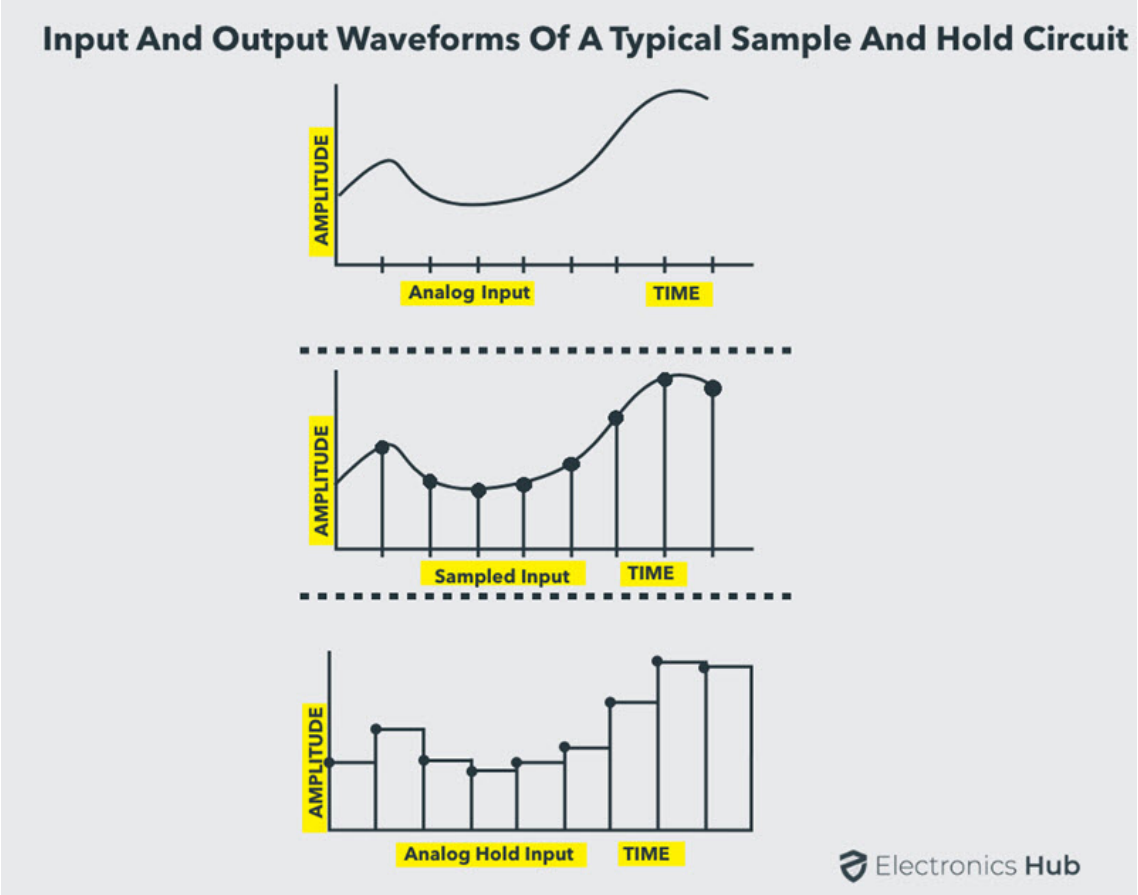

Figure 2.12: Working principle of sample and hold [23]

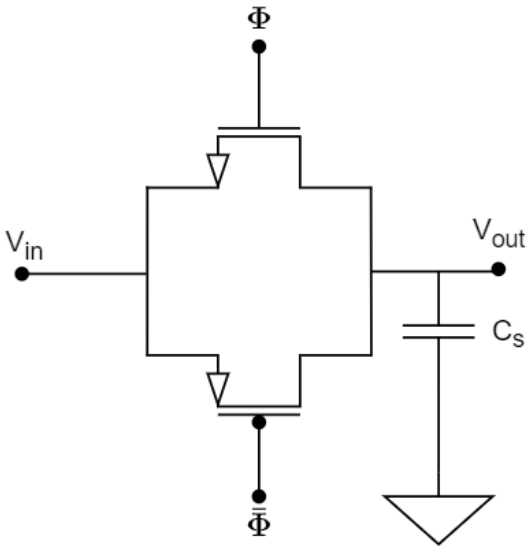

Figure 2.13: Sample and hold circuit example

Chapter 3

Delta Sigma Modulator design

From the introduction chapter, there are some specifications which is the goal to achieve in this design chapter. The specifications are shown in table 3.1.

Specifications	
Samples/s	80 kS/s
bit resolution	14 bits
Area	Not an issue
Power consumption	Not an issue

Table 3.1: Specification table

From the paper [16], the specifications falls under the ΔΣ ADC, and the SAR ADC. The ΔΣ is used for a high resolution, which is what is wanted in the project. The sample speed of the project is relatively low which is why it should be fine to oversample to achieve a higher resolution. Another choice is the SAR ADC, while the area used will not be a problem, the relatively high resolution can be an issue. The SAR can go up to 14 bits, but it is the high end of its range which would make the ΔΣ more suitable.

When designing the ΔΣ the TSMC (Taiwan Semiconductor Manufacturing Company) 65 nm CMOS (complementary metal oxide semiconductor) technology will be used. It uses a voltage ranges up to 1.2 V which is used as the V_{dd} in the project.

The ΔΣ that will be used will be a discrete time (DT second order delta sigma and the block diagram of this is shown in fig 3.1 [3].

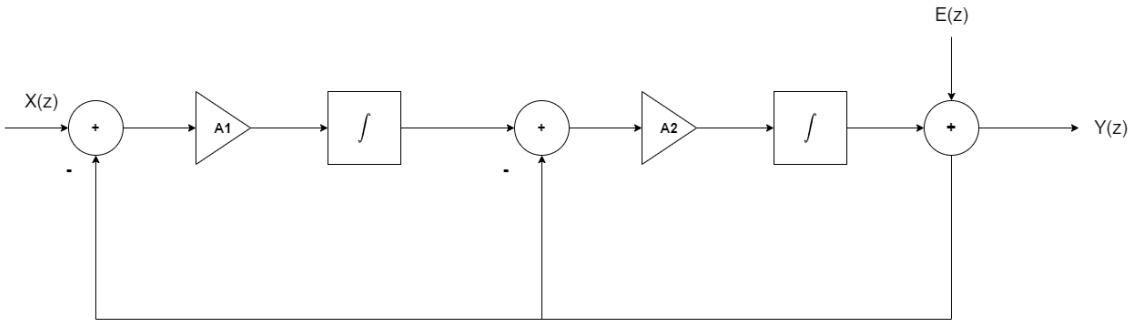

Figure 3.1: Block diagram of second order delta sigma

3.1 Second order Delta Sigma modulator

To realize the 2. order ΔΣ ADC, a Discrete time implementation was chosen since this has been preferred in the past, thus an abundance of papers and books describing the design process exists. While Continuous time (CT) is becoming popular, this is mostly used for higher sampling rates and lower power consumption [20]. For the given specifications for ENOB and sampling frequecy, DT should be sufficient. The chosen topology is based on [3] where the schematic is given as shown in fig. 3.2.

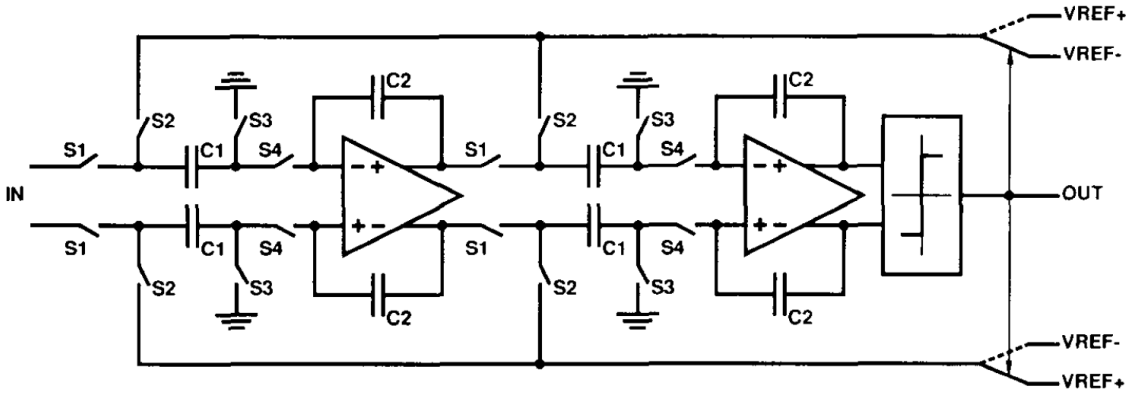

Figure 3.2: Second order ΔΣ from [4]

For higher order ΔΣ modulators, stability can become a concern, however a common high order architecture to simplify stability requirements often implements a serial second order as a single block. To have the circuit to work as a ΔΣ modulator, there are some requirements for $A1, A2$ amplifications in 3.1. According to [20] the following equations must be satisfied

$$k_q A_1 A_2 = 1 \tag{3.1}$$

$$k_q A_2 = 2 \tag{3.2}$$

Here k_q is the quantizer gain. For a single bit quantizer the output is determined by the input sign only, meaning that the gain is undefined. This means the gain of each integrator can be set randomly without altering performance [3]. The gain is set by the capacitor ratio $\frac{C_1}{C_2}$, here set to 0.5 for both integrators. To keep the capacative load low the unit size is set to 100 fF. All the switches are implemented with the transmission gates described in section 3.4.1. $S1$ and $S3$ is driven by clock ϕ_1 while $S2$ and $S4$ is driven by ϕ_2. Non-overlapping clocks with a frequency of $f_s = 80\,\text{kHz}$ are used. During ϕ_2 the signal output of the integrator is valid, and the quantizer is active. The output of the comparator (the last component in fig. 3.2) controls the feedback which is connected to $S2$. The amplifier used is not rail to rail, therefor the common mode voltage is used instead of ground at $S3$.

3.1.1 Calculating bit resolution

To get the required ENOB, the Over-Sampling Ratio can be calculated. ENOB is given by [11]:

$$ENOB = \frac{\text{SNDR} - 1.76\,\text{dB}}{6.02\,\text{dB}} \tag{3.3}$$

For a 2nd order ΣΔ modulator with ideal components, such as infinite gain, high slew rate and no added noise, SNDR is given as

$$SQNR_{\max} = 6.02N + 1.76 - 12.9 + 50\log OSR \tag{3.4}$$

Using a 1 bit quantizer, 13 bits are needed to get the required 14 Bits which give us $N = 13$ in the equation. This means an increase in SNDR of 78 dB. Going from no noise shaping to 2nd order noise shaping, the following equation is found [11]

$$OSR = 10^{\frac{78+12.9}{50}} \approx 66 \tag{3.5}$$

Compared to a 1st order ΔΣ the OSR would be

$$OSR = 10^{\frac{78+5.2}{30}} \approx 594 \tag{3.6}$$

Which would be unreasonable.

With a constant sample speed, this will give a signal bandwidth f_{bw} and a reasonable test input signal frequency f_{signal} of [11]:

$$f_{bw} = \frac{f_s}{2 \cdot OSR} = \frac{80\,\text{kHz}}{2 \cdot 66} = 588\,\text{Hz} \tag{3.7}$$

$$f_{signal} = \frac{f_s}{7 \cdot OSR} = \frac{80\,\text{kHz}}{7 \cdot 66} = 168\,\text{Hz} \tag{3.8}$$

For a constant data stream the equation will look like:

$$f_s = \frac{f_{bw}}{2 \cdot OSR} = \frac{40\,\text{kHz}}{2 \cdot 66} = 5.28\,\text{MHz} \tag{3.9}$$

$$f_{signal} = \frac{f_s}{7 \cdot OSR} = \frac{5.28\,\text{MHz}}{7 \cdot 66} = 11\,429\,\text{Hz} \tag{3.10}$$

3.2 Folded cascode amplifier

An amplifier was needed for the integrators that is used in the final ΔΣ modulator. The folded cascode amplifier topology is a single stage amplifier which means the Miller compensation is not needed, unlike multi stage amplifiers. Another good argument is the reduced amount of transistors and passive components used, which again will make the layout an easier job which again will probably have a better PEX result. A downside of the folded cascode would be the reduced output swing. Even though the output swing is less than any other multi stage amplifier, the cascode was chosen in this project. An example of a fully differential folded cascode amplifier is shown in fig. 3.3.

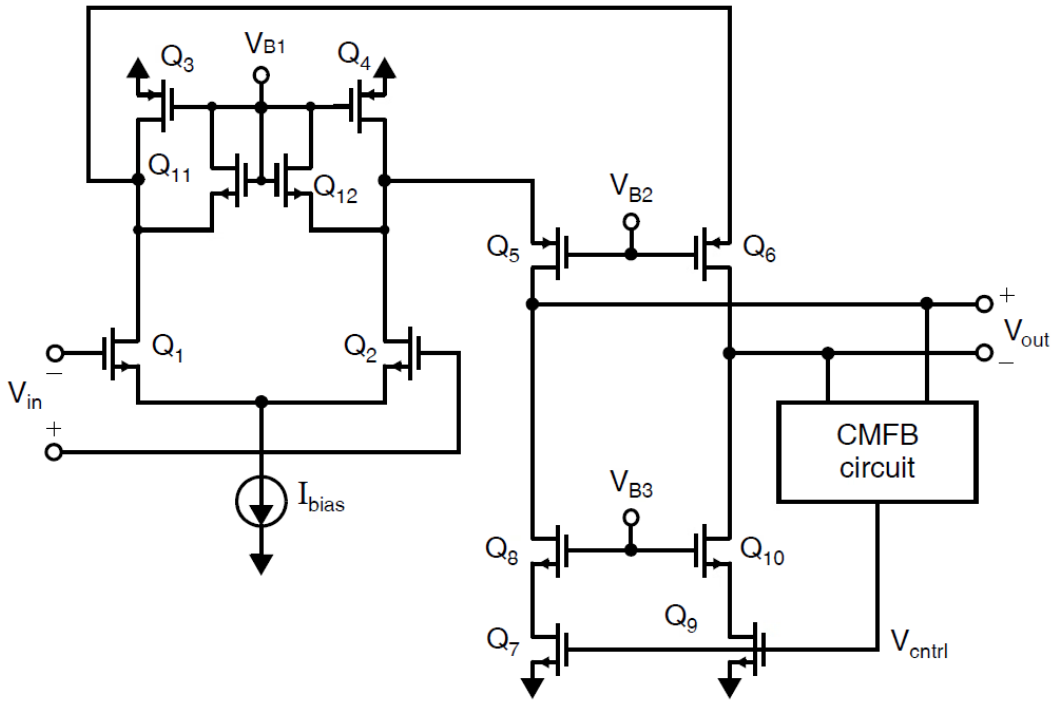

Figure 3.3: Fully differential folded cascode OPAMP [5, fig. 6.28]

3.2.1 Designing the cascode

When designing the folded cascode, the desired overdrive voltage was 200 mV and using the equation $V_{ov} = \frac{2i_d}{gm}$ [5, p.26]. First all the length was chosen to be 100 nm, but was increased to get a better gain from $A_{ol} \propto L$. The widths was chosen by aiming to have all the transistors in region 2 (region 2 when simulated in cadence) which is in saturation mode, but was later tweaked to fit in fully differential mode by sweeping the widths.

When using a fully differential circuit, a common mode feedback is needed. This is to ensure the outputs are going around the reference voltage to get a better differential output. This is implemented as shown in figure 3.6. The output of this common mode feedback is connected to the gate of the first pmos pair in figure 3.4.

The biasing is done through an ideal current source which is connected to a current mirror circuit shown in figure 3.8. The goal is to use the mirror current formula $\frac{W_1}{I_1} = \frac{W_2}{I_2}$ [5, p.179] to have the right amount of current through both branches and twice the current in the first pmos pair.

3.2.2 Slew rate

The slew rate is how fast the amplifier can change voltage and therefore is measured in MV/s and can be calculated using [5, eq.6.105]

$$SR = \frac{I_D}{C_L} \tag{3.11}$$

In cadence there is a calculator which finds the slew rate. In the circuit, the fastest changing component would be the clock, so the minimum slew rate should be chosen based on the formula:

$$SR = 2\pi \times f_{clk} \times V_{peak} \tag{3.12}$$

3.2.3 Gain

When choosing an amplifier, the folded cascode is a great choice due to it having a large gain, even though still working as a single stage. The gain should be as high as possible explained in formula $A_{ol} \geq \frac{2^{N+2}}{\beta}$ [15], where N is number of bits in the integrator and beta is the feedback factor. The higher open loop gain will give a higher number of bits which means the OSR can be lower and more achievable.

3.2.4 Folded cascode results

Schematic and layout

The final parameters of the cascode transistors is shown in table 3.2, and used in schematic in fig. 3.4. With these sizes the transistors are in the right mode with the input range found in fig. 3.14. The layout of the folded cascode was made and the results was DRC and LVS clean and the layout is shown in fig. 3.4.

	M0/1	M7/8	M2/3	M10/11	M4/5	M17
Width (µm)	4.2	1.5	1.5	12	9	1.5
Length (nm)	300	300	300	300	600	300

Table 3.2: Parameters of transistors used in folded cascode amplifier

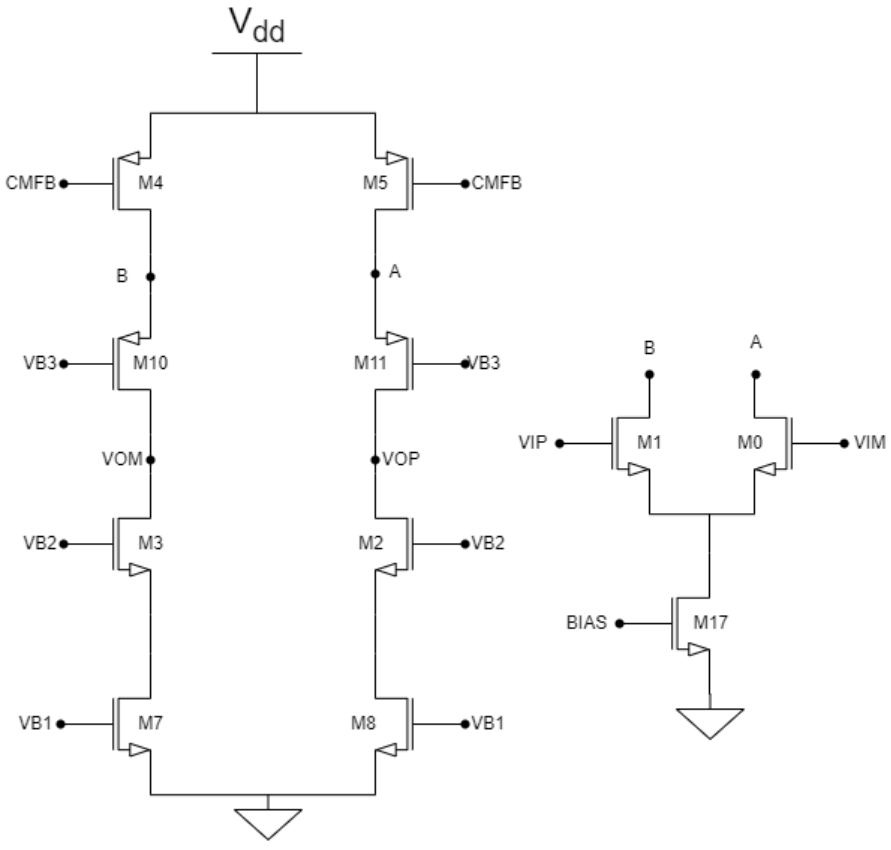

Figure 3.4: Folded cascode schematic

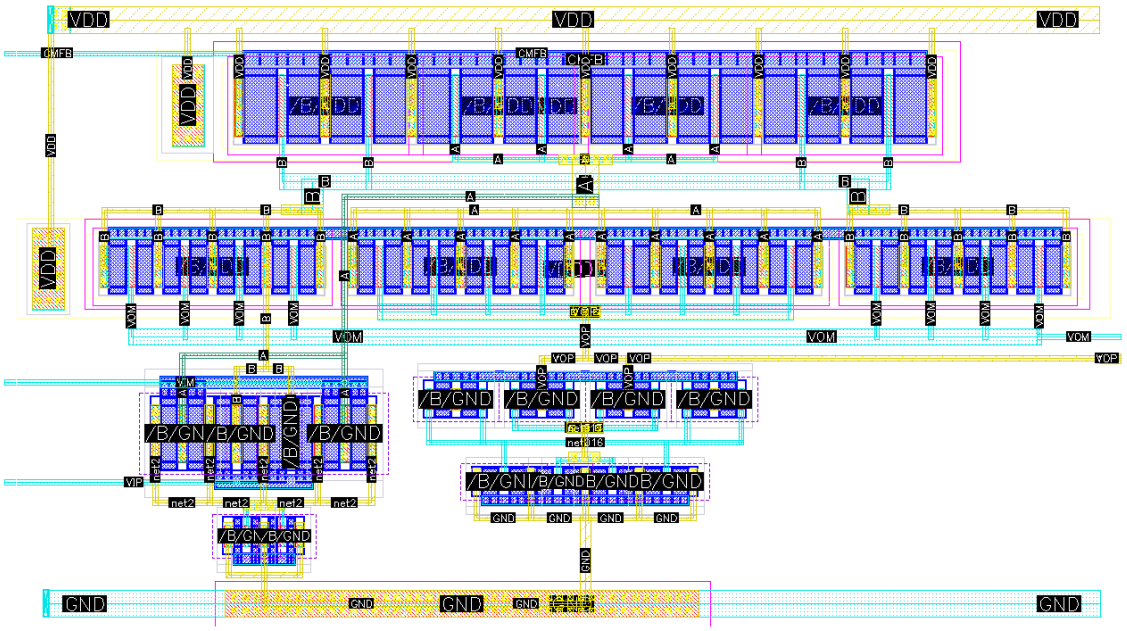

Figure 3.5: Folded cascode layout

Common mode feedback

The Common Mode Feedback schematic is shown in fig. 3.6 where the rectangles are transmissiongates, and this CMFB was chosen due to it fitting the switched capacitor circuitry in the ΔΣ, and usually have a high output swing. One downside is the amount of capacitors used which again will reduce the Unity Gain frequency (UGF) of the circuit. The capacitors used is chosen to be 10 fF and 100 fF, due to C6 and C8 should be between 4 and 10 times bigger than C4 and C7 [5, p.292]. The transistors used in the CMFB circuit is for biasing and the sizes is shown in table 3.3. The layout was made of the CMFB with DRC and LVS clean results, however there was no seperate test for this due to it only works together with the cascode.

	M2	M3	M5
Width (µm)	0.4	0.4	1.125
Length (nm)	150	150	600

Table 3.3: Parameters of transistors used in CMFB circuit

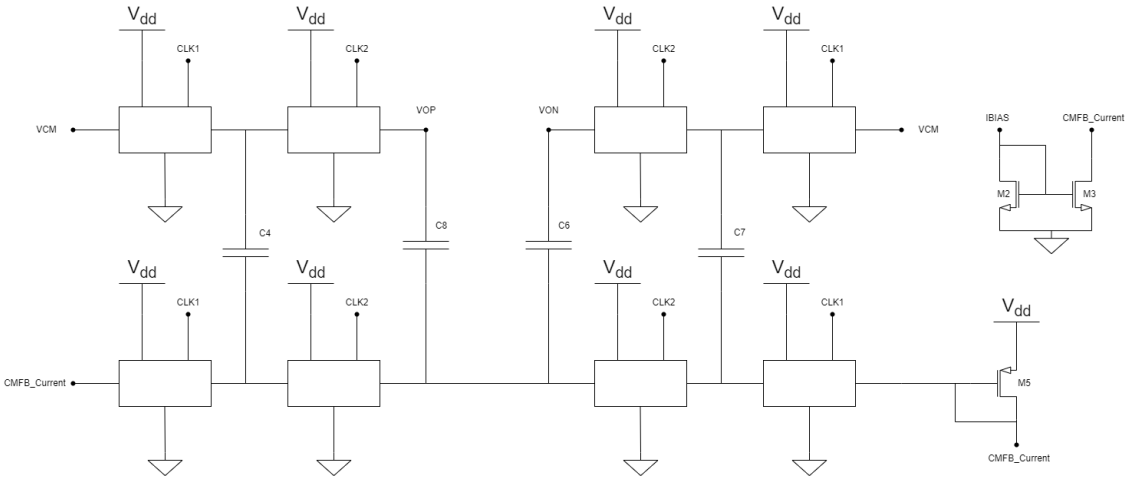

Figure 3.6: Common mode feedback circuit used for the folded cascode

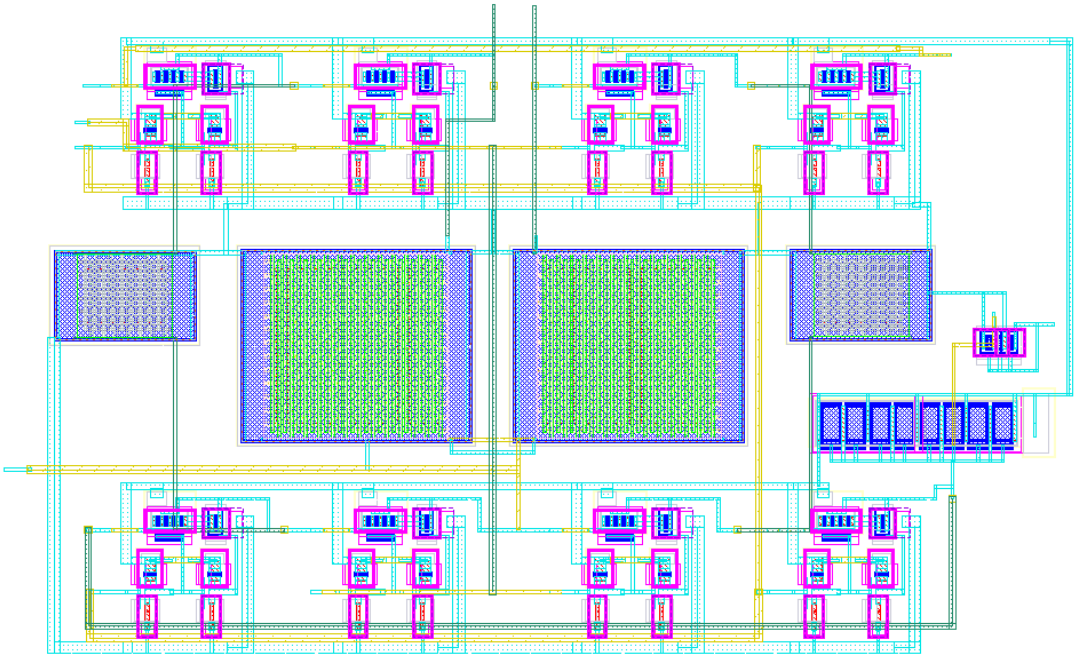

Figure 3.7: Common mode feedback layout

Bias circuit

Using the $\frac{g_m}{I_d}$ method gave a calculated value for i_d of 16 µA, which is the current from the current source (BIAS in fig. 3.8). The circuit in fig. 3.8 is multiple current mirrors with transistor sizes shown in table 3.4, where the current in the branch V_{B3} is simulated to be 16.22 µA, and the current in branch V_{B2} is simulated to be 76.25 µA.

	M5/9/10	M8	M6	M11	M12
Width (µm)	0.4	0.2	4	1	0.67
Length (nm)	150	150	150	1000	150

Table 3.4: Parameters of the transistors used in Biasing circuit

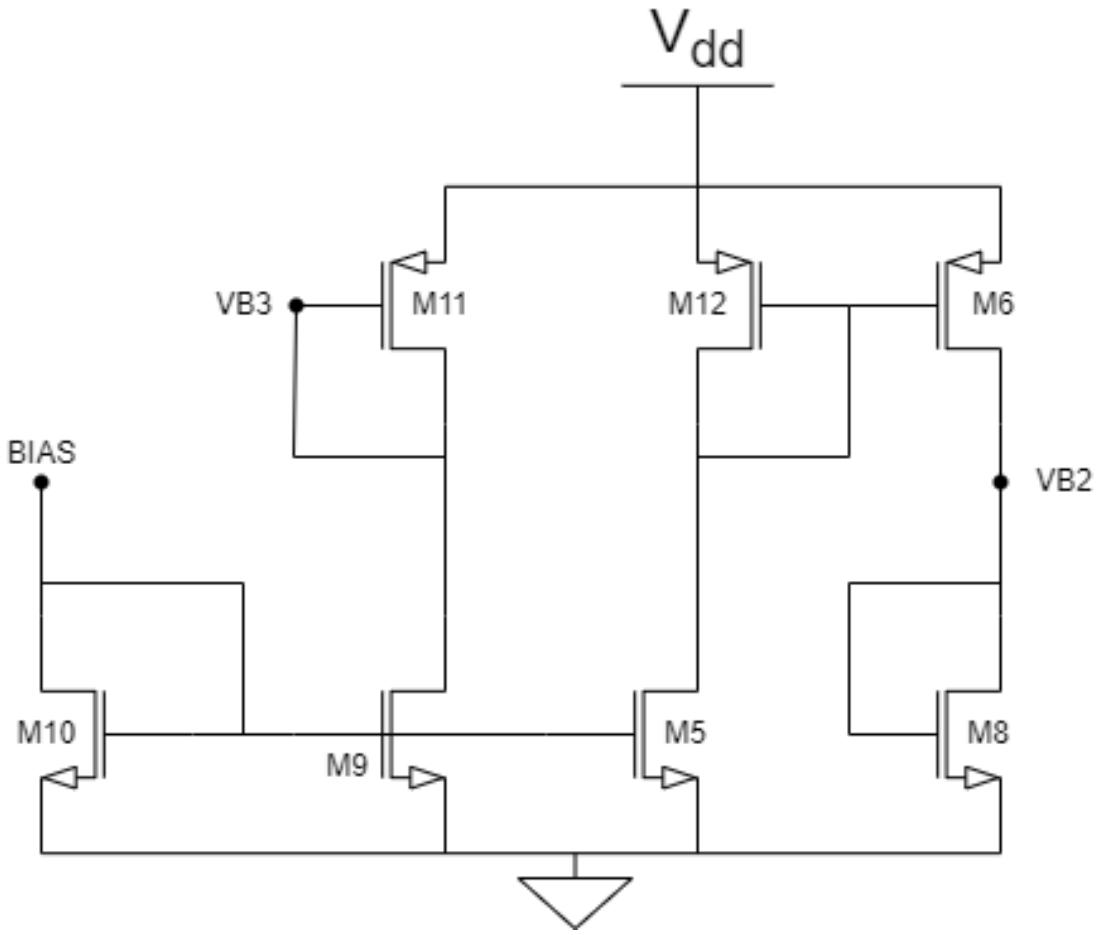

Figure 3.8: Bias circuit for folded cascode

Open loop gain

The open loop gain of the folded cascode amplifier was tested with the test bench in fig. 3.9 and the results is shown in fig. 3.10 which is calculated to be $160\frac{V}{V}$ by using $A_{OL} = \frac{V_o}{V_i}$. In the testbench the inputs are a differential sinus wave of 1 mV with a dc offset of 600 mV and a frequency of 50 kHz. To find the UGF, the same testbench is used and sweeping the frequency until the output is equal to the input signal (open loop gain = 1), which comes to about 30 MHz which is sufficient for this application.

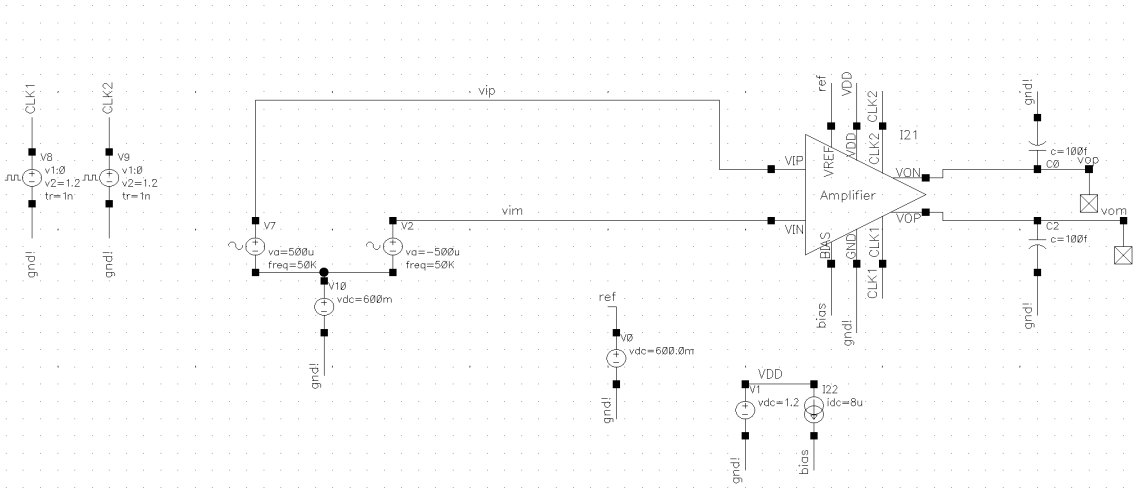

Figure 3.9: Open loop gain testbench

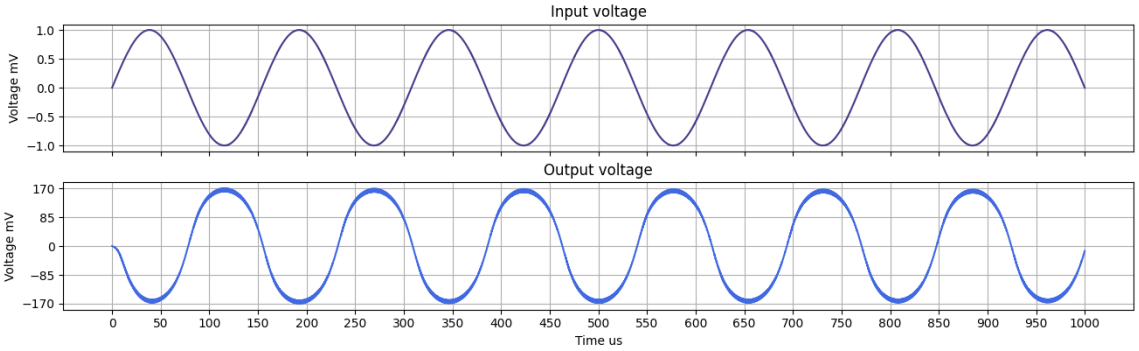

Figure 3.10: Open loop gain testbench

Output swing

The output swing was tested by inputting a differential dc signal which is sweep from 0 V to 1.2 V with an open loop configuration shown in the testbench in fig. 3.11. The output will be the input signal times the open loop gain of the amplifier which is why the output has only a small area where it is linear and will fast go towards vdd and -vdd. The linear area is where the output swing is simulated to be between $-600\,\text{mV}$ and $600\,\text{mV}$. Anything outside of this region, the amplifier will have a dampening of the gain which is not ideal.

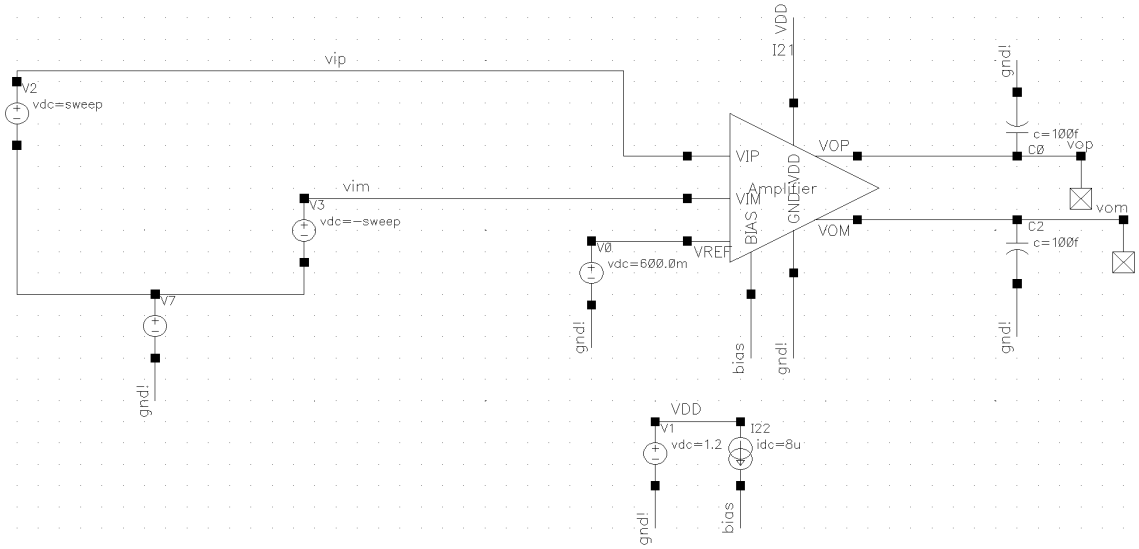

Figure 3.11: Folded cascode output swing testbench

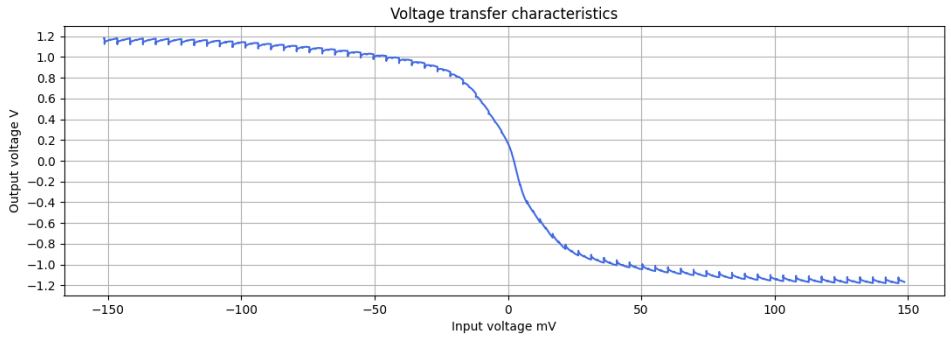

Figure 3.12: Voltage transfer curve of the amplifier

Input range

The input range is the range in which the amplifier is in its "working mode". As seen from fig. 3.14 the amplifier only gains when the common mode voltage has an offset at minimum 500 mV and maximum 950 mV. This is tested by sweeping a dc offset from 0-vdd and adding a very slow, 1 mV amplitude sinus signal.

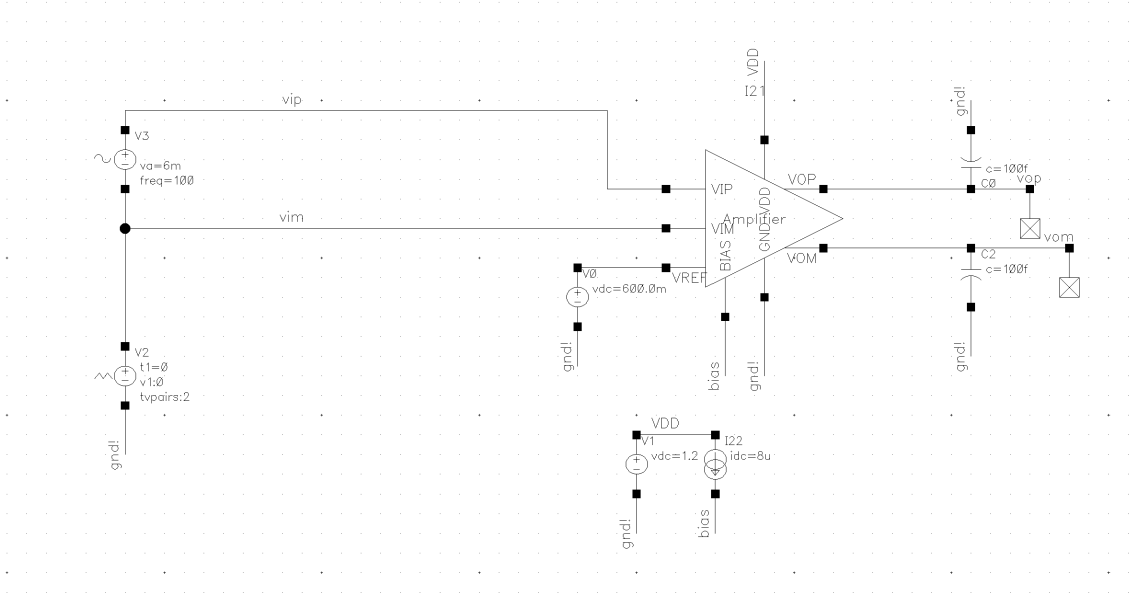

Figure 3.13: Folded cascode input range testbench

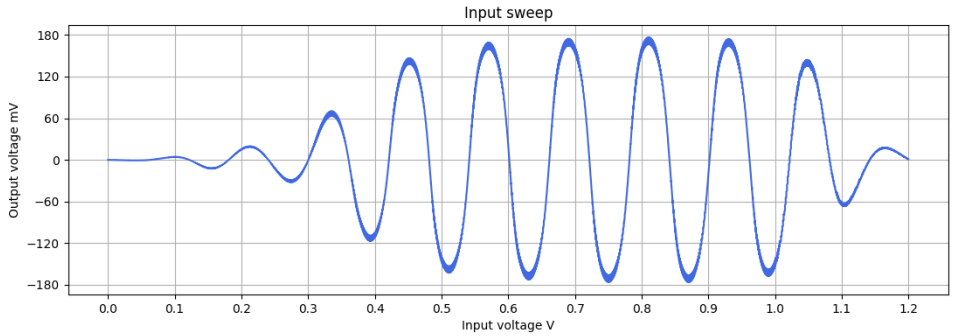

Figure 3.14: Folded cascode input range result

3.3 Comparator

3.3.1 Comparator development

A comparator was needed to act as the one bit quantizer of the final ΔΣ modulator. The comparator that was used in this project was originally designed for an assignment earlier in one of the courses at UiO (IN5220) [13]. It was designed to work with a higher frequency and a lower resolution than what is needed for the ΔΣ that is designed in this report. However it is assumes from the results that it can also work with the 14 bit specifactions as the design had a large margin to work with.

The comparator was designed to work with a clock frequency of 10 MHz. The period of the clock signal was used as a basis to begin calculating the transistor sizes in the following way:

Knowing that the period of the clock signal is $\frac{1}{10\,\mathrm{MHz}} = 100\,\mathrm{ns}$ the comparator could be designed to have a delay of one tenth of the clock signal period, which gives the following relationship [14]:

$$t_{delay} = 2\frac{C_L \cdot |V_{th(p)}|}{I_{tail}} + \frac{C_L}{g_{m,eff}} \cdot ln\left(2\frac{\Delta V_{out}}{\Delta V_0}\right) = 10\,\mathrm{ns} \tag{3.13}$$

Where C_L is the load capacitance. The following calculations was done with a C_L value of 100 fF. I_{tail} is the tail current drawn from the bottom of the strongARM circuit. ΔV_{out} is the voltage difference between the logic states of the comparator outputs. $V_{th(p)}$ is the threshold voltage of the pmos transistors in the circuit.

ΔV_0 is given by [26, eq. 6]:

$$\Delta V_0 = 2|V_{th(p)}|\sqrt{2\frac{\beta_{N1L,R}}{I_{tail}}} \cdot \Delta V_{in} \tag{3.14}$$

The value for ΔV_{in} was found through the resolution the comparator was designed for. The resolution the comparator was designed for was 12 bits with differential inputs which results in the following ΔV_{in}

$$V_{res} = \Delta V_{in} = \frac{2 \cdot V_{DD}}{2^{12}} = \frac{2.4\,\mathrm{V}}{2^{12}} = 0.586\,\mathrm{mV} \tag{3.15}$$

but to have the comparator work with 14 bit resolution the resolution in the comparator must be:

$$V_{res} = \Delta V_{in} = \frac{2 \cdot V_{DD}}{2^{14}} = \frac{2.4\,\mathrm{V}}{2^{14}} = 146\,\mu\mathrm{V} \tag{3.16}$$

According to [22] $\beta_{N1L,R}$ can be calculated as:

$$\beta_{N1L,R} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_{N1L,R} \tag{3.17}$$

Where 45 nm values from [5, table 1.5] was used for $\mu_n C_{ox}$.

Next eq. (3.13) was flipped and solved for $g_{m,eff}$ in the following way:

$$g_{m,eff} = C_L \cdot ln\left(\frac{\Delta V_{out}}{\Delta V_0}\right) \cdot \left(t_{delay} - 2\frac{C_L \cdot V_{th(p)}}{I_{tail}}\right)^{-1} \tag{3.18}$$

This was done to take advantage of the following relationship found in [22]:

$$g_{m,eff} = g_{mP1L,R} + g_{mN2L,R} \tag{3.19}$$

An assumption was made that the two cross coupled inverters in the strongARM topology had the same transconductance so that:

$$\frac{g_{m,eff}}{2} = g_{mP1L,R} = g_{mN2L,R} \tag{3.20}$$

After this assumption was made the sizes of the cross coupled inverters could be calculated with the following equation:

$$g_m = \sqrt{2\mu C_{ox}\left(\frac{W}{L}\right) \cdot \frac{I_{tail}}{2}} \Rightarrow W = \frac{g_m^2 \cdot L}{2\mu C_{ox} \cdot \frac{I_{tail}}{2}} \tag{3.21}$$

Before the previously layed out steps could be started, a few values had to be chosen as a starting point. Choosing a big width for the input transistors can help to reduce the offset voltage of the comparator [22]. To take advantage of that and to set a starting point for the other calculations, the transistors in the input pair had their width set to 5 µm. The tail current of the strongARM (fig. 3.15) was set to 30 µA and lastly the pmos threshold voltage was found to be 406 mV through a dc analysis done in cadence when the transistor length was set to 130 nm. With those values set, the following values for width was calculated using the previously presented steps:

N_0	10 µm
N_{in}^+ , N_{in}^-	5 µm
N_{2L} , N_{2R}	510 nm
P_{1L} , P_{1R}	1.7 µm
Pre-charge transistors	2 µm

Table 3.5: Transistor widths for fig. 3.15

Where the pre-charge transistors width was found through parametric sweep analyses.

3.3.2 StrongARM and results

The comparator topology for this assignment is the strongARM comparator with a SR-latch on its outputs with their schematics shown in figure 3.15 and 3.16 respectively. This combination results in a fast comparator with stable outputs at rail to rail voltages.

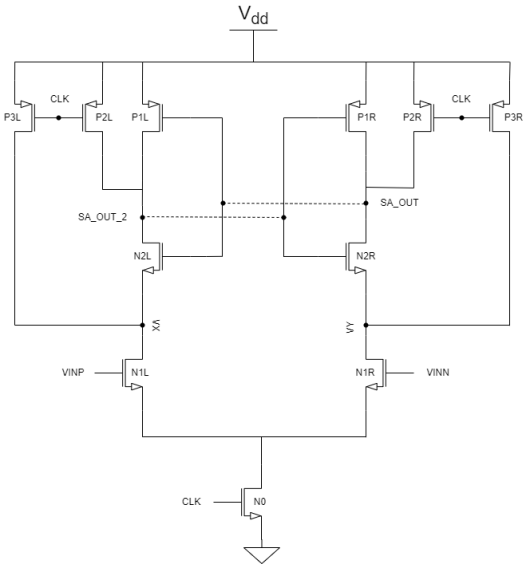

Figure 3.15: StrongARM schematic

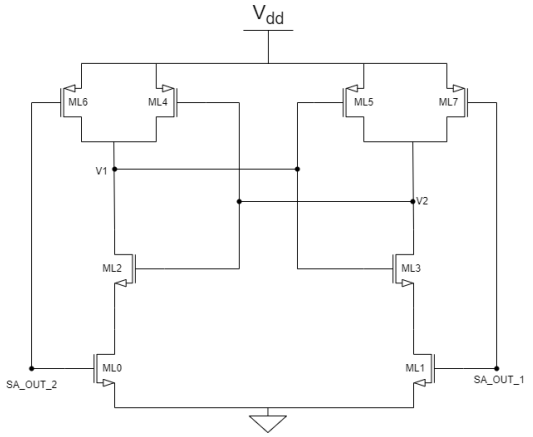

Figure 3.16: NAND based SR latch schematic

The comparator is designed to work with clock frequencies up to at least 10 MHz with a resolution of at least 0.586 mV with a common mode voltage of 0.6 V. The outputs of the comparator has a rise time of 1.814 ns and a fall time of 2.959 ns when tested pre-layout. After each transistor was sized with the calculations in section 3.3.1, some sizes had to be tweaked to get the desired functionality out of the comparator. A table of the final widths of the transistors in the comparator is shown below, while all transistor lengths are set to 130 nm.

N_0	16 µm
N_{in}^+ , N_{in}^-	5 µm
N_{2L} , N_{2R}	900 nm
P_{1L} , P_{1R}	1.8 µm
Pre-charge transistors	2 µm

Table 3.6: StrongARM latch transistor widths

NMOS	480 nm
PMOS	840 nm

Table 3.7: SR-latch transistor widths

A plot of a transient analysis that was conducted on the comparator is shown below for both the pre and post layout component. The analysis shows the result when one of the input voltages is kept at a voltage level of 0.61 V, which is 10 mV over the common mode voltage, and the other input voltage is stepped up to a level that is 0.586 mV above the first input. The result of this step output is that the comparator makes a decision and the output voltages is set to their correct logic values at the next rising clock edge.

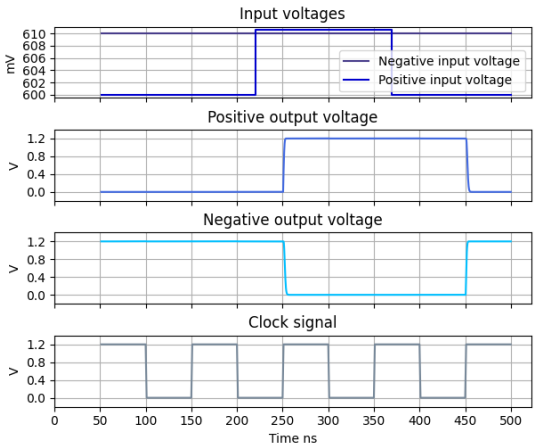

Figure 3.17: StrongARM latch transient test pre layout

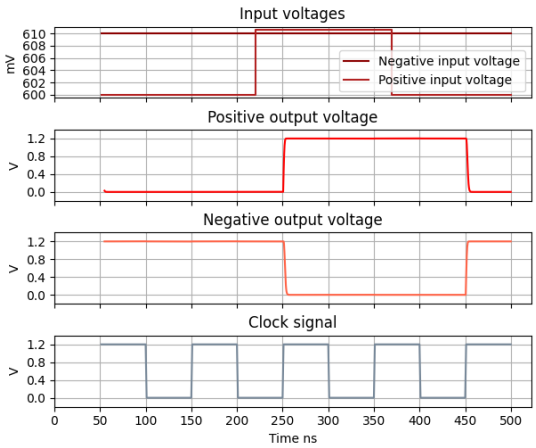

Figure 3.18: StrongARM latch transient test post layout

From the figures above it is shown that the pre vs post-layout is very similar which is the wanted result.

Below is a picture of the layout that was created for the strongARM latch:

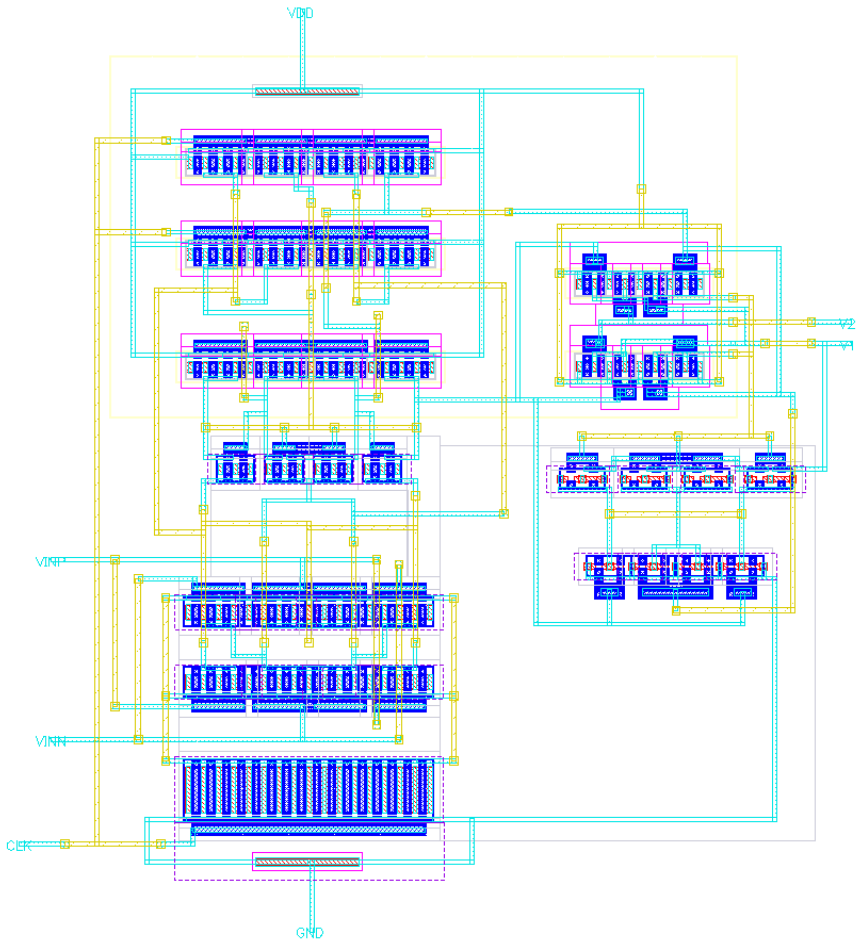

Figure 3.19: StrongARM layout

3.4 Transmission gate

A transmission gate was developed to work with the various switched capacitor mechanisms that are used in the the final $\Delta\Sigma$ circuit. A decision was made to include two inverters inside of the transmission gate cell so that only one clock signal would have to be supplied to the final transmission gate component. The inverters are used because a clock signal and its inverse are both used for the gate to function properly. Two inverters are used and connected in series where the clock signal is first inverted and then inverted back to its original form. This is done so that the clock signal that is supplied to the gate will be refreshed through the inverters and to make the two clock signals more similar. A schematic diagram of the transmission gate is shown below.

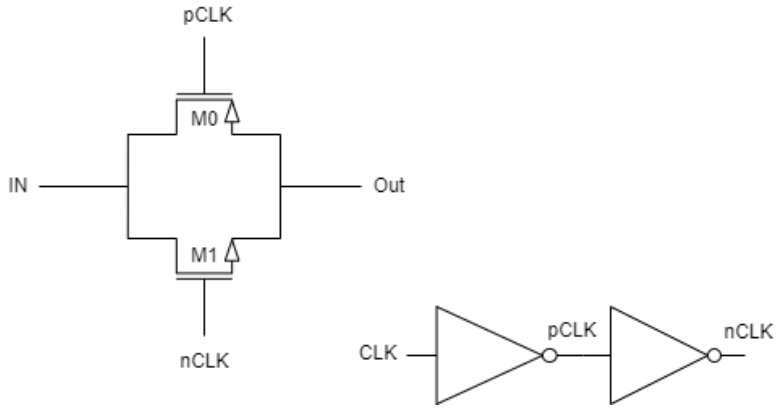

Figure 3.20: Schematic of transmission gate

To determine the sizes of the transistors, the resistance through the transmission gate was considered. To test the resistance through the transmission gate the clock signal was held high while the input voltage was swept from 0 V to 1.2 V. To begin with, the resistance was found by plotting the r_{on} (which is a feature in Cadence) parameter of both transistors in the transmission gate then calculating the parallel resistance of those plots. But after a parasitic extraction was done when the layout was completed this method was not as viable anymore. After this point the resistance was calculated through ohms law by dividing the voltage across the transmission gate by the current going through it.

A parametric sweep was performed where first the ratio between the PMOS and NMOS width was chosen to get a symmetric resistance curve. When four fingers are used for the PMOS the ratio between the NMOS and PMOS widths gave the most symmetric resistance curve at $w_p \approx 2 \cdot w_n$ which comes from the ratio of the carrier mobility $\frac{\mu_p}{\mu_n}$.

Then after the width ratio was established a sweep was conducted of the widths of both the transistors with a constant ratio between them. The parallel resistance that is formed by the two transistors was plotted for all the widths in the sweep, and the plot is shown below.

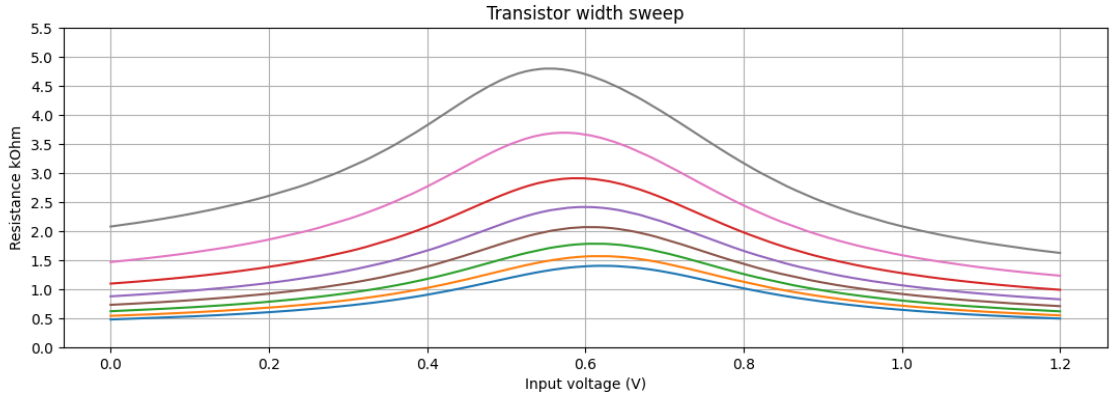

Figure 3.21: Parametric sweep of the transistor widths

From the parametric sweep it can be seen that the resistance of the transmission gate decreases as the widths of the transistors increases. With other words, a trade-off has to be made between keeping the area of the transmission gate low while also keeping the resistance through it low. The final sizes for the transmission gate was picked out from the plot and will be presented in the next section.

3.4.1 Results and layout

The final iteration of the transmission gate has the following widths for its transistors while all lengths are set to 60 nm:

Transmission gate PMOS	1.16 µm
Transmission gate NMOS	500 nm
Inverter PMOS	350 nm
Inverter NMOS	120 nm

Table 3.8: Transmission gate transistor widths

A schematic of the transmission gate and the inverters that is used for the activation signals are shown below:

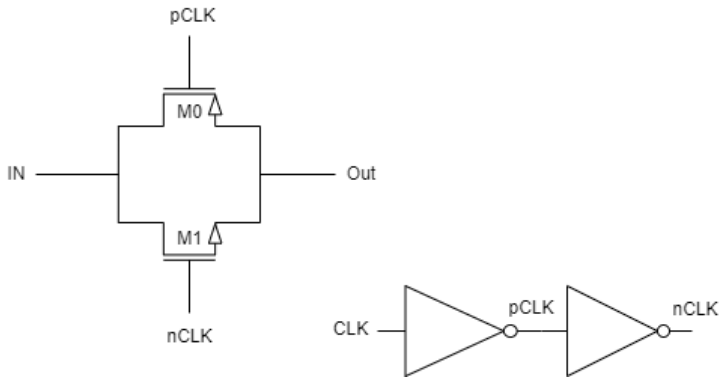

Figure 3.22: Schematic of the transmission gate

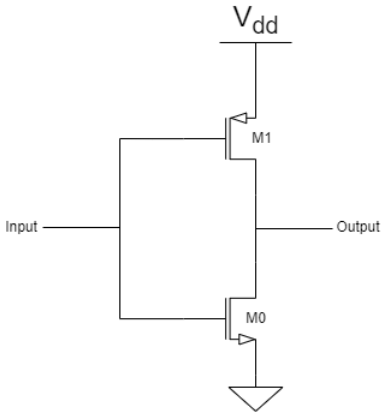

Figure 3.23: Schematic of the inverter

A layout was created for the transmission gate as shown below:

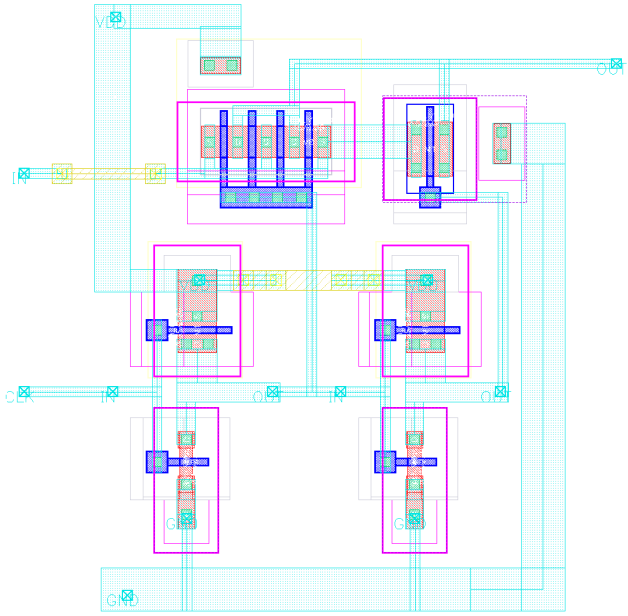

Figure 3.24: Transmission gate layout

The performance of the transmission gate was tested before and after parasitic extraction from the layout and the two tests are shown below.

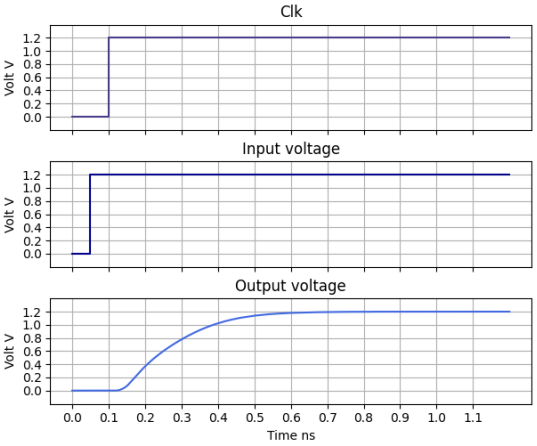

Figure 3.25: Test of pre-layout transmission gate circuit

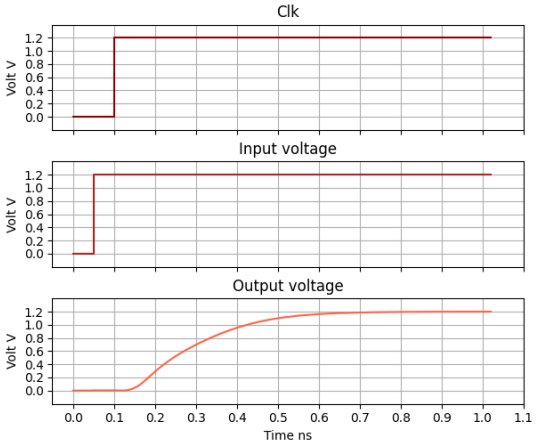

Figure 3.26: Test of post-layout transmission gate circuit

Not much difference can be seen in the performance of the transmission gate pre layout when compared to post layout other than a small difference in the risetimes of the two cases as shown in the plot below. Both risetimes are small enough to enable the switches to settle within a clock period from the system clock that is 10 MHz

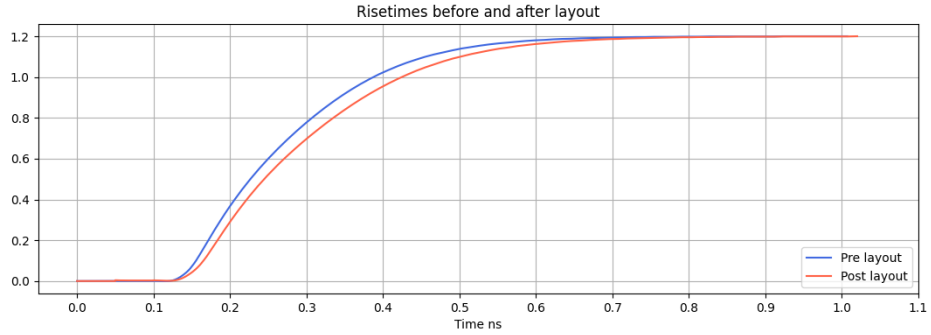

Figure 3.27: Transmission gate risetimes compared pre vs post layout parasitic extraction

One aspect of the transmission that showed a bigger difference when pre and post layout characteristics was compared was the peak resistance through the gate. The plots below show the difference in resistance through the gate when it is calculated through ohms law, like explained in section 3.4.1, both before and after the parasitic extraction was done. The plot shows that the peak resistance through the gate increased by $\approx 400\,\Omega$ after the parasitic extraction. Note that the post layout curve has a linear area around $x = 0.8\,\text{V}$ to $x = 0.9\,\text{V}$, this is because a divide by zero error was cut out of the plot.

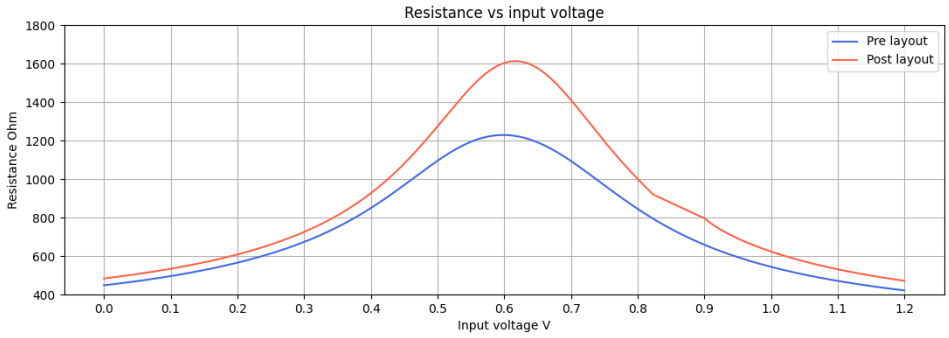

Figure 3.28: Resistance through the transmission gate compared pre vs post layout

3.5 AND gate

An AND gate was developed to be used in the MDAC construction that is used for the $\Delta\Sigma$ modulator. A standard CMOS construction for a NAND gate with a inverter on its outputs was chosen as the topology for this and is shown in the schematic below.

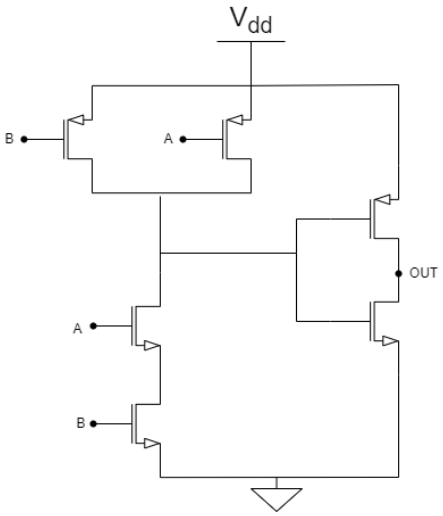

Figure 3.29: Schematic of the chosen AND gate topology

To size the transistors in the AND gate, all transistors was first set to have a length of 60 nm and a width of 120 nm, then the widths of the pmos transistors was increased through a parametric sweep to find the ration between the nmos and pmos transistor widhts that gave the most symmetric switching point. To test and verify the switching point symmetry, a DC analysis was conducted where one input was kept at 1.2 V while the other input was swept from 0 V to 1.2 V. The result of that sweep conducted on the circuit before PEX extraction is shown below.

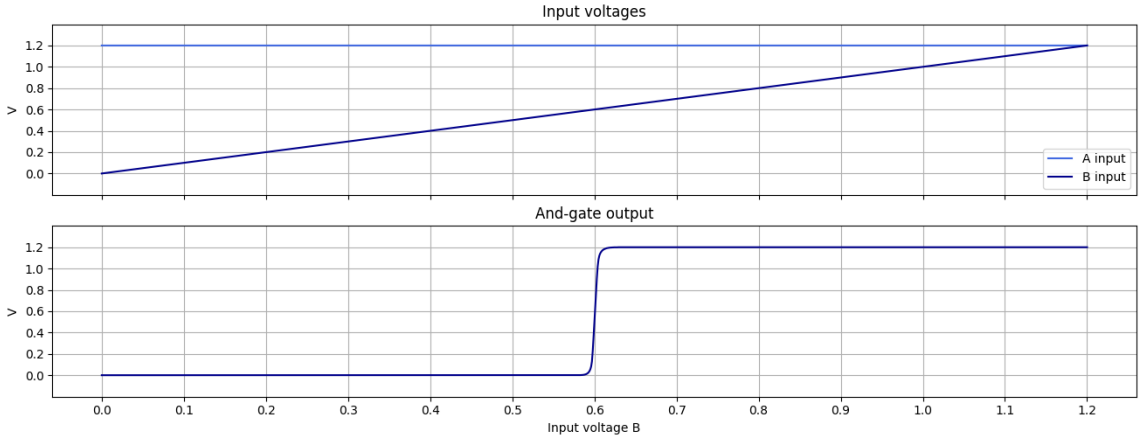

Figure 3.30: Input sweep of AND gate input voltage pre layout with 120 nm width

3.5.1 AND gate results

The final iteration of the AND gate uses transistors of length 60 nm. All pmos transistors has a width of 420 nm and all nmos transistors has a width of 200 nm. A schematic of the topology used in the AND gate together with the layout of the AND gate is shown below:

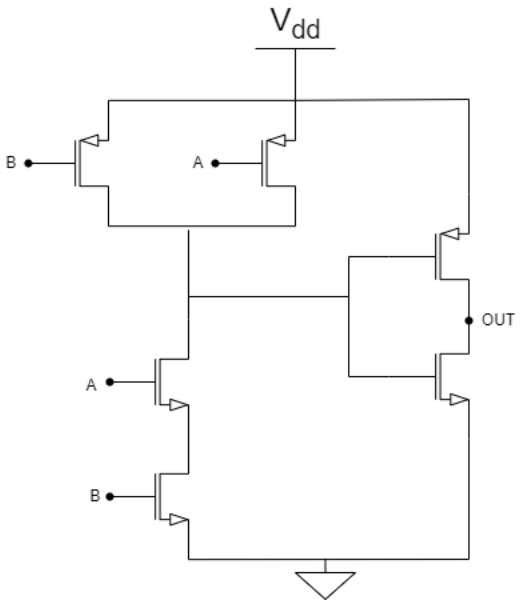

Figure 3.31: AND gate schematic

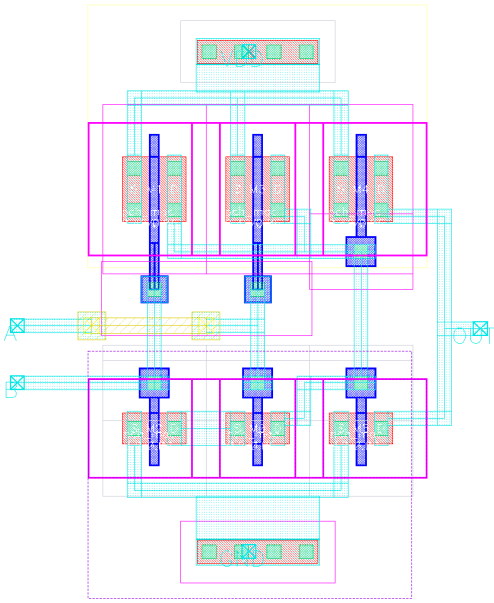

Figure 3.32: AND gate layout

Below are two plots showing the functionality of the AND gate, tested both before and after layout. Where both cases had a rise times of $\approx$ 1 ns to 2 ns which is sufficiently fast when compared to the system clock.

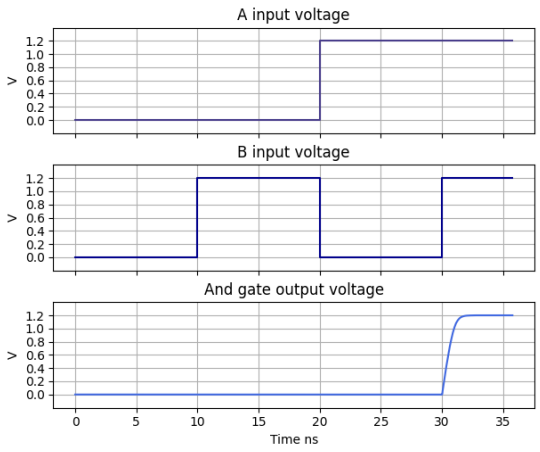

Figure 3.33: AND gate transient pre layout

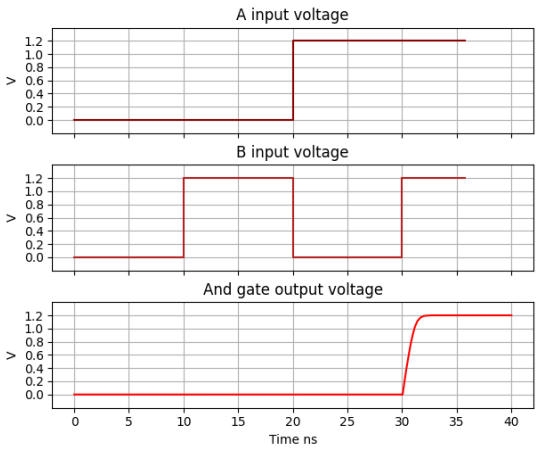

Figure 3.34: AND gate transient post layout

as shown in further detail in the plot below, a slight difference in the rise time of the AND gate can be seen in the post layout component.

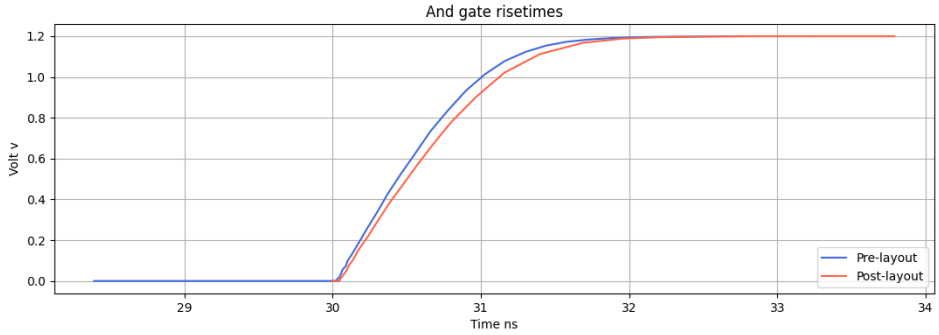

Figure 3.35: Rise time for pre vs post layout for AND gate

Another difference that was found when comparing the pre layout component with the post layout version is that the switching point during a DC analysis shifted $\approx 10\,\text{mV}$ downwards. A DC switching point analysis, like the one explained in section 3.5 of the pre and post layout component is shown below.

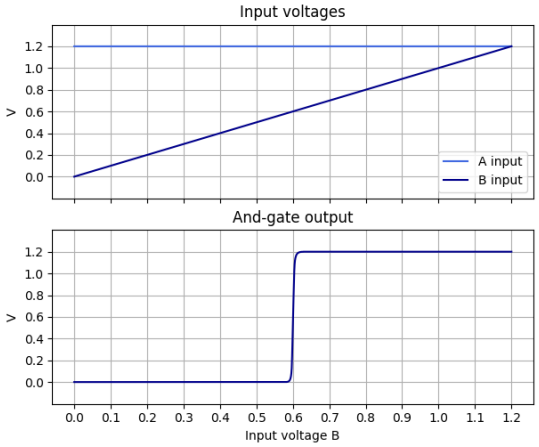

Figure 3.36: AND gate DC switching point pre layout

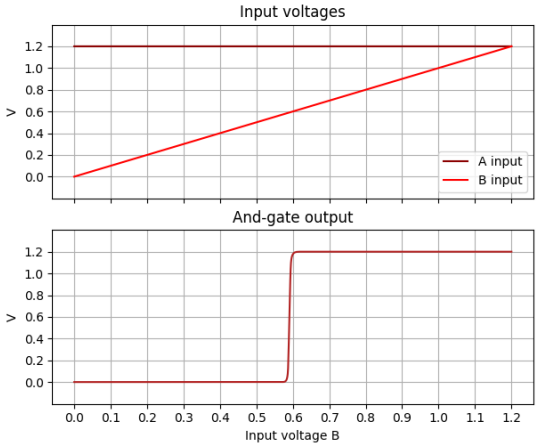

Figure 3.37: AND gate DC switching point post layout

As the figures above show, the pre vs post-layout is very similar which is the wanted result.

3.6 Transfer function for switch cap integrator with MDAC

From the fig. 3.1, the summing node, gain stage and the integrator is implemented as one component. This component consists of switching capacitors which holds and moves charges based on the concept of charge conservation:

$$\Delta Q = C \times \Delta V \tag{3.22}$$

Where C is constant and Q is changed when the voltage is changed over the capacitors.

The Multiplying digital to analog converter is integrated into the switch cap integrator where eq. (3.22) is used in the schematic from fig. 3.38.

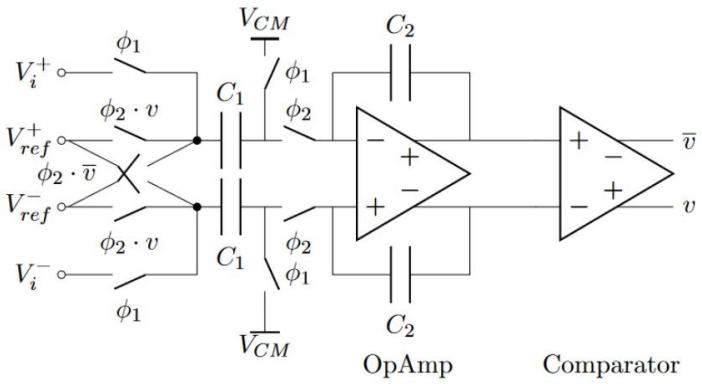

Figure 3.38: Full MDAC circuit with feedback [12]

When ϕ_1 is closed the charge Q_p^1 is shown as the red path and Q_n^1 is shown as the blue path in fig. 3.39 and is calculated using eq. (3.22):

$$Q_p^1 = (V_i^+[n-1] - V_{cm})C_1 + V_o^+[n-1]C_2$$
$$Q_n^1 = (V_i^-[n-1] - V_{cm})C_1 + V_o^-[n-1]C_2$$

Where the left side or positive side of the capacitors C_1 is $V_i^{+/-}$ and the right side or negative side is the common mode voltage which is constant, which means it is not a function of the sampling iteration "n". For the left side or negative side of C_2 there is a virtual ground, which means there is 0 V, while the right side or positive side is just the output of the OpAmp $V_o^{+/-}$.

The system is differential so the charge equation will be:

$Q_1 = Q_p^1 - Q_n^1 = V_i[n-1]C_1 + V_o[n-1]C_2$ [10]

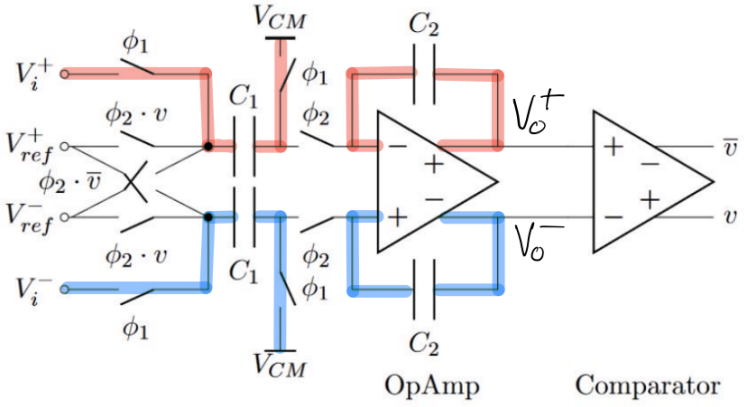

Figure 3.39: Full MDAC circuit with feedback when phi 1 is closed [12]

When ϕ_2 is closed the left side or positive side of C_1 will be either V_{ref}^+ or V_{ref}^-. If the output of the comparator is a logic "1", the V_{ref}^+ will be on the positive side of the capacitor in the red branch, and V_{ref}^- will for the blue path as shown in fig. 3.40. If it is a logic "0" on the output of the comparator, the V_{ref}^- will be connected to the positive side of the capacitor for the red path and the V_{ref}^- for the blue path as shown in fig. 3.41. The negative side or the right side will be connected to virtual ground. For the charge over C_2 it will remain the same as when ϕ_1 was closed. Mathematical explained as:

$$Q_p^2 = -V_{ref}(-1)^v C_1 + V_o^+[n]C_2$$
$$Q_n^2 = V_{ref}(-1)^v C_1 + V_o^-[n]C_2$$

Again due to the system being differential, the total charge when ϕ_2 is closed will be:

$$Q^2 = Q_p^2 - Q_n^2 = -2V_{ref}(-1)^v C_1 + V_o[n]C_2 \text{ [10]}$$

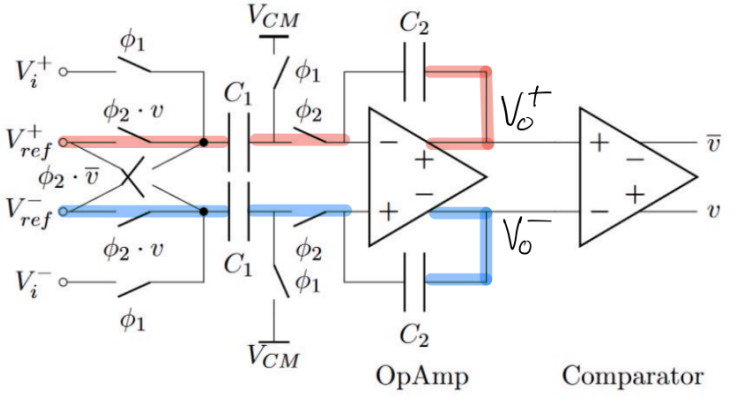

Figure 3.40: Full MDAC circuit with feedback when phi 2 is closed and $v = 1$ [12]

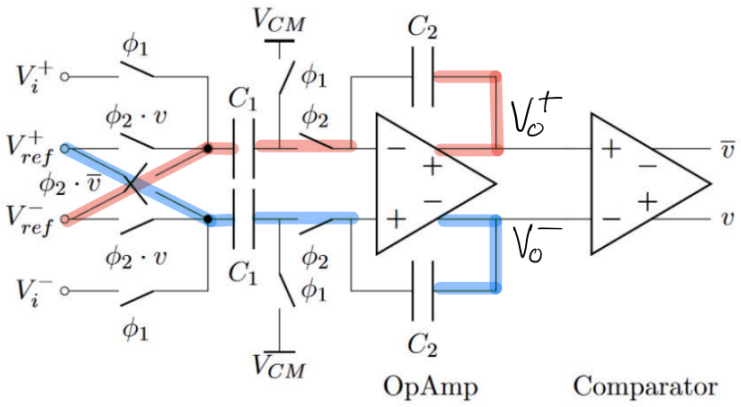

Figure 3.41: Full MDAC circuit with feedback when phi 2 is closed and $v = 0$ [12]

Using the conservation of charge, the charge in ϕ_1 must be the same as in ϕ_2:

$$Q^1 = Q^2 \iff -2V_{ref}(-1)^v C_1 + V_o[n]C_2 = V_i[n-1]C_1 + V_o[n-1]C_2$$

Solving for V_o:

$$V_o[n] = \frac{C_1}{C_2}V_i[n-1] + 2\frac{C_1}{C_2}V_{ref}(-1)^v + V_o[n-1]$$

Doing the Z transformation of the system to look at the response of the system:

$$V_o(z)(1-z^{-1}) = \frac{C_1}{C_2}(V_i(z)Z^{-1} + 2V_{ref}(-1)^v)$$

Solving for $V_o(Z)$:

$$V_o(z) = \frac{C_1}{C_2}[V_i(z)z^{-1} + 2(-1)^v V_{ref}] \times \frac{1}{1-z^{-1}} \text{ [10]}$$

Where the response $\frac{1}{1-z^{-1}}$ is the wanted low pass filter response and the Z^{-1} is a delay [19], which makes the system a delayed low pass filter with a gain equal to the ratio of the capacitors $\frac{C_1}{C_2}$.

3.6.1 Second order transfer function

As this system will be a second order, the transfer function will look like fig. 3.42.

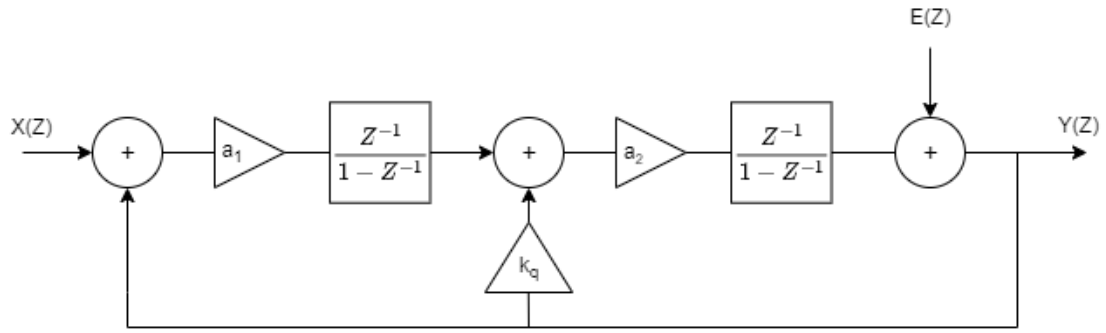

Figure 3.42: Second order ΔΣ block diagram with transfer function

In the fig. 3.42, the transfer function for the signal will be [10]:

$$H_X(Z) = \frac{a_1 a_2 Z^{-2}}{(1 - z^{-1})^2 + k_q a_2 Z^{-1}(1 - Z^{-1}) + a_1 a_2 Z^{-2}} \tag{3.23}$$

and the transfer function for the noise will be [10]:

$$H_{nq}(Z) = \frac{(1 - Z^{-1})^2}{(1 - z^{-1})^2 + k_q a_2 Z^{-1}(1 - Z^{-1}) + a_1 a_2 Z^{-2}} \tag{3.24}$$

To have the transfer function working as the intended way where the signal is delayed with the formula Z^{-2} and the noise transfer function is high pass filtered with $(1 - Z^{-1})^2$, the denominator for both eq. (3.23) and eq. (3.24) has to equal 1 [10]. This leads to what is previously explained in chapter 3.1 where $k_q a_2 = 2$ and $a_1 a_2 = 1$.

3.7 Final layout

The final layout of the ΔΣ is shown in fig. 3.43. This would have been a difficult part, but by making each component separately and building a hierarchy it was made easier. The final version of the schematic had a power consumption calculated as $P = V \times I$ where V is $V_{dd} = 1.2\,\text{V}$, and I is the current simulated to be 812 µA which comes to $P = 974.4\,\mu\text{W}$. This power consumption is relatively low compared to some average power distribution systems for satelites [8] . Something to notice is the outputs of the comparator has double inverts implemented. This is implemented to act as a buffer to drive the load better [7].

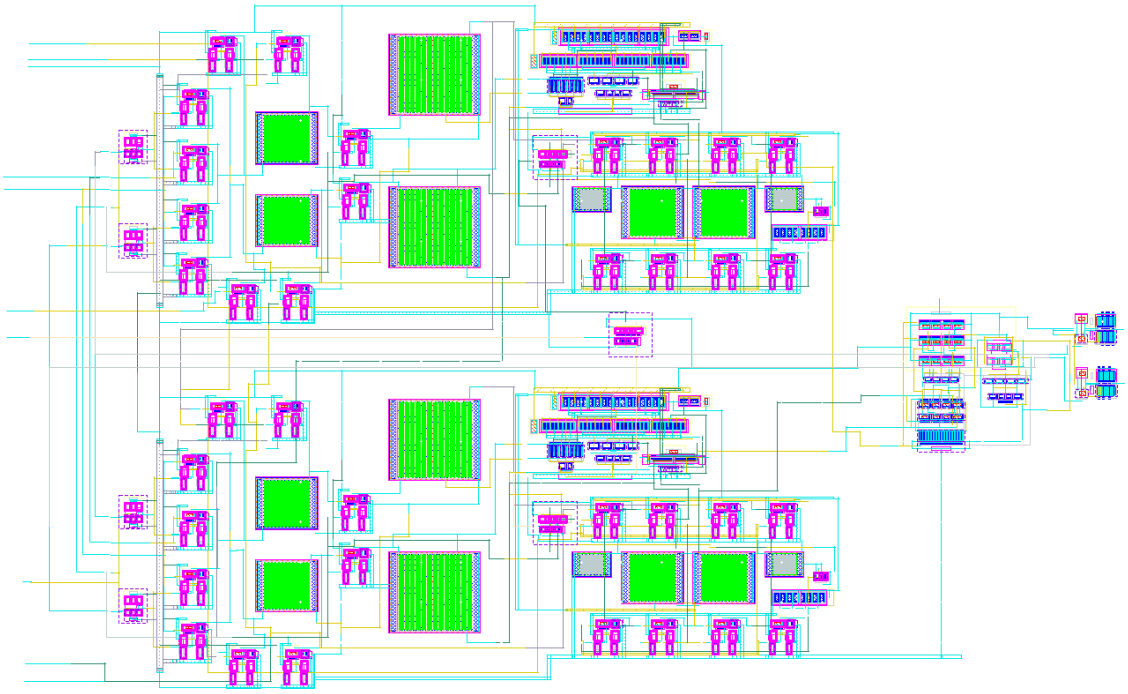

Figure 3.43: Full layout of ΔΣ modulator

Chapter 4

Results

4.1 Simulation results

The output of the ΔΣ is a one bit quantization which is either a 1 or a 0. The bit stream output is shown in fig. 4.1 and fig. 4.2 and the density of the 1's and 0's is what decides the resolution of the ADC. In the figure the density of 1's is much higher at higher voltages and the density of 0's is higher at lower voltages.

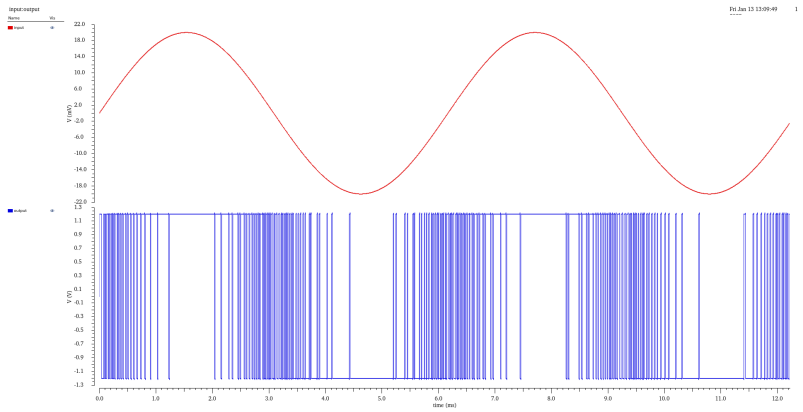

Figure 4.1: Output for a transient simulation of the ΔΣ modulator with constant sample speed

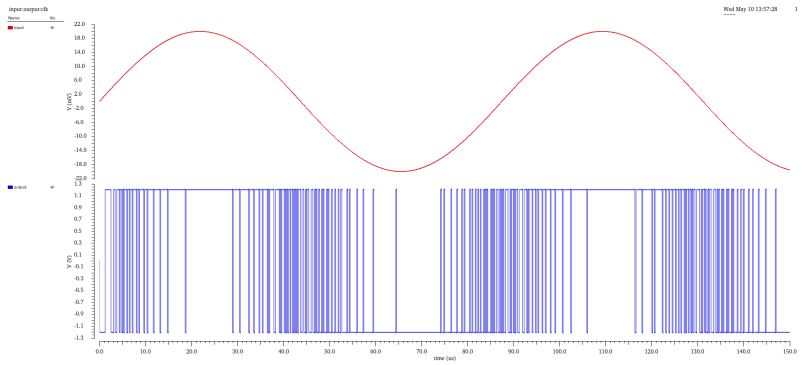

Figure 4.2: Output for a transient simulation of the ΔΣ modulator with constant data stream

To ensure it works for worst cases, a corner simulation was used. All the corner simulations was tested, however fig. 4.3 is the result which deviates the most from the typical value. The simulation time is less than in fig. 4.1 due to extremely long waiting time for the simulation. The post layout extraction is also tested with all the corner simulations, but the typical value is shown in fig. 4.4. The output is still a bit stream which has a higher 1's density at higher voltages and higher 0's density for lower voltages, but it is a little delayed from the peaks. This simulation will ensure that when the chip is fabricated, due to some error margins in the fabrication process, the chip will still work.

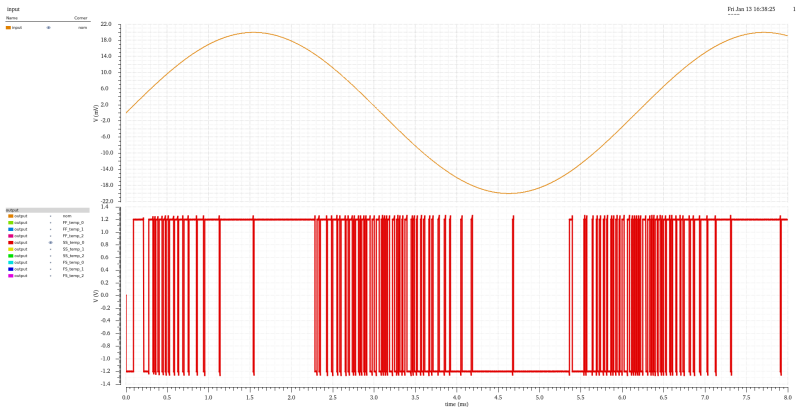

Figure 4.3: Corner simulation of the output of the ΔΣ modulator

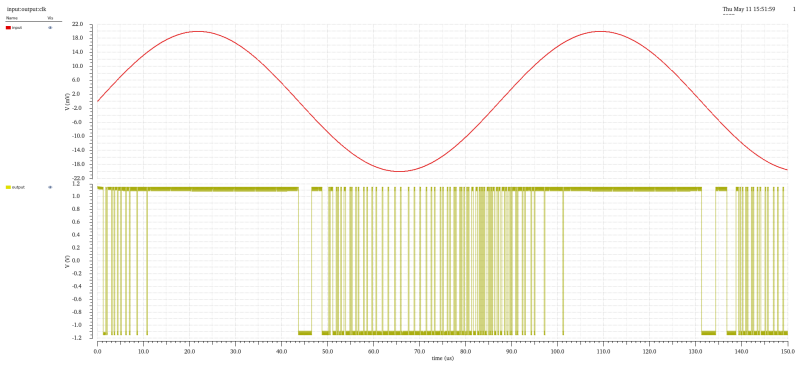

Figure 4.4: PEX simulation of the output of the ΔΣ modulator

In fig. 4.5, the signal has a peak at the input signal frequency and then the noise is shifted to a higher frequency with 40 db/decade slope. This is what was wanted which is called noise shaping and this will yield a higher SNR which again will impact the resolution of the ADC. This simulation was a transient simulation with a time of about half a second. To get a better plot, the time of the simulation has to increase, but due to the simulation stopping if the connection to Internet is lost, it was found to be very difficult.

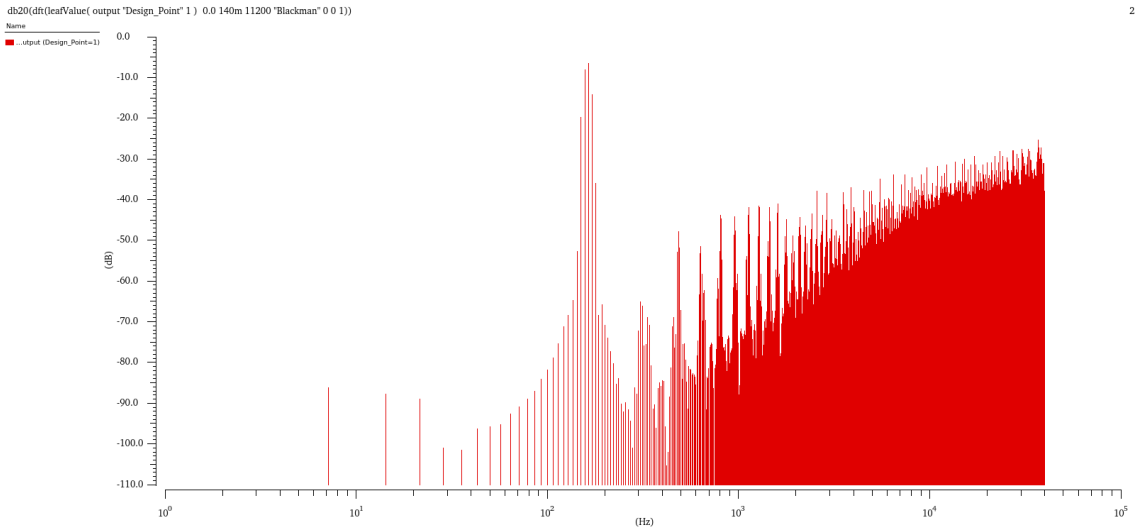

Figure 4.5: Noise shaping plot

4.2 PCB design for testing the chip

To test the chip created, a PCB was made. This chip contains the chip with the JCL44 package, decoupling capacitors and two level shifters for the clock, which will be generated from a FPGA. The PCB was designed using a program called KiCad, in the schematic the chip and level shifter has a custom design to have an easier time connecting the correct pins. The footprints are found in KiCad for each of the components which was used. The decoupling capacitors are as close to the chip as possible to maximize the decoupling effect. Some capacitors are connected very close to the level shifters as well as it was recommended in the datasheet. The PCB has a ground plane and a 1.2 V plane to have easy access to the respected connections which will lead to less traces.

The level shifters used are called TXU0101-Q1 which can input/output voltages from 1.1V to 5.5V which is wanted for this application. The wanted scenario is 5V clock is generated from an FPGA connected to the PCB which will be shifted down to 1.2V which the chip uses as a clock. Two level shifters are needed for the two non overlapping clocks.

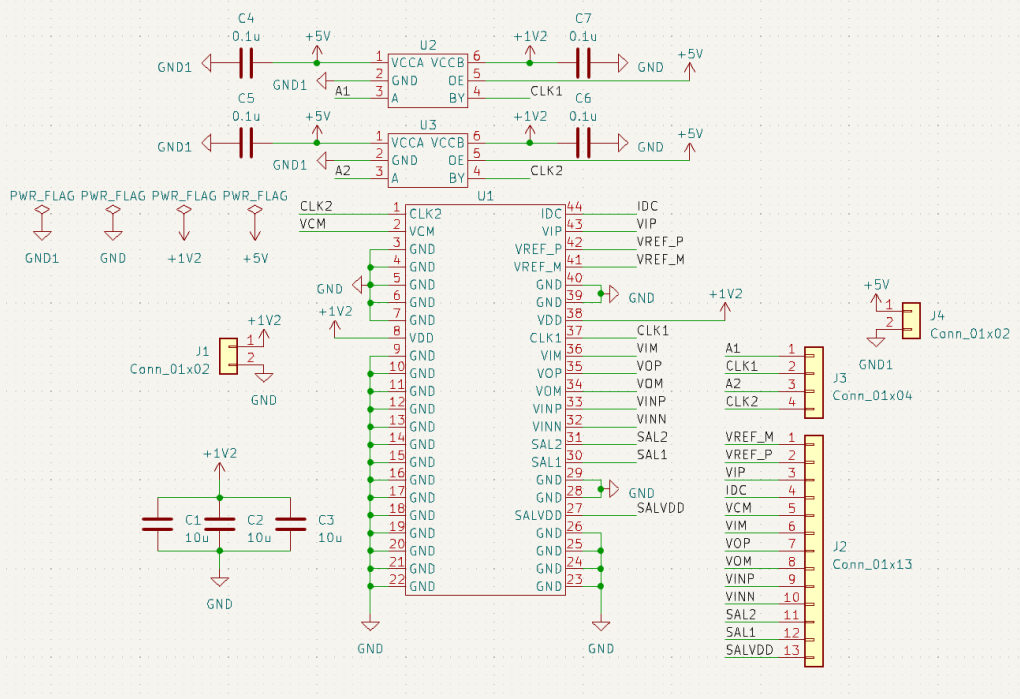

Figure 4.6: Schematic of the test PCB

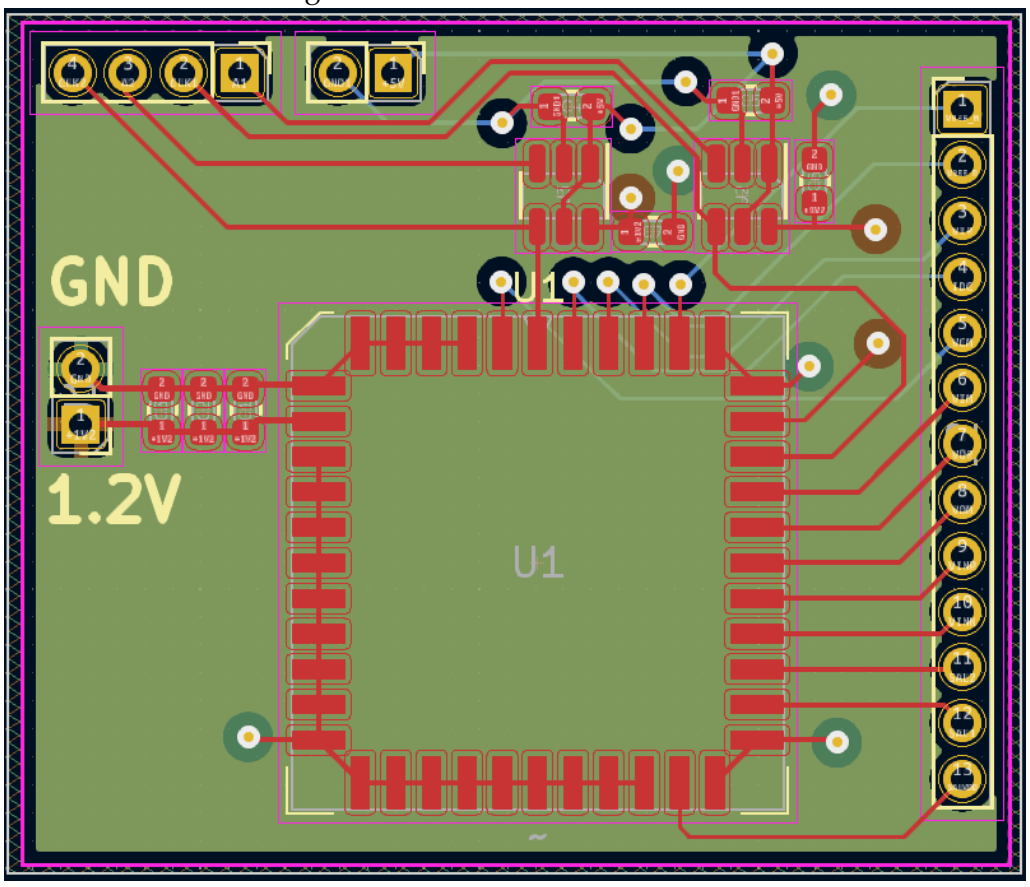

Figure 4.7: Layout of the test PCB

4.3 Chip results

To verify that the chip worked, testing was done on the chip in the lab using the PCB made and clock generator from the FPGA. While testing the chip, different amplitudes for the input signal was used, but not saved for plotting. Due to the chip "dying" no data was plotted and not a lot of testing was made, however some simple pictures from the phone shown in fig. 4.8 shows that the chip was able to get out a bit stream.

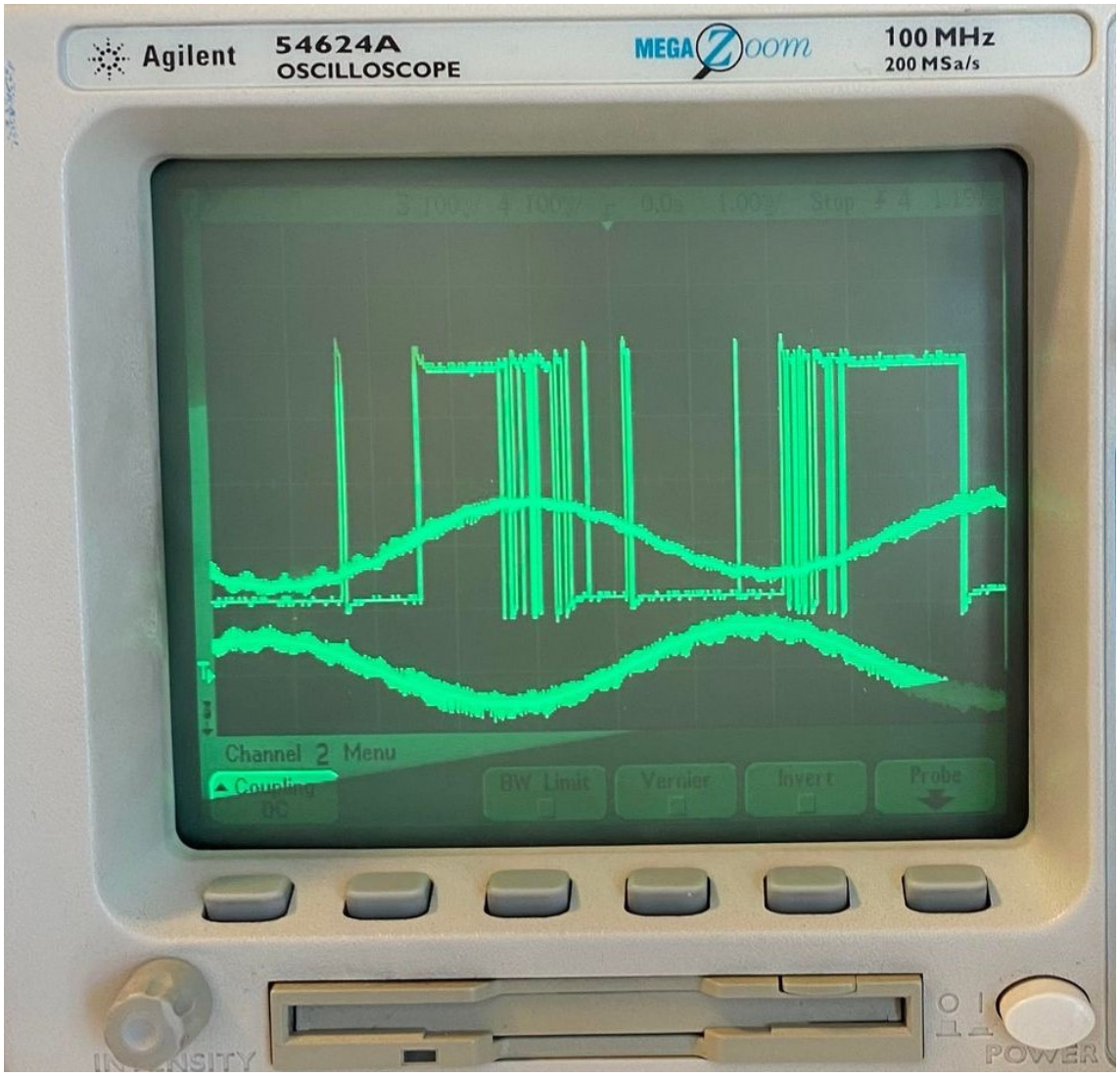

Figure 4.8: Input and output of the chip made

Chapter 5

Discussion and future work

5.1 Topology choice

As mentioned in the introduction chapter, the sampling frequency was chosen from 20 kHz $\times$ 4 or 80 kHz $\times$ 1. It was chosen to be 80 kHz due to the frequency is relatively low either way. However the area used for the current $\Delta\Sigma$ is also very small, meaning four of these could be implemented and used as 20 kHz $\times$ 4 which would yield better bit resolution. The sample frequency comes from a multiplexing system which a SAR ADC is proven to be be more suitable for [16], but it requires a bigger area.

5.2 Layout

The layout has not been extensively optimized. Place and route could be improved to reduce interconnection length and thus parasitic capacitance. Supply lines should be thicker to avoid any danger of a supply voltage gradient. Common centroid layout has already been used to match critical pairs/arrays of devices. However, adding dummy devices around these matched structures to have uniform neighbourhood conditions could improve matching further. Better shielding/separation of slow analog signals from fast digital signals could reduce cross talk [6].

5.3 Testing the chip

When ordering the chip, there was some miscommunication which lead to the chip comming without the package, however eLAB was able to wire bond the naked chip to my chip socket on the PCB. Due to time constraints and lack of chips for testing i was not able to get much results. However i was able to do some testing before the chip died and it has the potential to work as in the simulations. More testing needs to be done, and hopefully i will have more results when i defend the master thesis.

The pictures shown as results in the appendix are indeed a bit stream, however it is not as good as the simulation results. I suspect that some of the voltages used are too small and it is in the range of noise levels. I cannot conclude much with the current data other than that the chip can give out a bit stream, but more testing will show if the chip is as good as the simulations.

5.4 Test more stand-alone components on the chip

Testability is notoriously underestimated in student's first ever tape-out, something I quickly realized when planning and starting the circuit testing. The modules used in the project could be added as stand-alone elements to the chip but placed and tested alone to check if they work alone. This can be very helpful when troubleshooting on the chip.

5.5 Decimation filter

A decimation filter has not been in the scope of this project, but would need to be added to complete the ADC design. To verify the resolution of the ADC, the decimation filter will hopefully output a signal that reconstructs the input signal.

5.6 Monte Carlo simulation

Monte Carlo simulation is a mathematical technique that predicts possible outcomes of uncertain events [1], this is very helpful for designing IC's. However the reason it was not done in this thesis is its long simulation time. As explained in the corner simulation, the simulations can take multiple days for a millisecond of transient simulation, which was difficult to do.

Chapter 6

Conclusion

The main objective of this thesis was to design the ADC for the multi-need Langmuir probe which is used to predict space weather like solar storms which can cause damage to satelites and global positioning systems. When doing so i look at the different types of ADC's and chose the Delta Sigma ADC which has the ability to give high bit resolution using its principles of oversampling and noise shaping.

The design part is done in the program Cadence which is used for schematic, simulations, layout and post layout simulations. Using Cadence I built up each module in a hierarchy and test each of these modules alone. When every module was tested I connected each module together to make the final second order Delta Sigma. By looking at the output results a bit stream with a high density of 1's at higher voltages and a high density of 0's at lower voltages can be seen. Corner simulations was done to verify that the physical chip will work in the same way as the simulations. This is also tested when doing the post layout extraction. Finally a FFT is used for the bit stream and it is confirmed that the noise shaping works by seeing a 40 dB / decade slope after the input spike.

Due to issues with the chip arriving for testing very late, few tests was done on the chip. I was able to confirm that it is not short circuited and is able to give out a bit stream, but more testing is needed to verify the results of the chip.

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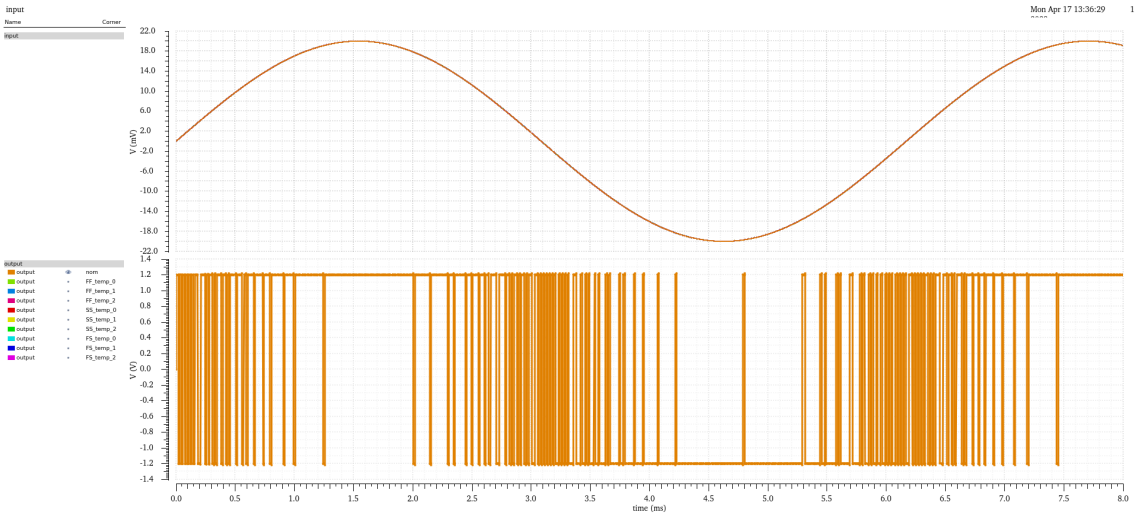
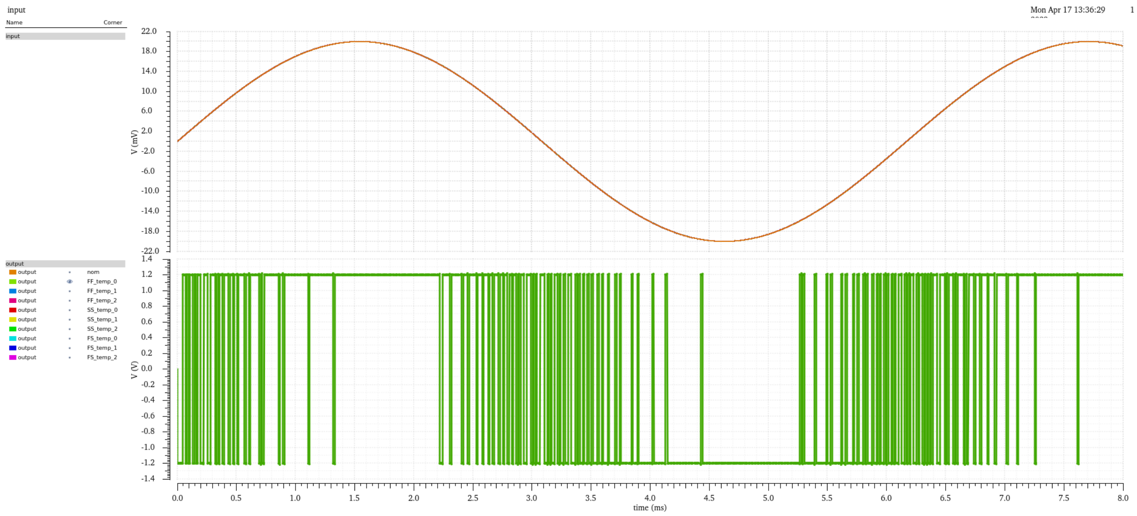
Appendices

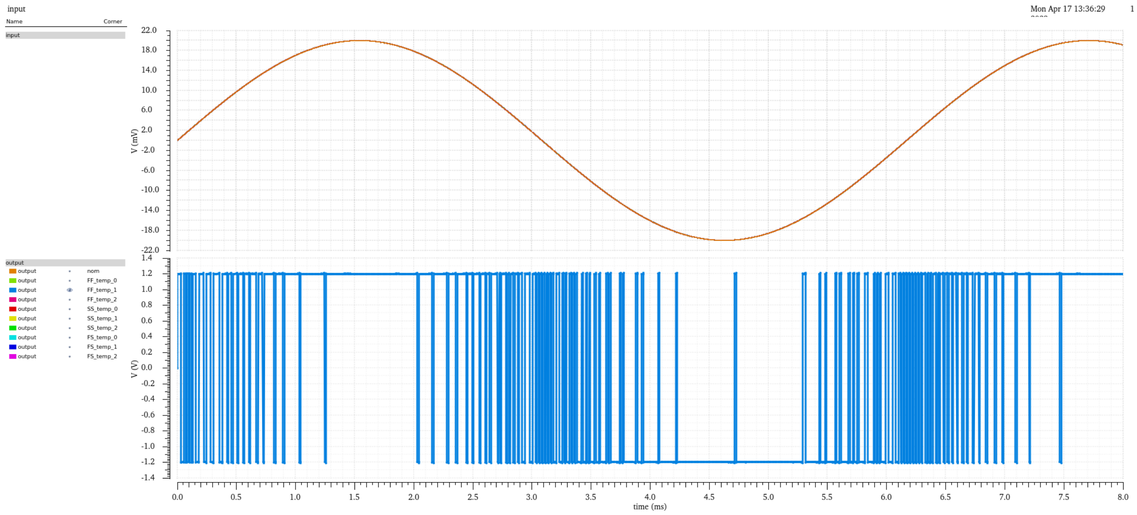
Appendix A

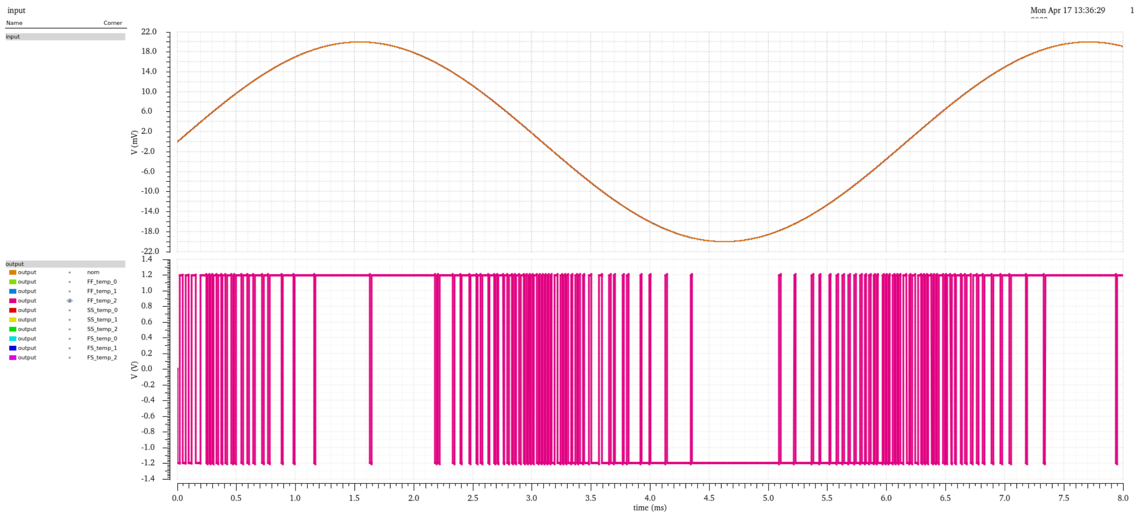
Corner Simulations

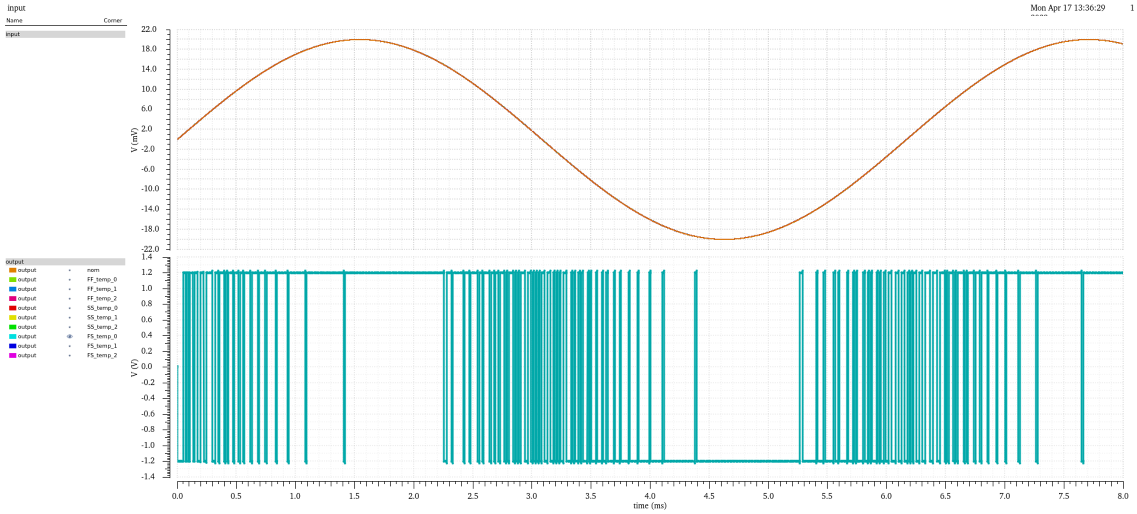
Corner simulations with "normal" speed, fast speed and slow speed for the n and p type transistors. Each configuration is also tested for different temperatures ranging -40 to 80 °C. The last 9 corner simulations are tested with post layout extraction with the constant data stream values.

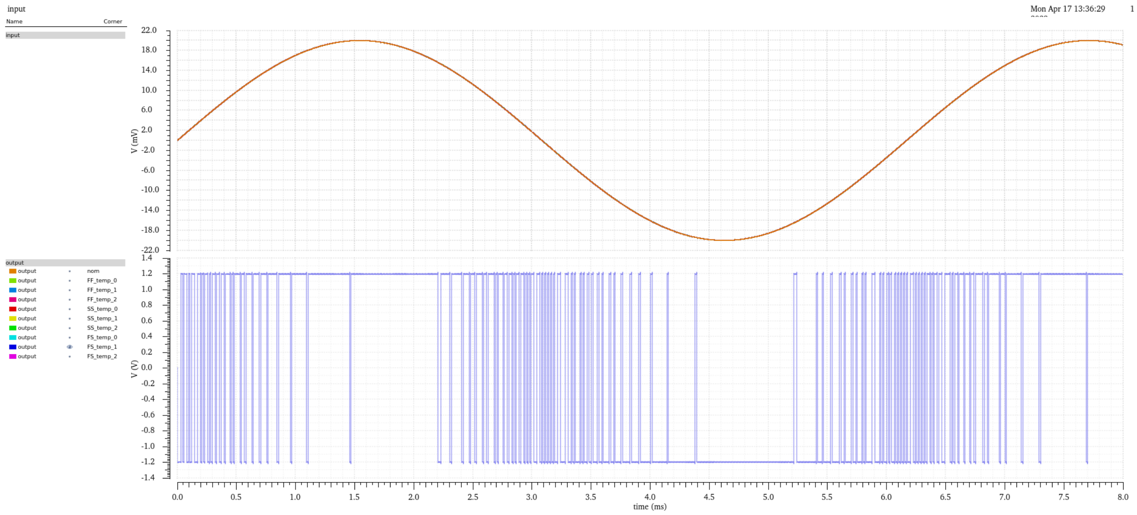


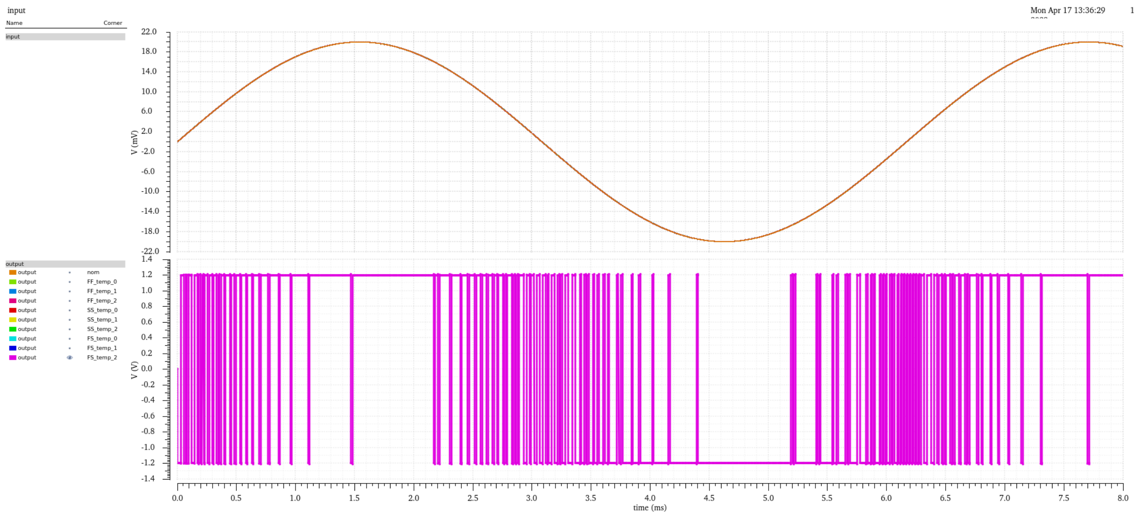

input
Name
Corner
input
Mon Apr 17 13:36:29
1
V (mV)
output
nom
FF_temp_0
FF_temp_1
FF_temp_2
SS_temp_0
SS_temp_1
SS_temp_2
FS_temp_0
FS_temp_1
FS_temp_2
V (V)
time (ms)

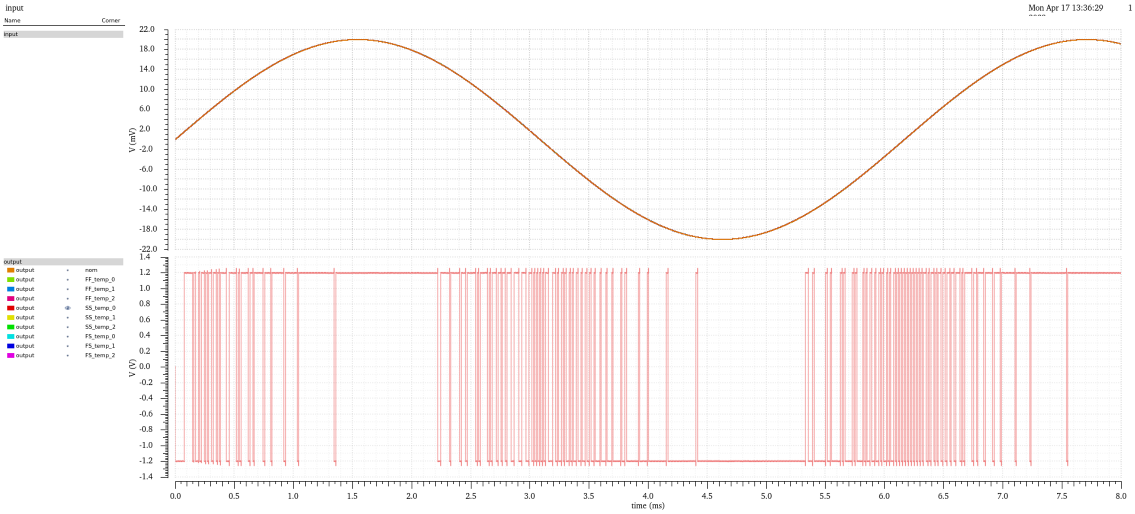

input
Name
Corner
input
Mon Apr 17 13:36:29
1
V (mV)
output
nom
FF_temp_0
FF_temp_1
FF_temp_2
SS_temp_0
SS_temp_1
SS_temp_2
FS_temp_0
FS_temp_1
FS_temp_2
V (V)
time (ms)


input
Name
Corner
input
Mon Apr 17 13:36:29
1
V (mV)
output
nom
FF_temp_0
FF_temp_1
FF_temp_2
SS_temp_0
SS_temp_1
SS_temp_2
FS_temp_0
FS_temp_1
FS_temp_2
V (V)
time (ms)

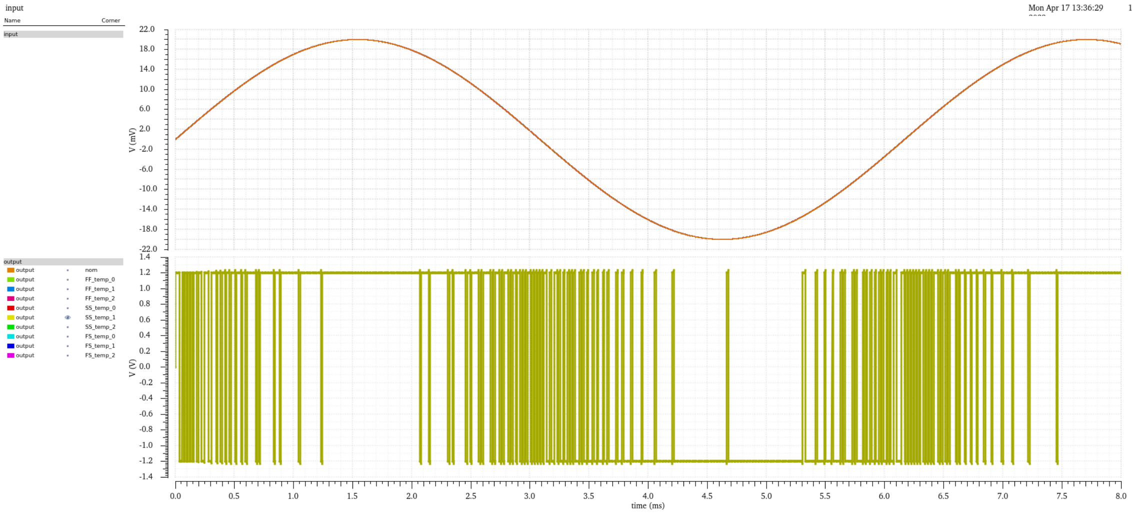

input
Name
Corner
Mon Apr 17 13:36:29
1
V (mV)
output
V (V)
time (ms)


input
Name
Corner
Mon Apr 17 13:36:29
1
V (mV)
output
V (V)
time (ms)

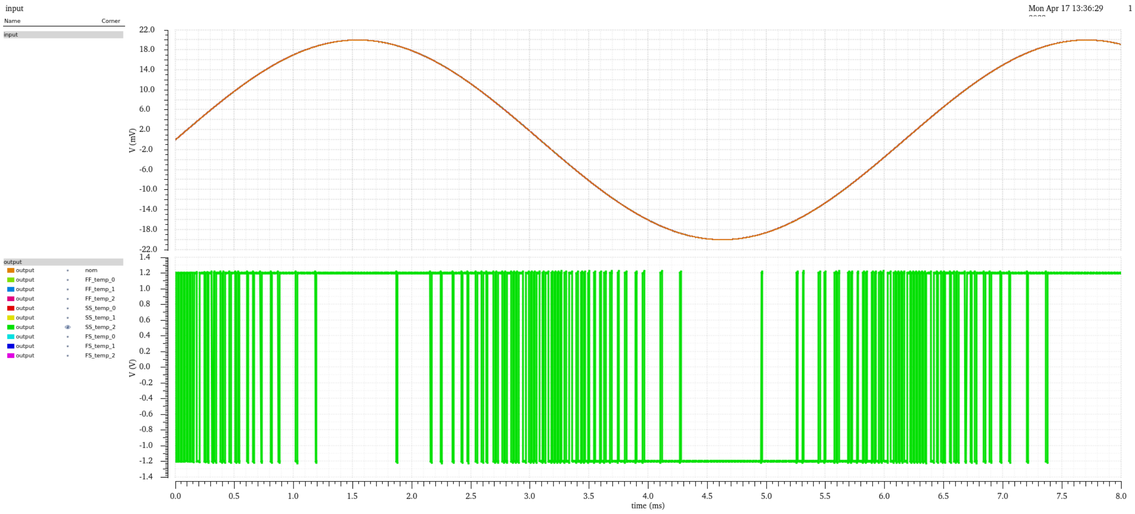

input
Name
Corner
Mon Apr 17 13:36:29
1
V (mV)
output
V (V)
time (ms)



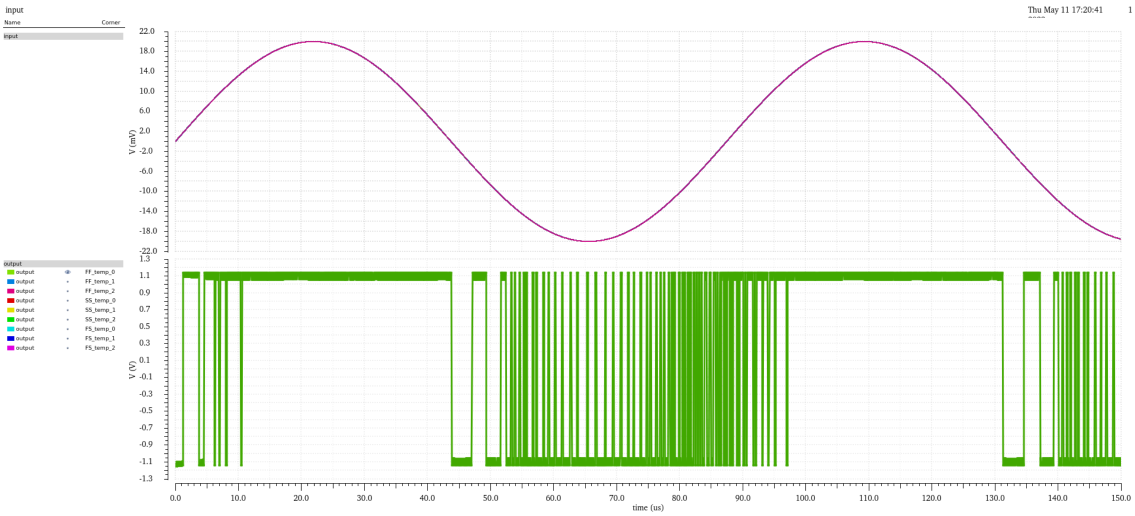
input
Name
Corner
Mon Apr 17 13:36:29
V (mV)
V (V)
output
time (ms)

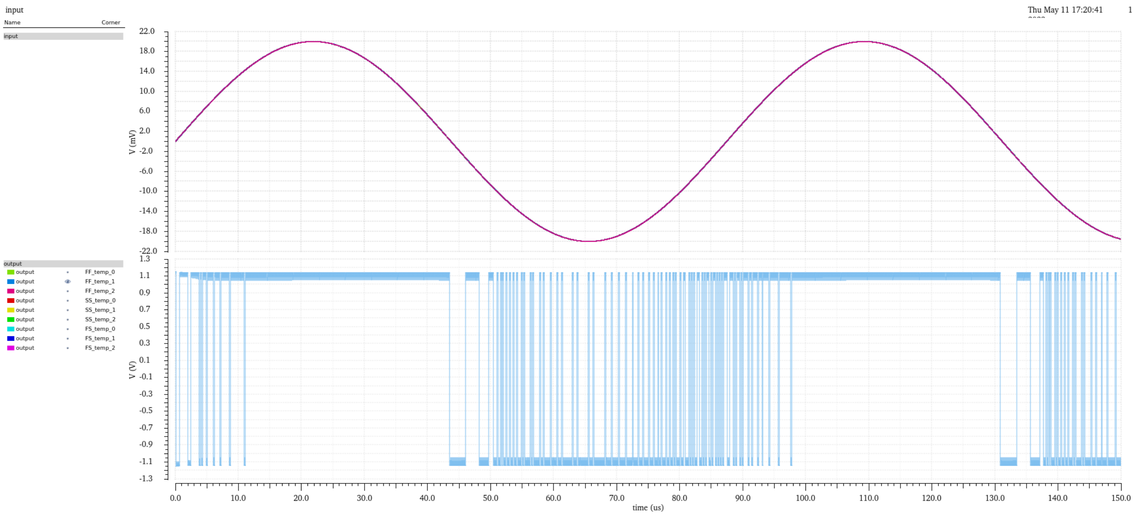


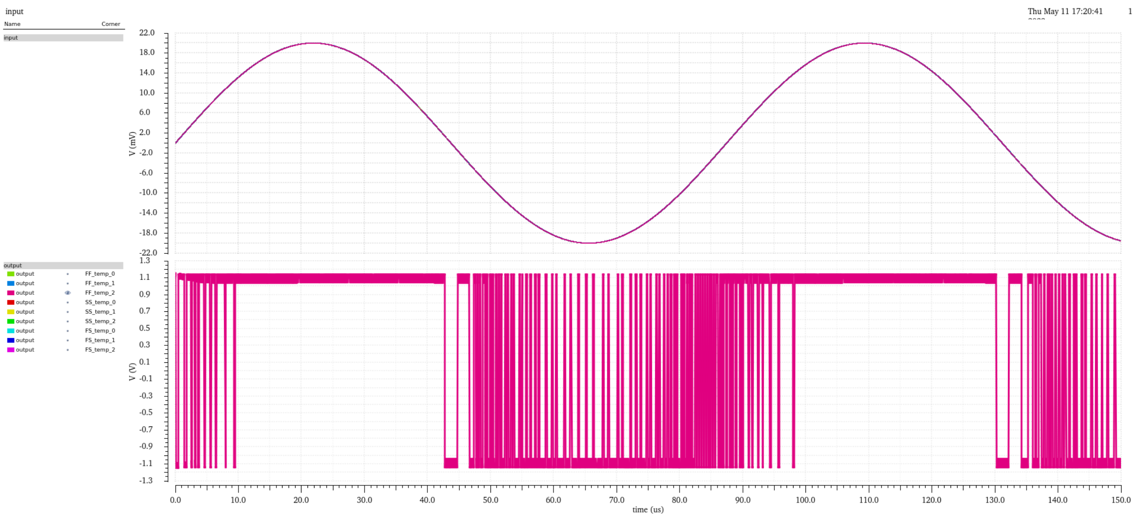
input
Name
Corner
Mon Apr 17 13:36:29
V (mV)
V (V)
output
time (ms)

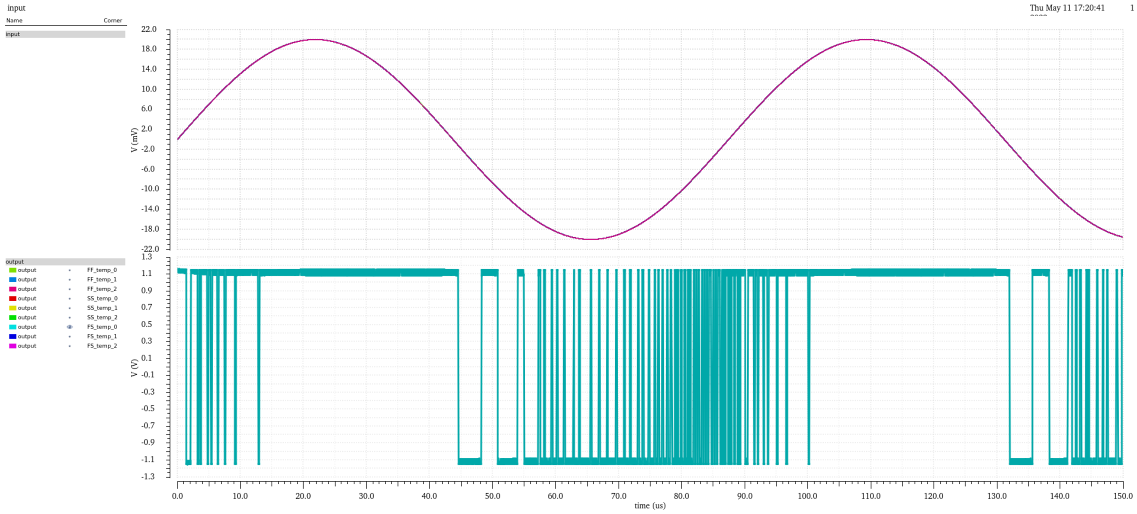


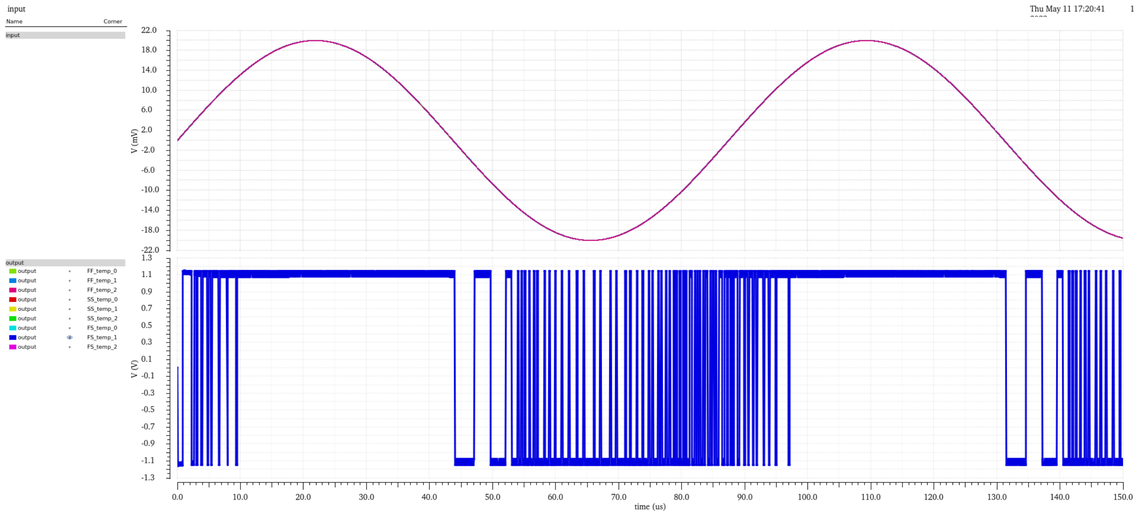
input
Name
Corner
Mon Apr 17 13:36:29
V (mV)
V (V)
output
time (ms)

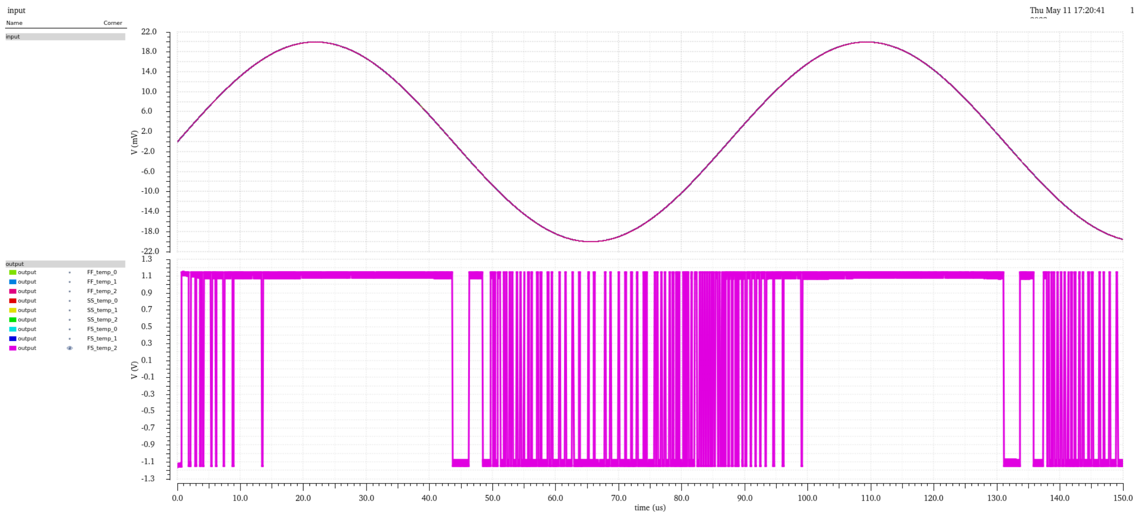

input
Name
Corner
Thu May 11 17:20:41
V (mV)
output
FF_temp_0
FF_temp_1
FF_temp_2
SS_temp_0
SS_temp_1
SS_temp_2
FS_temp_0
FS_temp_1
FS_temp_2
V (V)
time (us)

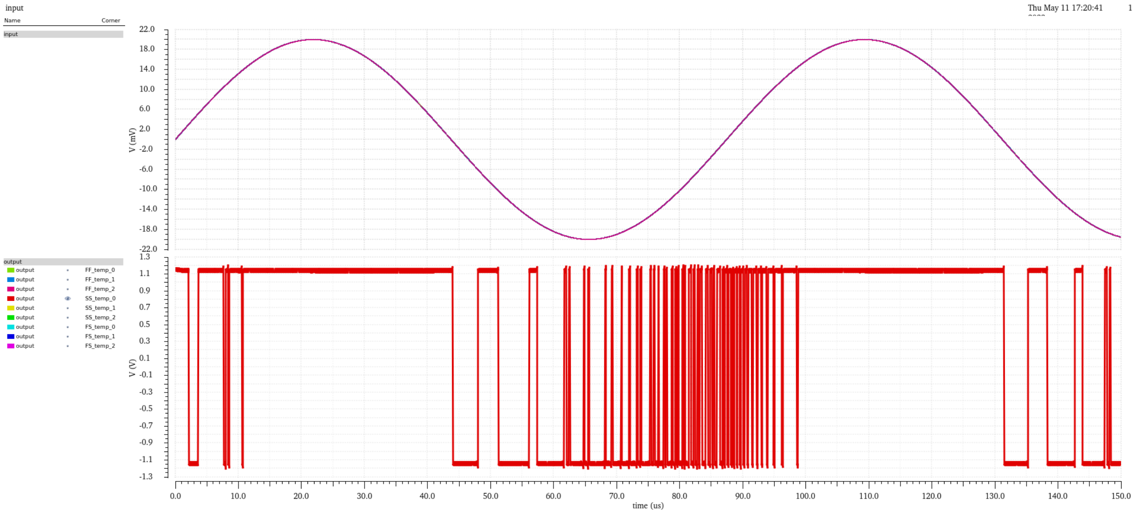

input
Name
Corner
Thu May 11 17:20:41
V (mV)
output
FF_temp_0
FF_temp_1
FF_temp_2
SS_temp_0
SS_temp_1
SS_temp_2
FS_temp_0
FS_temp_1
FS_temp_2
V (V)
time (us)

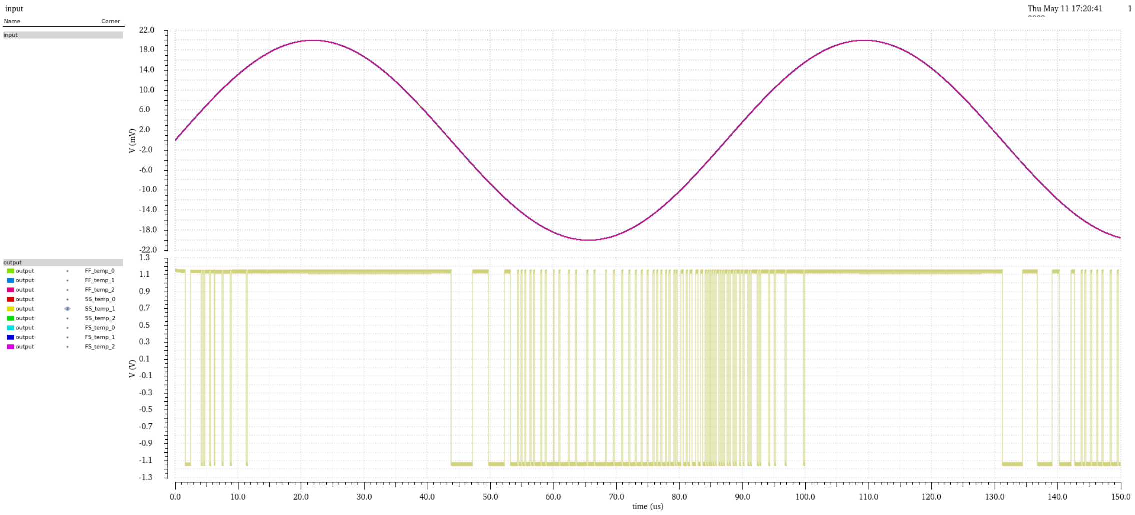

input
Name
Corner
Thu May 11 17:20:41
V (mV)
output
FF_temp_0
FF_temp_1
FF_temp_2
SS_temp_0
SS_temp_1
SS_temp_2
FS_temp_0
FS_temp_1
FS_temp_2
V (V)
time (us)

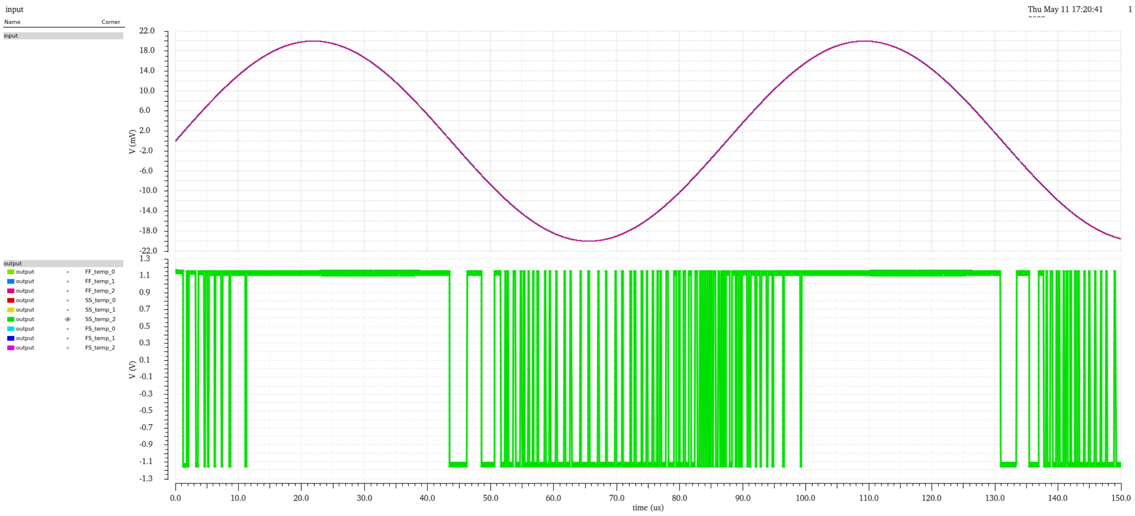

input
Name
Corner
input
Thu May 11 17:20:41
1
V (mV)
output
FF_temp_0
FF_temp_1
FF_temp_2
SS_temp_0
SS_temp_1
SS_temp_2
FS_temp_0
FS_temp_1
FS_temp_2
V (V)
time (us)


input
Name
Corner
input
Thu May 11 17:20:41
1
V (mV)
output
FF_temp_0
FF_temp_1
FF_temp_2
SS_temp_0
SS_temp_1
SS_temp_2
FS_temp_0
FS_temp_1
FS_temp_2
V (V)
time (us)


input
Name
Corner
input
Thu May 11 17:20:41
1
V (mV)
output
FF_temp_0
FF_temp_1
FF_temp_2
SS_temp_0
SS_temp_1
SS_temp_2
FS_temp_0
FS_temp_1
FS_temp_2
V (V)
time (us)


input
Thu May 11 17:20:41
V (mV)
V (V)
time (us)


input
Thu May 11 17:20:41
V (mV)
V (V)
time (us)


input
Thu May 11 17:20:41
V (mV)
V (V)
time (us)

Appendix B

VHDL and TCL code

VHDL code used to make two non-overlapping clocks on the DE10-Lite board which is used to test the PCB.

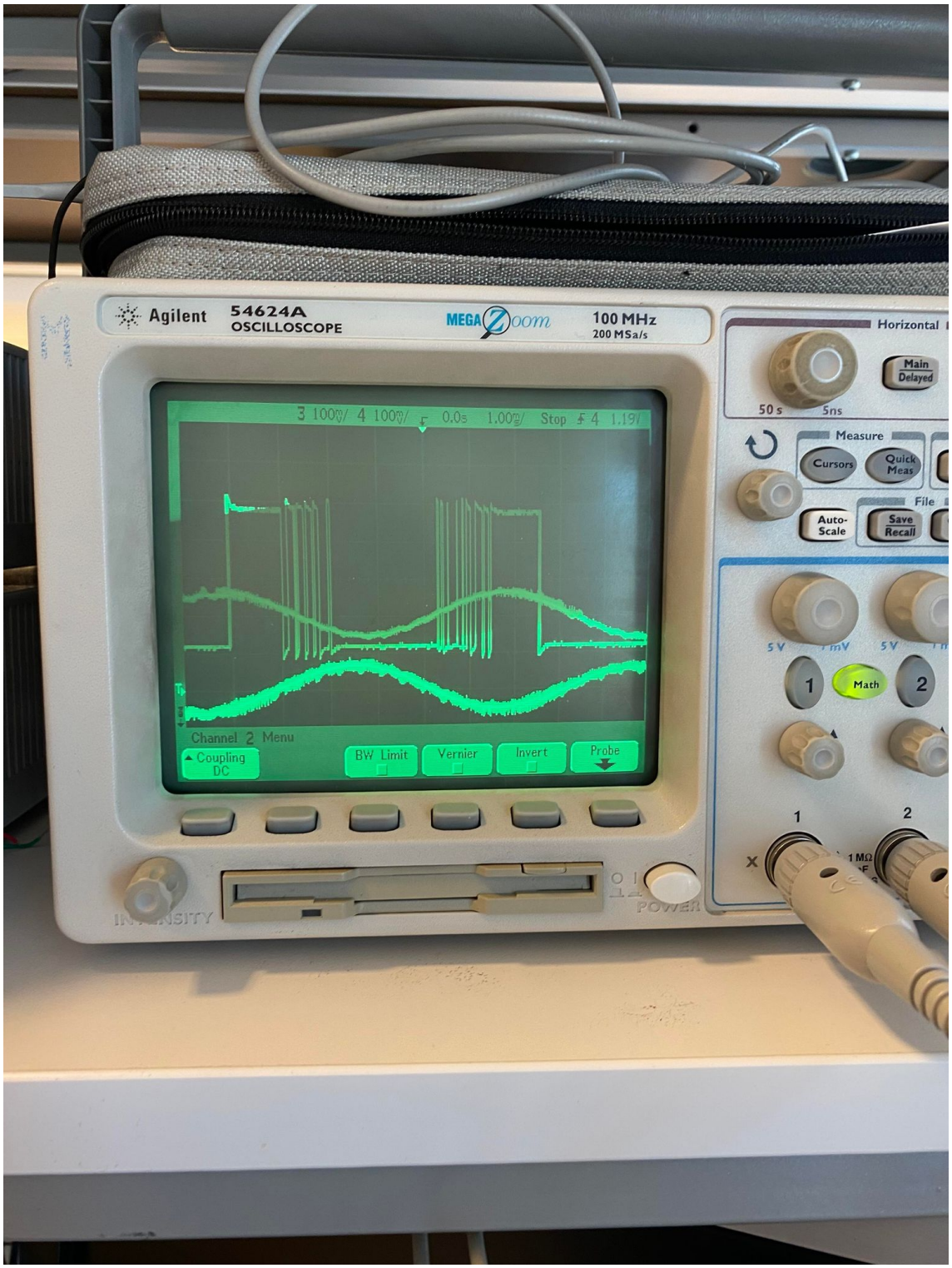
```
library IEEE;
use IEEE.std_logic_1164.all;
use ieee.numeric_std.all;

entity DSM_clock is
  port (

    clk : in std_logic;

    DSM_clock_1 : out std_logic;
    DSM_clock_2 : out std_logic
  );
end entity DSM_clock;

architecture top_level of DSM_clock is

  signal    counter : unsigned (9 downto 0) := "0000000000";
  signal         DSM_clock_1_p : std_logic;

constant fpga_clock : integer := 50000000; -- 50 MHz clock
constant clk_out : integer := 80000;      -- 80KHz clock
constant clk_ratio : integer := fpga_clock/clk_out; -- frequency ratio

begin

DSM_clock_1 <= DSM_clock_1_p;
DSM_clock_2 <= not(DSM_clock_1_p);

  p_uart_tx : process (clk)
  begin

    if rising_edge(clk) then
        counter <= counter + 1;

        if counter < clk_ratio/2 then
          DSM_clock_1_p <= '0';
        else
          DSM_clock_1_p <= '1';
        end if;

        if counter = clk_ratio - 1 then
          counter <= "0000000000";
        end if;

    end if;
  end process;
end architecture top_level;
```

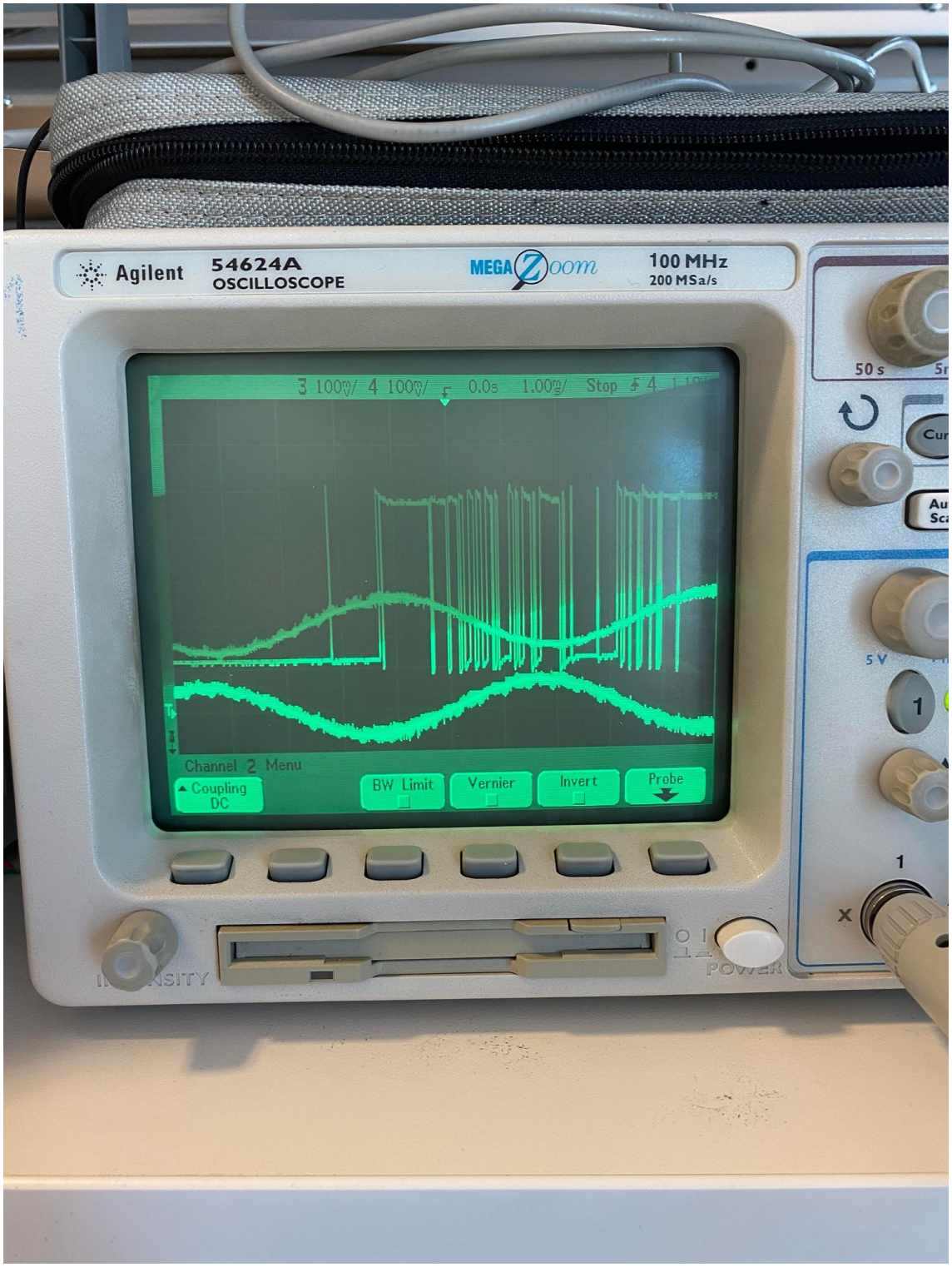
TCL file to assign the correct pins.

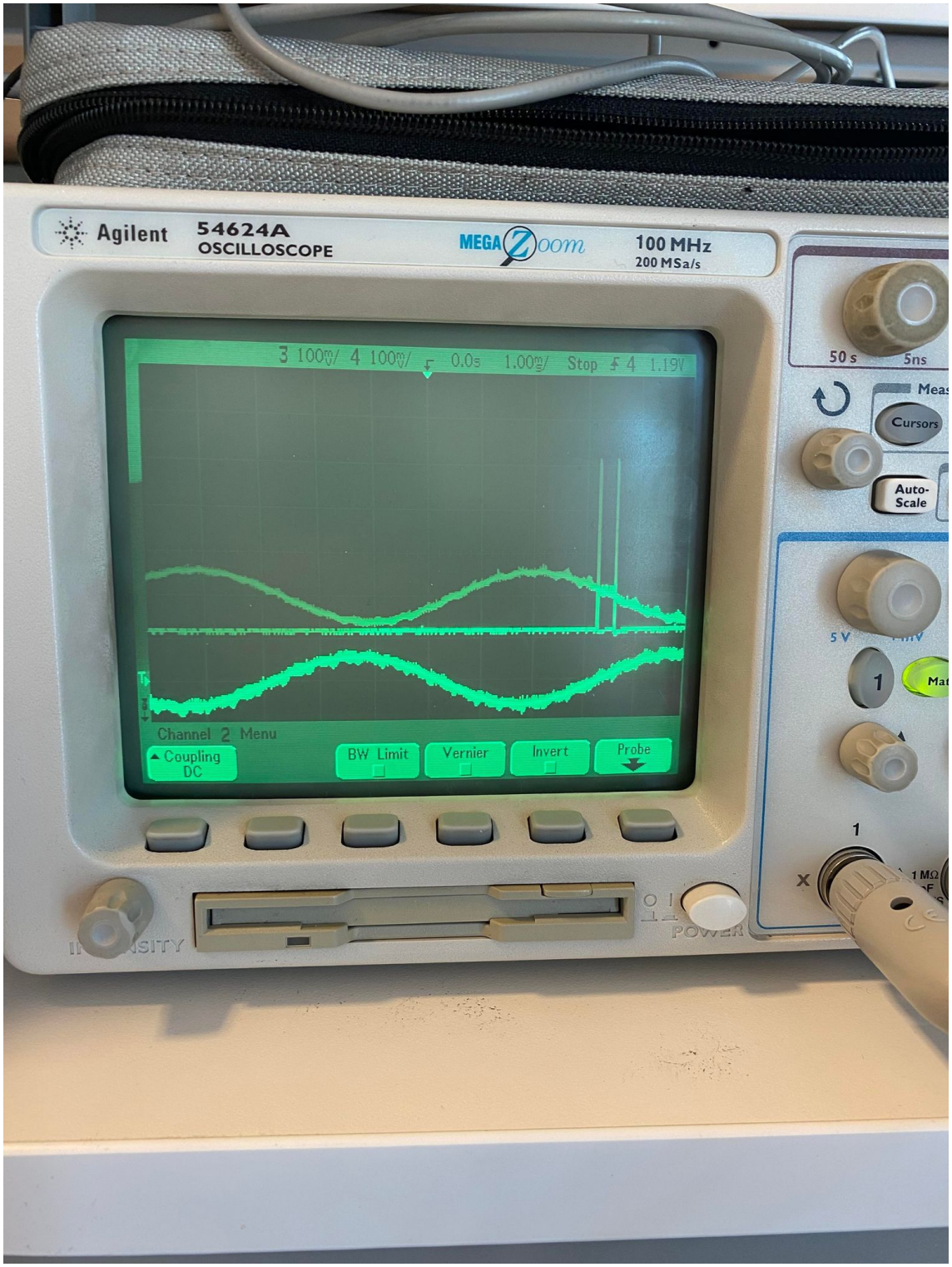
```
#clock in
set_location_assignment PIN_P11 -to clk

# clock outputs
set_location_assignment PIN_V10 -to DSM_clock_1
set_location_assignment PIN_W10 -to DSM_clock_2

#To avoid that the FPGA is driving an unintended value on pins that are not in use:
set_global_assignment -name RESERVE_ALL_UNUSED_PINS "AS INPUT TRI-STATED"
```

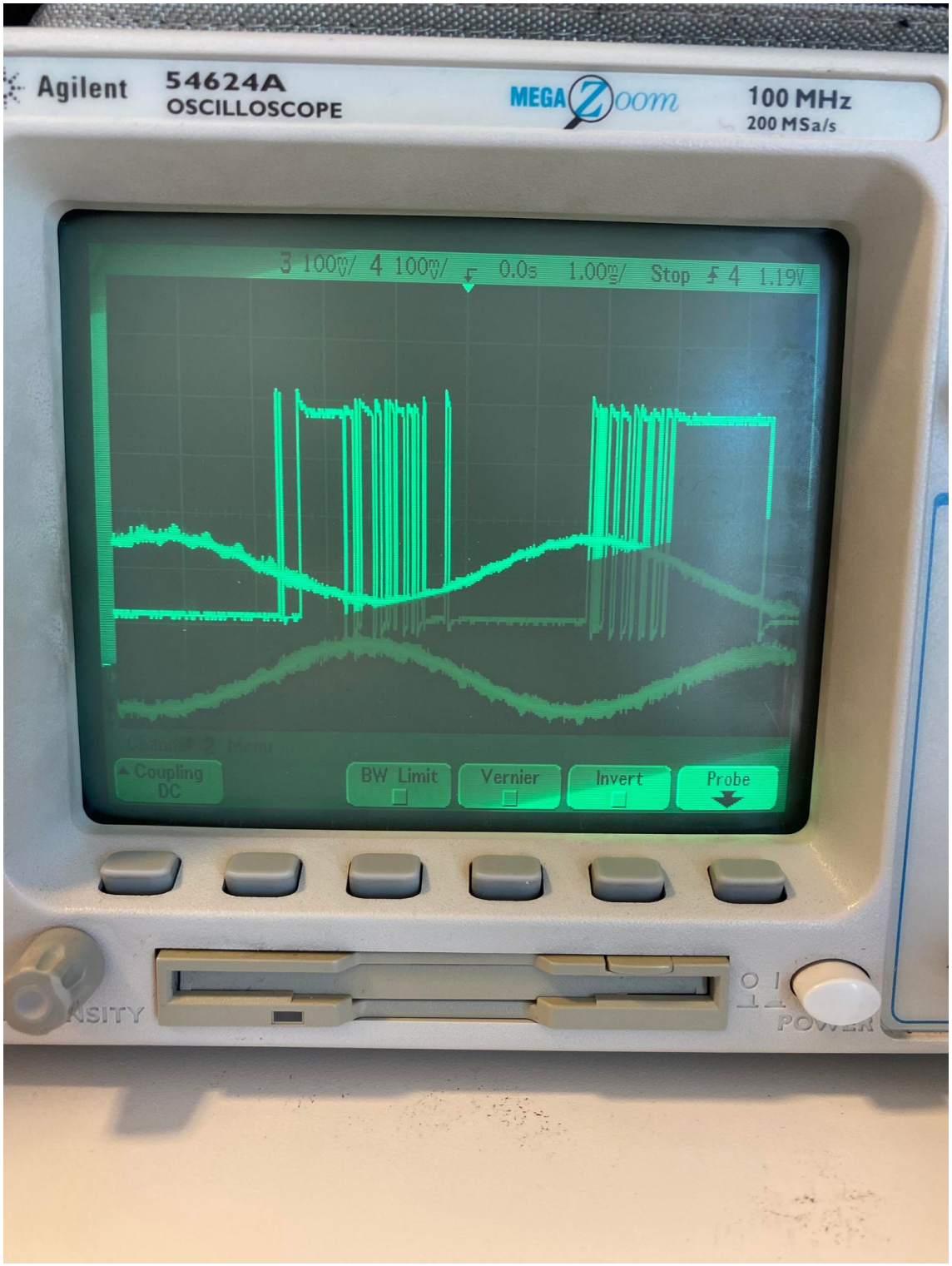
Appendix C

Chip results


Agilent
54624A
OSCILLOSCOPE
MEGAZoom
100 MHz
200 MSa/s
Horizontal
Main
Delayed
50 s
5ns
Measure
Cursors
Quick
Meas
File
Auto-
Scale
Save
Recall
Math
Channel 2 Menu
Coupling
DC
BW Limit
Vernier
Invert
Probe
INTENSITY
POWER


Agilent
54624A
OSCILLOSCOPE
MEGA Zoom
100 MHz
200 MSa/s
3 100mV/ 4 100mV/ 0.0s 1.00ms/ Stop
Channel 2 Menu
Coupling
DC
BW Limit
Vernier
Invert
Probe
50 s
5 V
1
POWER


Agilent
54624A
OSCILLOSCOPE
MEGA Zoom
100 MHz
200 MSa/s
3 100mV/ 4 100mV/ 0.0s 1.00ms/ Stop 4 1.19V
Channel 2 Menu
Coupling
DC
BW Limit
Vernier
Invert
Probe
50 s
5ns
Cursors
Auto-
Scale
5 V
1
POWER


Agilent
54624A
OSCILLOSCOPE
MEGAZoom
100 MHz
200 MSa/s
3 100mV/ 4 100mV/ 0.0s 1.00ms/ Stop 4 1.19V
Coupling
DC
BW Limit
Vernier
Invert
Probe
POWER

Appendix D

PCB with components