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Pre-amplification for electron density measurement in the ionosphere

Espen Otervik Granum

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Faculty of Mathematics and Natural Sciences

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Espen Otervik Granum

Pre-amplification for electron density measurement in the ionosphere

Supervisors:
Joar Martin Østby
Philipp Dominik Häfliger

Abstract

The electronics group at the physics institute has developed an instrument called 'Multi-Needle Langmuir Probe' (m-NLP) to measure electron density in plasma. This instrument flies on various space probes, e.g. on the ICI rocket series, where the latest generation of sounding rockets ejects miniature sensor platforms from the '4DSpace module' into the ionosphere in flight. The nanoelectronics group (NANO) at IFI is developing integrated circuits to read out the sensor measurements, called the 'Multi-Needle Integrated Circuit' (m-NIC). The electronics to read out the sensor values, in a first step, needs to power the sensor and amplify the sensing signal current before it is passed on to an analog-to-digital converter (ADC). This sensor supply and pre-amplification are summarized under the term sensor front end (FE). the task of this project is to implement a version of this FE as application specific integrated circuit (ASIC) in a specific CMOS technology, the TSMC BCD2 180nm technology.

Acknowledgements

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Nomenclature

- ASIC - Application-Specific Integrated Circuit
- ADC - Analog-to-Digital Converter
- BCD - Bipolar-CMOS-DMOS
- CMOS - Complementary metal–oxide–semiconductor
- CMRR - Common-Mode Rejection Ratio
- CPLD - Complex Programmable Logic Device
- FE - Front End
- FET Field-Effect Transistor
- LSA - Level Shift Amplifier
- LPF - Low-Pass Filter
- m-NIC - multi-Needle Integrated Circuit
- m-NLP - multi-Needle Langmuir Probe
- opamp - Operational Amplifier
- PSRR - Power Supply Rejection Ratio
- SNR Signal to Noise Ratio
- TG - Transmission Gate
- TIA - Transimpedance amplifier
- TSMC - Taiwan Semiconductor Manufacturing Company

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Chapter 1

Introduction

The earth's atmosphere consists of layers categorized by their physical qualities. The 4D Space Research Initiative at UiO is concerned with the ionosphere, having sent several instruments aboard sounding rockets and satellites for measurements.

The measured phenomena stem from radiation from the sun, that interacts with matter in the atmosphere. This is causing electrons to be freed from atoms and molecules (ionization), resulting in unbound charges in a medium with no net charge. Having a higher concentration of ions and free electrons, the matter is in a state called plasma. The highest concentration can be found in the ionospheric layers located approximately between altitudes of $50km$ and $1000km$. A practical consequence is the effect plasma has on radio waves. One example is reflections from terrestrial sources, causing RF signals to be reflected towards the surface called back-scatter. This enables stronger signal levels than would be expected beyond the line of sight. However, the plasma structures also have a negative impact when it comes to time-critical signals passing through. This is the case with GNSS satellites, where spatial irregularities in the concentrations of plasma cause the RF path to be diverted to a longer path. This effect is called scintillation. To measure these irregularities was the motivation behind the first m-NLP.

The multi-Needle Langmuir Probe (m-NLP) was invented at UiO by Knut Stanley Jacobsen as a way to measure spatial variations in plasma. The measurement principle is based upon a way to characterize plasma, which was presented in a paper by H. M. Mott-Smith and Irving Langmuir in 1926. The implementation was later called the Langmuir probe. Its function is based upon applying an electric potential between a probe and another reference point, for example, another probe or the vessel situated in the same volume of plasma. The probe will attract charges dependent on its bias level, resulting in a current through the probe. Measuring the current and relating it to the bias voltage relates to properties of the plasma, such as electron density.

A physical implementation of m-NLP was made at UiO by Tore André Bekkeng[1]. It was designed as a 4-probe system, implemented as discrete components on PCBs. It was to be launched along with other instruments on the Investigation of Cusp Irregularities 2 (ICI-2) sounding rocket. Its objective was to characterize spatial variations of plasma in the ionosphere to determine irregularities in backscatter. The first launch was on the 5th of December 2008 at Svalbard[12]. ICI-2 reached a peak altitude of $329km$ and had a mission time of $\sim 500s$. The results showed that the m-NLP was successful in its ability to measure electron density in the ionosphere aboard a high-velocity vehicle.

In addition to sounding rockets, the m-NLP has been implemented in several CubeSats. One is the NorSat-1 scientific satellite[9]. It was launched on July 14th, 2017 into low earth orbit at an altitude of $600km$. The m-NLP shares power and bandwidth with other instruments and therefore transmits data sporadically over several years of mission time.

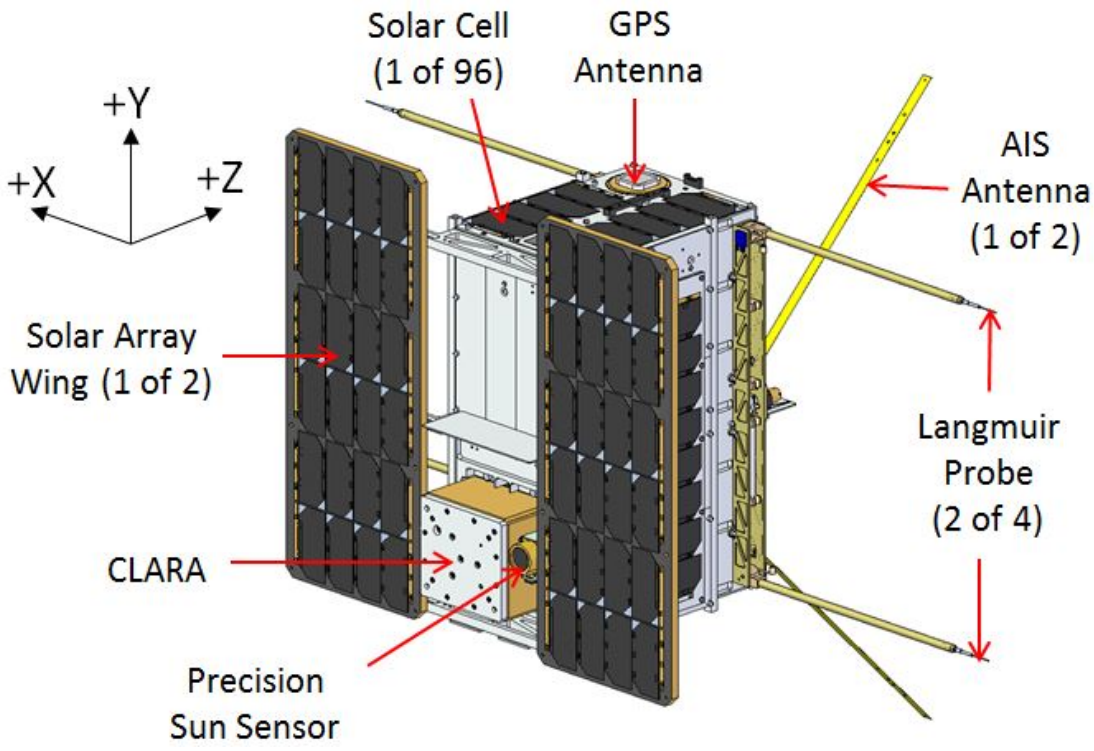


Figure 1.1: NorSat-1, showing the m-NLP along with other instruments. Credit: The University of Toronto Institute for Aerospace Studies

It has also been situated on 11 satellites in the QB50 research project, which orbits between 200-380km. Of which data has been received from ExAlta-1, Hooeng, and Pegasus[10]. Furthermore, on the Dutch military satellite Brik-II[8], which explored the usefulness of CubeSats for military applications.
In March of 2023, the m-NLP is scheduled to be launched to The International Space Station[5]. Though it is not the first Langmuir probe situated on the ISS, as a sweeping type with a spherical tip has been operational since 2006[4].

1.1 Motivation

In order to improve upon the m-NLP a similar design was implemented as an ASIC, called the Multi-Needle Integrated Circuit (m-NIC). So far there has been made two versions m-NIC1 and m-NIC2. The primary reason for integration is a reduction in size, power consumption, and reliability over discrete soldered components.

The size reduction has become a more pressing issue, given the current development of incorporating sensors on board 'daughter payloads' being ejected from the ICI-5 sounding rocket. In addition, all previous launches with the m-NLP have been CubeSats. It is

likely that this will be the case for future satellite applications as well. This work takes on challenges with the high-voltage front-end posed by the previous versions.

1.2 Thesis overview

- **Chapter 2 Background** Explains the theory of operation for the Langmuir probe. Further details into previous work and design requirements. Finishing with the goals of this work.
- **Chapter 3 Langmuir Probe FE** Presents the design implemented as an ASIC and explains the design choices made. A detailed listing of specifications. Continuing with details on each sub-circuit and its design elements.
- **Chapter 4 Simulation** Consists of detailed simulations.
- **Chapter 5 Testing** Describes the methods used for testing the ASIC.
- **Chapter 6 Results** Presents the results and compares them to simulations.
- **Chapter 7 Design Improvements** As there were faults in the ASICs design, this chapter shows possible design improvement as a new schematic design.
- **Chapter 8 Discussion and Conclusions**

Chapter 2

Background

The m-NLP is based upon a novel readout system, compared to standard Langmuir probes. This section describes some of the background theory.

2.1 The Langmuir probe

The Langmuir probe is implemented in several forms, but common to all is the principle of biasing a probe inside plasma and attracting electrons or ions resulting in a plasma current(I_p). When a probe is inserted into a body of plasma, the less massive and therefore faster electrons will initially be attracted to the probe tip. Thus resulting in a net negative current, giving the probe a negative charge. Eventually, the positive ions will be attracted to the now negative tip potential resulting in a net neutral current. This state indicates the floating reference potential V_f. In floating vessels, the chassis has the V_f potential. For electron density measurements, the probe is biased higher than V_p relative to V_f, in the electron saturation region. This results in more electrons in the nearby plasma, which in turn is attracted to the measurement probe resulting in a negative current.

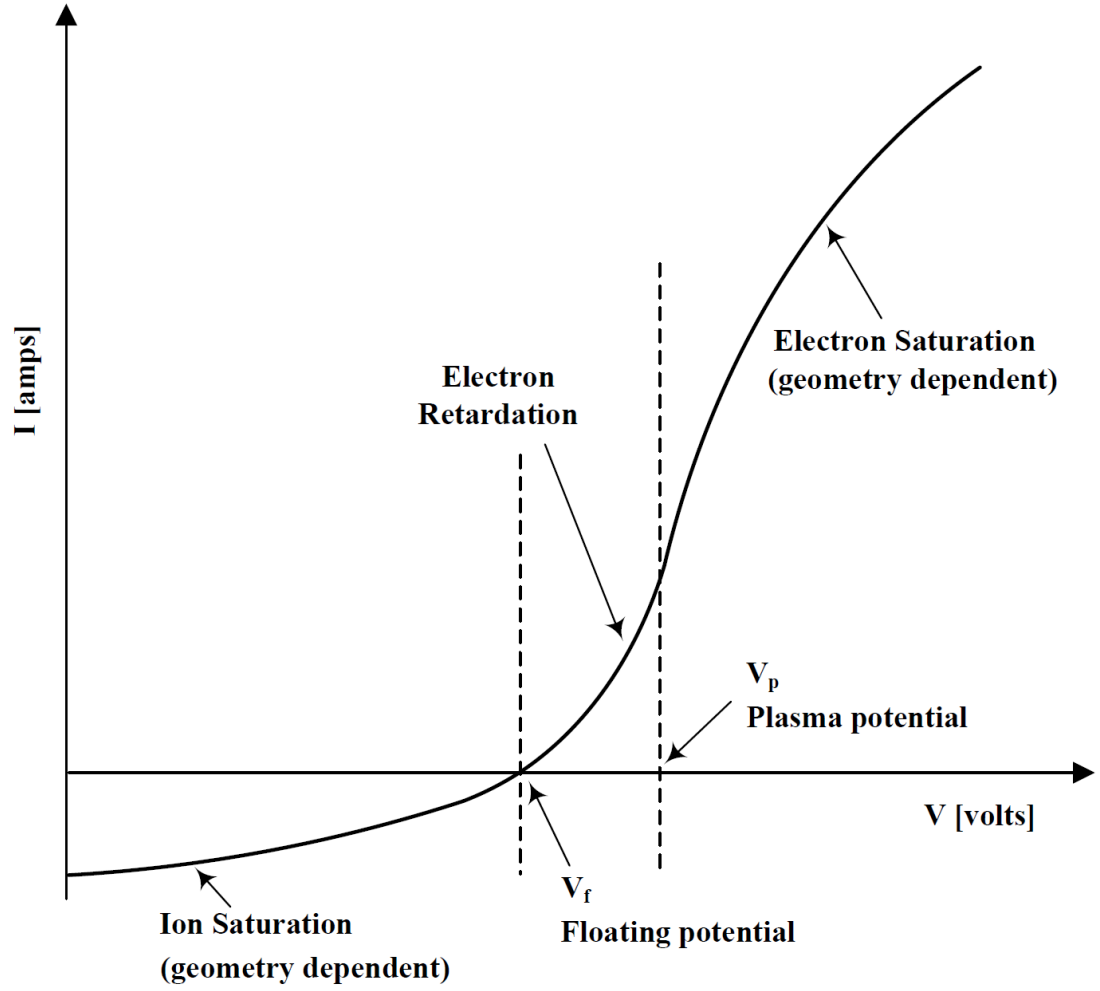


Figure 2.1: Illustration of the different operational regions http://tid.uio.no/plasma/norsat/mnlp_instrument.html.

2.2 multi-Needle Langmuir Probe

The classical approach to using Langmuir probes is to sweep the screen bias and measure the change in plasma current. The sweep takes on the order of a second, given the relatively slow movement of charges. This poses an issue, as the probe was intended to be launched on a sounding rocket reaching a velocity of $1km/s$-$2km/s$. Thus causing poor spatial resolution. This is the motivation behind the development of the multi-Needle-Langmuir-Probe(m-NLP) [11]. Here several measurement alternatives are weighted, but no alternative provides the kH_z sample rate needed. The suggested alternative: having a multiple of probes biased differently. This method is based on the equation for plasma current for cylindrical Langmuir probes[11]:

$$\Delta I_p^2 = \frac{2q}{m_e}(n_e q 2rl)^2 \Delta V_b \tag{2.1}$$

Where I_p is the plasma current, q is the charge of an electron, m_e electron mass, n_e electron density, r the probe radius and l is the exposed probe length.

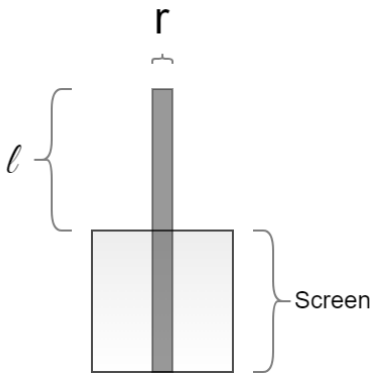


Figure 2.2: The probe used in the m-LMP is a cylindrical type with the measurement probe as a center conductor and a coaxial reference as a screen.

The underlying assumption that makes this relation usable is that the electron density has negligible variance between probes. This makes I_p^2 linear for changing V_b. While 2 probes will give a sample of the electron density, 3 or more are needed to verify that the relationship is linear.

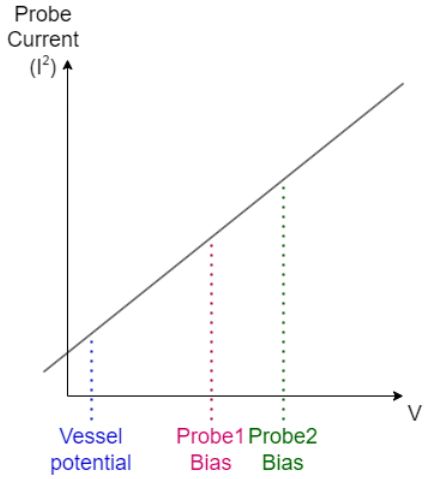


Figure 2.3: Measurement principle with unknown vessel potential.

The m-NLP is equipped with 4 probes to provide redundancy. An example of the importance of redundancy is the first launch 5 of December 2008. Here the 4 channels were biased $2.5V$, $4V$, $5.5V$ and $7V$. However, the $7V$ channel was in fact $10V$ caused by a known error in the circuitry[11]. Compensating for the bias error, the data from all channels showed promising results.

The first implementation of m-NLP was made in 2008 [1]. The circuit consists of discrete components on PCBs. The sub-systems are made up of an analog front-end and filter for each channel, ADC, and CPLD for readout and data handling. The system is responsible for biasing, converting the plasma current to a voltage, amplifying, and filtering the final signal and finally converting it to a digital value.

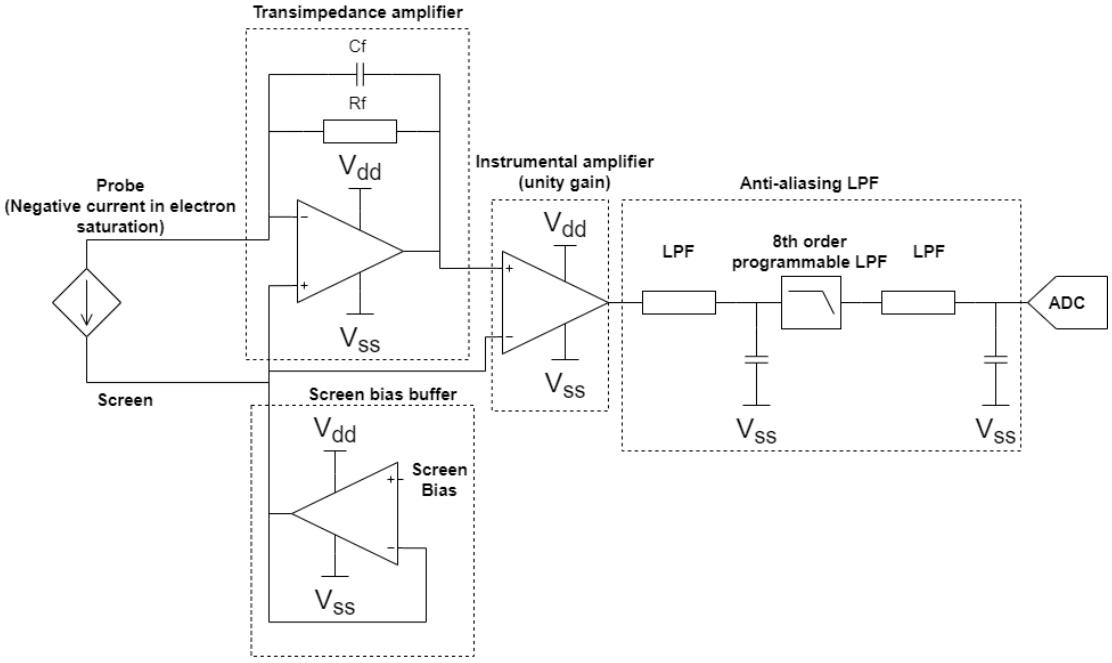


Figure 2.4: Analog front end including ADC aboard the first MNL-p launch.

The starting point of the signal chain is the current signal entering the transimpedance amplifier. Here an opamp has the measuring resistor R_f connected as feedback. The resultant voltage drop by the current is a differential voltage signal with respect to the screen bias. To make the signal single-ended for the following low-pass filter, an instrumental amplifier is used. The programmable LPF reduces the amplitude of frequency components beyond the Nyquist rate of the ADC, reducing the effect of aliasing. As the programmable LPF is clocked, passive LPF before and after are used to reduce its effect as a noise source.

The final component determining the performance in the analog domain is the ADC. Here a 16-bit ADC is used, which would ideally quantize its $+/-10V$ range to $2^{16}b$. However, the preceding programmable LPF(MAX293) has a range of $+/-5V$ resulting in a maximum resolution of 15 ENOB. Taking the ADC SNR into account, specified at $83dB$ minimum [21]. This results in $log_2(83dB) \approx 13.8$ENOB. Resulting in worst case $10V/2^{13.8} \approx 708\mu V$ and ideal case $10V/2^{15} \approx 305\mu V$. Using the value of the feedback resistor an approximation of the quantized current, not taking noise of the preceding circuits into account: $I_{step} = \frac{708\mu V}{4.7M\Omega} = 150pA$ and $I_{step} = \frac{305\mu V}{4.7M\Omega} = 65pA$. In addition to the limit of the lowest absolute value that can be determined, the maximum sampling rate limits the spatial resolution. For this ADC the maximum sampling rate is $9kHz$.

These values are used to quantify the desired performance for this project.

2.3 Multi-Needle Integrated Circuit

Having circuits implemented as individual components on a PCB has its drawbacks. The most obvious being area consumption and mass. The die area itself is negligible, as the necessary package is much larger. Assuming a package area on the order of $\sim 1cm^2$, the aforementioned m-LMP PCB uses $\sim 70cm^2$. Furthermore, the power consumption

is generally much lower with ICs. Another is reliability, as seen in the first launch. ICs has essentially no internal mechanical weak spots, as their most likely point of failure being is their package connection to the PCB.

These are the main motivations behind the multi-Needle Integrated Circuit (m-NIC). The first iteration (m-NIC1) has roughly the same signal path as the original circuit, the main difference being the lack of a LPF. It was fabricated in 2017 using the XFAB 180nm 10V process. The high voltage process resulted in the capability to drive the screen bias between $1.5V \Rightarrow 9.5V$[14].

The ASIC consists of the FE and the DAC partially implemented with high voltage devices. The rest of the system uses the lowest digital signal level, area-efficient transistors.

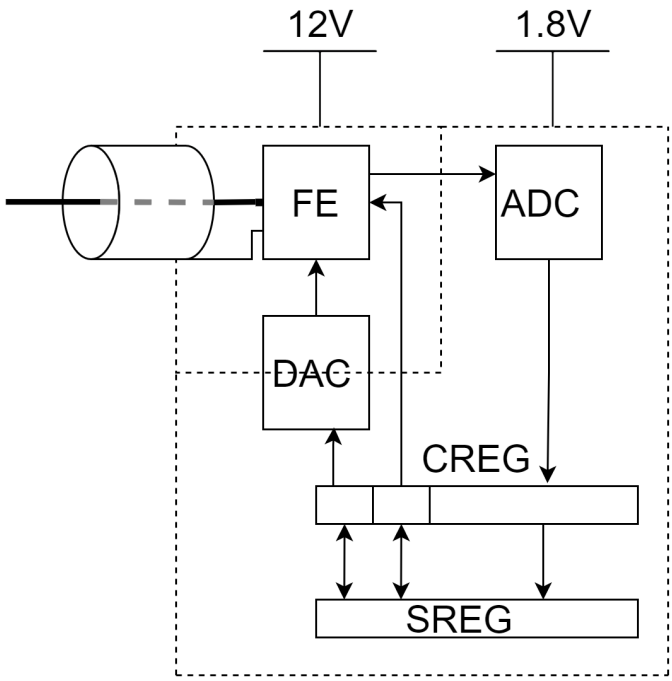


Figure 2.5: Overview of a proposed system similar to m-NIC2, showing the front end in relation to other functional blocks.

m-NIC2 was developed to resolve issues with m-NIC1 and improve performance. The FE was redesigned with a configurable gain in the level shift amplifier and trans-impedance amplifier, increasing the dynamic range of the system. In addition, the output of the opamp had much higher drive capability and a LPF was added for anti-aliasing. A 7-bit DAC was added to give the option for the ASIC to provide an internal screen bias. Unfortunately, the FE part is not functioning, as the result of a wrong pad type used to input the bias current. A $3.3V$ pad was used, when the biasing transistor is a PMOS. Given the $10V$ process limit, the ESD diodes in the pad clamped the bias to an unusable level.

For a more systematic test of the m-NIC, a test circuit controlled by an FPGA was developed [20]. Here the front end of m-NIC1 was tested and the (identical) ADC of both versions was tested. Measurements performed on the m-NIC1 by Joar showed a

functioning circuit. However, measurements made with the aforementioned circuit by Candice Quinn did not replicate these results[17].

2.4 Requirements

The FE must be able to handle the signal levels posed on previous versions. What this entails is being able to handle the input signal range, bias voltage range, and output to a signal level within the range of the ADC. The FE is to be implemented as an ASIC. Following the same motivation behind the m-NIC, in addition, to be compatible with future integration with further down-line circuitry.
To comply with this, the CMOS process chosen needs to be able to handle the high bias voltages. The TSMC BCD Gen2 180nm process has device models that tolerate voltages up to $70V$.

2.4.1 Current conversion

As a first step in the FE, the current signal needs to be converted to a voltage signal that is easier to respond to with FETs. The ideal case would be to convert the signal without affecting the signal amplitude. Using a simple measurement resistor as an example. There is an inverse relationship between the voltage gain and the current limiting effect of the resistor $\Delta V = \Delta I * R$. This trade-off is impractical for low currents.

Using the fact that an opamp with feedback at one input, will create a virtual copy of the other input; a low input impedance current measurement can be made. A transimpedance amplifier uses the feedback to source or sink the signal current:

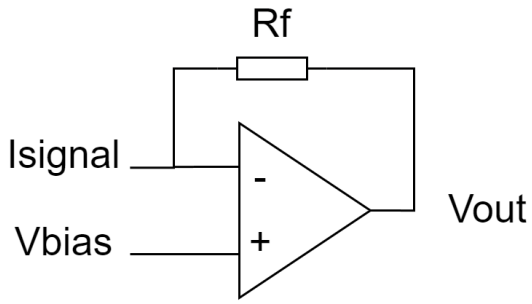


Figure 2.6: Transimpedance amplifier.

Assuming an infinite gain of the opamp, there will be no voltage difference between V_{bias} and I_{signal} and thus zero input impedance. The voltage response is however dependent on R_f: $V_{out} = -I_{signal}R_f$. In this application, the output increases with a higher negative current.
Taking the feedback noise into account, an increase in R_f results in a higher gain. However, the inherent Johnson-Nyquist noise of R_f also increases. In a TIA this is most likely the dominant noise source. Another drawback of increased feedback value is a

lower bandwidth with a co-dependence on input capacitance. Another drawback is the larger adie-area used up by the opamp, when compared to a simpler common gate stage. Given these advantages and disadvantages, the TIA is popular for low current signal conversion.

2.4.2 Amplification

As with m-NIC2, the FE needs to be able to select between different gain levels. Firstly for the TIA, to be able to set different R_f values dependent on input signal level. The feedback should be high enough to convert to a voltage well above the noise of the TIA, while not going into saturation or having an unnecessarily large noise contribution from the feedback itself.
The level shift amplifier shall also have selectable gain, with the purpose of having the highest possible amplification without going into saturation.

Chapter 3

Langmuir probe FE

This section describes the design implemented into the ASIC. Starting with an overall description and goal specifications. Then going into the background theory of each sub-circuit, design choices, schematic and layout. This system is a FE for one LMP, with a single screen and probe input. The output and ADC_Ref+ are intended to be supplied by a future integrated ADC and bias. The design is based on the m-NIC2 with minor alterations. One is that the outputs of the TIA and level shift amplifier is tri-state. Another is the gain levels. The m-NIC2 had a configurable gain for the level shift amplifier of 1,120,240. Following simulations to determine the saturation levels for each gain setting, the following gain levels is used: 4,16,64,256. The design of the transmission gates is also altered to be compatible with the process.

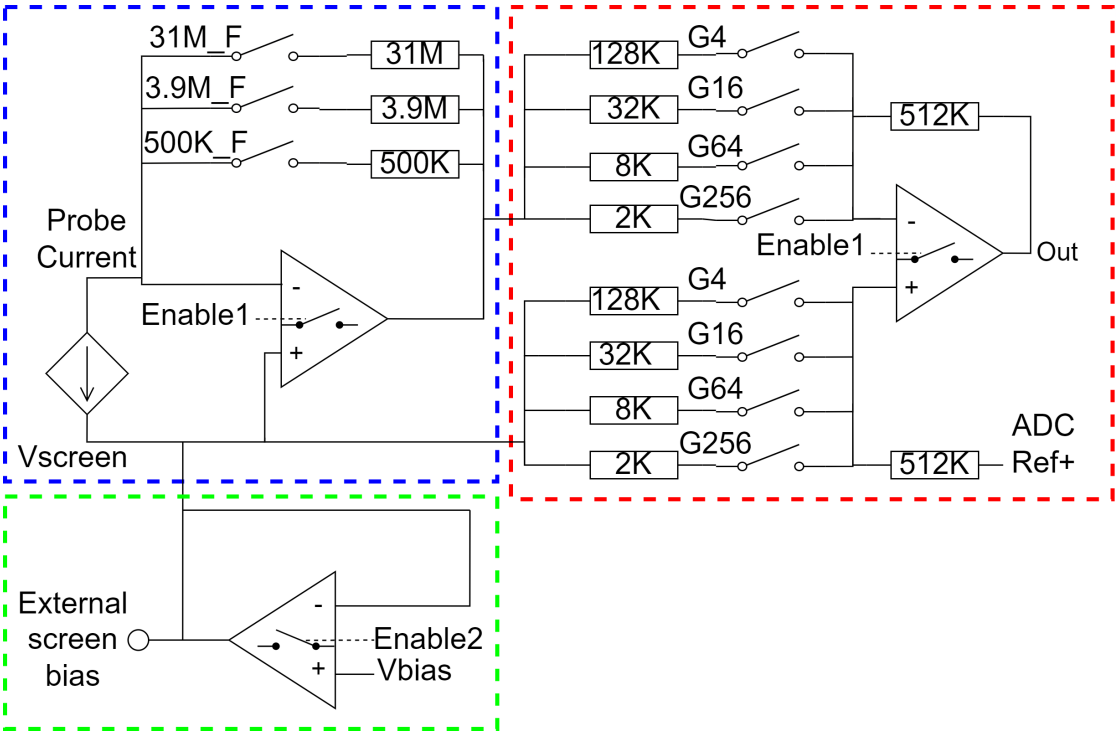


Figure 3.1: Circuitry implemented into the ASIC. TIA (blue), level shift amplifier (red) and screen bias buffer (green).

Table 3.1: Normalized gain values.

LSA Gain	TIA Feedback		
	$500k\Omega$	$3.9M\Omega$	$31M\Omega$
4	1	7.8	62
16	4	31.2	248
64	16	124.8	992
256	64	$499,2$	3968

To measure the plasma current a TIA is used. The plasma current enters the TIA through either of the 3 feedback resistors controlled independently. The output is differentiated by the screen voltage: $V_{TIAout} = -I_{signal}R_f + V_{screen}$.

V_{screen} is driven by either a source external to the ASIC or internally through V_{bias}. When driven by V_{bias}, the opamp acts as a buffer for the internal bias to the relatively high capacitance of the screen. When the external source is used, the output of the opamp is switched to high impedance mode (Enable2). As all opamps are based on the same design, they all have switchable outputs. The TIA and level shift amplifier control signals are connected (Enable1), for testing purposes.

The level shift amplifier shifts down the voltages from upwards the process limit, to a level compatible with the lower voltage devices in the ADC. ADC_Ref+ is the positive reference voltage of ADC and sets the upper limit of the output voltage. Given the direction of the plasma current, the output will decrease with an increased plasma current level. Having a controllable gain level enables amplification of even lower input signal levels above the subsequent ADC noise floor.

As this is the entirety of the ASIC, all IO signals visible lead off-chip.

3.1 Specifications

The specifications for this circuit are based on the previous langmuir probe front ends. m-NIC1 and m-NIC2 are the latest iterations of the langmuir signal conditioners and since this design is also an ASIC, they are the most relevant. The following table is based upon m-NIC1s measurements[16] and simulations from m-NIC2[15]. The following table is the goal specifications for the design.

Table 3.2: Specifications

Parameter	Min. value	Max. value
Supply voltage (VDD-VSS)	NA	$12V$
Signal current	$150pA$	$1.5\mu A$
Signal variation satellite	NA	10%, $\Delta t = 1ms$
Signal variation sounding rocket	NA	10%, $\Delta t = 10ms$
NMOS input Opamp CM range	$1.5V$	$12V$
PMOS input Opamp CM range	$0V$	$10.5V$
Opamp output range	$0.3V$	$11.7V$
Opamp open loop gain	$80dB$	NA
Noise	$< 15pA$(goal)	$\leq 150pA$ (requirement)
GBWP	$1MHz$, $\geq A = 100$ at $10KHz$	NA
Opamp Phase Margin	$60°$	$90°$
Load	$50pF$, $Z = 50\Omega$	NA
Input impedance	NA	500Ω(frequency dependent)
PSRR	$40dB$	NA

The supply voltage is important for the screen bias. Having a wide spread across the bias of each probe provides more reliable data points for the determination of electron density. The maximum value is due to the transistor model limit, this is explained in more detail in chapter 3.2.

The plasma current range is based on the probe dimensions and the achievable screen bias voltage. The upper screen bias in an ASIC application is limited by the CMOS process. The m-LMP has measured electron density in a range between $N_e = 10^{-8}m^{-1} \Rightarrow 10^{-13}m^{-1}$). This resulted in a signal range of $1nA \Rightarrow 1\mu A$. The expanded signal region is based upon the simulations done with m-NIC2.

The signal variation criteria sets a goal for the TIA to handle a certain input bandwidth when connected to a probe as a capacative load. Two different criteria are set dependent on the vessel that is used. For a satellite application 10% span over $1ms$ and for a sounding rocket its 10% span over $10ms$.

Common mode input range is dependent on the input type. Subtracting $1.5V$ from each rail to give room for input pair and current source overdrive results in $0 - 10.5V$

for PMOS, and $1.5 - 12V$ for NMOS. The output range is close to rail-to-rail, due to the design of the output stage of the opamp. As reaching a power rail, especially under load is challenging then a output voltage range of $0.3 - 11.7V$ is more realistic.

The open loop gain (A_{OL}) of the opamp sets the DC performance in all operations of the system. As the m-NIC also contains high voltage opamps, the minimum is based on simulations of m-NIC2.

The noise specification is affected by the system noise up until the output. This adds a noise floor which limits the minimum signal level that can be discerned at the output. Taking into account a finite resolution and sampling rate ADC as a receiving end, the noise must be below the effective resolution (ENOB) at a $10kHz$ sampling rate for this application. This is a metric of whether the FE can amplify a minimum signal amplitude of $150pA$ above the noise floor of the ADC, with a goal value of $15pA$.

The gain bandwidth product is set to $> 1MHz$ with an additional requirement to have at least $A = 100$ at $10KHz$, because of the kHz sampling needed for the end application.

The phase margin should be $> 60°$ for stability. This is especially important when it comes to the TIA and the higher feedback values.

As the opamp is tasked to drive the screen from an internal reference, then the output has to drive a minimum load. A minimum of $50pF$ capacitive load with a $50ohm$ characteristic balanced transmission line ensures that the output can be measured with a typical oscilloscope probe and drive the screen.

The input impedance is a parameter of the probe inputs to the TIA. It is a measure of the voltage difference between the screen and probe times the plasma current: $Z_{input} = (V_{screen} - V_{probe})I_{probe}$. The difference in potential stems from the limited gain and input offset. At the DC this can be determined by A_{OL}. When taking a changing input signal into account, the GBWP becomes an important parameter.
To have a limited impact on the signal, a maximum of $\leq 500\Omega$ is required.

PSRR is the factor of how much a noise amplitude on a power rail affects the output, often specified as a logarithmic value of $20\log(V_{INnoise}/V_{OUTnoise})$. As it is frequency dependent it is often displayed as a bode plot. The minimum is based on a comparison of the typical values from datasheets of other ICs, and lower to a reasonable goal value. Usually this varies between $60dB$ to $120dB$. The minimum value for this application is lower as it is expected to be supplied by a low-noise voltage source.

3.2 TSMC BCD Gen2

To accommodate the desired signal range, a high voltage process is needed. For this ASIC the TSMC 180nm BCD (Bipolar-CMOS-DMOS) Gen2 HV CMOS process was chosen, as it consists of transistor families up to 70V.

Having higher voltage transistors would be beneficial from a signal conversion point of view. However, as the voltage increases on the transistor nodes, the spacing rules for the process increases. The table below uses measurements taken from the innermost point where another transistor can be adjacent. The transistors chosen are all of the available of the same type.

Table 3.3: Transistor family size comparison (NMOS).

Family (V_{ds})	μm^2	Min $\frac{L}{W}$
6	340	$0.4\mu/10\mu$
7	342	$0.3\mu/10\mu$
12	360	$0.4\mu/10\mu$
29	401	$1.3\mu/10\mu$
45	1985	$1.5\mu/10\mu$
70	2493	$1.5\mu/10\mu$

What makes up most of the area is the surrounding isolation structure. All HV devices are surrounded by a $p+$ isolation ring connected to the base substrate. It also has spacing restrictions to the inner deep N-well that all transistors of this family are embedded in.

For this application, the 12V models were used. Intended as an increase from the previous 10V process used for m-NIC. It is also a compromise in size and has a good linear IV response, as seen in the below plots. Unfortunately, it was discovered after the design was sent to fabrication that the circuit would not be able to safely handle voltage levels up to the device model limit. These transistors can only withstand a high voltage from drain to any other node. The V_{gs} and V_{gb} has a safe limit $5.5V$. As several circuits in the ASIC connects V_{dd} to the gates of NMOS with bulk/source connected to GND, the supply of the ASIC must be limited to $5.5V$. These include NMOS used as bypass and control circuits for the opamps. Simulations performed hereafter will be of $V_{dd} = 12V$ to inspect the potential of the FE in this process. In addition, some simulations will be made with $V_{dd} = 5.5V$ as a comparison of the expected ASIC performance.

The transistors must be implemented as an even number of gates sharing bulk/source in the middle, with drain contacts at each end. All gates, sources, and drains must have the same potential. The design is non-symmetrical with regard to the bulk contact and source/drain contact. Meaning that the bulk and source contact substrates are butting and thus, the bulk contact is spaced apart from the drain contact. The Poly-silicate gate is also closer to the bulk/source contacts. The proximity of gate, bulk and source is probably the reason for the $5.5V$ maximum V_{gs} and V_{bs} restriction.

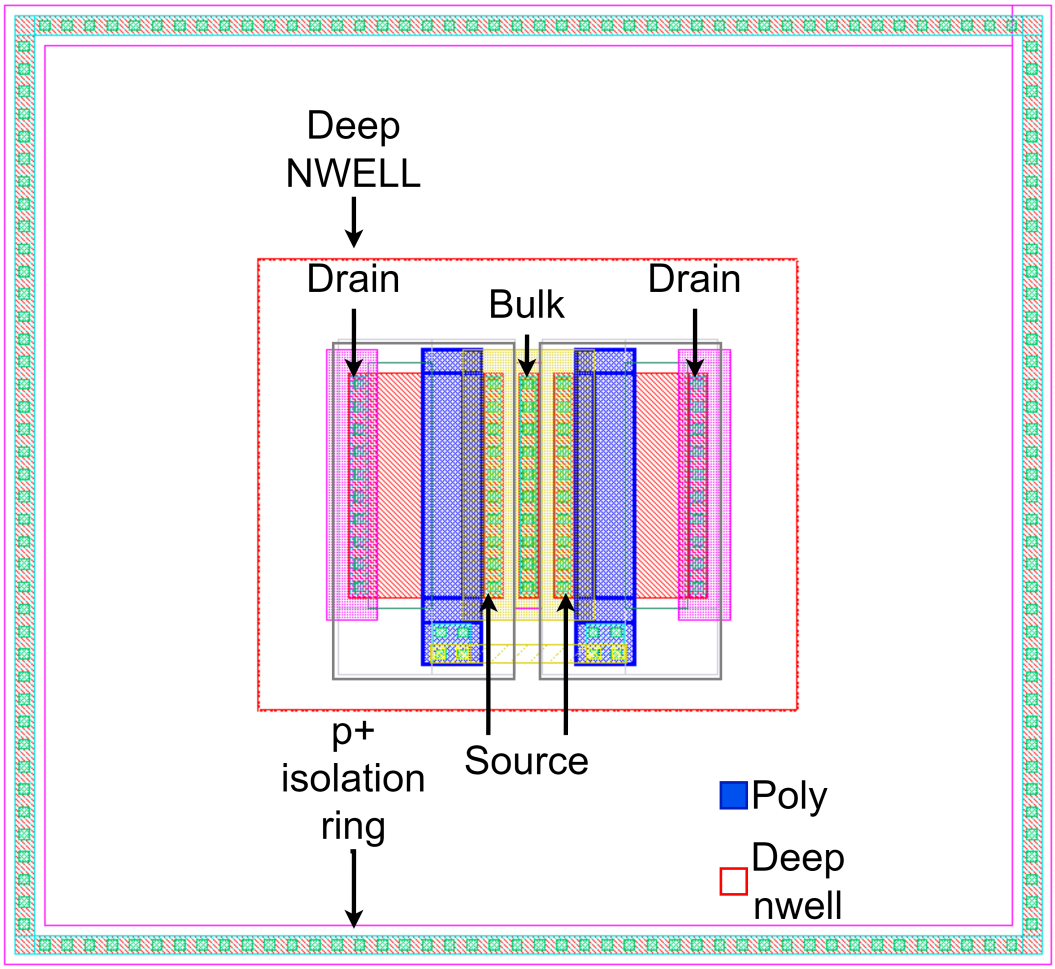


Figure 3.2: Layout of a 12V NMOS.

An IV simulation is made to compare the response from the above transistors. Grouped together are the $6V$, $7V$, $12V$ and $29V$, $45V$, $70V$ respectively as they share similarities in minimum device length.

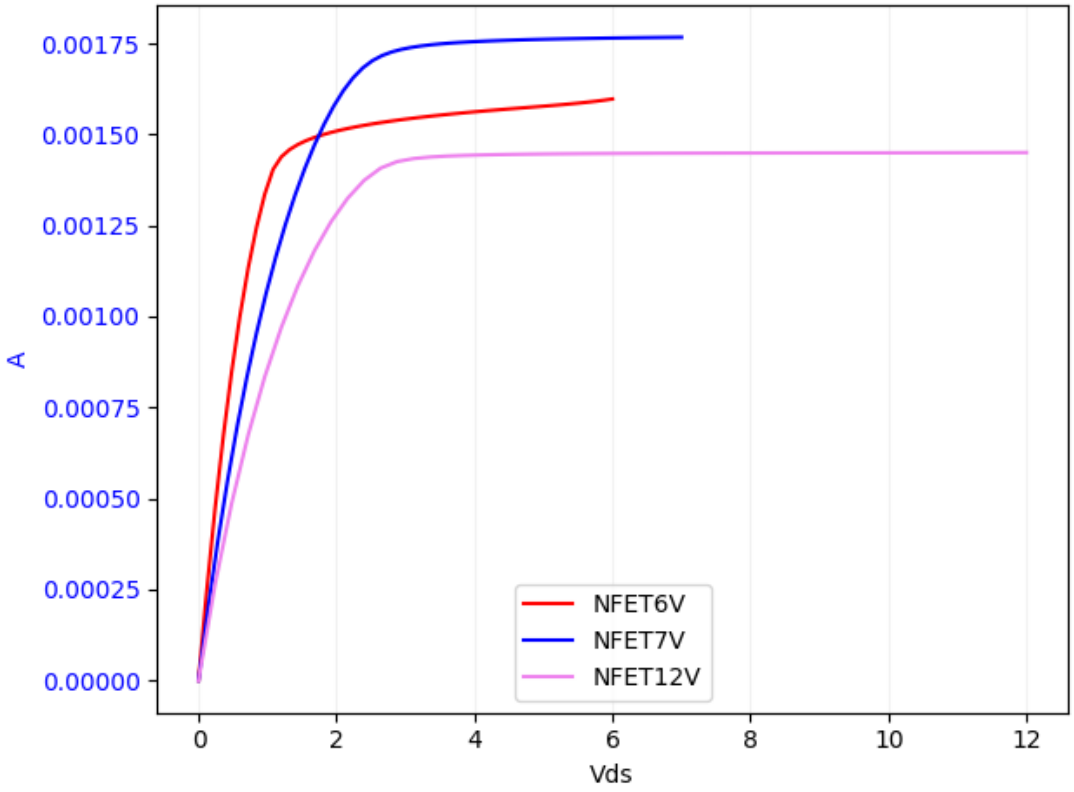


Figure 3.3: IV curve comparison for 6,7 and 12V NMOS. $V_{ds=0V \Rightarrow MAX}$, $V_{gs} = 2.5V$

Both the $6V$ and $7V$ NMOS had clear signs of channel length modulation as seen by their slope beyond saturation. However, the $12V$ NMOS had little change in drain current by increased V_{ds}. This is unexpected, as all have similar nominal channel lengths.

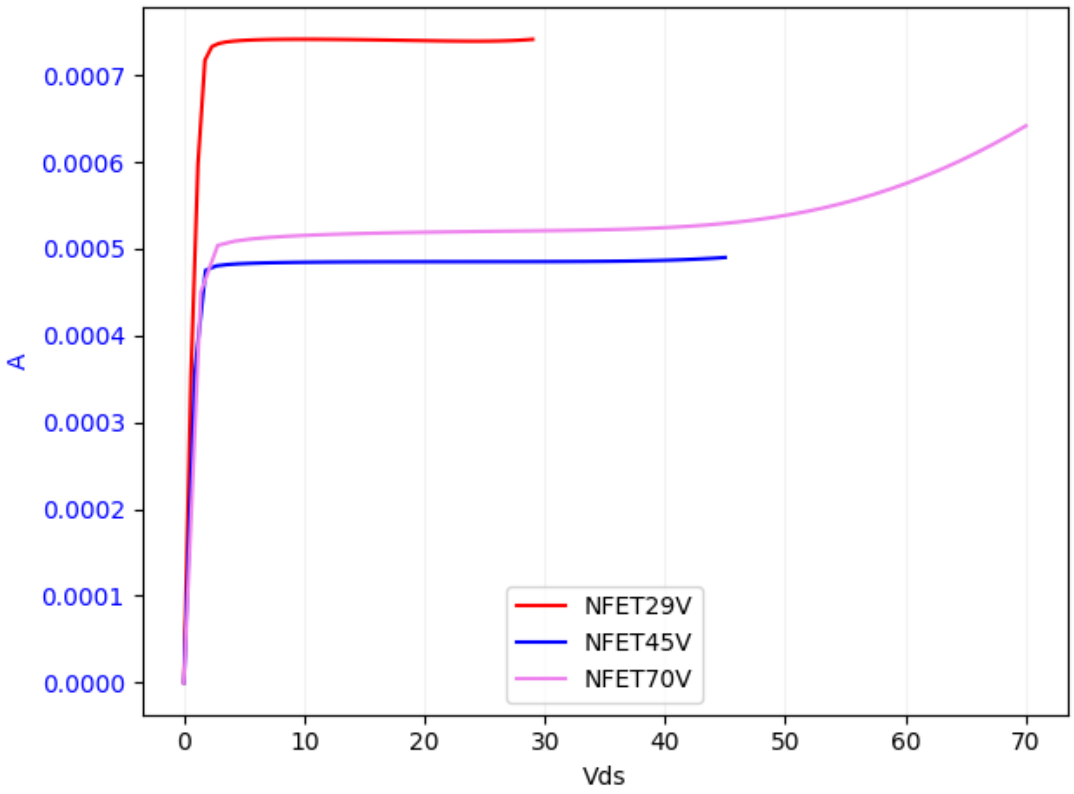


Figure 3.4: IV curve comparison for 29, 45 and 70V. $V_{ds=0V \Rightarrow MAX}$, $V_{gs} = 2.5V$

The higher voltage devices showed little signs to channel length modulation. There is an exponential response towards maximum V_{ds}, most notably on the 70V NMOS.

3.3 Operational amplifier

A opamp is at the center of all functions of the FE, making the design critical when it comes to the choice of topology, size of transistors, and layout. All opamps are copies of the same schematic and layout This section will describe each portion of the opamp circuit as well as some layout design. All schematic figures are of the design used for the layout. $IDRAIN$ is supplied from a simple diode-connected PMOS acting as a current mirror, sourcing all three opamps in the design. The opamp has PMOS input.

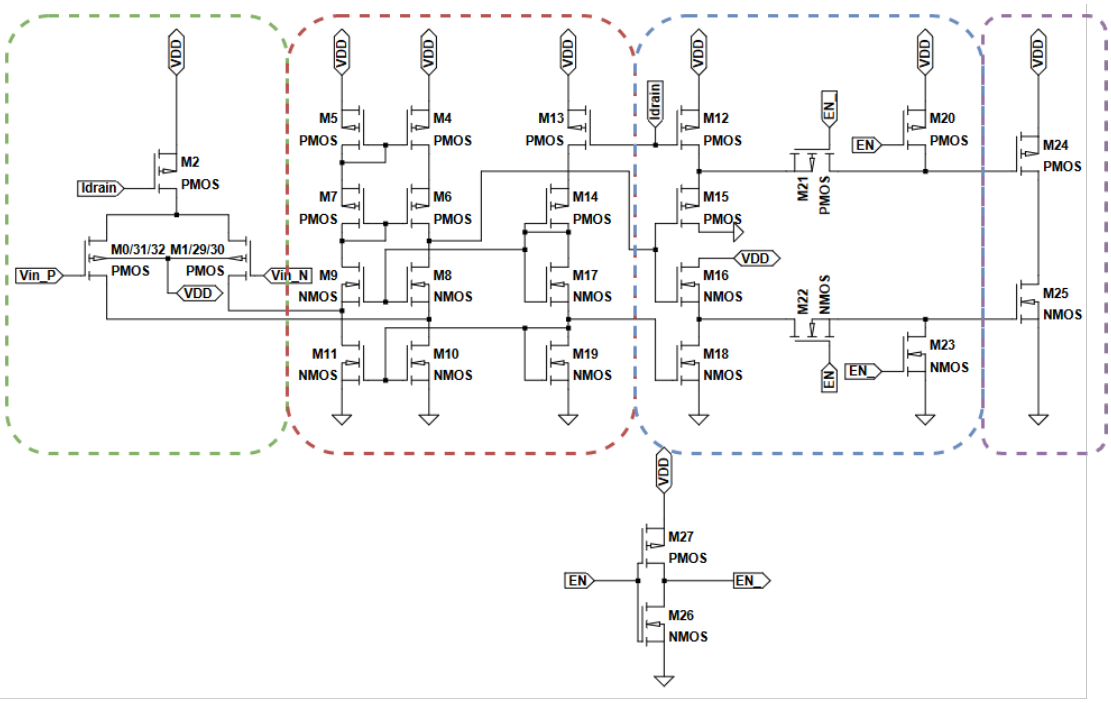


Figure 3.5: Opamp schematic. Differential input (green), folded cascode with biasing (red), tri-state switch (blue), and the CS power stage (purple).

Table 3.4: Opamp transistor sizes

Transistor	**W/L**
Differential input	
M2	$40\mu/1.2\mu$
M0/31/32	$30\mu/1\mu$
M1/29/30	$30\mu/1\mu$
Folded cascode and biasing	
M4/M5	$10\mu/4.8\mu$
M6/M7	$10\mu/4.8\mu$
M8/M9	$20\mu/1.2\mu$
M10/M11	$40\mu/1.2\mu$
M13	$40\mu/1.2\mu$
M14	$20\mu/1.2\mu$
M17	$10\mu/9.8\mu$
M19	$40\mu/1.2\mu$
Tri-state switch	
M12	$20\mu/1.2\mu$
M15	$20\mu/1.2\mu$
M16	$20\mu/1.2\mu$
M18	$20\mu/0.5\mu$
M21	$10\mu/0.5\mu$
M22	$10\mu/0.4\mu$
M20	$10\mu/0.5\mu$
M23	$10\mu/0.4\mu$
CS power stage	
M24	$60\mu/1.2\mu$
M25	$40\mu/1.2\mu$
Inverter	
M26	$10\mu/0.4\mu$
M26	$10\mu/0.5\mu$

3.3.1 Differential pair

The differential pair functions as the input for the opamp, with their gates as a high impedance endpoint for the voltage signals. When all transistors operate in saturation, it provides a differential current response in proportion to the difference in voltage at the gates. A common implementation consists of a pair of common source stages driven by a common constant current source(gmV_{Idrain}), splitting this current among the drains according to the differential input: $gmV_{Idrain} = gmVinP + gmVinN$. The output from this step is two current signals, IN_P_DRAIN for the non-inverting input and IN_N_DRAIN for the inverting input.

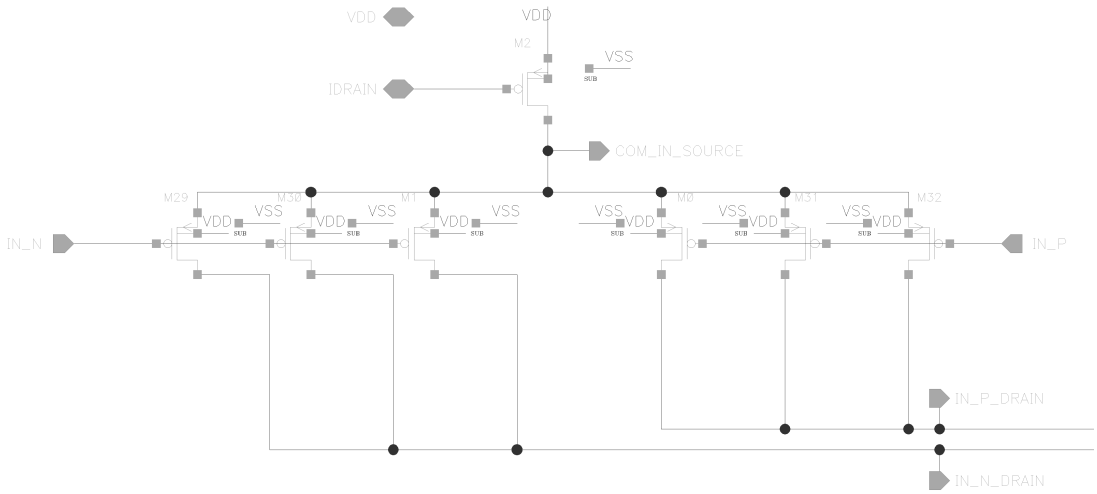


Figure 3.6: Differential input stage.

Having the differential pair working as current sources entails that they must be working in saturation. However, they have to be in saturation over a wide desired input common-mode range (V_{CM}):

$$V_{GS} < V_{TH}, V_{DS} \leq V_{GS} - V_{TH} \tag{3.1}$$

This is done by regulating V_{GS} according to the V_{CM}, accomplished by the constant current source(M2). As V_{TH} decreases, the differential pair's small signal resistance r_o decreases relative to M2. This will increase the voltage drop across M2 and thus decreases V_{DS}, and vice versa for an increasing V_{CM}. With PMOS input there is an upper limit to V_{CM}, as there must be at least a V_{TH} drop across V_{GS}.

An advantage of a well-matched differential pair is its response to V_{CM}. As the common source current source delivers a constant current, split across the inputs. Any change of V_{CM} will, in an ideal case be canceled. This is true, under the assumption that the transistors that make up the differential pair, have an identical response to the same DC offset. However, variability in the manufacturing process will cause changes between two transistors using the same layout; called mismatch. One factor causing this can be seen as random changes to the edges of a layer. A solution is to increase $W * L$, thus decreasing the relative size of the random process changes. Another effect causing mismatch is inhomogeneity in the substrate. As doping levels will not be completely

even across the substrate, the location of a transistor will affect its characteristics. As the input pair are usually large relative to their process minimums, they can easily be split up as several devices with gates, sources, and drains connected. Interleaving split devices in the layout reduces the risk of variations in the substrate affecting one transistor more than the other. These inequalities are not only dependent on the blank substrate itself. The surrounding structures affect each split transistor providing unequal parasitic effects, for example capacitance to a nearby metal layer. The middle transistors in such a setup experience a homogeneous surrounding with neighboring transistors having the same dimensions. However, in the end will experience unequal surroundings. To solve this, identical dummy transistors are placed on each end, with V_{GS} connected to V_{DD}.

To reduce mismatch, the lengths are double the minimum: 1μ. To accommodate splitting up each device, the width must be multiples of the minimum $(2 * 5\mu)$. In this design, each transistor has $W = 15\mu * 2 = 30\mu$, given the dual gate process requirement. Each input consists of three transistors, making the total width 90μ. The higher W/L increases the transconductance:

$$g_m = -\mu_p C_{ox}(W/L)V_{OV} \tag{3.2}$$

While this is desirable, having larger input devices also results in higher input capacitance and thus lower input impedance.

Other than dimensions, the choice of input type affects the performance. The most prevailing consequence being input common mode. For NMOS, V_{CM} can be close to the positive rail, though it is limited by a $V_{TH} + 2V_{OV}$ -drop towards the negative rail. Another difference lies in g_m, as hole mobility(μ_p) is usually 2-3 times less than that of electron mobility(μ_n). Moreover, FETs have an intrinsic 1/f, or 'flicker' -noise. This is caused by charges being randomly trapped and released from between the channel substrate and the gate oxide. This results in a noise density increasing towards DC. The level of 1/f noise differs between PMOS and NMOS. PMOS generally has an order of magnitude less 1/f noise [13]. This is especially important for the TIA, as the opamp noise density should be lower than the intrinsic noise of the feedback.

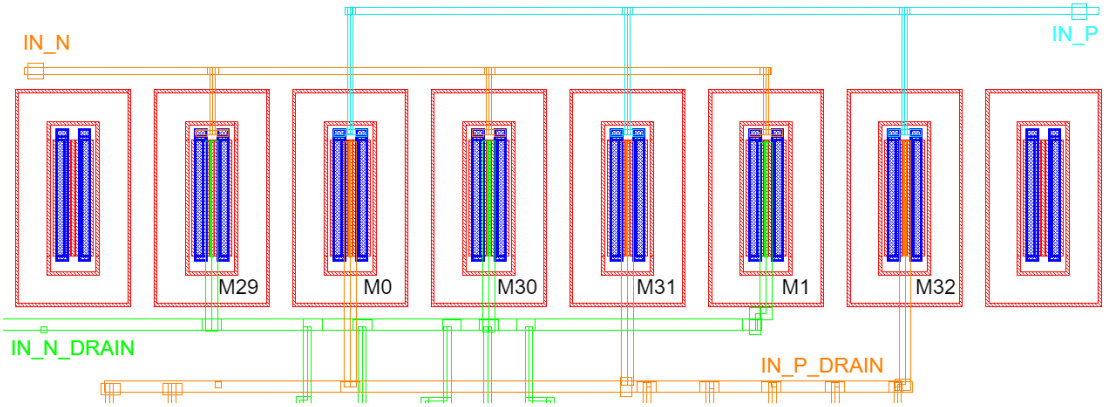


Figure 3.7: Layout of the differential input pair. Six interleaved devices in the middle, with a dummy on each end.

In the layout, there is an attempt to limit the overlap between the input signals and the drain signals. Not seen in the figure are the interleaved V_{DD} and ground planes in

between each PMOS. This is done in an attempt to limit crosstalk and provide a stable reference.

3.3.2 Folded cascode

Having the current signals from the differential pair as input, the folded cascode provides further amplification and outputs a single-ended voltage signal ($OUT\_CASCODE$). A cascode is a combination of a common source (CS) and a common gate stage (CG). If the CS and CG are of different types, the connection is branched or 'folded' between them and a current source:

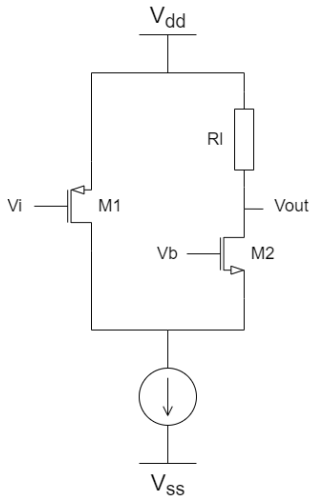


Figure 3.8: Functional schematic of a folded cascode.

The differential pair acts as the common source. The small signal currents are sunk by M11 and M10(fig 3.5) working as current sources. The total current passing through the current sources is divided between the CS and CG (M9 and M8). M5 and M7 act as diode loads and current mirrors for M4 and M6, mirroring the current not passing through $IN_{ND}RAIN$:

$$gm_5DLOAD1|gm_7DLOAD2 = gm_{11}VBIAS2 - I_{IN\_N\_DRAIN} \tag{3.3}$$

An increase in the small signal current through IN_N_DRAIN, results in less current through M7 and M5. This causes M4 and M6 to have a reduced overdrive voltage and thus a higher voltage drop across each. IN_P_DRAIN will source less current, resulting in more current conduct through M4 and M6, assisting in the voltage drop. The two differential current inputs thus work inversely, resulting in the single ended output($OUT\_CASCODE$).

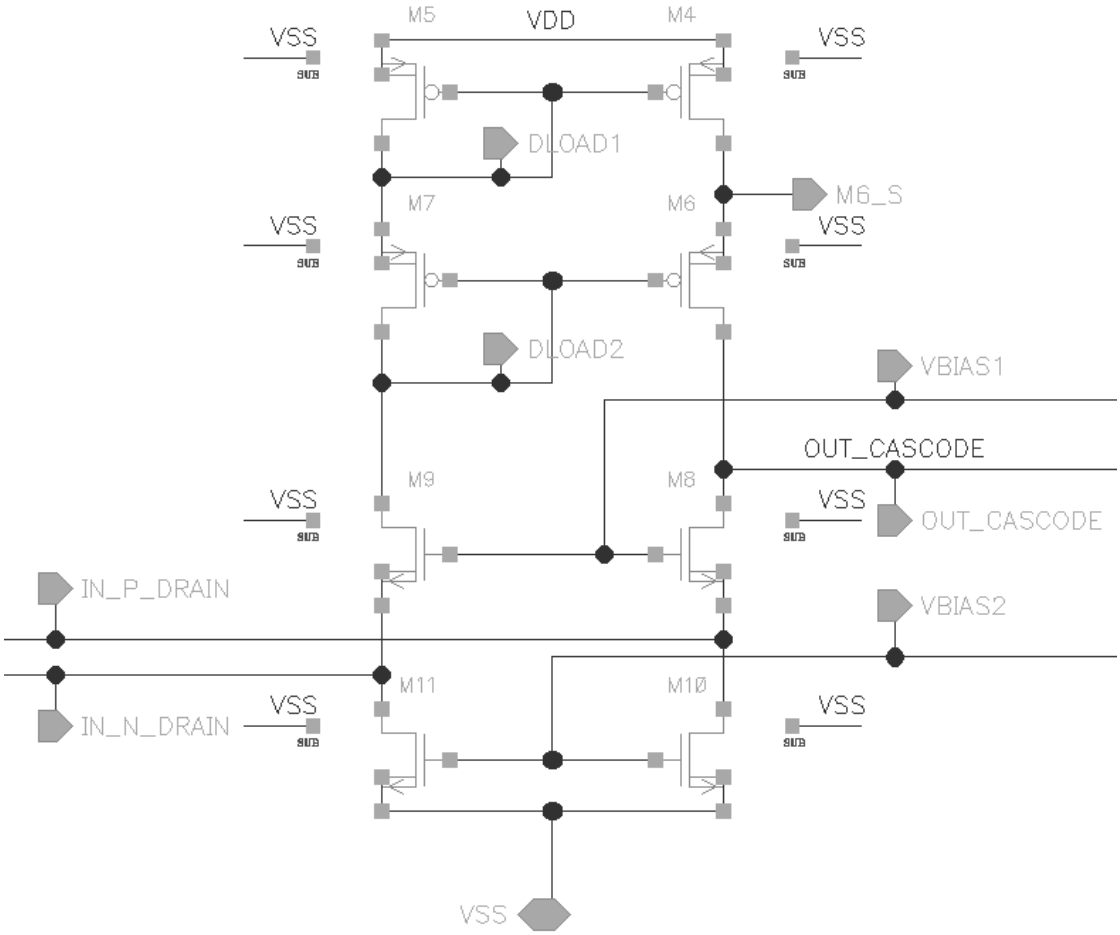


Figure 3.9: Folded cascode with diode loads.

An advantage of a cascoded CG stage is the high gain (G_mR), given the high output impedance. The CG stages increase the output impedance, but at the cost of one V_{OV} output voltage headroom as a consequence of the biasing. The impedance at $OUT\_CASCODE$ seen towards the drain of M8 (CG), is found by simplifying M10 as an ideal current source. Defining one PMOS of the input pair as $ro_{CS} = (ro_0||ro_{31}||ro_{32})$(Figure 3.5), the output impedance can be written as [18, p. 91]:

$$Z = [1 + (gm_8 + gmb_8)ro_8](ro_{CS}||ro_10) + ro_8 \tag{3.4}$$

Where gmb_8 is the transconductance caused by the base terminal.

For proper operation, all transistors must be biased in saturation. M11 and M10 are mirrored from $IDRAIN$ by M19($VBIAS2$). M8 and M9 are biased by $VBIAS1$, which is generated by M13 mirroring the bias current. The diode connected M19 and M17 drops the bias current according to their V_{TH} and V_{OV}:

$$VBIAS1 = V_{TH17} + V_{TH19} + V_{OV17} + V_{OV19}$$

(3.5)

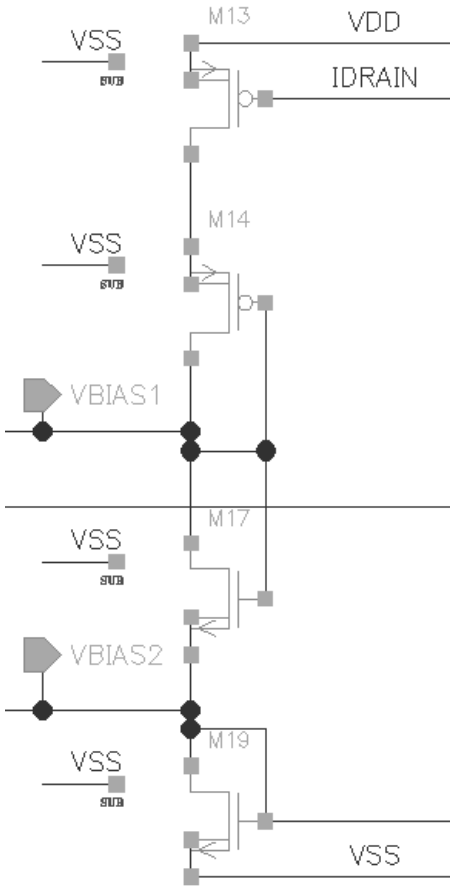


Figure 3.10: Biasing circuit

The layout is designed such that transistors pairs of equal function for each folded cascode are placed close together.

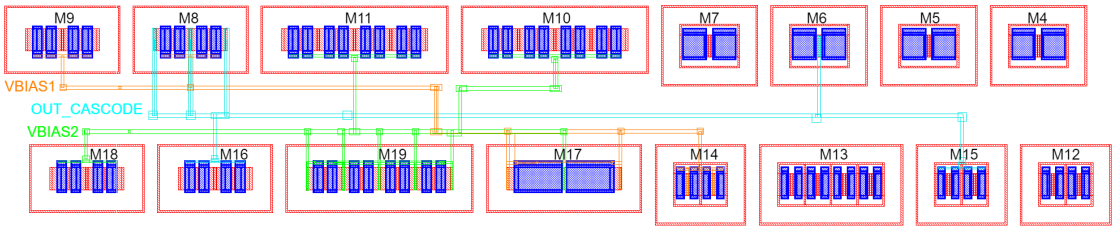


Figure 3.11: Layout of the folded cascode and biasing circuit.

3.3.3 Tri-state switch

The ASIC is specified to have the ability to either bias the probe screen from an internal source or externally. This entails that the opamp must either be acting as a follower, and be able to switch the output to a high impedance mode when an external source is used. This circuitry acts as a middle portion between the folded cascode and the CS power stage. Having $OUT\_CASCODE$ as input and OUT_P_GATE and OUT_N_GATE as output signals.

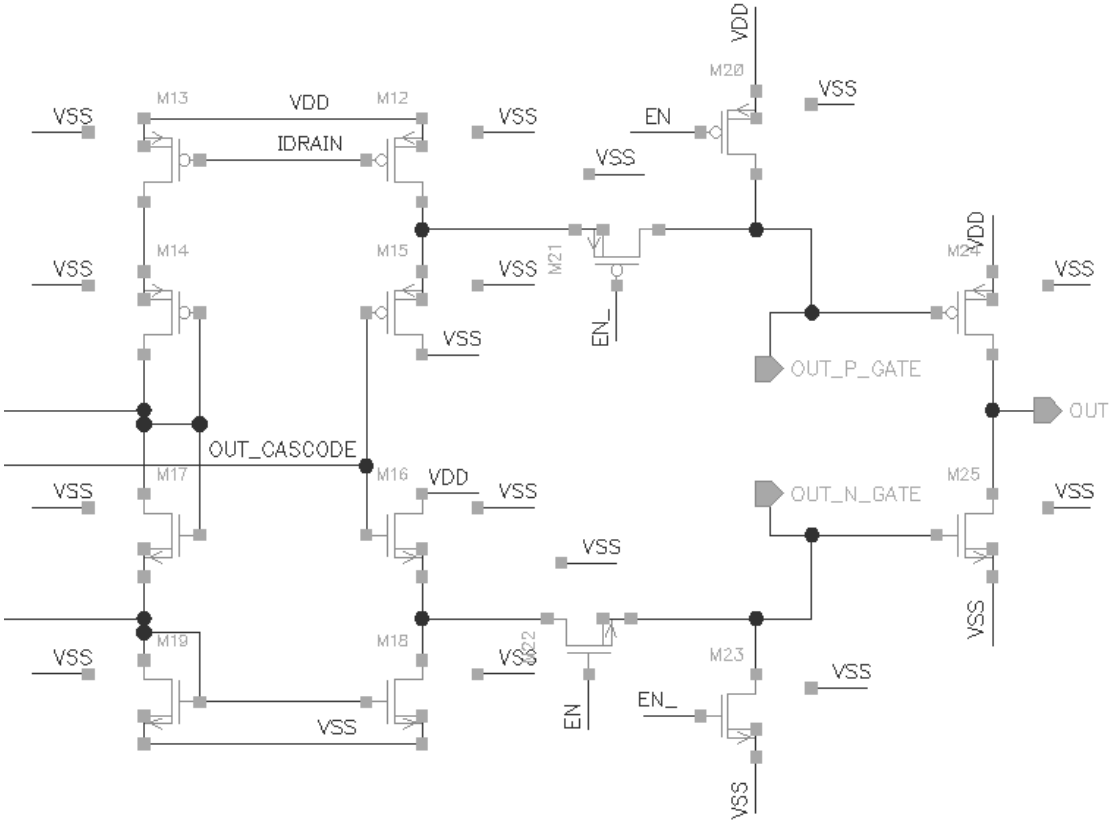


Figure 3.12: Output tri-state switch.

$OUT\_CASCODE$ enters two separate source followers $M15$ and $M16$. Each is connected to their respective current source, biased by $IDRAIN$ mirrored in the folded cascode biasing circuit. The SF stage separates the signal to enable separate control of M24 and M25. It also acts as a buffer for the folded cascode to the much larger CS power stage, helping with the low drive capability of the folded cascode.

The outputs from the source followers go into $M21$ and $M22$ acting as switches. They are controlled by EN and its inversion $EN\_$. In conducting mode ($EN = HIGH$), the signal conducts to the AB power stage. $M20$ and $M23$ act as either open ends ($EN = LOW$) or as straps, connecting OUT_P_GATE to V_{DD} and OUT_N_GATE to GND. This shuts off the AB power stage, thus acting as a high impedance for an external bias source.

M21 is connected with bulk/source connected to the source follower, resulting in it not being able to turn off when the output of the SF goes low. For the output to be completely shut off when the opamp is connected as a follower, the non inverting input must be connected to ground. This is corrected in chapter 7.

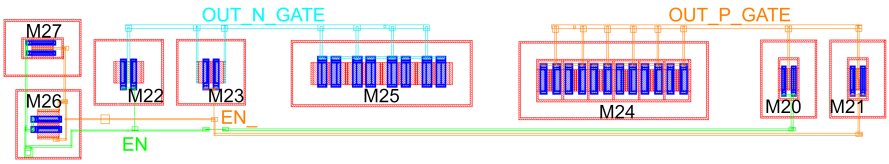


Figure 3.13: High impedance tri-state switch layout.

3.3.4 CS power stage

While the folded cascode has high gain, as a result of the high output impedance, the current driving capability suffers. Therefore it is not sufficient as a final amplification stage driving the probe screen. The CS power stage acts as a high drive capability final amplification stage of the opamp. Consists of two transistors, M24 and M25; having OUT_N_GATE and OUT_P_GATE as inputs. They can be viewed as a CS stage with an active load. In this case with a shared input signal with separate DC bias.

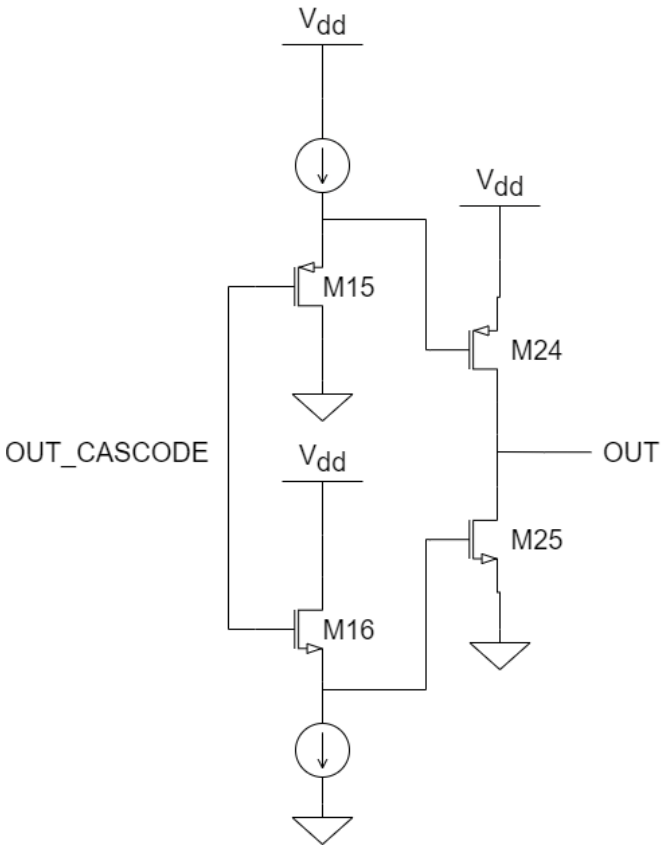


Figure 3.14: Functional schematic of the CS power stage.

The CS output stage is chosen given that it has a lower output impedance than the folded cascode. While it does offer some impedance and thus acts as further amplification over a source follower stage. This creates a compromise between drive capability and amplification. The following equation describes the parallel nature of a CS with active load[18, p. 59]:

$$A = -(gm24 + gm25)(r_{24}||r_{25}) \tag{3.6}$$

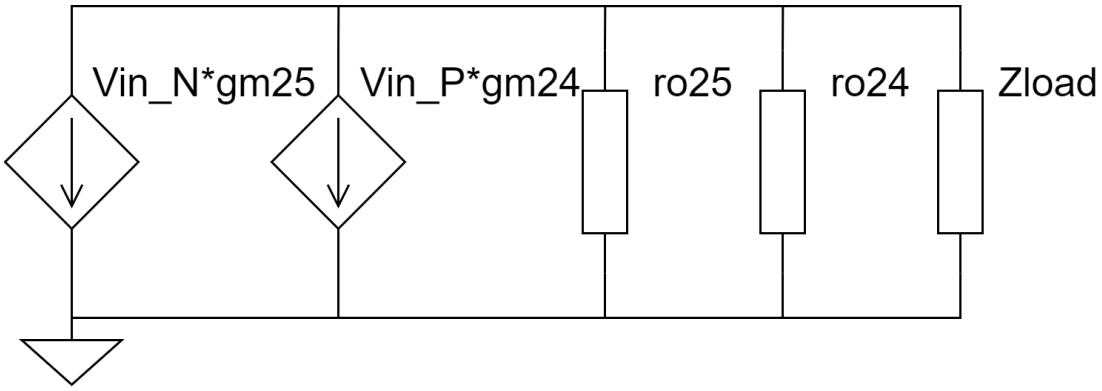


Figure 3.15: Small signal model of CS stage with active load and output load.

The operating range of the source followers is limited by V_{OV} below the input for M16 and over the input for M15, thus clipping a full-scale sweep of $OUT\_CASCODE$. This lowers the quiescent current when the output is close to either rail. The internal current is at its highest when $gmro_{24} = gmro_{25}$ and the output is $V_{DD}/2$. This is highly dependent on the size of the transistors, as it is a compromise between power consumption and drive capability. The ability to drive a load is a key characteristic of this stage, stemming from its use of singular regulatory transistors towards each rail; as this provides a high W/L-ratio. Another benefit is the large output span, provided by its inverting configuration of PMOS and NMOS. Both M24 and M25 have their bulk/source connected to either rail, having no V_{OV} drop to the output.

The output range depends on the drive current. When no load is attached and the opamp is simulated in an open configuration, the output is within a few millivolts from reaching either rail. However, when a load is used as a strap to a rail and the input is executed to draw the output to the opposite rail, the load and driving output transistor makes a voltage divider. As the follower is the only opamp tasked with a high load and it is not to drive the screen to either rail, this will not be an issue.

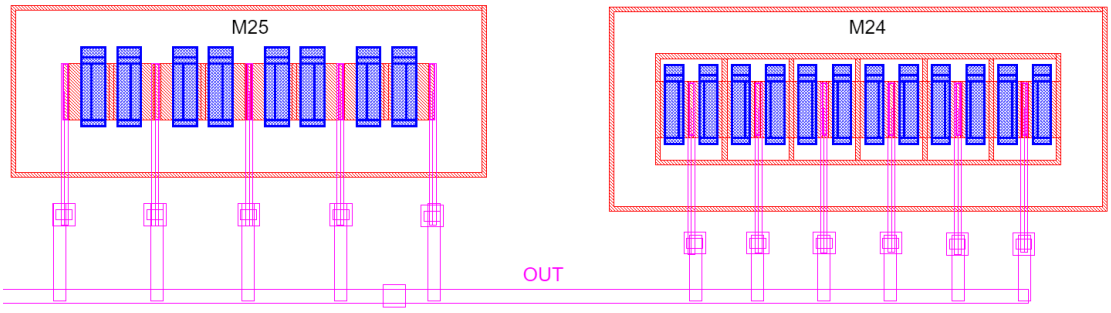


Figure 3.16: CS power stage layout.

3.4 Transimpedance Amplifier

A stage in the measurement of the plasma current is its transformation from a current to a voltage signal. In this design, a trans-impedance amplifier (TIA) is used for this function, as it provides low input impedance and is easily implemented with configurable feedback. The TIA consists of an opamp with a feedback resistor, through which the plasma current is sourced.

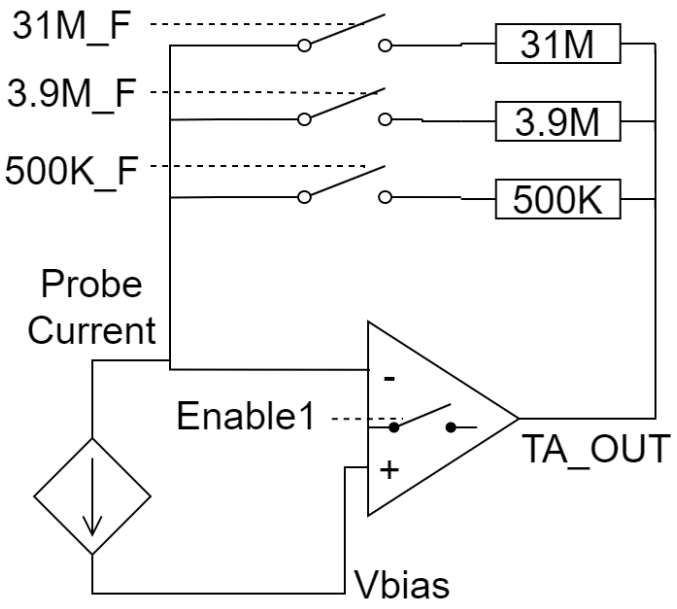


Figure 3.17: TIA functional schematic.

In this design, three optional values of feedback are used. This increases the dynamic range of the FE, as smaller currents can be amplified with higher feedback and larger currents will not reach saturation through smaller feedback values. The non-inverting terminal is connected to V_{bias} and this sets the lowest output value of the TIA.

The feedback is configured through three transmission gates. Each connects a feedback resistor of $500K\Omega$, $3.9M\Omega$ and $31M\Omega$. Each is dedicated to a region of the input range, with overlapping operation and saturation ranges. Starting with the lowest input signal with input being ($I_s = 150pA$), the voltage response with $31M\Omega$ is $4.65mV$ assuming an ideal OpAmp. Assuming the worst-case scenario with $10V$ screen bias, the output will increase until saturation at the highest output level close to $11.7V$. The saturation level will be $I_s \approx 55nA$. The mid-range low-end current can be discerned by scaling by the feedback value decrease ($31M/3.9M = 7.94$): $7.94 * 150pA \approx 9.4nA$. Switching to a $3.9M\Omega$ feedback results in $\Delta V \approx 36.6mV@9.4nA$ and saturation at $I_s \approx 436nA$. At the high end of the range ($7.8 * 9.4nA \approx 73nA$), a feedback value of $500k\Omega$ results in $\Delta V \approx 36.6mV@73nA$ and saturation at $\approx 3.4\mu A$. The following table displays these values for each feedback resistor value, and at each end of the screen bias range ($2V$ and $10V$).

Table 3.5: Ideal TIA feedback response

I_s	Feedback	$\Delta V@I_s$	Saturation level $2V$ bias	Saturation level $10V$ bias
$150pA$	$31M\Omega$	$4.65mV$	$312nA$	$55nA$
$9.4nA$	$3.9M\Omega$	$36.6mV$	$2.49\mu A$	$436nA$
$73nA$	$500k\Omega$	$36.6mV$	$19.3\mu A$	$3.4\mu A$

This table is meant as a signal range overview, as especially the lower-end bias is not

expected to result in such high currents for actual N_e values in the ionosphere.

The most important advantage of the TIA over a shunt ammeter is its low input impedance. Using an ideal opamp with infinite V_{OL}, infinite input impedance, and no input offset voltage(V_{OS}), the voltage between the inputs is $0V$. In this case, this creates a virtual copy of V_{bias} at the probe node. Viewing the signal source as an ideal current sink, the lack of voltage drop across the nodes makes the input impedance 0Ω. Introducing finite A_{OL} creates a limitation on the feedback response, using the design specification of $80dB$ as an example:

$$V_{out} = -I_{probe}\frac{R}{1+\frac{1}{A_{OL}}}, 50nV \approx -(-150pA)\frac{31M}{1+\frac{1}{80dB}} \tag{3.7}$$

This results in an input impedance of 333Ω. Input offset voltage is another source.

The noise at the output of the TIA defines the noise performance of the system. The Johnson–Nyquist noise of each resistor in the FE is an intrinsic part of the noise budget, creating a noise floor and thus a limit on the smallest discernible plasma current:

$$V_n(RMS) = \sqrt{4K_bTR\Delta f} \tag{3.8}$$

Where K_b is the Boltzmann constant, T is the temperature in Kelvin and Δf is the measured bandwidth. As the feedback resistors of the TIA is the largest in the FE it sets the best-case noise floor for the entire system. While mission temperatures may vary greatly, 20° is assumed for the following calculations. The bandwidth is based on previous implementations of m-NLP ($10kHz$):

Table 3.6: Thermal noise from feedback

Feedback	$V_n(RMS)$
$31M\Omega$	$70.82\mu V$
$3.9M\Omega$	$25.12\mu V$
$500k\Omega$	$8.99\mu V$

The opamp should have an internal noise level low enough for the feedback to be the dominant noise source. However, the behavior of the opamp noise sources and the white, thermal noise of the resistor is not necessarily the same. The $1/f$ noise from the FET will be higher than the thermal noise when integrating over arbitrarily long periods. In both satellite and sounding rocket applications, the signal will consist of frequency components in the hundreds of Hz.

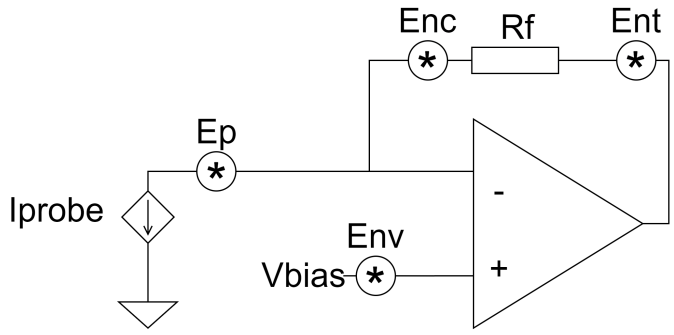


Figure 3.18: TIA noise model. E_p is noise from the probe, E_{nc} is the opamp input current noise multiplied by the feedback, Env is the input voltage noise, and E_{nt} is the thermal noise from R_f.

Assuming that the noise sources are independent of each other, the RMS value of the noise sources combined are:

$$E_{RMS} = \sqrt{E_p^2 + E_{nv}^2 + E_{nc}^2 + E_{nt}^2} \tag{3.9}$$

3.5 Level shift amplifier

The receiving end of the FE is intended to be a low pass filter and finally an ADC. The ADC is impractical to implement with high voltage transistors, making signal level conversion necessary. The level shift amplifier (LSA) has the output of the TIA, V_{bias} and the positive reference of the ADC (ADC_{ref+}) as inputs:

$$V_{out} = ADC_{ref+} - \frac{(TIA_{out} - V_{bias})512k}{R_G} \tag{3.10}$$

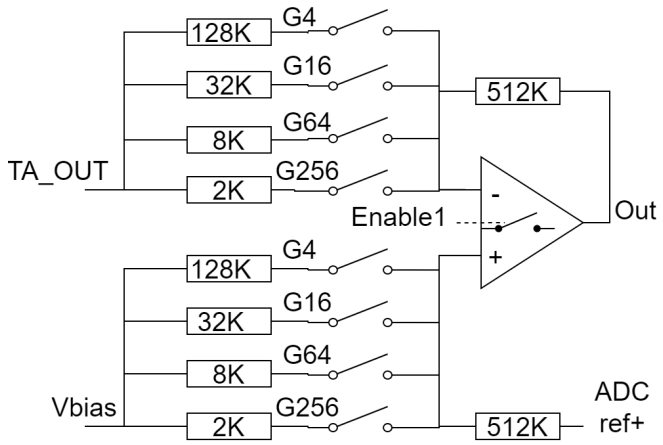


Figure 3.19: LSA functional schematic.

TIA_OUT is amplified with respect to its differential counterpart signal V_{bias}. The output level is ADC_{ref+} at zero plasma current and reaches $0V$ at saturation. The gain values are based on PEX simulations, ensuring that the output for each gain value has some overlap for each feedback value for the TIA. When sweeping the plasma current from $150pA$ to $1.5\mu A$, each of the TIA feedback values used in separate simulation runs.

For each TIA feedback, all four discrete gain values are selected resulting in 12 runs. $V_{bias} = 10V, ADC_{ref+} = 3.3V$

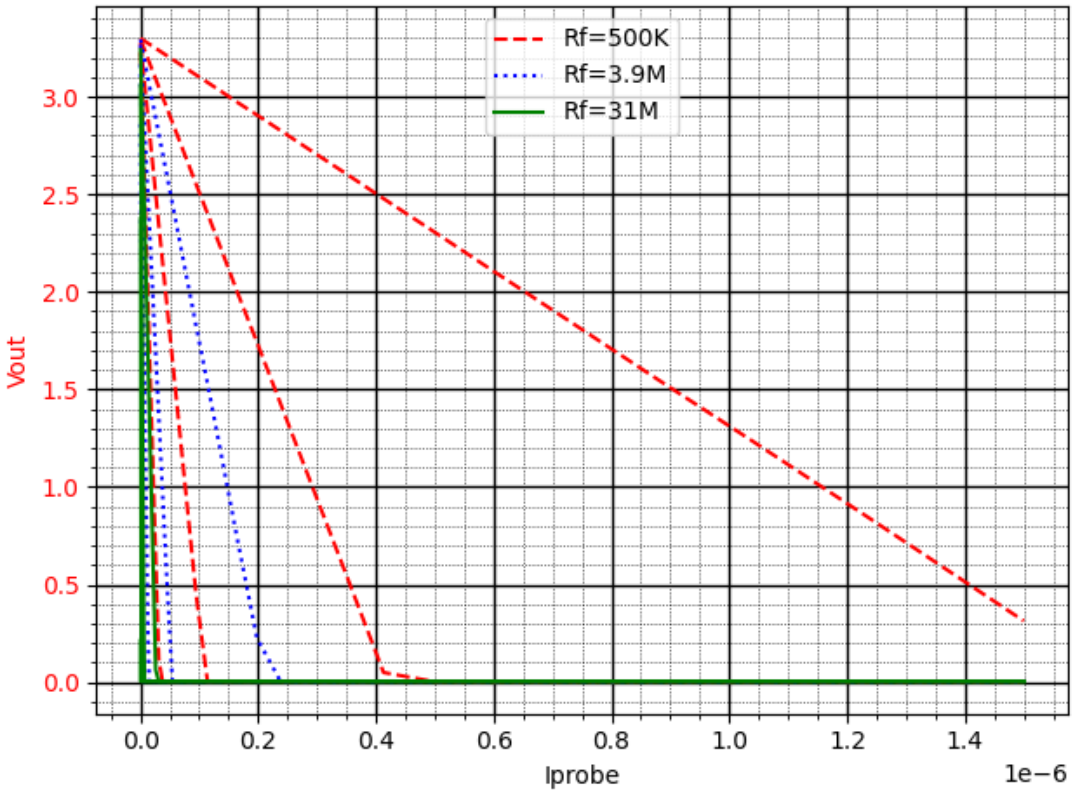


Figure 3.20: LSA output, Iprobe $150pA \Rightarrow 1.5\mu A$.

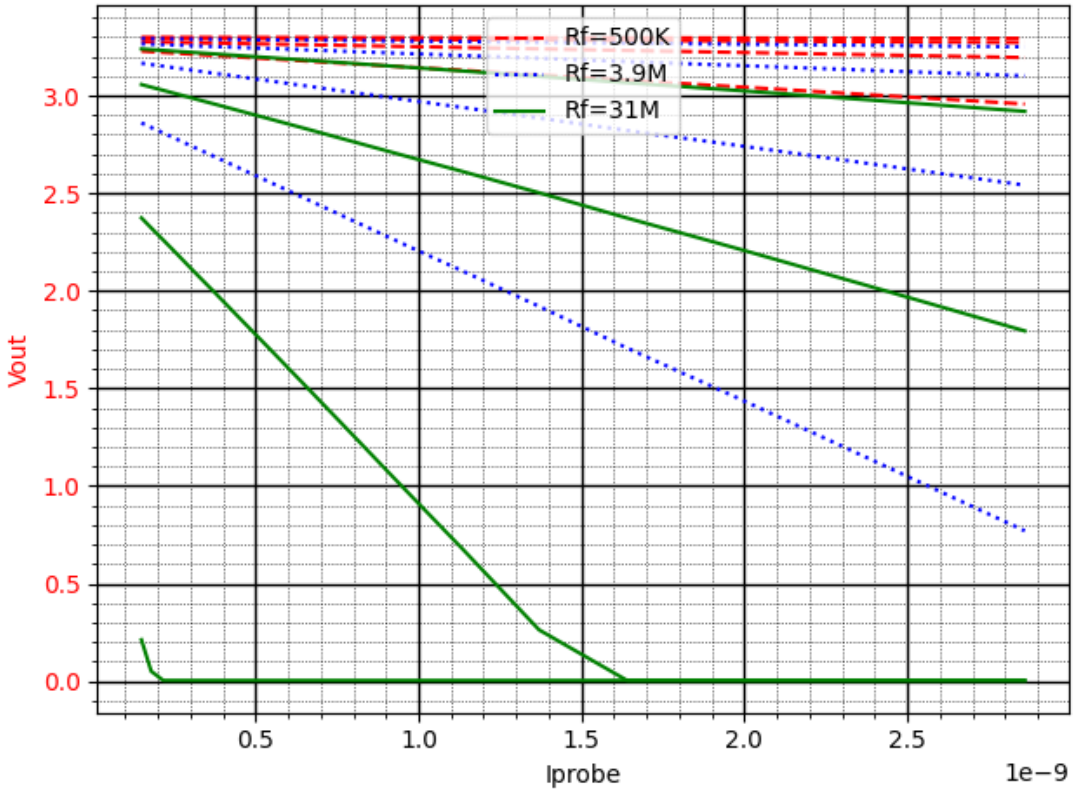


Figure 3.21: LSA output, Iprobe $150pA \Rightarrow 2.8nA$.

The two lower gain values have an operational overlap with the two highest of the lower TIA feedback. This provides a margin of error for process and off-chip variations.

3.6 Transmission Gate

A Transmission Gate TG operates as a solid-state electronic switch, either opening or closing a connection between two nodes (A and B). A common implementation consists of a NMOS and PMOS with opposing drains and sources connected to the two nodes. Controlling the switch is a logic-level control signal (EN) and an inversion (EN) of this signal. EN controls the NMOS and $EN\_$ controls the PMOS.

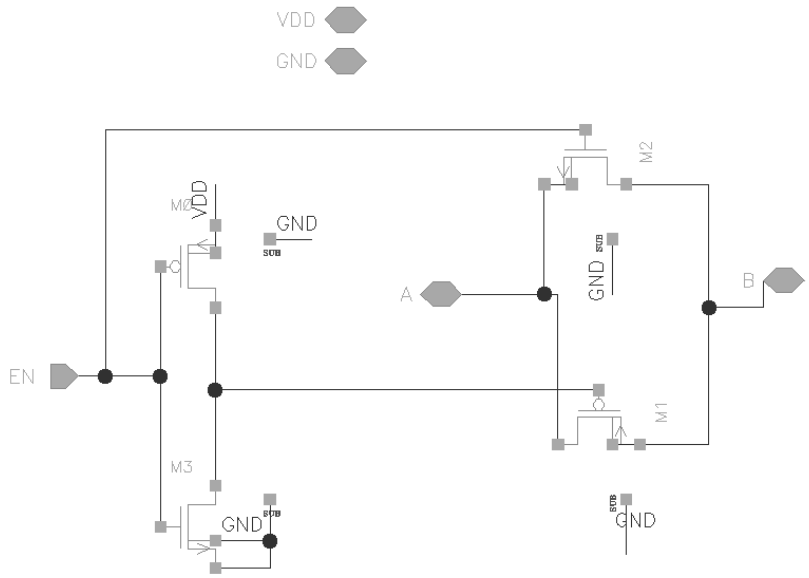


Figure 3.22: Standard TG

Using both types ensures conductivity from ground to VDD level from both points, either well above V_{TH_N} or well below V_{TH_P}. In the ideal case, a TG would operate as a switch with either infinite or zero impedance. However, as with all real devices, there are factors causing non-ideal behavior. For the 'ON'-state, there is an $\frac{W}{L} \propto Z$ -relationship. Increasing W will lower the on-state impedance, but will also slightly lower off impedance because of capacitance between drain and source. In addition, this will also cause a higher leakage current. As this application has low expected input frequencies, the increased capacitance is negligible. Leakage current showed a 14% increase from a $10*W$ increase, suggesting a weak relationship.

Implementing the above circuit with the transistor family chosen for this design, proved problematic in the OFF state. When the voltage source is connected to node A and a load to node B. There is a leakage current from node A that is $22\mu A$ at its highest when sweeping A $0V \Rightarrow 12V$. However, when swapping ports and putting the source at node B the leakage current is $97pA$ at $12V$. Separating the P-type bulk from the source and connecting to V_{dd} doesn't improve this problem.

Using the fact that the open mode is functioning well in one direction, the circuit can be mirrored. Ending up with TG that operates properly in the off state, independently of the direction of the higher voltage. The main drawback of this is the increased impedance.

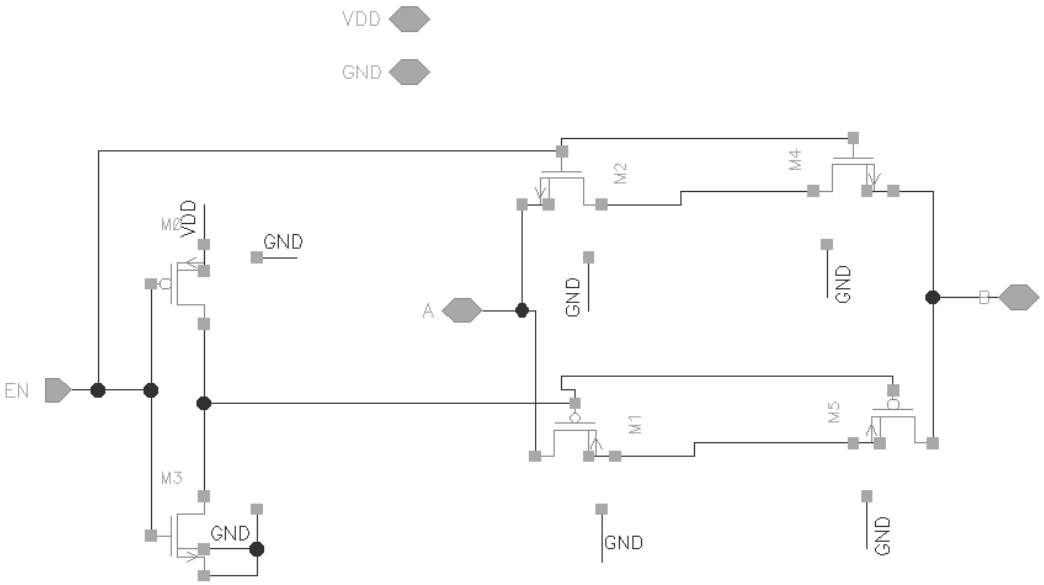


Figure 3.23: Dual mirrored TG

Table 3.7: TG transistor sizes

Transistor	W/L
M1	$20\mu/500n$
M5	$20\mu/500n$
M2	$20\mu/400n$
M4	$20\mu/400n$
M0	$10\mu/500n$
M3	$10\mu/400n$

The width of the conducting MOS is larger to minimize ON state impedance. Each is divided into 4 gates(fingers) and all current carrying connections are made with wide metal.

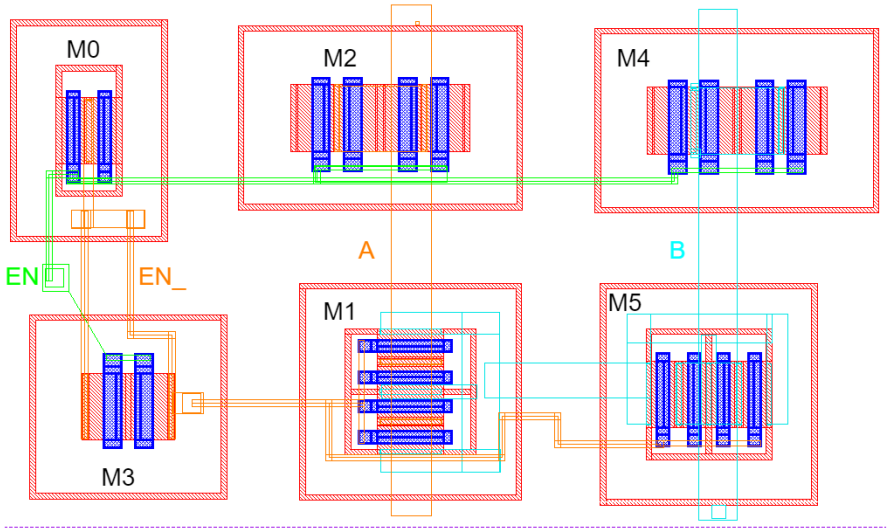


Figure 3.24: Bode plot of the PEX model of the opamp.

DC simulations are made to asses the ON and OFF state non-ideal characteristics:

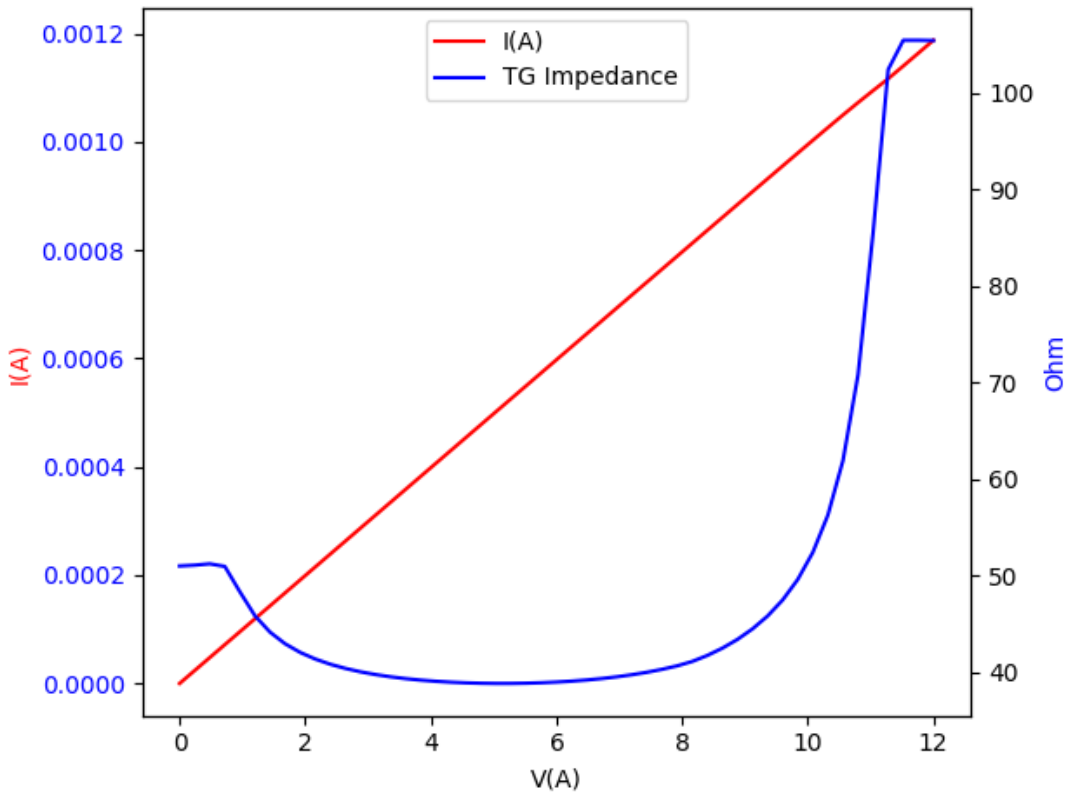


Figure 3.25: TG ON state impedance, $V(A)$ sweeped with a $10k\Omega$ load at node B.

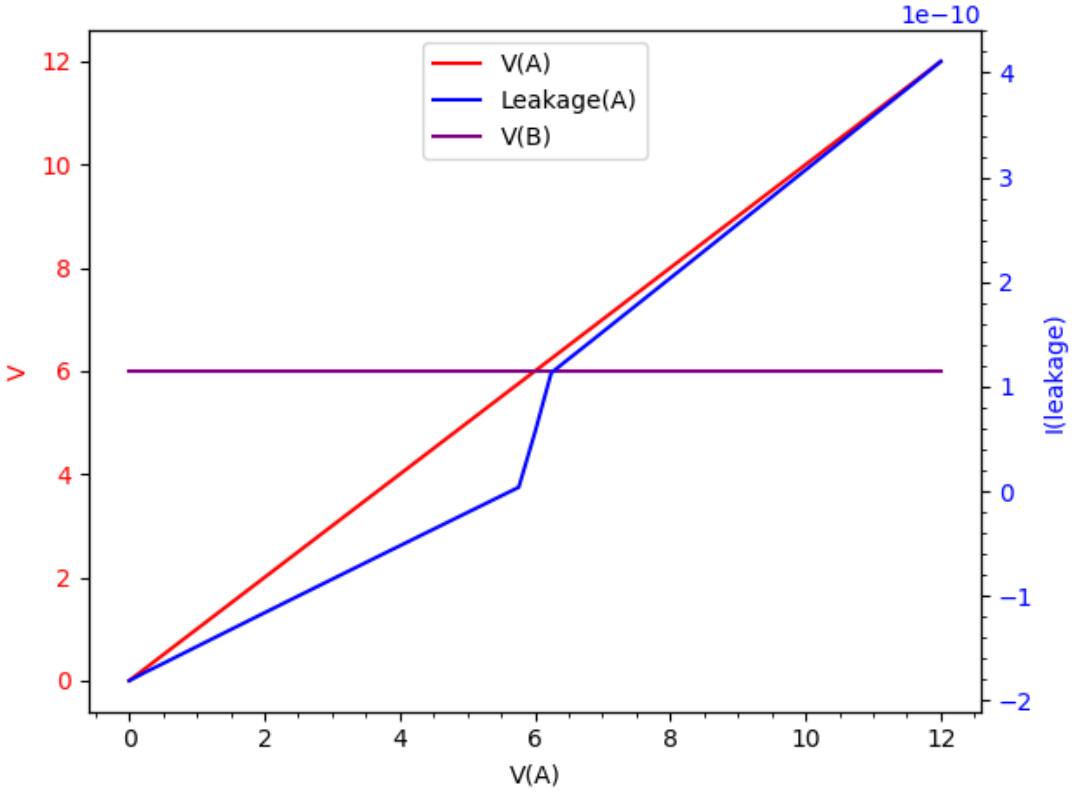


Figure 3.26: TG off-state leakage.

Interestingly there is a large variance of the impedance in the higher voltages. Though most of the resistors connected by the TGs are much larger relative to this change, the most sensitive is the $2k\Omega$ feedback for the LSA. However, the voltage difference between the two TG is small as it relates to the open loop gain of the opamp.

To characterize the leakage current, node A is swept $0V \Rightarrow 12V$ with node B kept at a constant $6V$. Where $V(A) = V(B)$ the leakage at node A is $60pA$. This can be an issue with the TIA. As 2 TG in parallel in an off-state can result in a leakage current of $120pA$. While it is unlikely that all three TG has the same leakage current. A mismatch can cause conflicting directions of current, canceling the effect. While leakage can cause an offset, calibrating the FE using a known current sink should mitigate this effect.

3.7 Overall layout

This section presents the overall layout design and describes details common to all functional blocks. The complete design is implemented as a stand-alone section on an ASIC containing other designs. The ASIC was packaged in a JLCC-84 package[2].

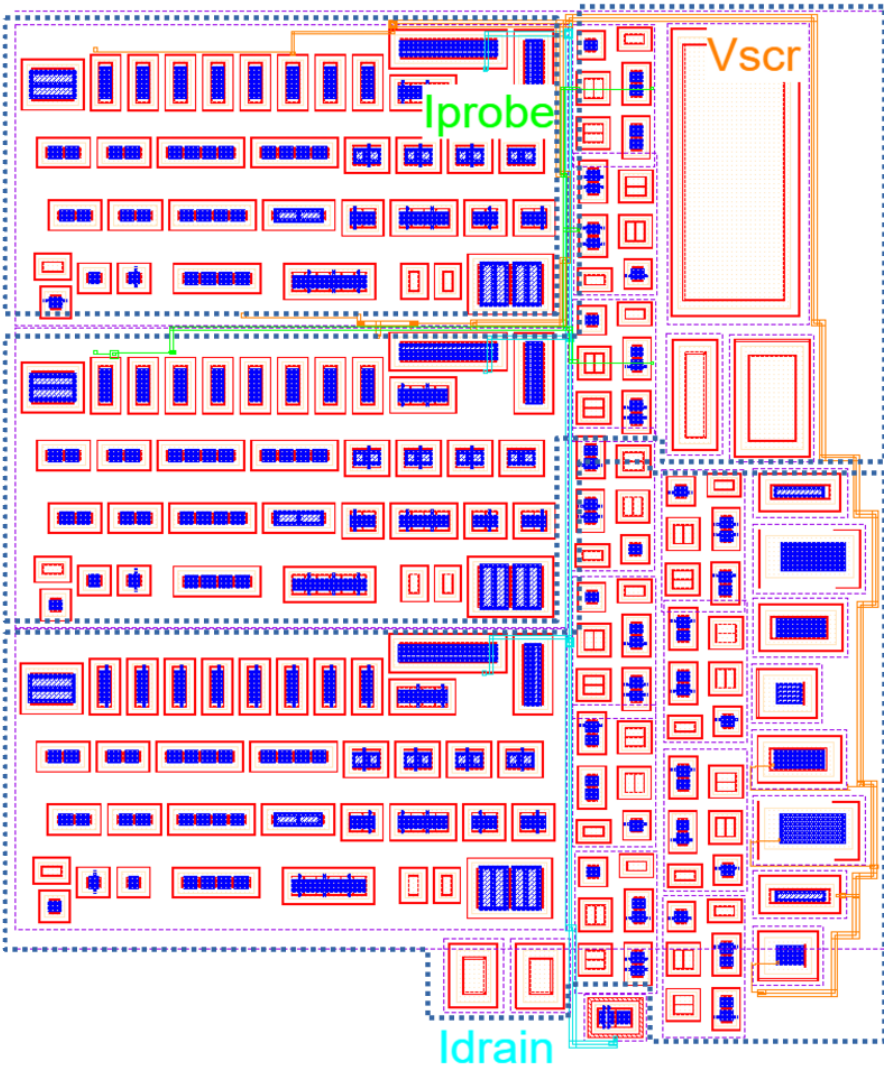


Figure 3.27: Complete layout, excluding connections to padframe. Key analog signals are highlighted. Top-left markup: follower for V_{bias}, center: TIA, and bottom: LSA. Dimesions: $W = 420\mu m, H = 522\mu m$.

3.7.1 Resistors

The resistors used in this design, especially the feedback for the TIA are of high value. To reach the needed resistance values, the resistive material needs a high enough $\Omega/area$ to be practical to implement. The same polysilicon layer used for the MOS transistors was chosen, with $R = 435\Omega/\mu m^2$. Starting with the smallest resistor, the $2k\Omega$. While a single 'finger' using the minimum process width of $180nm$ would result in lower area consumption, using a larger width($W/L = 4\mu/22\mu$) results in better matching and less dependence on the geometry of the connection point. The higher value resistors ($500k\Omega, 512k\Omega, 3.9M\Omega, 31M\Omega$) are made by using minimal width, multi-finger poly

structures. The fingers are meandered to mitigate the mutual induction between lines. Using a minimum-width resistor puts a limitation on the current carrying capacity. Since the maximum current passing through any resistor is on the order of $\approx 20\mu A$, any thermal effect is negligible given the large resistor layouts.

The resistors used in this design are connected to signals that can reach voltage levels up to V_{DD}. To protect the base substrate from high voltage, the poly layer needs to be put in the same structure as the $12V$ MOS.

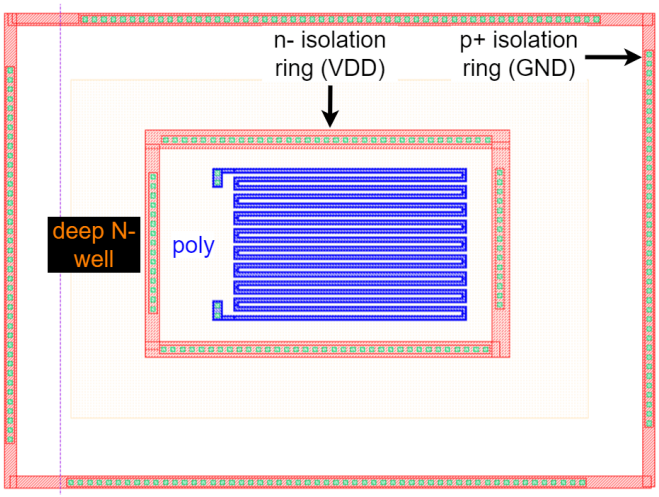


Figure 3.28: $512k$ resistor layout.

3.7.2 Power delivery network

This section focuses on the on-chip power delivery network. The PCB-mounted decoupling capacitors will filter the current spikes drawn by the ASIC from reaching the external inductive connections. However, the power delivery network from the board capacitors up until the ASIC is in need of on-chip decoupling. This is because of the packaged IC using bonding wires will have relatively long power supply lines. V_{DD} and GND are distributed with wide metal planes. Firstly as a means to lower the inductance and better the reference between individual parts of the system. To achieve some capacitance the metal layer fills are connected to V_{DD} and GND and interleaved. Larger areas within each design block are filled and connected to a power plane. On the top level, every design block is connected by metal layer 5 and 6 which is exclusively used for power distribution. Besides good power delivery, another positive effect is that the density design rules are upheld.

Inter-metal plane capacitance is relatively low per unit area. To reach higher capacitance, NMOS of the same transistor family are used. The source/bulk and drain are connected to GND with the gate connected to V_{DD}, exploiting the close proximity provided by the thin gate oxide layer for the higher capacitance than inter-metal layer capacitance per unit area. However, as the gate-bulk capacitance relies heavily of the DC level of V_{GB} it behaves as a less ideal capacitor than metal planes.

Decoupling capacitors do not only decouple current spikes stemming from the ASIC from reaching the inductive power lines off-chip, but it also filters external noise sources.

This helps increase the overall PSRR of the system.

3.7.3 Padframe connections

All connections between the ASIC and the chip carrier are made through pads connecting the bonding wire. Each pad is equipped with a *pn* junction to provide ESD protection. More intricate ESD structures are part of the non-disclosed pads supplied by TSMC.

To reduce the impact of induced noise on analog input and output signals, differential signals are grouped together on the padframe and kept close in the layout.

Chapter 4

Simulation

This section describes the schematic and post-layout simulation of the opamp, TIA, LSA, and the system as a whole. Results are discussed and compared to the goal specifications. The post-layout simulation takes the parasitic extraction (PEX) effects from the layout design. The parasitic for this process involved resistance and capacitance as there was no model for inductance. Comparing the schematic and PEX model gives a comparison between ideally connected transistor models and an approximation of the real connections to the transistor nodes.

Another important simulation technique is the Monte Carlo simulation. Which consists of several runs of the same simulation, with random variations according to the process and mismatch. What comes out of this is a figure of spread in performance between fabricated units(process) and variations between identical layout structures(mismatch). Unfortunately, the part of the Process Design Kit (PDK) that contains the process and mismatch variation for the HV transistors was not available.

4.1 Opamp simulations

4.1.1 Open loop gain and phase margin

Open loop gain A_{OL} is the amplification in an operational amplifier without feedback. This value is characterized at DC and varies greatly between types of amplifiers, usually in the order of $100dB$ to $160dB$. The reason it is specified at DC is the coupling of gain and bandwidth and since A_{OL} is high relative to the amplifier, the bandwidth will be low. Any feedback reducing the gain will also increase the bandwidth.

Gain is tightly coupled with the bias current (Idrain). Open loop AC analysis with several bias currents was performed to find a current level that provides high gain:

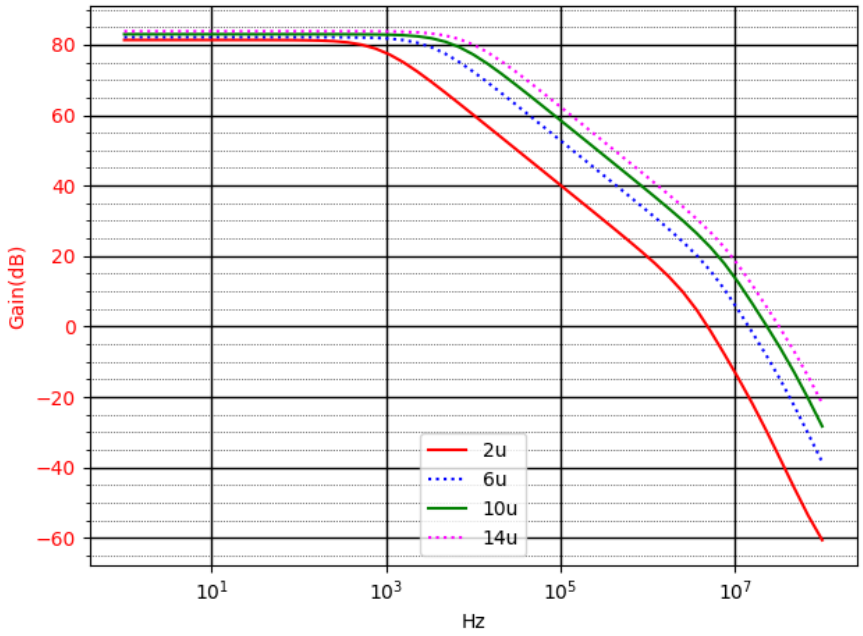


Figure 4.1: Idrain simulation, PEX model.

This design uses $I_{drain} = 14\mu A$, as simulations with higher currents resulted in diminishing returns.

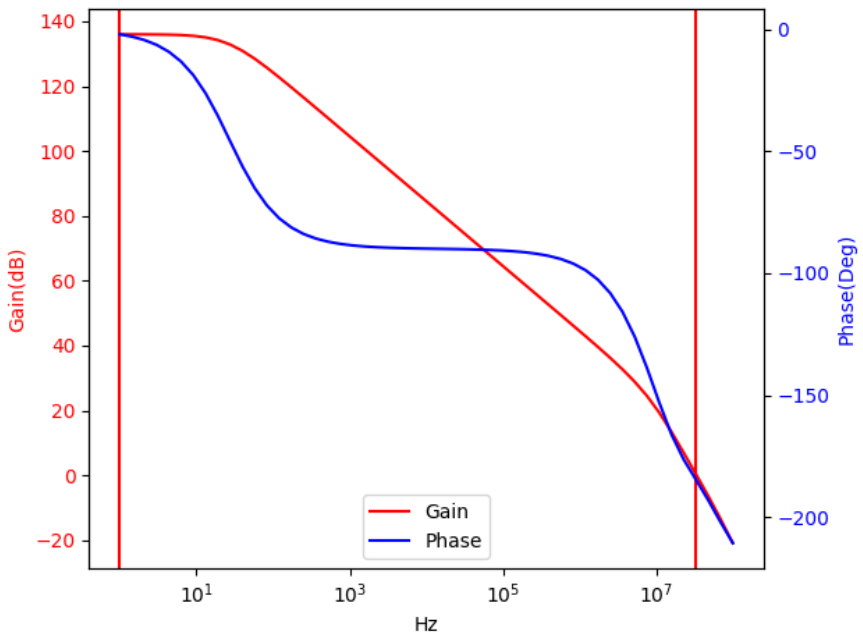


Figure 4.2: Schematic bode plot.

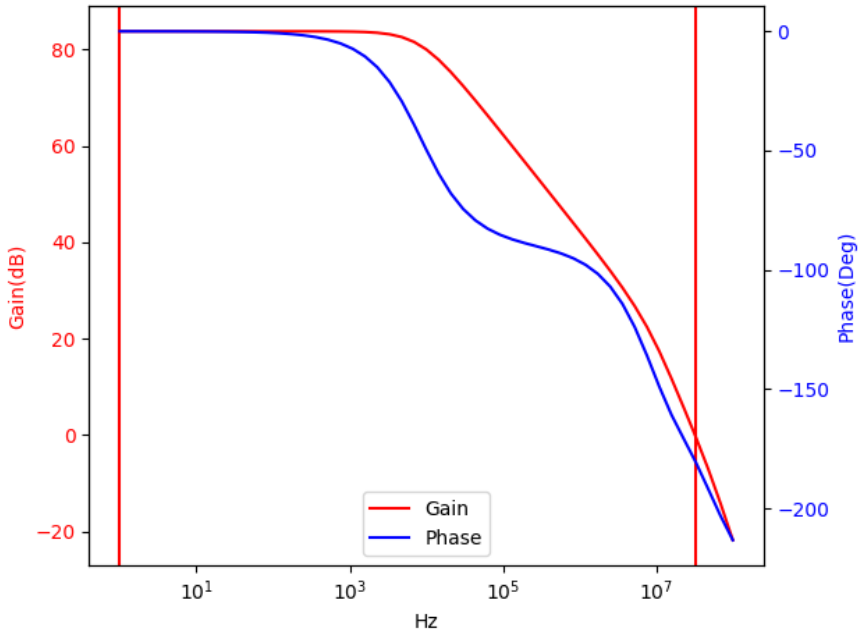


Figure 4.3: PEX bode plot.

The open loop DC gain is $136dB$, which is relatively high and can cause issues with stability. When inspecting the phase, the two poles are clearly visible. The phase margin is a concern for the follower having 0° -PM. This could be solved with a compensation capacitor[19, p. 160] between the output and the single-ended output of the folded cascode, forcing the second pole to a higher frequency and thus leaving some phase margin even for unity gain. However there were difficulties with implementing a high voltage capacitor in the layout before the tape-out, so the final design is without.

The gain dropped considerably in the PEX model ($83.78dB$). Another difference in the result is the increased frequency of the first pole corner frequency. This results in a delayed drop in gain and results in the same issues regarding phase margin. This misses the goal criteria and is a risk with regard to the follower.

To Find the source of the large variation in A_{OL} between PEX and schematic, measurement points were attached to nodes throughout the schematic. When performing a transient simulation, open loop with $V_{CM} = 6V$ and a $10mV$ sine on the inverting input; the output of the folded cascode deviated between the schematic and PEX model(signal labels are the same as in chapter 3):

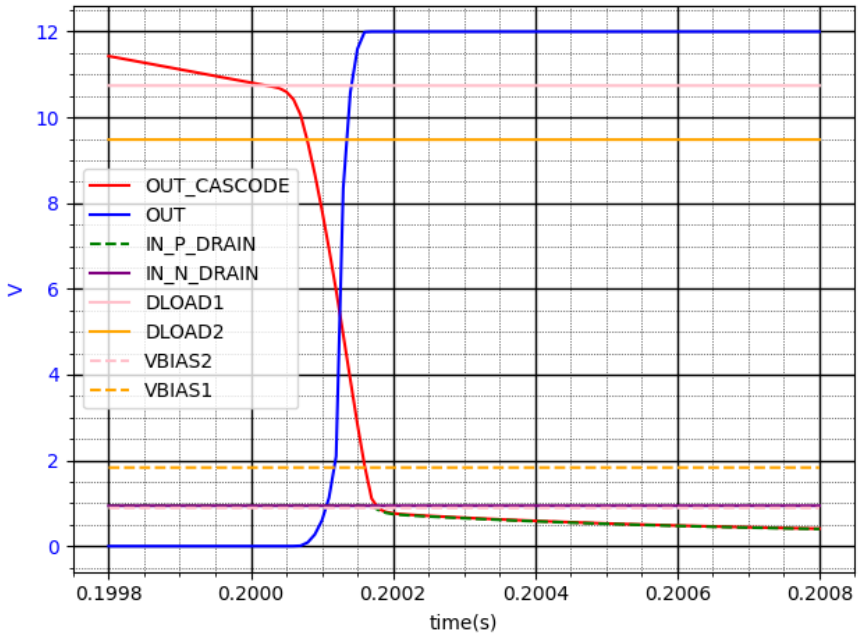


Figure 4.4: Schematic transient simulation.

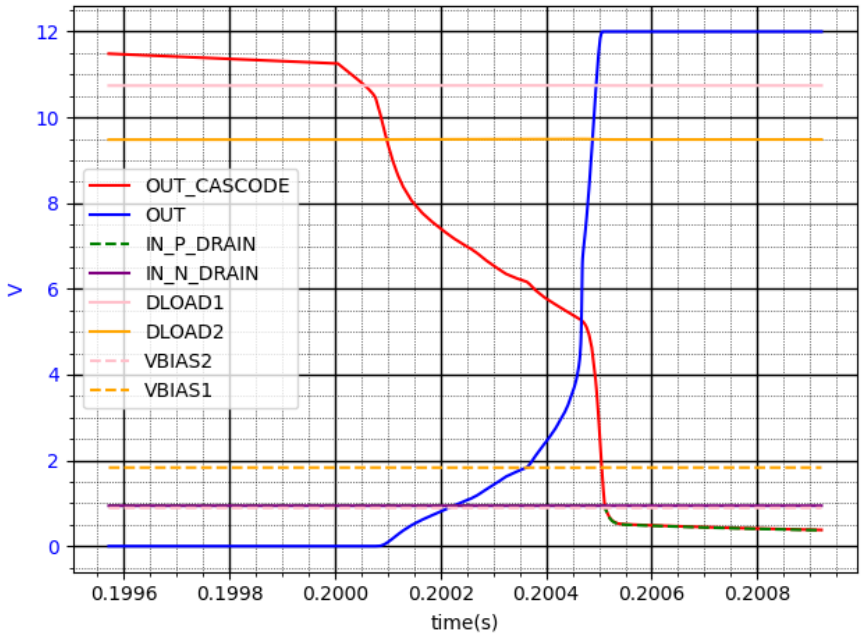


Figure 4.5: PEX transient simulation.

The results showed that the largest deviation is when the output steps are high. Here the output of the folded cascode has a lower response to the input currents and results in a non-linear response for most of the range. This does not occur when the output goes low, here there are no discernible differences between the PEX and schematic model. Though no differences in bias voltages were found, the response suggests that some transistors are outside of the saturation region.

4.1.2 Common Mode Range

The common mode range is the range in which the gain is at an acceptable level. To test the drop in gain, V_{CM} -levels close to the upper limit of the input pair is tested in an AC simulation in an open loop.

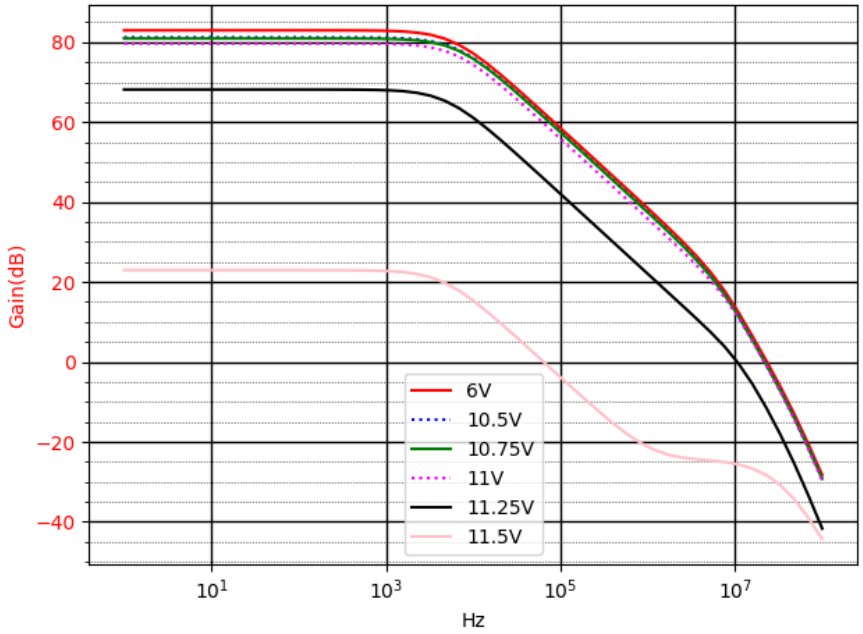


Figure 4.6: CM corner simulation.

The decrease in gain from mid range to the $V_{CM} = 10.5V$ -criteria is $83.78dB@6V_{CM}$ vs $81.18dB@10.5V_{CM}$.

4.1.3 PSRR

The PSRR is simulated by executing an AC component in series with V_{DD} supply. The opamp is connected as a follower with $V_{in} = 6V$ and $V_{DD} = 12V$. The simulated model is PEX, which includes some inter-planar and MOS decoupling capacitors.

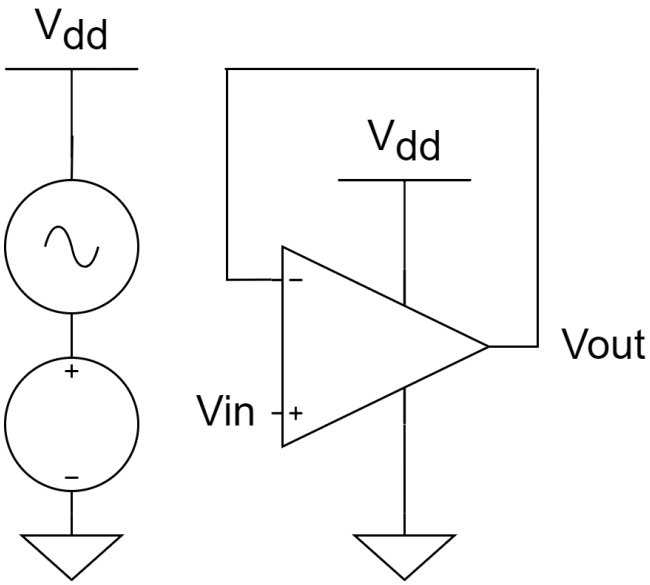


Figure 4.7: PSRR simulation setup.

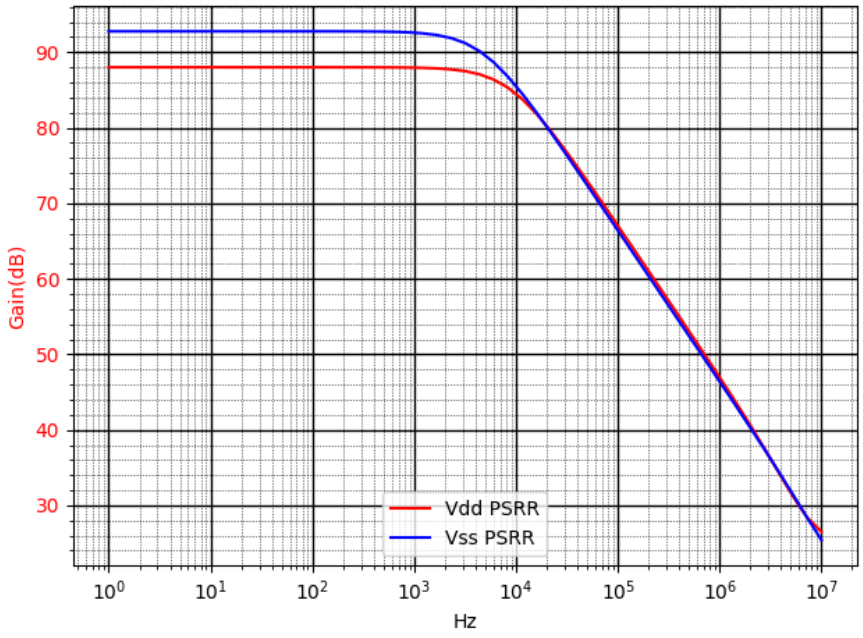


Figure 4.8: PEX opamp PSRR frequency dependency.

PSRR is given in dB as a value of $20log(V_{rail(AC)}/V_{OUT})$ The resultant $PSRR_{V_{DD}} = 88dB$ and $PSRR_{V_{SS}} = 92.77dB$ from DC to a corner frequency of $f_c = 8300kHz$ and $f_c = 5000kHz$ respectively. As seen, the value drops considerably into the MHz range. These values do not take into account external bypass structures, however, they do provide a pointing pin as to the robustness of the system with regard to noise on the power rails.

4.1.4 Output range and load drive capability

As the opamp is unstable at unity gain, the load simulations are done without transient noise. Any AC noise artifacts reaching the follower would result in oscillations. Without a load, the output is capable of reaching each power rail within $1mV$. Adding a load will add an external current draw, which will limit the output range. The load in this case is either the probe screen or an oscilloscope probe with a standard load value of $50pF$. The two configurations dealing with external loads are the voltage follower and LSA. To simulate the follower, the capacitive load is connected to the output with an AC simulation run of the input with $V_{CM} = 6V\ 75dB$.

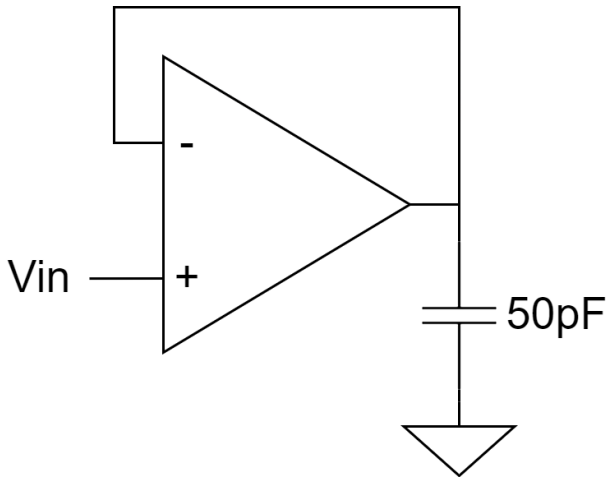


Figure 4.9: Output load simulation.

This resulted in $G = -80\mu dB$ up until a corner of $15kHz$, similar results as without the load. Displaying the ability to drive a realistic load in the bandwidth of interest. A more demanding test while using a load is when the opamp is configured with a higher gain. Testing the LVS with its highest gain $G = 256$, the AC simulations revealed no differences. With and without load resulted in $G = 48.11dB$, within expectations of the ideal $G = 48.16dB$.

4.2 Transimpedance amplifier and level shifter/amplifier

This section describes the simulations performed on the TIA and LSA.

4.2.1 Input impedance

Simulating the input impedance of the TIA provides a value of how much the TIA impacts the plasma current. The input impedance is a function on the gain of the amplifier and the feedback resistor. To map the input impedance over a frequency range, the gain bandwidth product is used:

$$Z_{in} = \frac{R_f * f}{GBP} \tag{4.1}$$

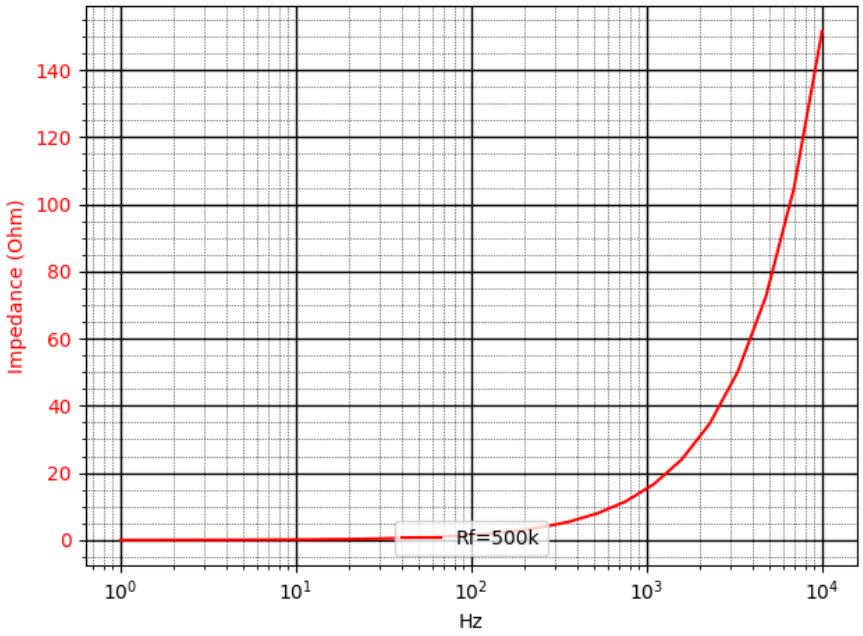


Figure 4.10: TIA input impedance, $R_f = 500k\Omega$

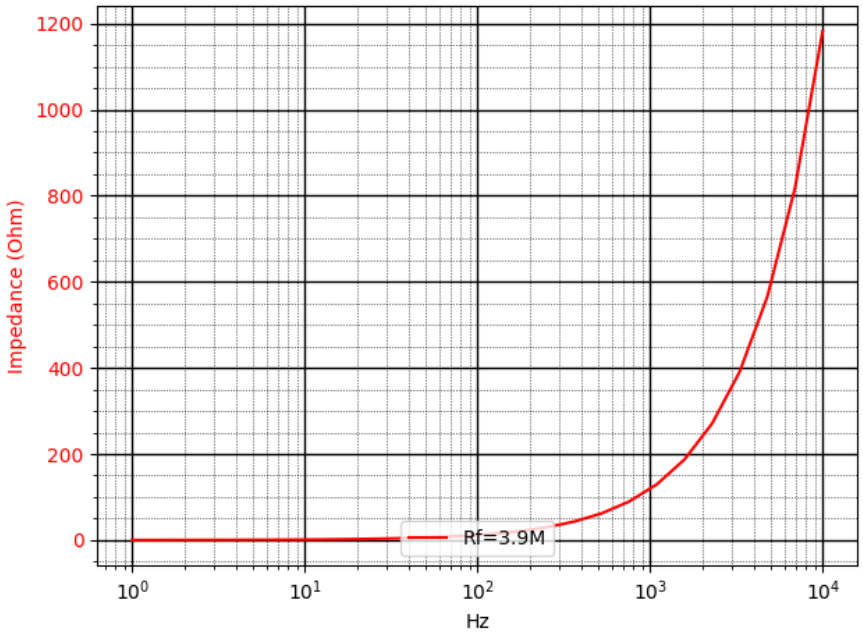


Figure 4.11: TIA input impedance, $R_f = 3.9M\Omega$.

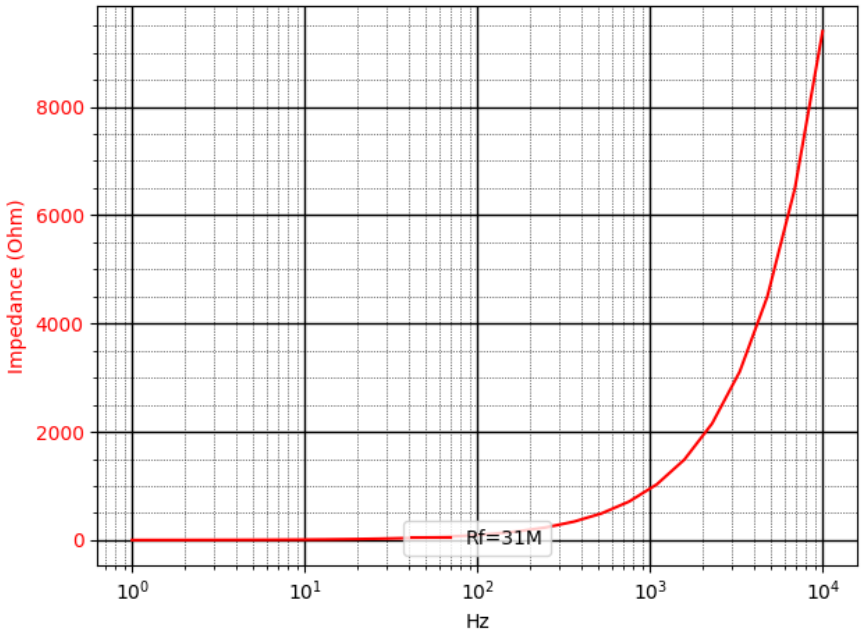
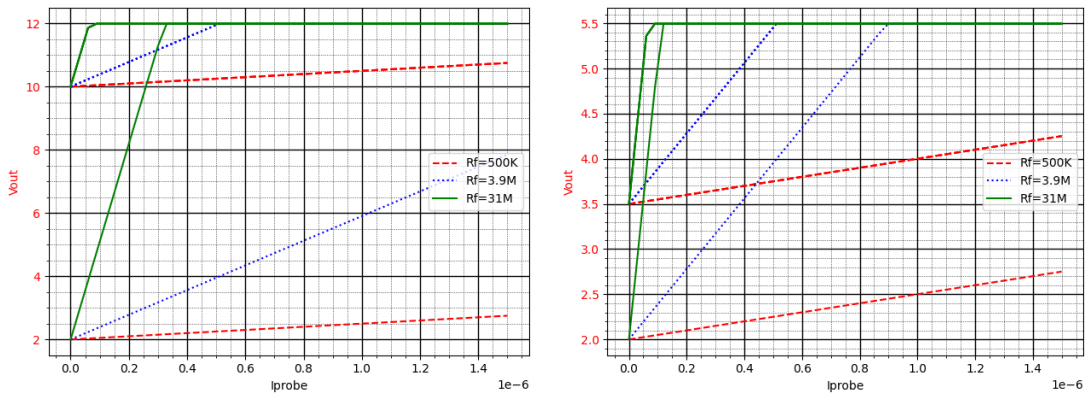


Figure 4.12: TIA input impedance, $R_f = 31M\Omega$.

4.2.2 TIA signal variation

To test the TIA against the expected signal variations, a DC-simulation is made for the upper and lower end of the V_{bias} range for $V_{dd} = 5.5V$ and $V_{dd} = 12V$



(a) TIA signal range for all feedback values, upper and lower signal levels for V_{bias}. $V_{DD} = 12V$.

(b) TIA signal range for all feedback values, upper and lower signal levels for V_{bias}. $V_{DD} = 5.5V$

Figure 4.13: TIA output range.

The requirement to handle a 10% signal sweep within $1ms$ was tested through transient simulation. When switching between feedback values of the TIA, it always resulted in full-sweep oscillations. This issue is resolved in Chapter 7.

4.2.3 Noise

To map the noise stemming from the opamp itself over a frequency range, the opamp is connected as a follower for unity gain.

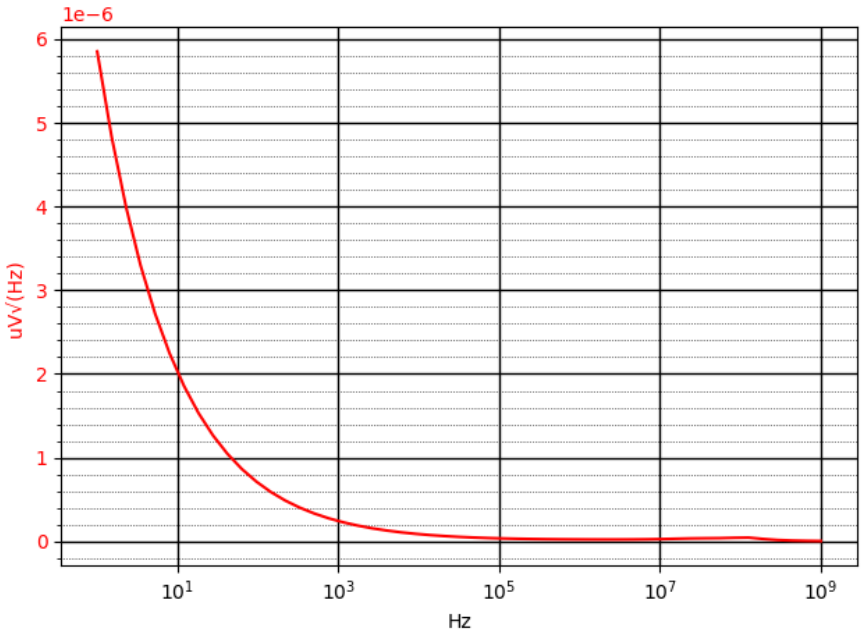


Figure 4.14: Opamp AC voltage noise simulation.

The initial response shows a clear $1/f$ frequency dependency. Having a density in several $\mu V/\sqrt{Hz}$ is quite high, especially when considering the large dimensions used for all analog MOS. In the higher frequencies, the white broadband noise ($\approx 20nV/\sqrt{Hz}$) becomes dominant.

The FE is simulated using transient noise models from all components. Given the extensive time it takes to simulate the entire system, some limitations are made. Firstly, the maximum noise bandwidth is limited to $10MHz$. Secondly, schematic models are used to simplify the simulation.

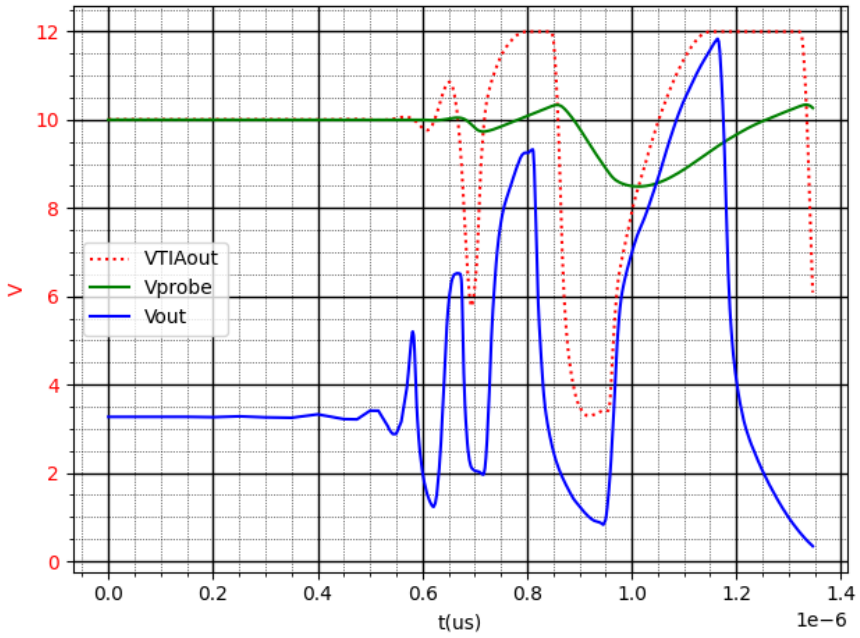


Figure 4.15: FE schematic model transient noise simulation. $I_p = 15nA$, Gain=4, $R_f = 500k\Omega$.

The stability issues with the opamp become apparent when higher frequency transient noise sources are introduced. All feedback values for the TIA and all gain settings for the LSA results in wide voltage swings.

Given that the LSA is inverting the output of the TIA, a feedback capacitor can be used to limit the large voltage swings. Through experimentation a feedback value of $50nF$ between the output of the LSA and the probe input achieved a stable noise response:

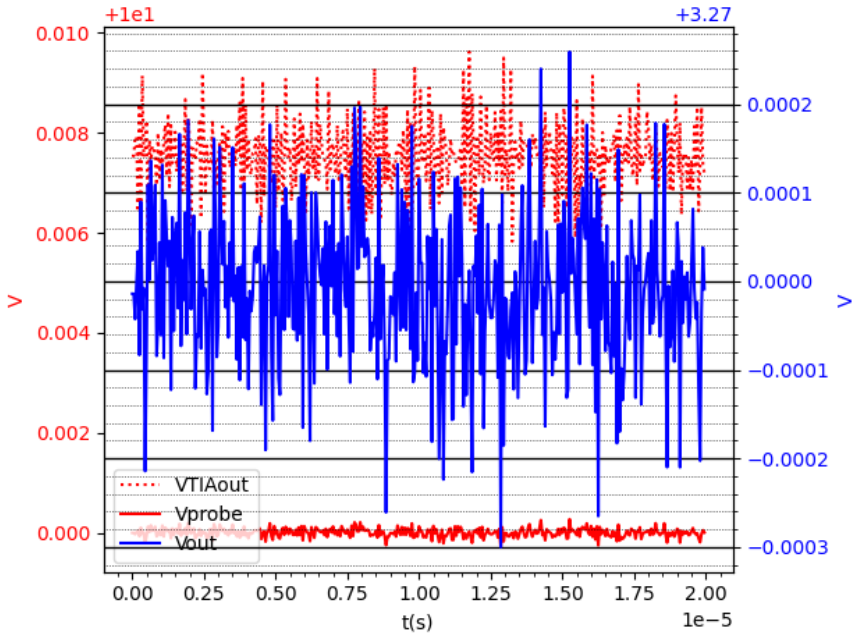


Figure 4.16: FE schematic model transient noise simulation, with a $50nF$ feedback capacitance. $I_p = 15nA$, Gain=4, $R_f = 500k\Omega$.

The system-wide feedback capacitor stabilizes the system for $R_f = 500k\Omega, 3.9M\Omega$, combined with $G = 4, 16$. However, for higher gain stages, the output noise from the TIA results in high-frequency oscillations on the output of the LSA. Details on how this is resolved are described in Chapter 7.

Chapter 5

Testing

This section describes the methods used to test the ASIC.

5.1 Test Setup

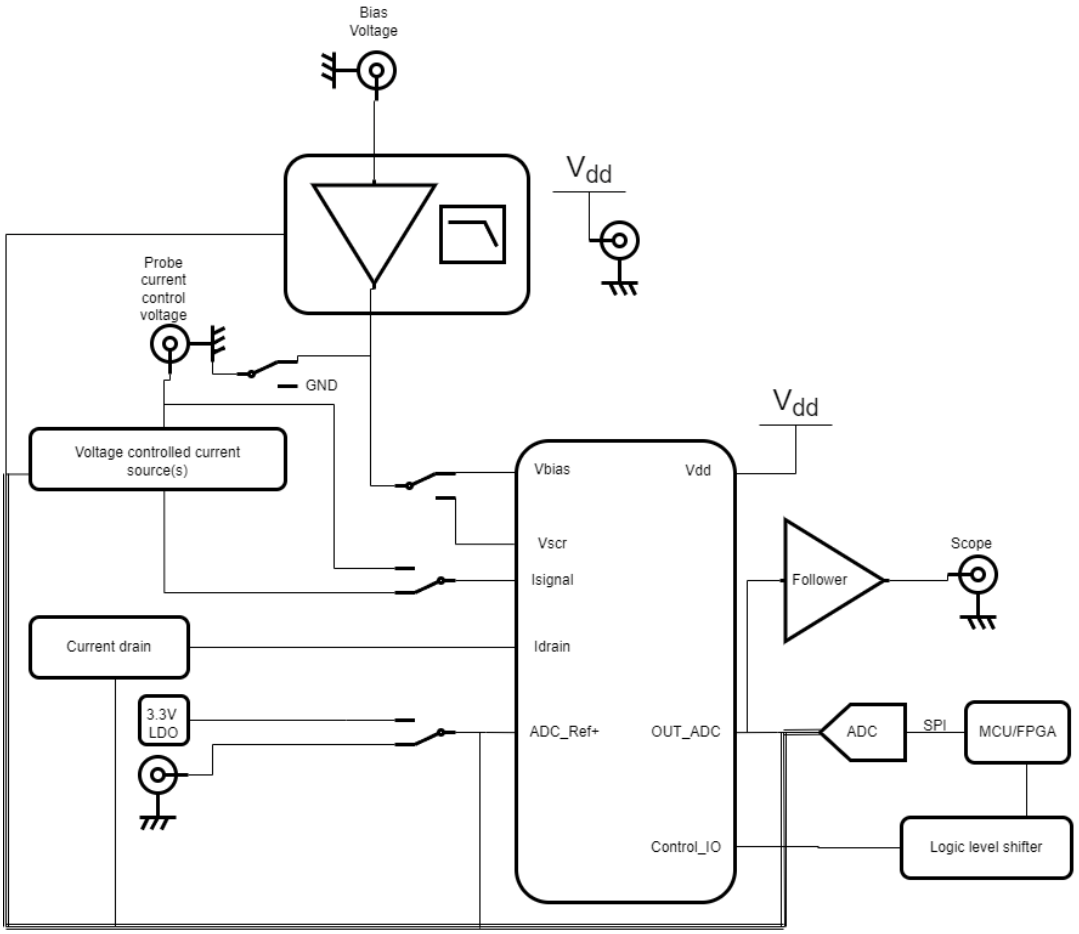


Figure 5.1: Functional block diagram of the test PCB.

The original test PCB was made up of separate functional blocks serving the ASIC IO. They consist of a LPF for the bias voltage, voltage controlled current source for the plasma current, ASIC ADC reference voltage, current drain, logic level shifter, ADC, and follower from the output to external scope. Analog IO and supply conducted by COAX BNC connectors to mitigate induced noise. Selector switches and strapping points provide flexibility for changing the test setup.
The test PCB was made with the intention of being able to characterize the FE with inputs down to the system noise floor. However, as the transient noise simulations revealed, and later confirmed by initial testing of the ASIC, the design setup was simplified to the use of external instruments connected directly to the ASIC. The goal shifted towards verifying the functionality using the lower feedback values. The feedback capacitor seen below is $100nF$,increased from the $50nF$ used in simulations, based on measurements.

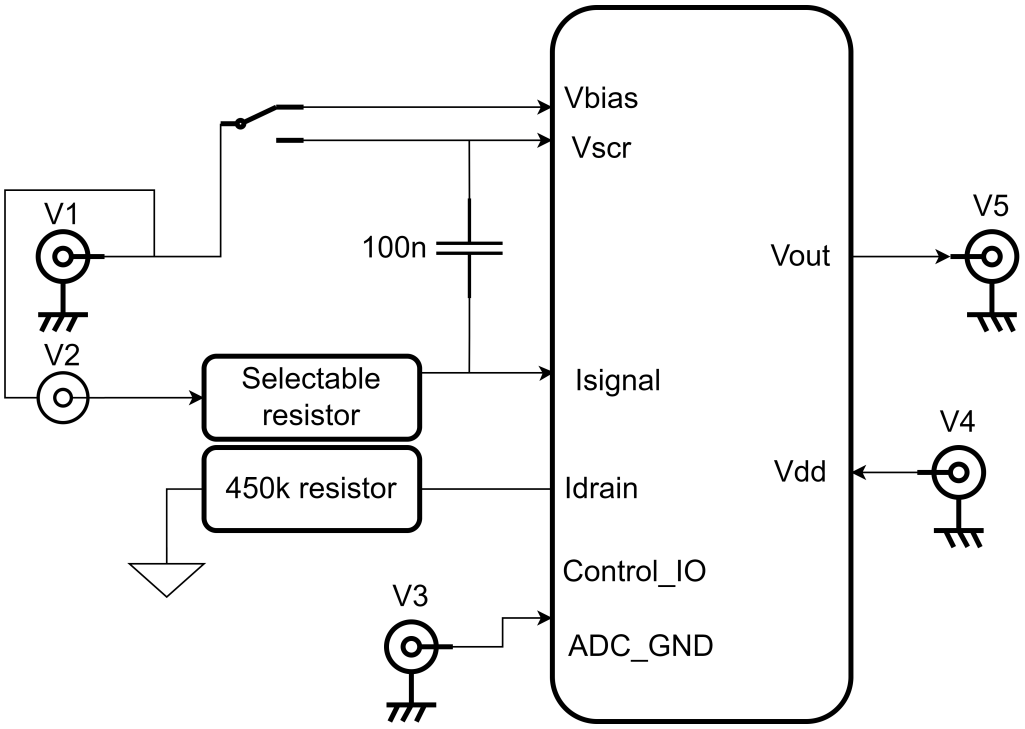


Figure 5.2: Simplified test-setup.

Table 5.1: Instrument overview

Node	Instrument
V1	HP E3614A
V2	HP E3631A
V3	HP E3614A
V4	PL330DP
V5	Pico Technology 2205MSO

5.2 Test PCB

To supply power, execute inputs, and read outputs from the ASIC package a test PCB was made. For a complete schematic, refer to Appendix B

To decouple the AC currents drawn by the ICs from the power rails, ceramic SMD capacitors are used. Given the high DC level across the decoupling capacitors, the dielectric class has a significant effect on actual capacitance. For this design, $NP0$ capacitors are used where applicable. These have little degradation in effective capacitance when increasing the DC level. They do however come in larger packages with increased inductance and series resistance. Since this circuit will operate at low frequencies, this should not affect the performance.

The bias voltage source can either drive the screen (TIA input) directly or simulate an internal reference driven by the follower in the ASIC. This can be selected through a switch to either V_{SCR} (directly) or V_{bias} (through the follower).

To simulate the plasma current, a voltage source and a resistor is used.

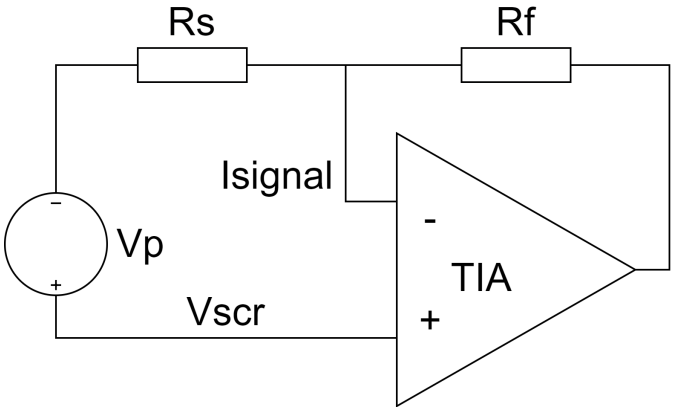


Figure 5.3: Current sink setup with a voltage source and current limiting resistor.

R_s can be selected between $1M\Omega, 10M\Omega, 20M\Omega$ and $51M\Omega$. As a practical limit, the largest resistor used on the test board is $51M\Omega$. Executing the target low end of the signal ($150pA$) requires a voltage drop of $7.65mV$. Leakage caused by the PCB itself is also of concern. Because of this, the circuitry related to the current signal has good separation between traces and other circuits. Another cause for concern is the stackup of the 4-layer PCB. Layer 1 and 2, 3 and 4 are placed close together with a thick $\approx 1.4mm$ core between layer 2 and 3. All components and most signal lines are on layer 1 with a ground plane on layer 2 for good ground coupling. However, the area underneath all the circuits concerning the current signal is empty down to layer 4(ground plane):

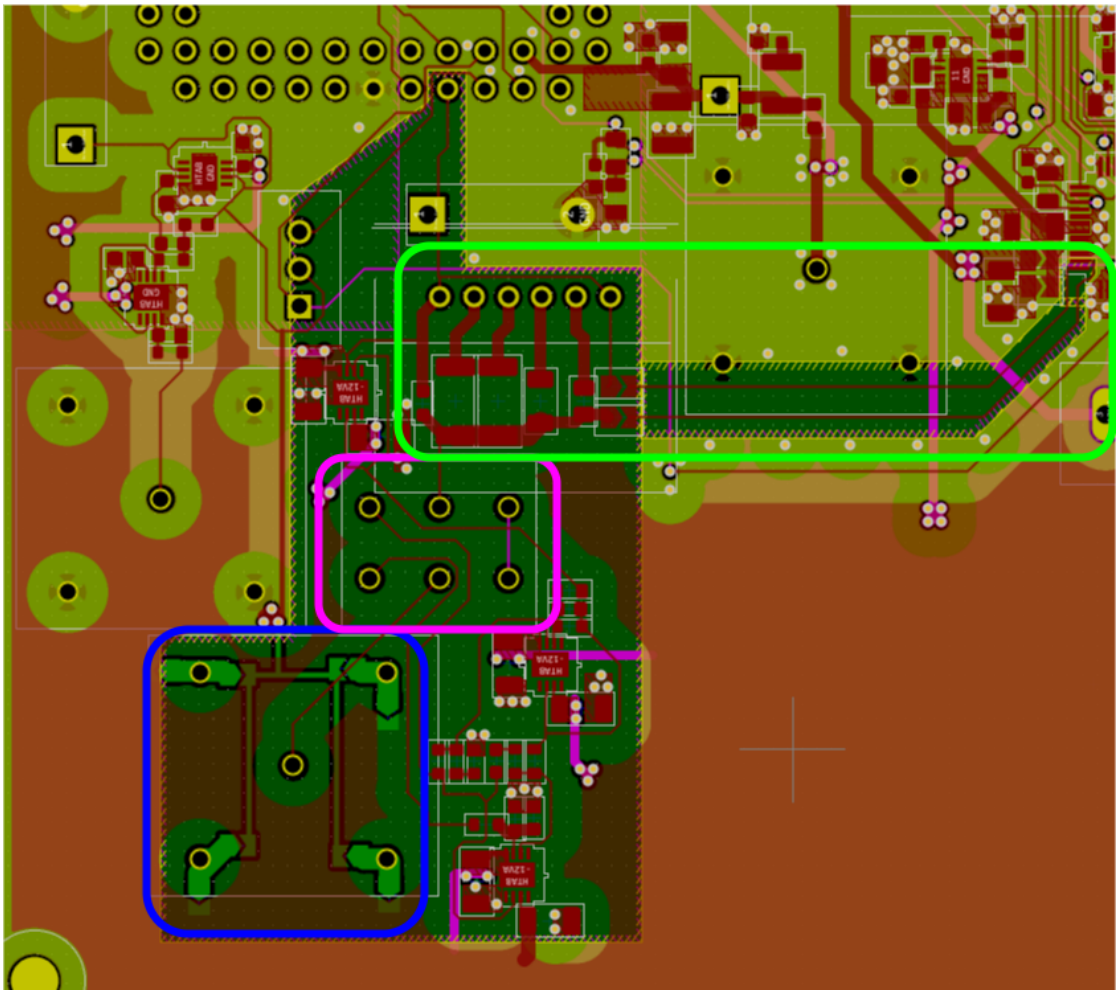


Figure 5.4: PCB layout, area containing the probe signal and bias circuits. Control voltage input (blue), current drive circuit bypass (pink) and current limiting resistors and selector switch (green). Layers: 1 red, 2 yellow, 3 magenta, and 4 green.

To generate the drain current, external resistors are used to connect the PMOS current mirror inside the ASIC to ground.

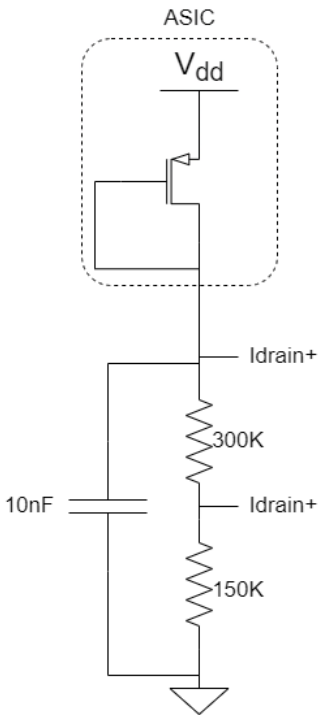


Figure 5.5: Bias current regulation.

The positive reference voltage for the intended internal ADC of the ASIC is connected to an external source through a BNC connector.

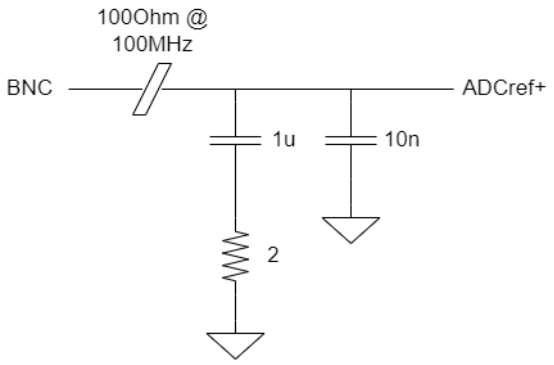


Figure 5.6: Ferrite with dampened capacitor.

To attenuate noise from the external voltage source, a ferrite is used. The parasitic inductance of the ferrite makes a resonant loop with the $10nF$ capacitor. However, this is mitigated with the dampened $1\mu F$ capacitor. A SPICE simulation of the circuit with an equivalent model for the ferrite, ignoring the series resistance of the capacitors yielded a cutoff frequency of $1.75MHz$. The same circuit is used for the V_{dd} supply going into the ASIC.

Chapter 6

Results

Measurements were made on the system as a whole, the follower and the LSA. The Input current to output voltage -mapping is made by changing the voltage drop across R_S step-wise and measuring the output through the oscilloscope using a real RMS. As the follower creates an uncertainty caused by its oscillations, V_{screen} is connected directly to the external voltage source. This means that the output of the follower is in high impedance mode. The points indicate the measurements, and the stapled lines are extrapolations. Comparisons to an ideal response are made where the output is somewhat linear. Feedback values that result in unstable behavior are not included.

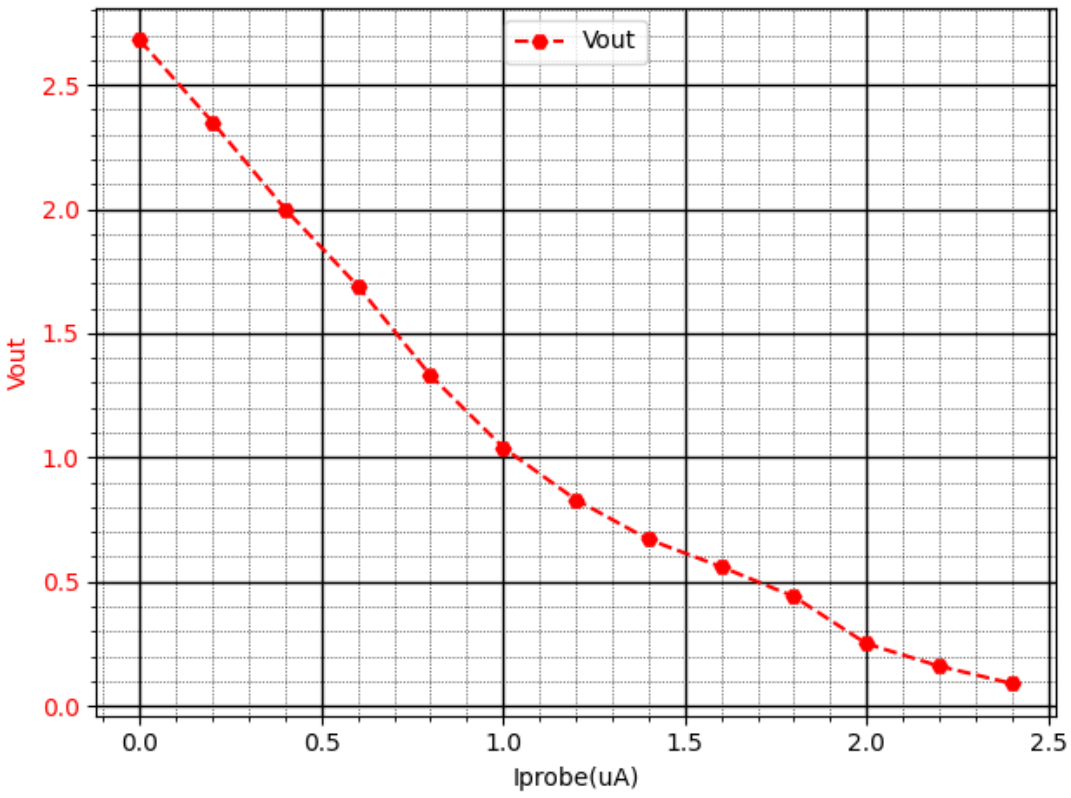


Figure 6.1: $V_{screen} = 2V, ADC_{ref+} = 3.3V, G = 4, R_f = 500k\Omega$. $\Delta V_{out_{0\rightarrow 1uA}} = 1.6V$, ideal= $2V$.

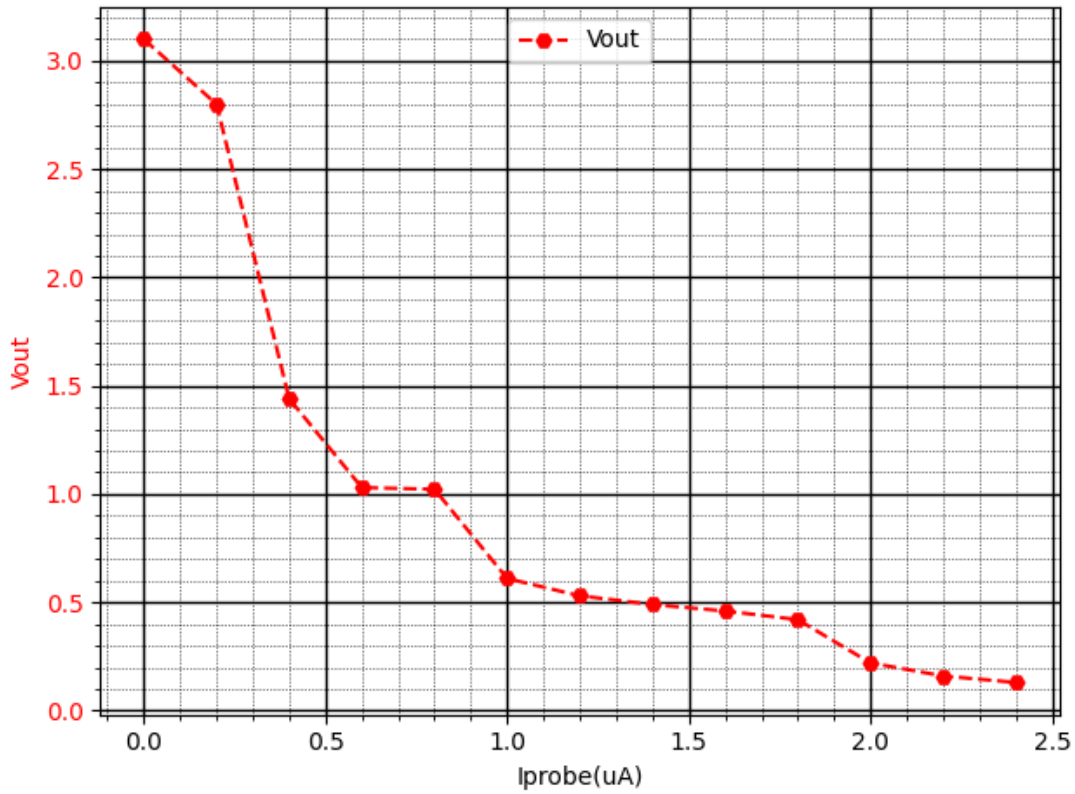


Figure 6.2: $V_{screen} = 2V, ADC_{ref+} = 3.3V, G = 16, R_f = 500k\Omega$. $\Delta V_{out_{0\rightarrow 600nA}} = 2.1V$, ideal= $4.8V$.

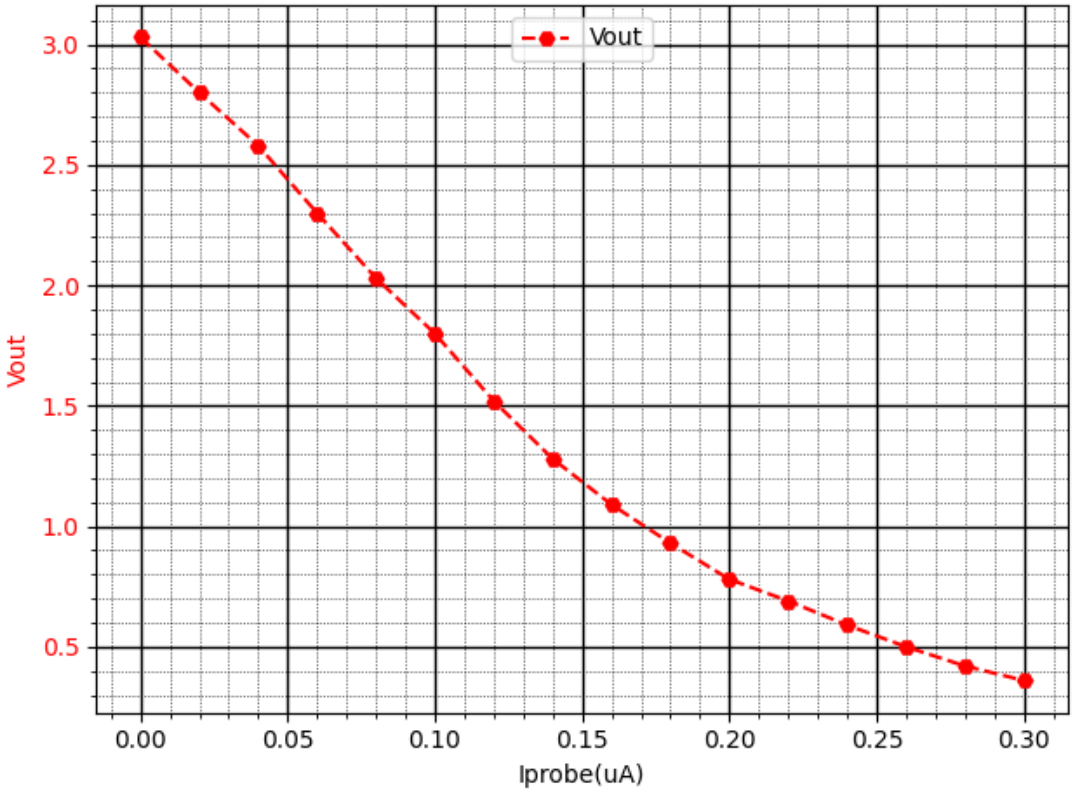


Figure 6.3: $V_{screen} = 2V, ADC_{ref+} = 4V, G = 4, R_f = 3.9M\Omega$. $\Delta V_{out_{0\rightarrow 300nA}} = 2.7V$, ideal= $4.68V$.

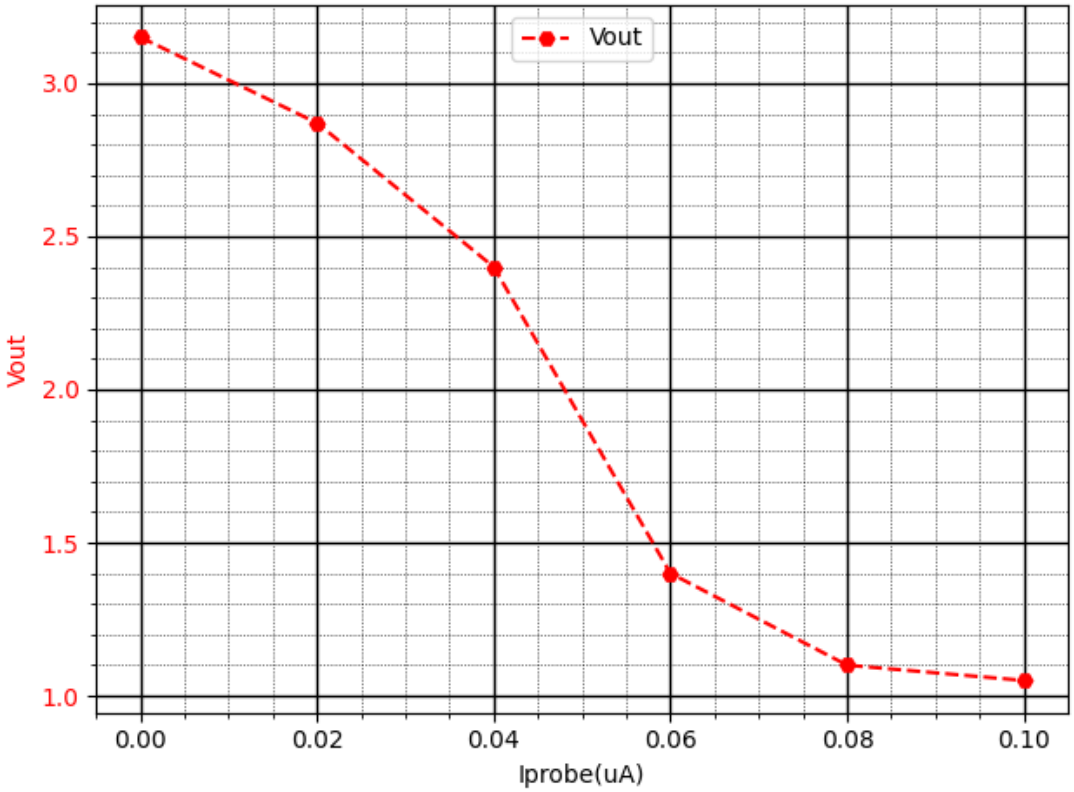


Figure 6.4: $V_{screen} = 2V, ADC_{ref+} = 4V, G = 16, R_f = 3.9M\Omega$.

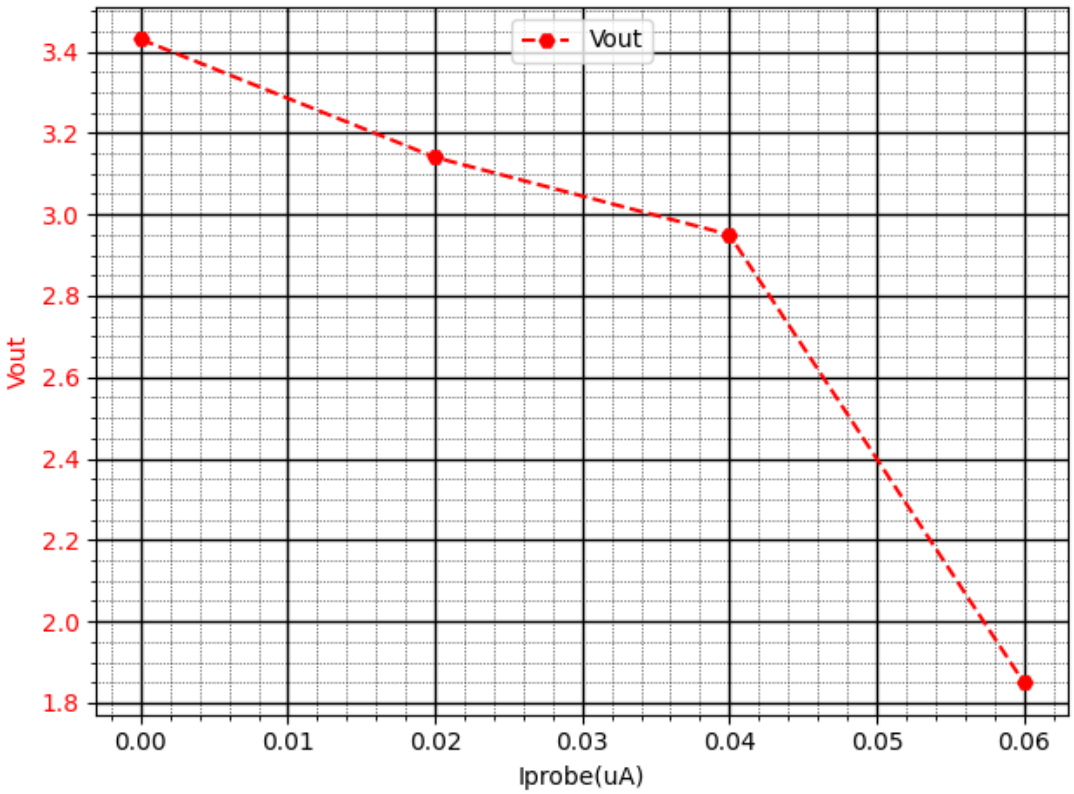


Figure 6.5: $V_{screen} = 2V, ADC_{ref+} = 4V, G = 64, R_f = 3.9M\Omega$.

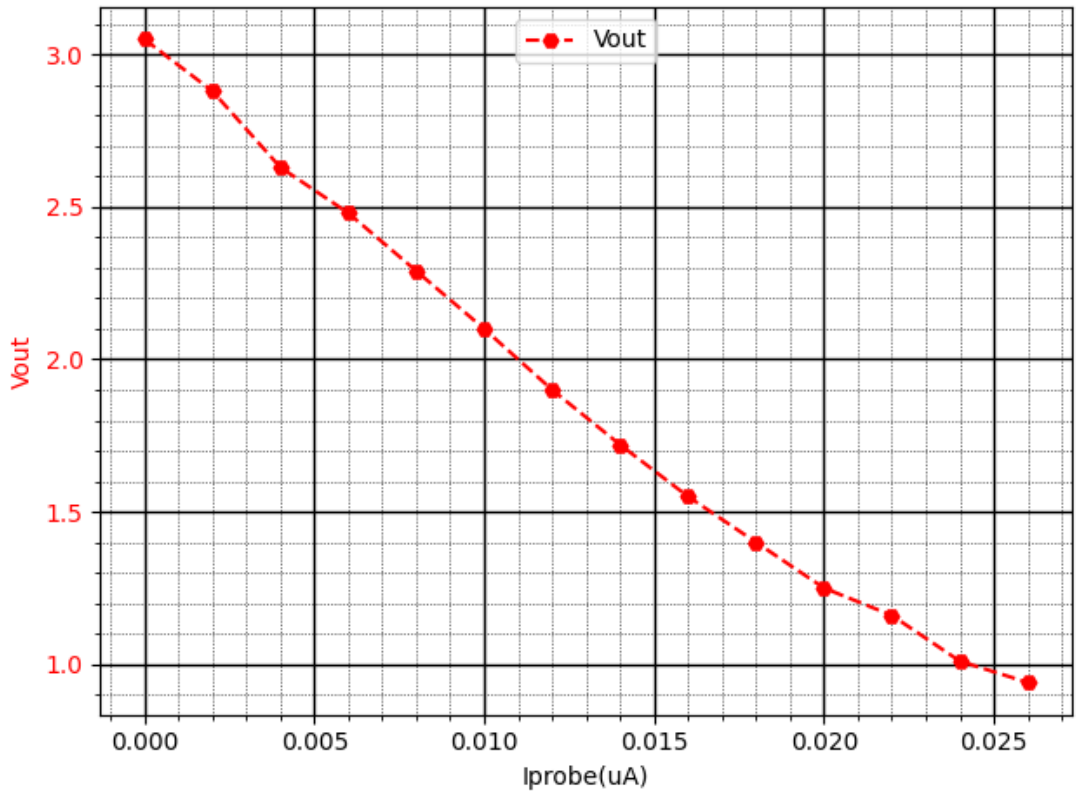


Figure 6.6: $V_{screen} = 2V, ADC_{ref+} = 4V, G = 4, R_f = 31M\Omega$. $\Delta V_{out_{0\rightarrow 26nA}} = 2.1V$, ideal= $3.22V$. .

This result is better than the simulation, in which the output would oscillate between power rails for $R_f = 31M\Omega$

To test the follower, the instrument was switched to the V_{bias} input. Measurements are made of both the input and output of the follower.

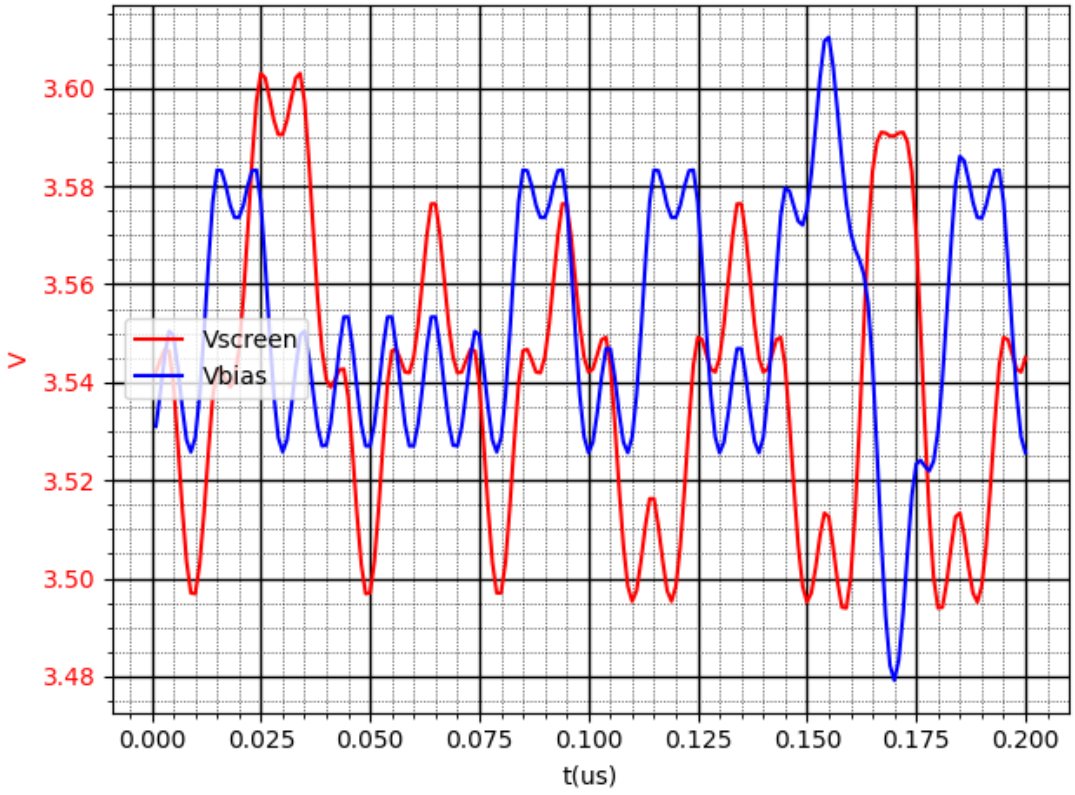


Figure 6.7: V_{bias} is the input of the follower, V_{screen} is the output. Test of upper end of bias range.

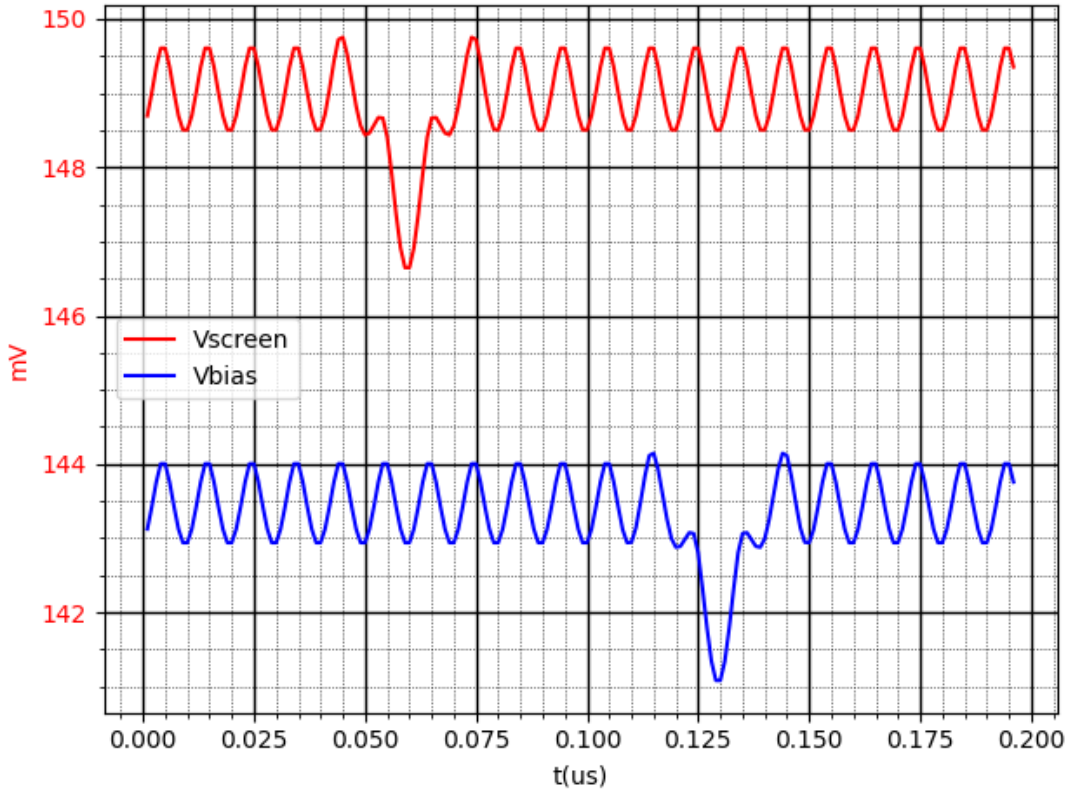


Figure 6.8: V_{bias} is the input of the follower, V_{screen} is the output. Test of the lower end of the follower output range.

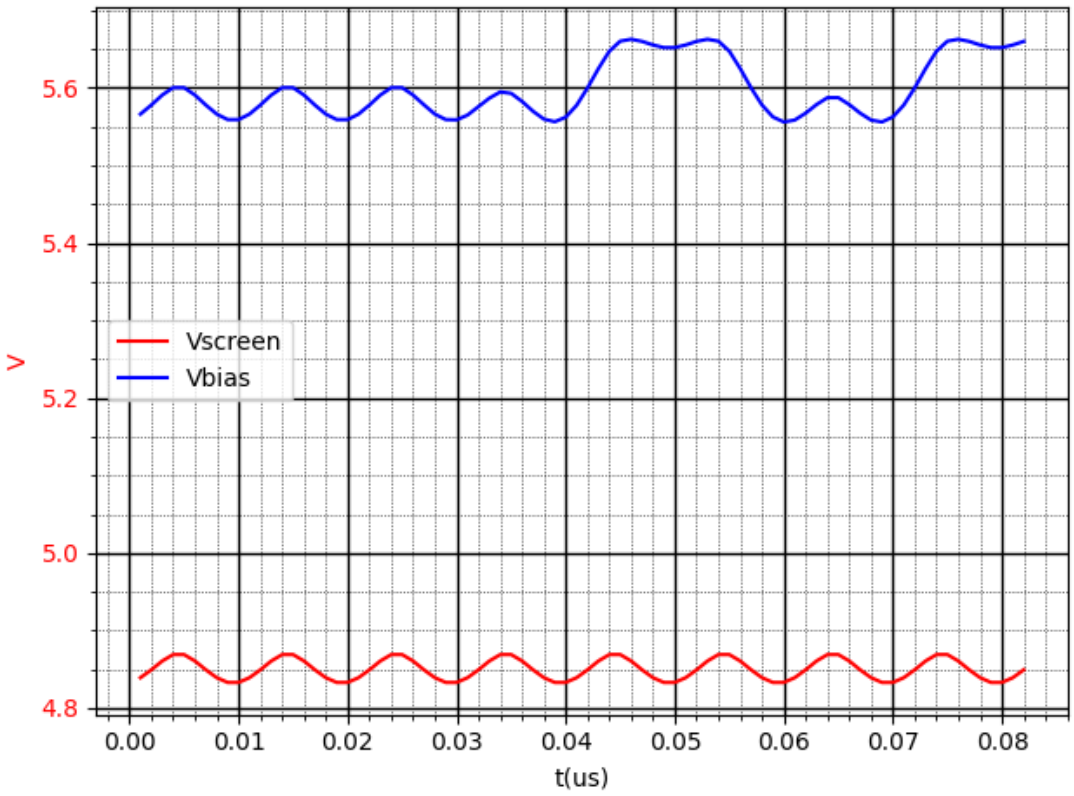


Figure 6.9: V_{bias} is the input of the follower, V_{screen} is the output. Test of the upper end of the follower output range.

Given the large deviation from an ideal response to ΔI_p, the LSA was tested by disabling the feedback resistor. This changes the LSA to a follower and simultaneously tests the ability of the TG to switch.

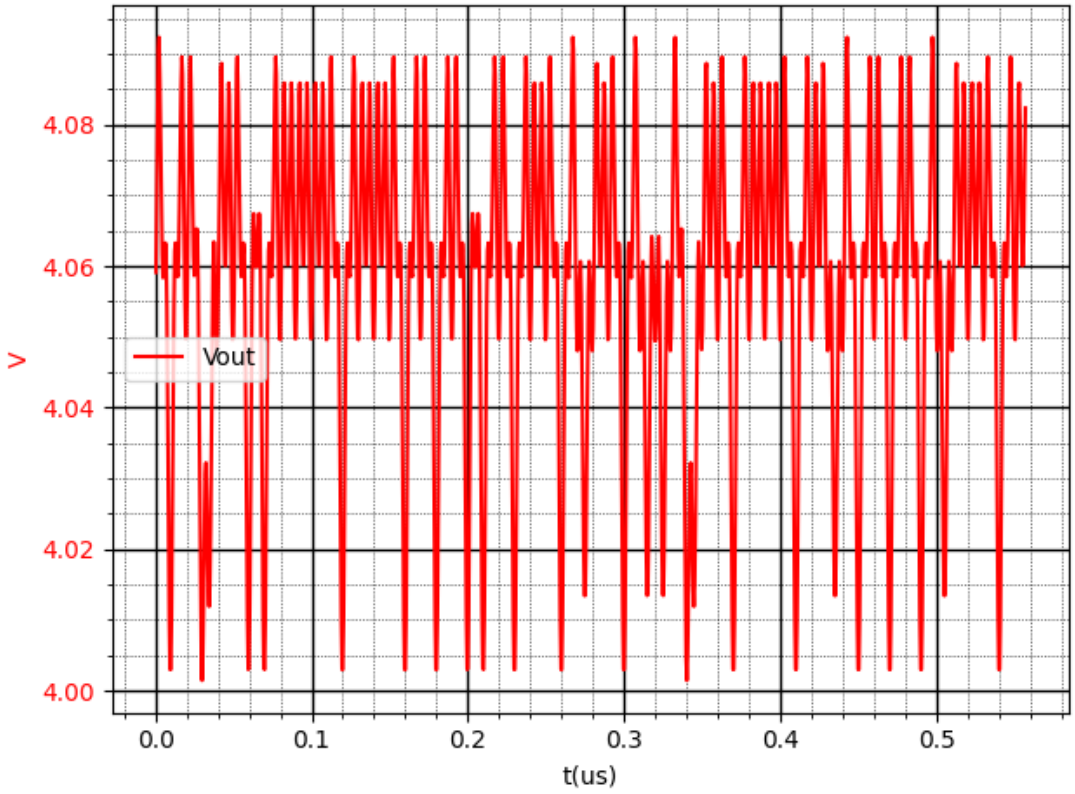


Figure 6.10: All TIA connected to the LSA in the open state, LSA is a follower for $ADC_{ref+} = 4V$.

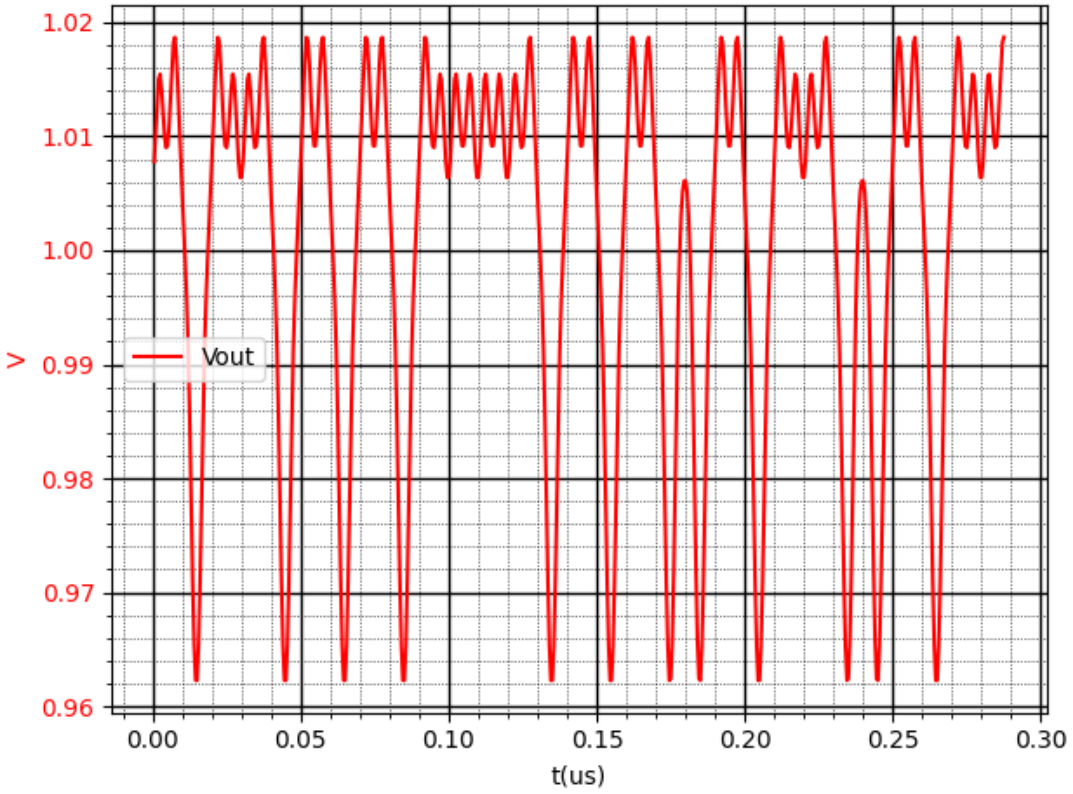


Figure 6.11: All TIA connected to the LSA in the open state, LSA is a follower for $ADC_{ref+} = 1V$.

Chapter 7

Design Improvements

This section describes a revised version of the FE presented. The design consists of a schematic using the same CMOS process, with alterations to keep $V_{GS}, V_{GB} < 6.05V$(nominal +10%), $V_{BS} < 5.5V$, with $V_{dd} = 12V$. Changes are also made to the stability of the opamp, and the circuit as a whole to enable the functionality of all gain stages.

7.1 Resistor matching

The absolute value of an integrated resistor can vary by as much as 25% [7, p. 77]. The mismatch between resistors can be much more accurate. In the design used in the ASIC, the resistors are embedded in separate wells/guard rings. The resistors to be matched should be interleaved and placed in the same structure. This will not only improve matching but also area consumption and better rejection of common mode noise given the closer proximity of differential signals.

7.2 Transmission gate V_{GS}

To make the transistors in the TG operate within safe voltages, the voltage span of V_{GS}/V_{GB} needs to be lowered by altering the control voltages. Using the fact that the TG is not exposed to the full supply range on either node in operation, the control voltages can be changed according to the operating region. The TG used for the TIA will be exposed to $2 - 10V$ according to the screen bias. Assuming a full range for the TG of $2 \rightarrow 12V$, the lower voltage limit for the upper range is: $V_{GS_N} = 6.5V$. Using two TG voltage spans ($2 \rightarrow 7V$ and $7 \rightarrow 12V$), the control voltages can thus be at a safe level. The inputs are split between controlling the PMOS(EN_PMOS) and NMOS(EN_NMOS):

Table 7.1: TG logic levels

Voltage span	EN_NMOS 'ON'	EN_NMOS 'OFF'	EN_PMOS 'ON'	EN_PMOS 'OFF'
$2 \rightarrow 7V$	$7.5V$	$2V$	$2V$	$7.5V$
$7 \rightarrow 12V$	$12V$	$6.5V$	$6.5V$	$12V$

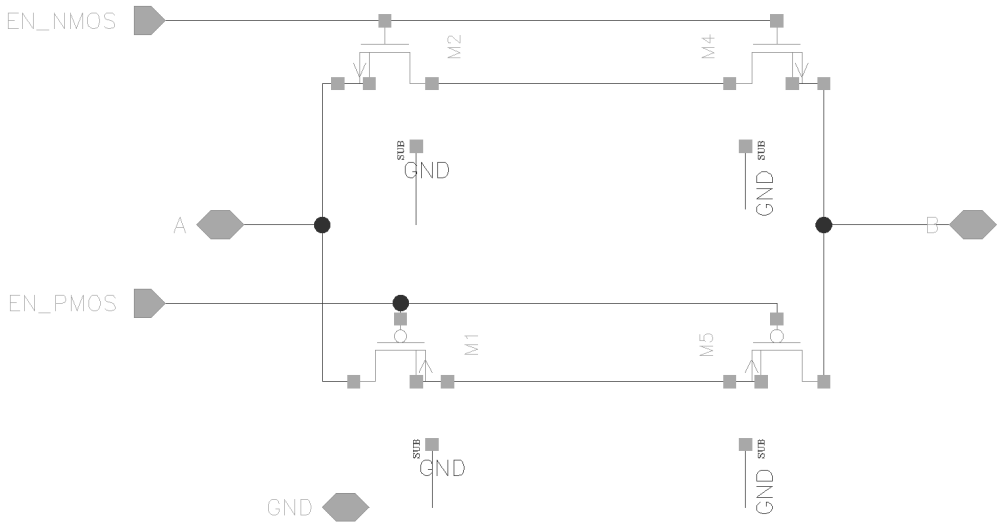


Figure 7.1: TG with split control signals.

7.3 Opamp

Starting with the opamp and using the open loop CM input simulation, simulating $0V - 12V$ with the output enabled and disabled will reveal any crossing of operational limits. The calculations assume ideal voltage rails up until the transistor contacts.

7.3.1 Differential input

Since the base is connected to V_{dd}, having either input lower than $5.95V$ goes beyond the V_{GB} maximum. The bulk potential causes issues with source as well, as the common source of the input tracks the CM level. When $CM = 0V$ then source reaches: $V_{Sdiff} = 3.26$, causing $V_{BS} = 8.74V$. Connecting bulk to source will solve these issues. Since all opamps are connected with feedback, the differential voltage will remain small. However, to completely test for any unsafe voltages, the inputs are also simulated with the same $0V - 12V$ ramp on either input and the other connected to ground. Here $V_B = V_S = 1.6V$ while one of the inputs reaches $12V$. This revealed the maximum differential voltage of $7.65V$.

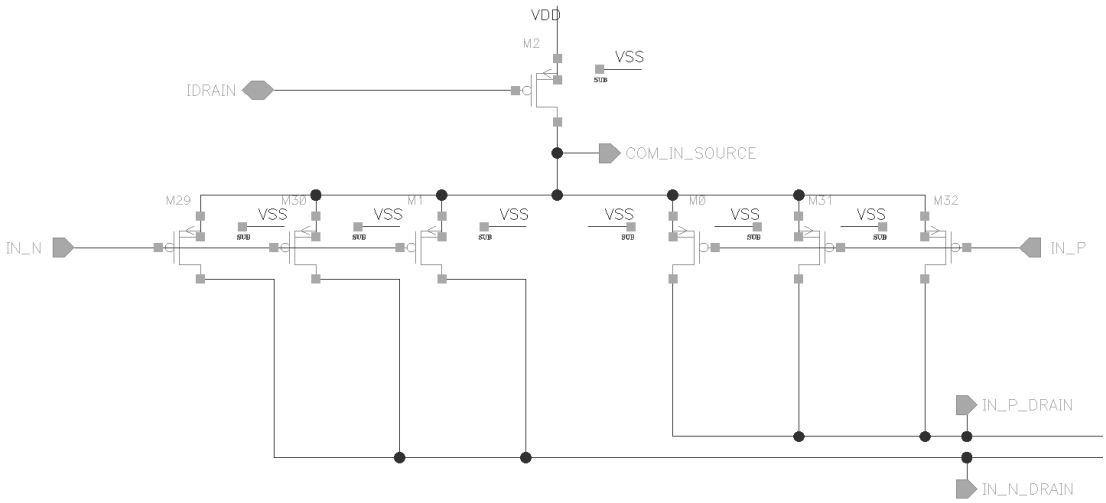


Figure 7.2: Differential input. Changes: bulk connected to source instead of V_{dd}

The only situation where the maximum differential voltage can be exceeded is when the source follower is disconnected and the screen is biased from an external source. This is only a problem if the ASIC screen bias is kept at an unsafe level with regard to the external source. The simplest solution is to set ASIC screen bias to 6V before disabling the output of the follower.

7.3.2 Folded cascode, bias and source follower

The folded cascode, biasing and source follower circuits all operated within safe limits. This is because of all the transistors having their source connected to bulk and any high voltage drops occurs across source to drain. All gates should have a voltage level beyond saturation, however well below $V_{GS} = 6.05V$.

7.3.3 Tri-state switch

The PMOS switch (M21) following the PMOS source follower has an issue with incorrectly connected source and drain. With $EN = 0V$, the gate of M21 is $12V$. In this configuration, the lowest potential is at the source/bulk contact causing M21 to conduct. This results in that M24 of the AB power stage recieving signal from the source follower. Turning output on ($EN = 12V$), causes the gate of M21 to be $0V$. The source follower outputs $12V$ and results in $V_{GS21} = V_{GB21} > 6.05V$. Switching the drain and bulk/source connections of M21 makes the circuit operate properly. However, EN still causes $V_{gs/gb} > 6.05V$ when $EN = 0V$.

The issue with a voltage difference between source/drain and gate affects all transistors in the tri-state switch, as the control signals are either $12V$ or $0V$. To resolve this, two new control signal ranges are needed. $0V$ and $5.5V$ for $M22$ and $M23$ (EN5.5), $6.5V$ and $12V$ for (EN12).

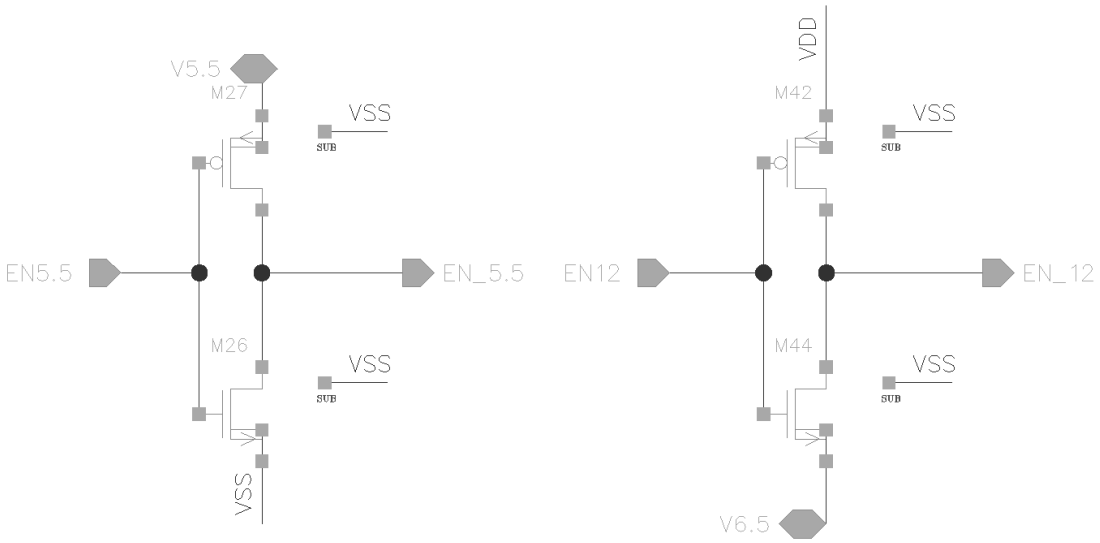


Figure 7.3: Inverters for the new control signal ranges. Changes made is the addition of an inverter (M47 and M44) and new voltage levels for both inverters.

Voltage levels from the source followers can reach any level as they go into the drains of M21 and M22.

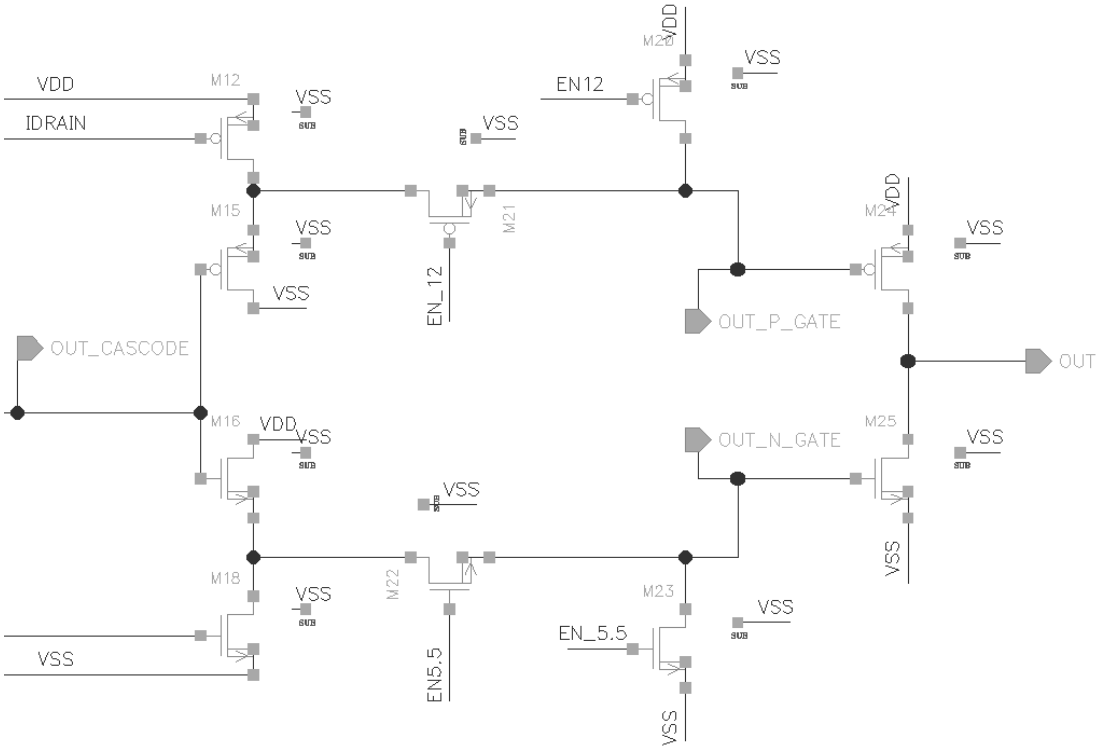


Figure 7.4: Overview of tri-state switch and AB power stage. Changes made: switched source/dran of M21, new control signal voltage levels.

Testing av full CM range input and open circuit resulted in no overvoltage at any nodes. Connecting the opamp as a follower, $V_{inp} = 6V$, $EN5.5 = 0v$, $EN12 = 6.5V$ and

sweeping a voltage source on the output node $0V \Rightarrow 12V$ worked properly and without any overvoltage problems.

7.3.4 Compensation capacitor

The changes thus far made no impact on the gain and PM. To achieve 60° a $1.2pF$ compensation capacitor is placed between the output of the final stage (CS) and the output of the first gain stage (folded cascode).

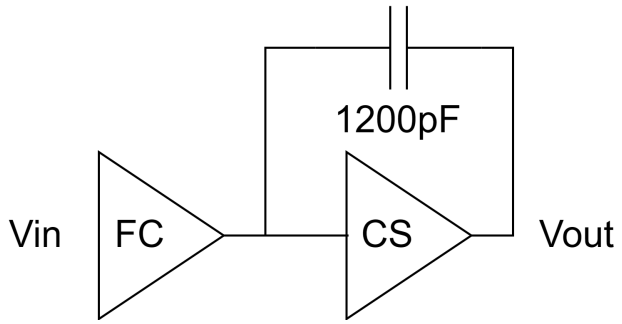


Figure 7.5: Compensation capacitor functional diagram.

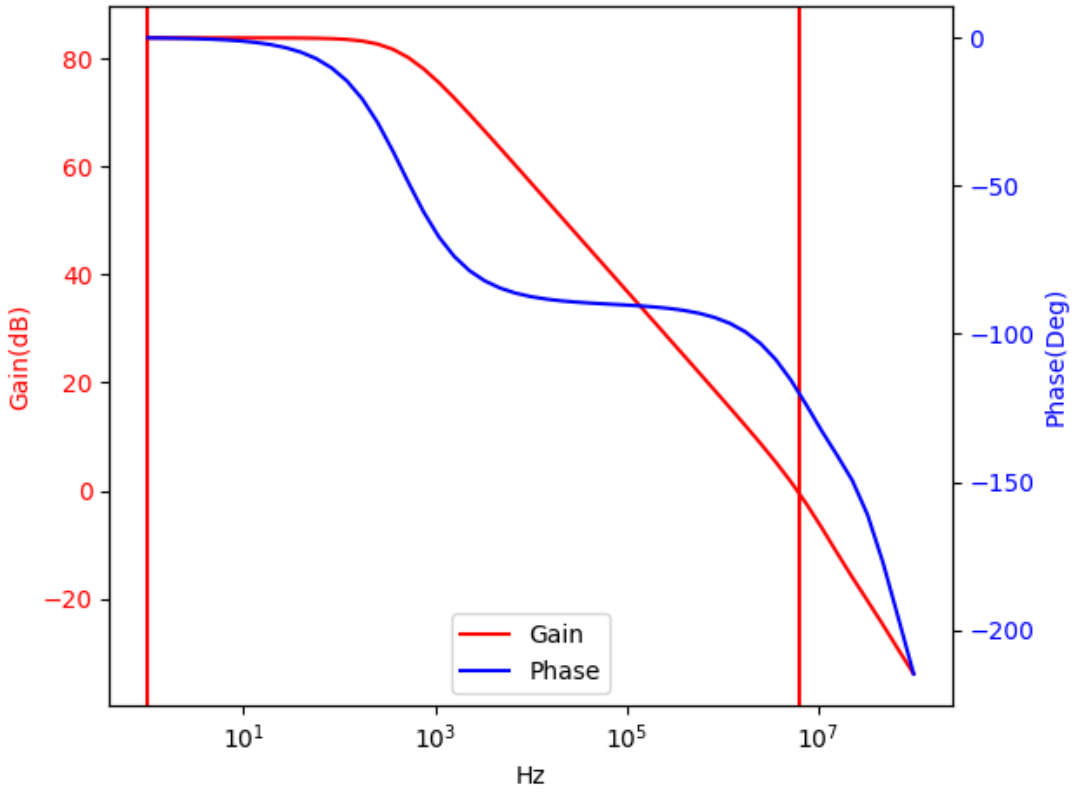


Figure 7.6: The phase margin is increased to 60°, while GBW is reduced to $6.24Hz$.

7.3.5 Output stage

When simulating the design and measuring the current draw, the CS-stage was the node that consumed the most. The peak of several mA occurs when $V_{out} = V_{dd}/2$, when

the conductivity is equal between the PMOS and NMOS. One concern is the energy consumption, while this was not a part of the specification for this work. Another is the lack of short-circuit protection. This became evident when measurements were made on one ASIC and the output of the follower was active, while an external source was connected. This resulted in the follower not functioning, likely due to a short-circuit. A new design should have some current limiting circuitry.

7.4 Feedback capacitor

Testing the transient noise response of the FE with stable opamps works as expected for lower gain values of the LSA. Higher gain values resulted in oscillations between ADC_{ref+} and $\approx 1V$. Placing a feedback capacitor ($300fF$) on the TIA and LSA, the FE is stable for all feedback values.

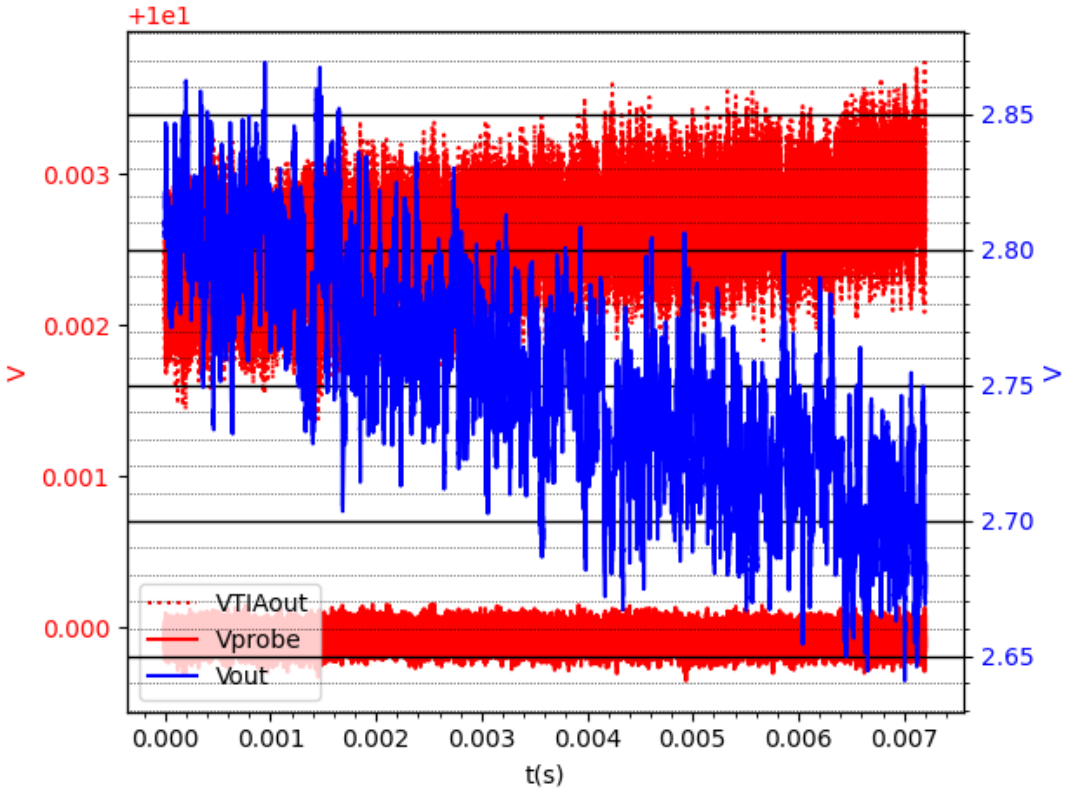


Figure 7.7: Transient noise simulation of PEX model of the FE. $V_{screen} = 10V, ADC_{ref+} = 3.3V, G = 256, R_f = 31M\Omega, I_p = 0 \rightarrow 17pA$.

Testing switching between R_f values for the TIA results in stable behavior. The output is table $\approx 3ms$ after switching to the final feedback value.

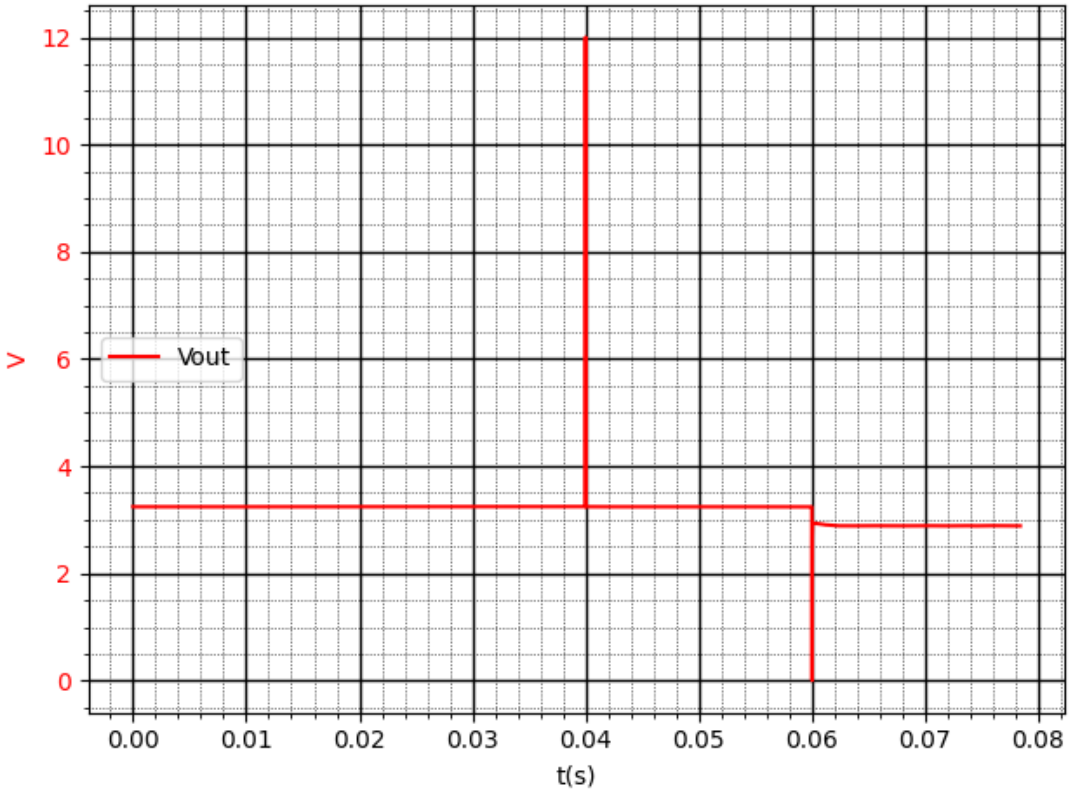


Figure 7.8: Transient simulation of PEX model of the FE. TIA feedback is $R_f = 3.9M\Omega @ t = 0$, $R_f = 3.9M\Omega \| 31M\Omega @ t = 40m$, and $R_f = 31M\Omega @ t = 60m$.

7.5 Reduced feedback noise TIA

The Johnson-Nyquist noise of the feedback resistor acts as an intrinsic noise floor of the TIA. However, there is a way to overcome this by exploiting voltage division from a higher voltage source[3]:

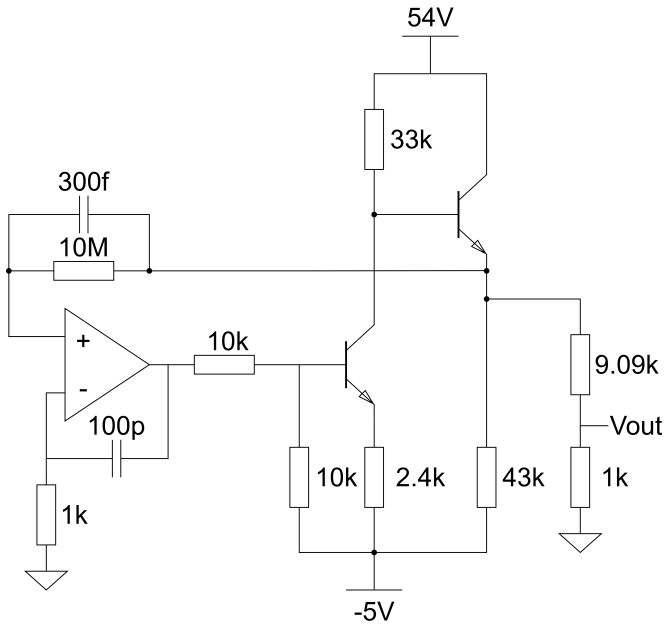


Figure 7.9: TIA with lower output noise density than that of the feedback.

The $10M\Omega$ feedback has a noise density of $400nV/\sqrt{Hz}$ at $20°C$. However, the $50V$ output swing at the emitter (emitter-base voltage= $4V$) is reduced to a voltage swing of $5V$. This reduction of a factor 10, also reduces the voltage noise density to $40nV/\sqrt{Hz}$ and the effective feedback to $1M\Omega$. A $1M\Omega$ feedback would have resulted in a $130nV/\sqrt{Hz}$ minimum at the output.

While the FE uses quite large feedback values, and this circuit operates by reducing its effective voltage translation, the reduced noise also means that the TIA output can be that much more amplified by a later stage without reducing the SNR.

Chapter 8

Discussion and Conclusions

In this chapter, the measurements and simulation results are compared and related to the design. Finally, a conclusion is made for the process and a note on further work.

8.1 Measurement versus simulation results

Depending on the simulation method used, the contrast between simulation and measured results varies greatly. The DC simulations of the FE were close to an ideal response and deviates greatly from the measured results. This is likely caused by the lack of phase margin in the opamp, resulting in oscillations from the internal and external noise sources. The similarities between simulated versus actual are apparent when simulating with transient noise sources included. The FE 'as is' oscillates for all gain stages. However, the FE feedback capacitor added to the schematic results in an oscillation-free output in simulation for the lower gain stages, while the measured output had a $50mV$ standard deviation for each RMS measurement at best.
Given that the external environment most likely has a considerable effect on the results, the similarity between simulations and measurements lends some credence to the dependability of the design with regard to process variations.

The simulations results after the compensation capacitor for the opamp, and feedback capacitor for the TIA and LSA were implemented, the PEX noise transient simulations resulted in an output response above the noise floor $I_p = 0 \rightarrow 17pA$ (Figure 7.7). Assuming that the output is passed through a LPF before reaching the input of an ADC with 14 ENOB, the signal would probably be discernible at $10pA$.

8.2 Process

The TSMC 180nm BCD (Bipolar-CMOS-DMOS) Gen2 HV CMOS process is demonstrated, through simulation to be able to handle signal levels required. A Major drawback is the requirement of having the same potential on all gates, sources, and drains sharing the same isolation structure/ deep N-well, as this makes the proximity of matched devices difficult. This coupled with the lack of model data to perform process and missmatch simulation with Monte Carlo, creates a great deal of uncertainty. The layout also consumes a relatively large die area.

The process offers a wide selection of devices and the ones used for the FE do not necessarily represent the possible performances of this design. The availability of higher

voltage devices is an exciting option, for example for an implementation of the circuit in Section 7.5.
Another point of interest is the low-voltage devices to implement the ADC and digital circuits of a complete m-NIC. Though they have not been investigated for this work.

8.3 Further work

Unfortunatly, the TSMC BCD Gen2 process is not a part of Europractice any longer. This removes the chance of any direct. However, another high-voltage BCD process from TSMC is available: 0.13µm CMOS High Voltage, Low Power, BCD Pluss[6]. There are no current plans to use this process.

There is work being done on the ADC for the m-NIC. Another implementation of the FE, filters and readout logic is then needed for a complete system. The X-FAB XH018 is likely to be used in the future, as there are no separate limitations on the maximum V_{gs}, making the design process simpler. There is a library for radiation hardened logic cells for this process, making applications for long term usage in satellites more viable.

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Appendix A

Layout figures

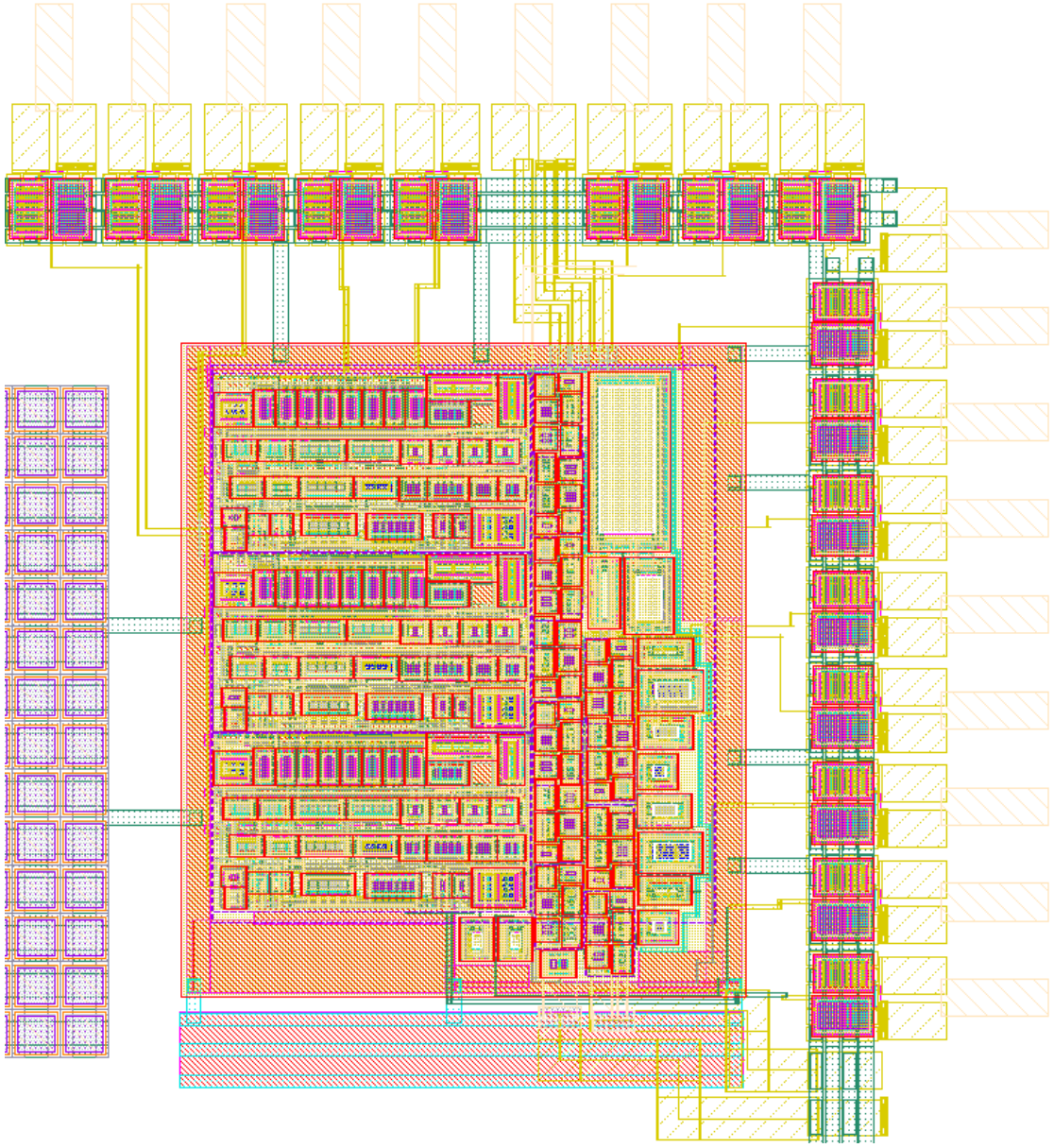


Figure A.1: Complete FE layout with the pad-frame visible.

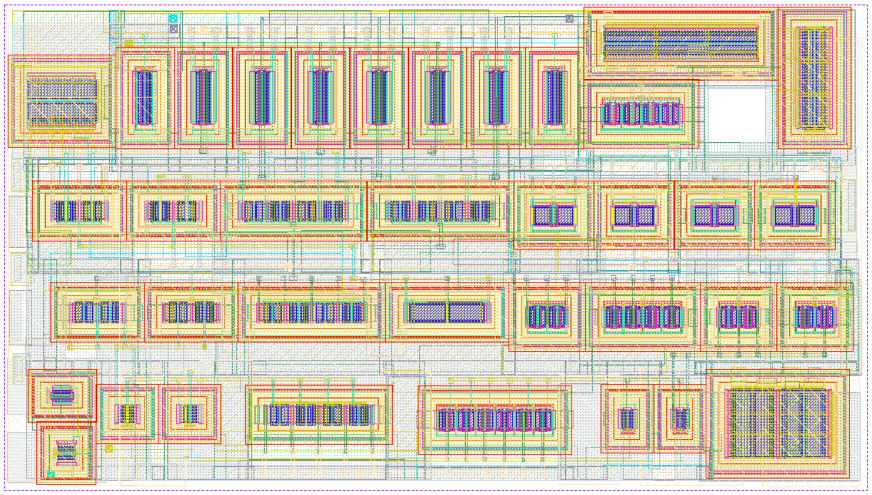


Figure A.2: Opamp layout, $W = 265\mu m, H = 148\mu m$.

Appendix B

Test setup

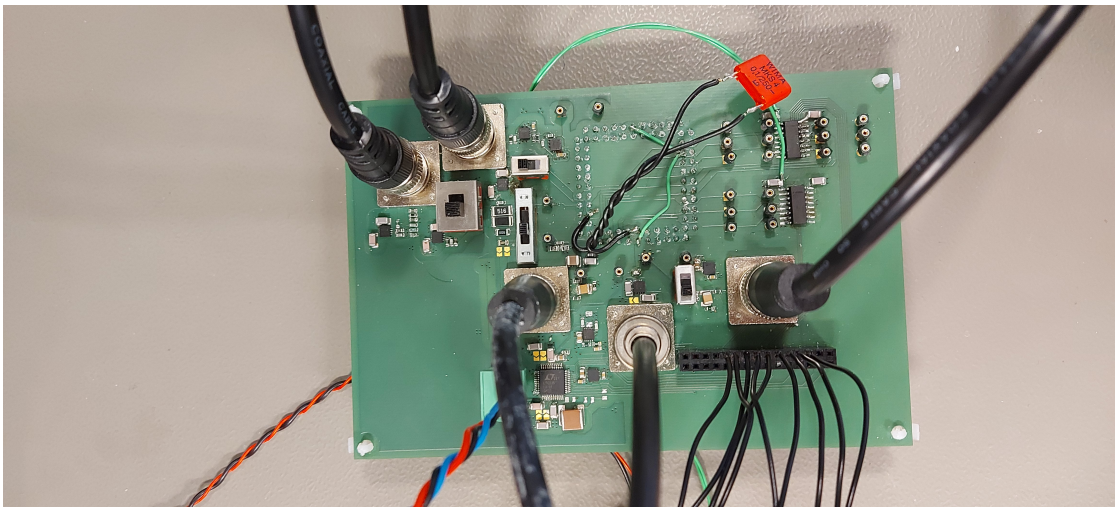


Figure B.1: Test PCB with all connections for testing.

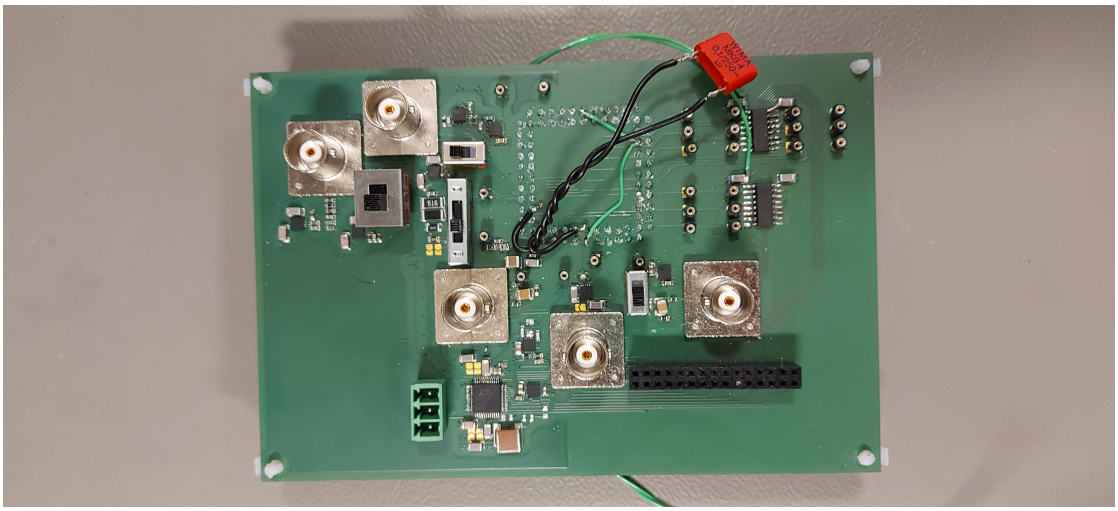


Figure B.2: Test PCB top view.

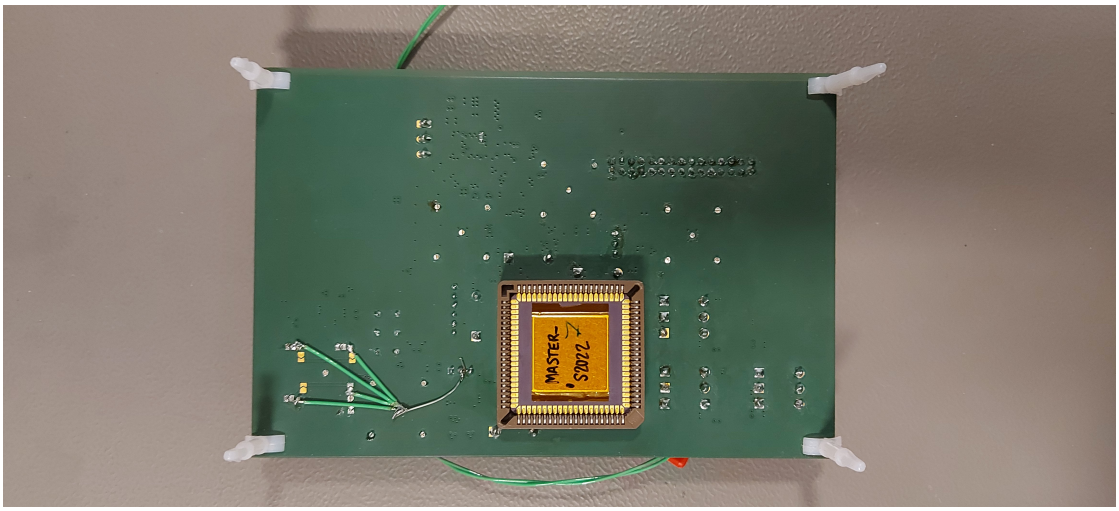
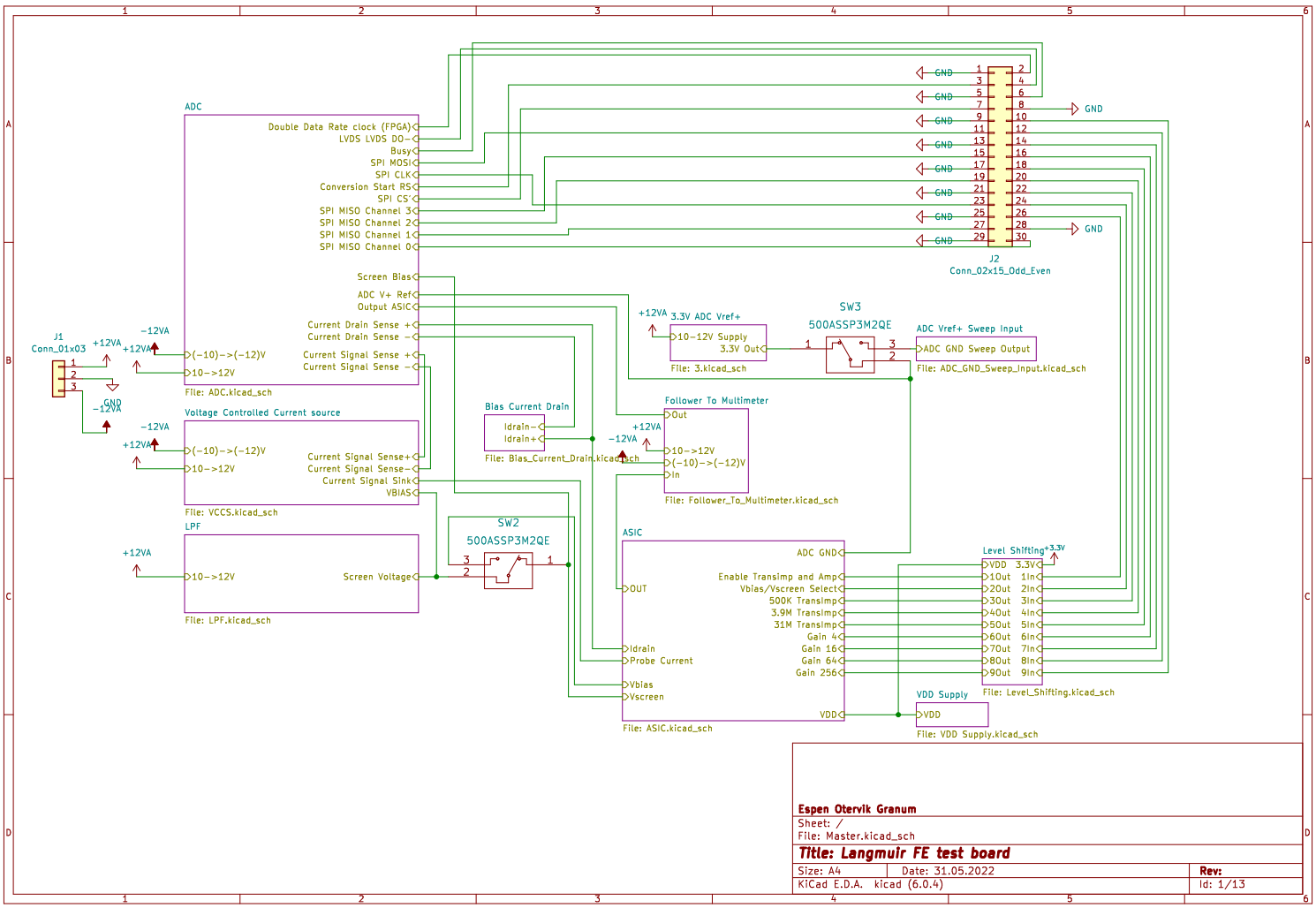


Figure B.3: Test PCB bottom view, with ASIC inserted.

Appendix C

Test PCB Schematic



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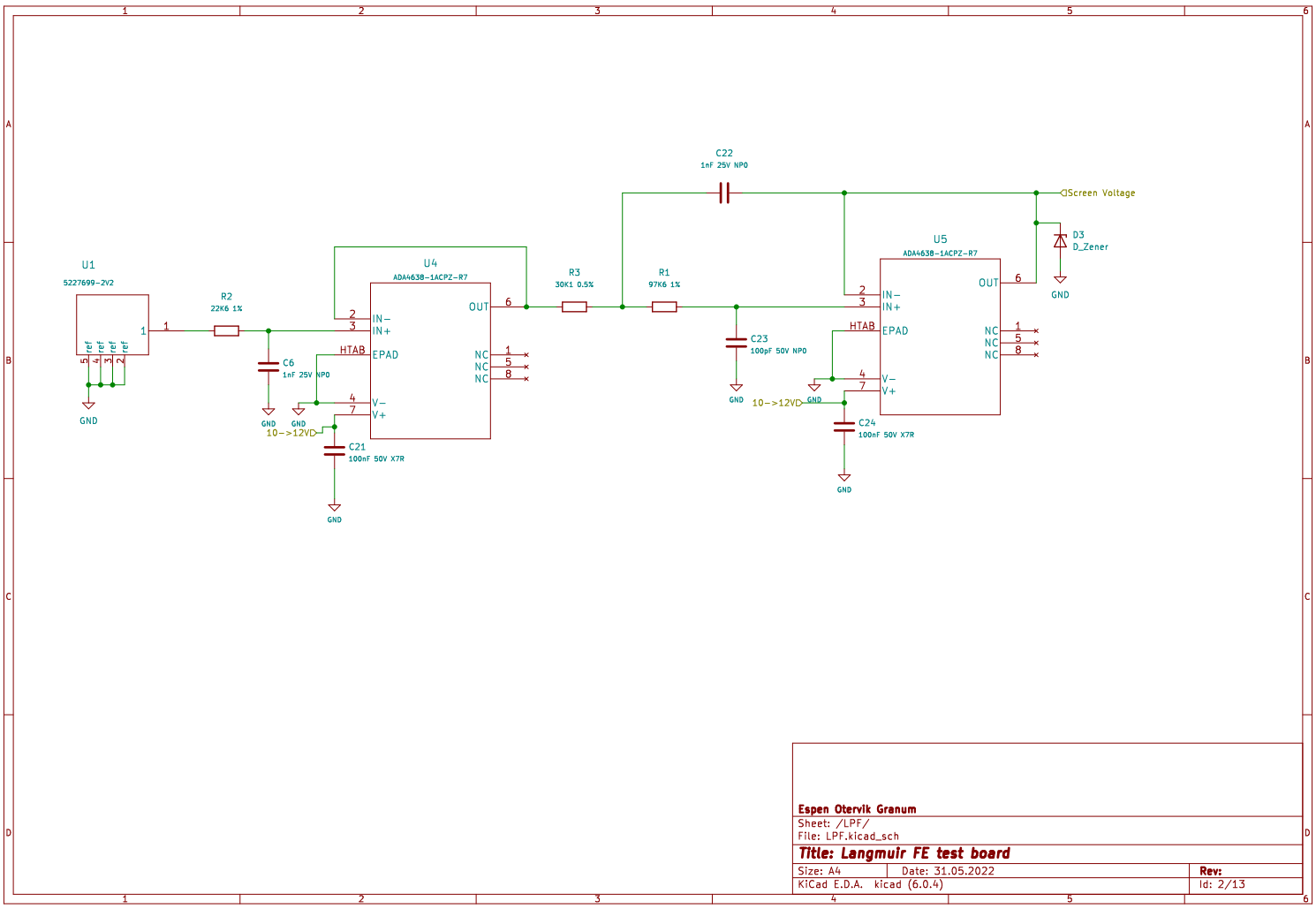
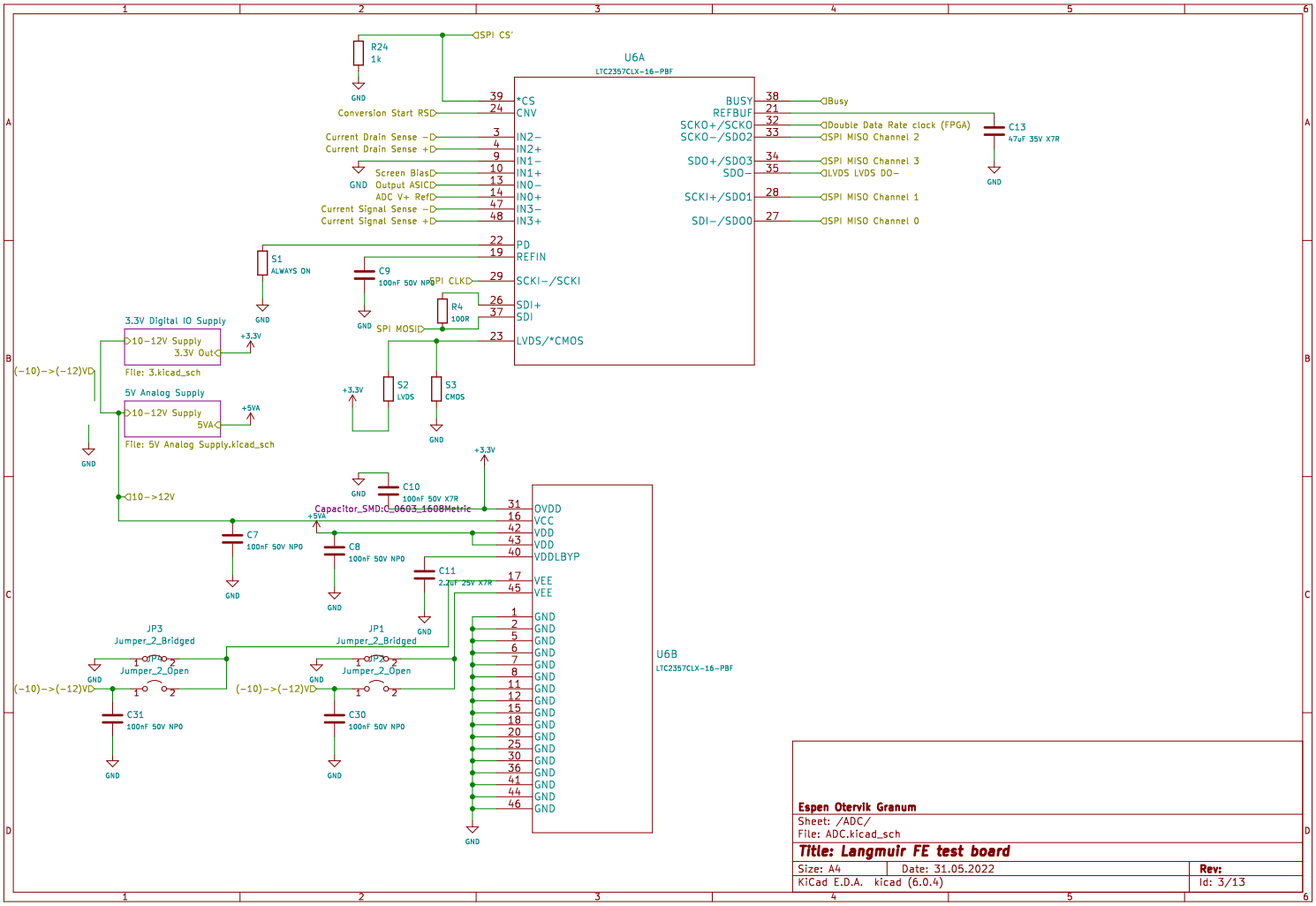
Size: A4	Date: 31.05.2022	**Rev:**
KiCad E.D.A. kicad (6.0.4)		Id: 1/13



Espen Otervik Granum		
Sheet: /LPF/		
File: LPF.kicad_sch		
Title: Langmuir FE test board		
Size: A4	Date: 31.05.2022	**Rev:**
KiCad E.D.A. kicad (6.0.4)		Id: 2/13


SPI CS'
R24
1k
GND
U6A
LTC2357CLX-16-PBF
39 *CS
24 CNV
Conversion Start RS
3 IN2−
4 IN2+
Current Drain Sense −
Current Drain Sense +
9 IN1−
10 IN1+
Screen Bias
13 IN0−
GND Output ASIC
14 IN0+
ADC V+ Ref
47 IN3−
48 IN3+
Current Signal Sense −
Current Signal Sense +
22 PD
19 REFIN
29 SCKI−/SCKI
SPI CLK
26 SDI+
37 SDI
R4
100R
SPI MOSI
23 LVDS/*CMOS
BUSY 38 Busy
REFBUF 21
SCKO+/SCKO 32 Double Data Rate clock (FPGA)
SCKO−/SDO2 33 SPI MISO Channel 2
C13
47uF 35V X7R
SDO+/SDO3 34 SPI MISO Channel 3
SDO− 35 LVDS LVDS DO−
SCKI+/SDO1 28 SPI MISO Channel 1
SDI−/SDO0 27 SPI MISO Channel 0
S1
ALWAYS ON
C9
100nF 50V NPO
S2
LVDS
S3
CMOS
+3.3V
3.3V Digital IO Supply
10-12V Supply
3.3V Out
File: 3.kicad_sch
(−10)->(−12)VD
5V Analog Supply
10-12V Supply
5VA
+5VA
File: 5V Analog Supply.kicad_sch
10->12V
C10
100nF 50V X7R
Capacitor_SMD:C_0603_1608Metric
C7
100nF 50V NPO
C8
100nF 50V NPO
C11
2.2uF 25V X7R
31 OVDD
16 VCC
42 VDD
43 VDD
40 VDDLBYP
17 VEE
45 VEE
1 GND
2 GND
5 GND
6 GND
7 GND
8 GND
11 GND
12 GND
15 GND
18 GND
20 GND
25 GND
30 GND
36 GND
41 GND
44 GND
46 GND
U6B
LTC2357CLX-16-PBF
JP3
Jumper_2_Bridged
JP4
Jumper_2_Open
JP1
Jumper_2_Bridged
JP2
Jumper_2_Open
C31
100nF 50V NPO
C30
100nF 50V NPO
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Sheet: /ADC/
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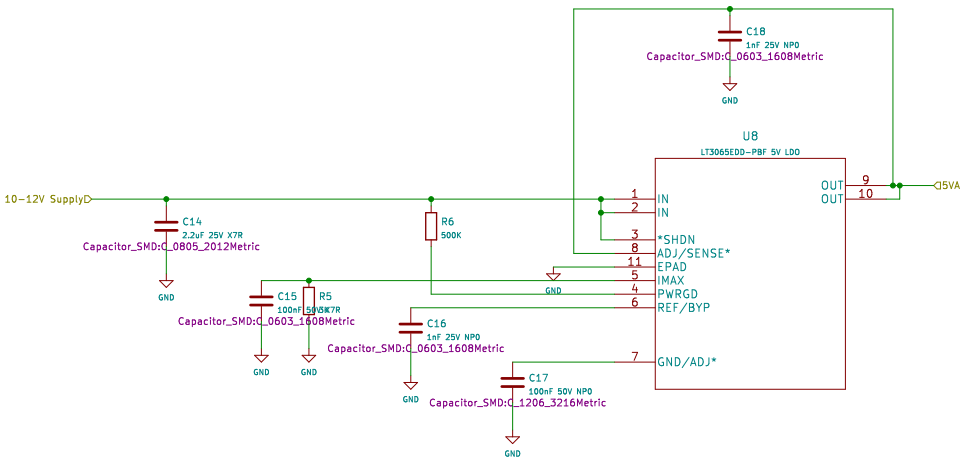
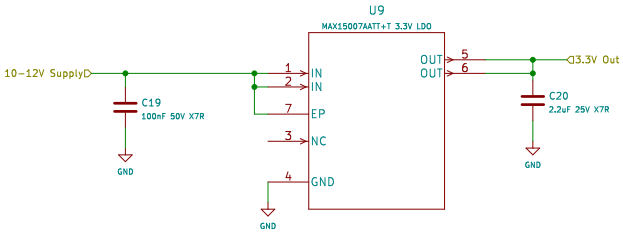
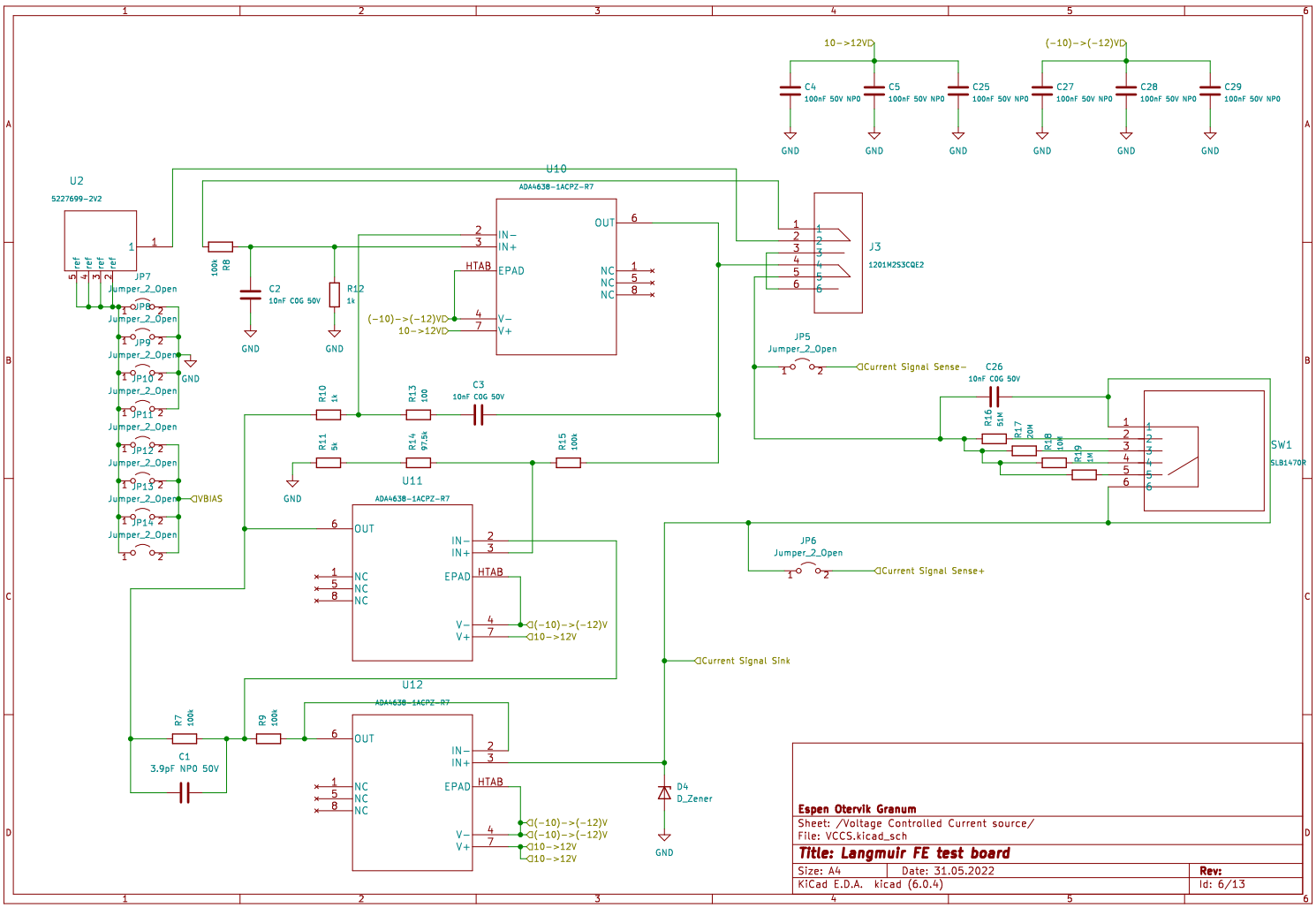
Title: Langmuir FE test board
Size: A4
Date: 31.05.2022
KiCad E.D.A. kicad (6.0.4)
Rev:
Id: 3/13



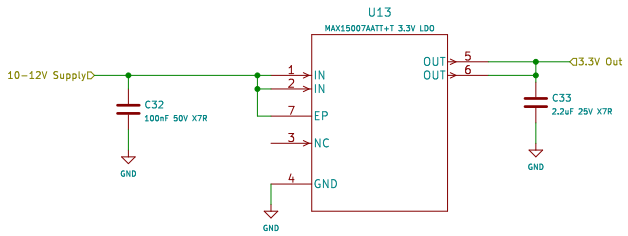
Espen Otervik Granum		
Sheet: /ADC/5V Analog Supply/		
File: 5V Analog Supply.kicad_sch		
Title: Langmuir FE test board		
Size: A4	Date: 31.05.2022	**Rev:**
KiCad E.D.A. kicad (6.0.4)		Id: 4/13



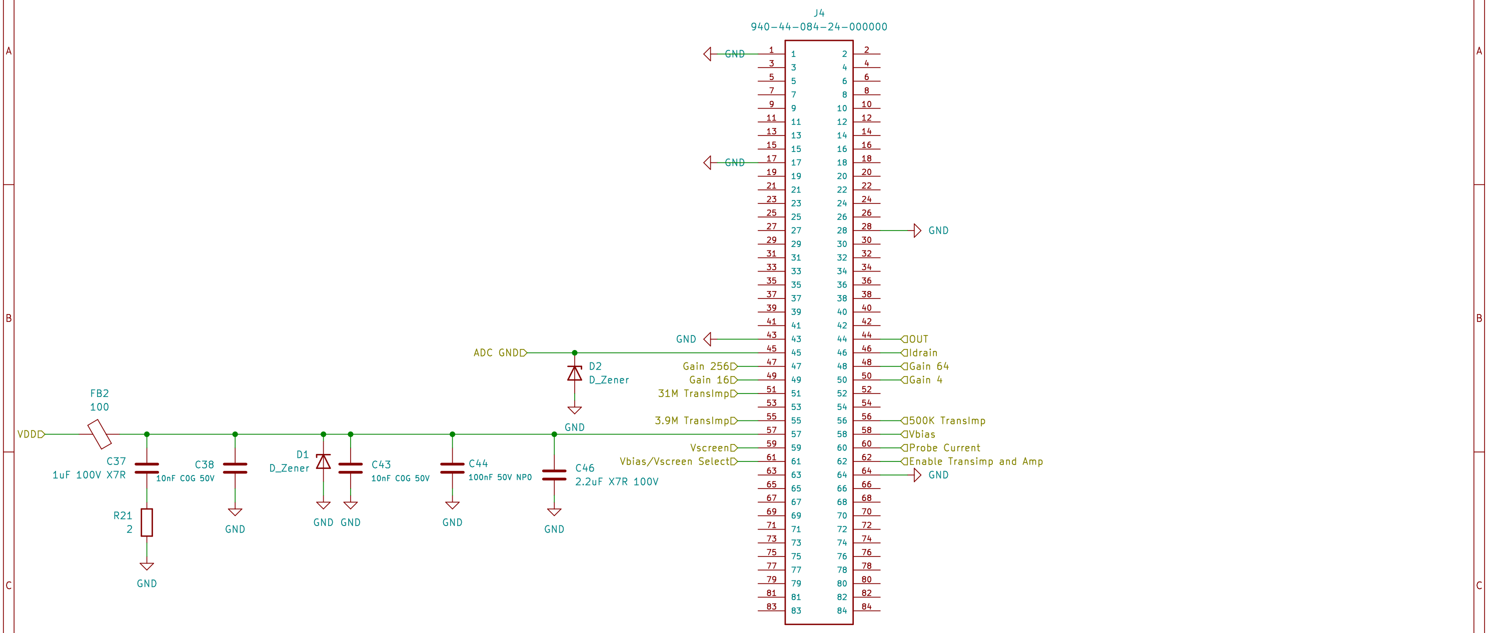
Espen Otervik Granum		
Sheet: /ADC/3.3V Digital IO Supply/		
File: 3.kicad_sch		
Title: Langmuir FE test board		
Size: A4	Date: 31.05.2022	**Rev:**
KiCad E.D.A. kicad (6.0.4)		Id: 5/13



Espen Otervik Granum	
Sheet: /Voltage Controlled Current source/	
File: VCCS.kicad_sch	
Title: Langmuir FE test board	
Size: A4	Date: 31.05.2022
KiCad E.D.A. kicad (6.0.4)	**Rev:** Id: 6/13



Espen Otervik Granum		
Sheet: /3.3V ADC Vref+/		
File: 3.kicad_sch		
Title: Langmuir FE test board		
Size: A4	Date: 31.05.2022	**Rev:**
KiCad E.D.A. kicad (6.0.4)		Id: 7/13



Espen Otervik Granum

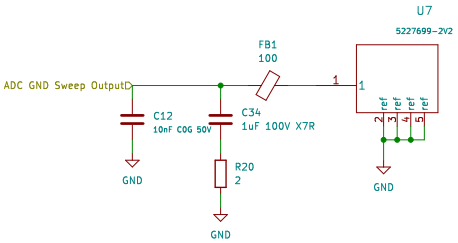
Sheet: /ASIC/

File: ASIC.kicad_sch

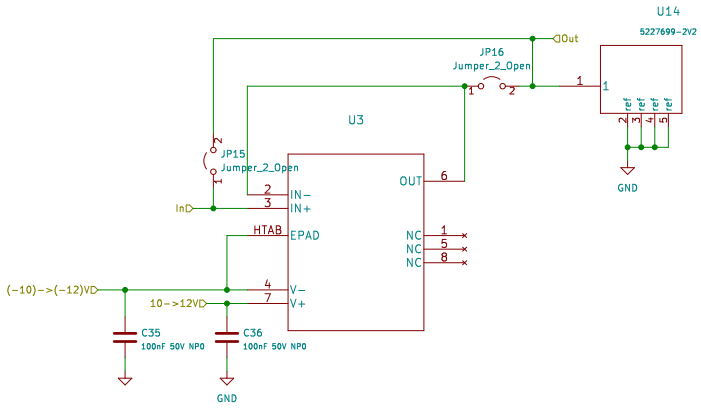
Title: Langmuir FE test board

Size: A4 | Date: 31.05.2022 | Rev:

KiCad E.D.A. kicad (6.0.4) | Id: 8/13



Espen Otervik Granum		
Sheet: /ADC Vref+ Sweep Input/		
File: ADC_GND_Sweep_Input.kicad_sch		
Title: Langmuir FE test board		
Size: A4	Date: 31.05.2022	**Rev:**
KiCad E.D.A. kicad (6.0.4)		Id: 9/13



Espen Otervik Granum		
Sheet: /Follower To Multimeter/		
File: Follower_To_Multimeter.kicad_sch		
Title: Langmuir FE test board		
Size: A4	Date: 31.05.2022	**Rev:**
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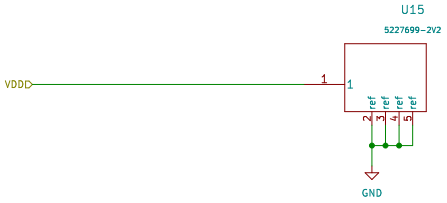

Espen Otervik Granum		
Sheet: /VDD Supply/		
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Title: Langmuir FE test board		
Size: A4	Date: 31.05.2022	**Rev:**
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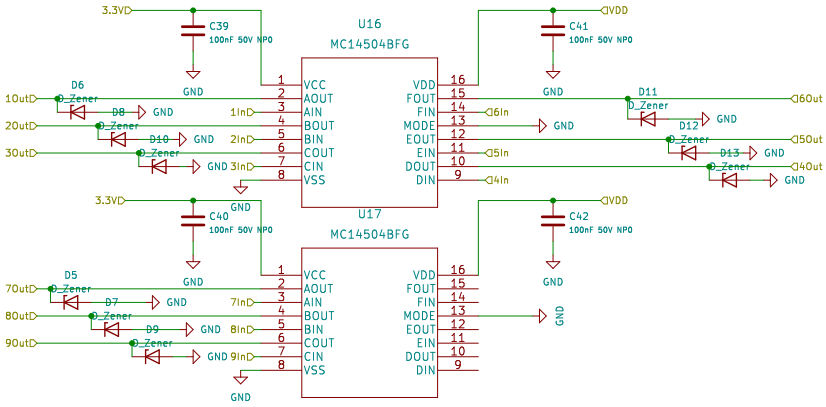

Espen Otervik Granum		
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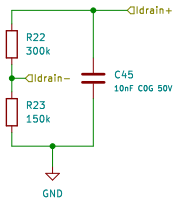
File: Level_Shifting.kicad_sch		
Title: Langmuir FE test board		
Size: A4	Date: 31.05.2022	**Rev:**
KiCad E.D.A. kicad (6.0.4)		Id: 12/13



Espen Otervik Granum		
Sheet: /Bias Current Drain/		
File: Bias_Current_Drain.kicad_sch		
Title: Langmuir FE test board		
Size: A4	Date: 31.05.2022	**Rev:**
KiCad E.D.A. kicad (6.0.4)		Id: 13/13