Identification and Suppression of Majority Surface States in the Dry-etched β-Ga_2O_3

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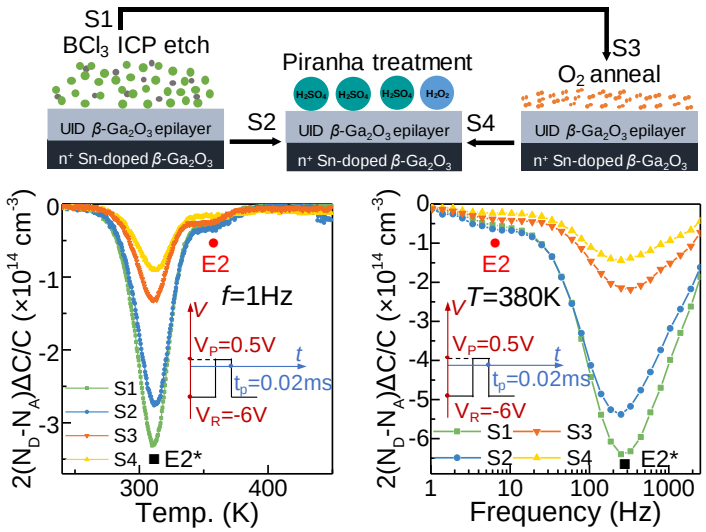
Abstract

Surface treatment after dry etching is vital to enhance surface quality of the material and thus improve device performance. In this letter, we identified the majority surface states induced by the dry etching of β-Ga_2O_3 and optimized surface treatments to suppress these electrically active defects with the improved performance of Schottky barrier diodes. Transient spectroscopies suggested that the majority traps (E_C−0.75 eV) related to di-vacancies (V_{Ga}-V_O) were enhanced in the concentration of 3.37×10^{14} cm^{-3} by dry etching, and reduced to 0.90×10^{14} cm^{-3} by the combined means of oxygen annealing and Piranha solution treatment. The trap evolution is support by the suppressed donor-acceptor-pair radiative recombination related to oxygen vacancies, the improved carrier transport (negligible hysteresis current-voltage and unity ideality factor) and the reduced surface band bending. These findings provide a straightforward strategy to improve surface quality for the further performance improvement of Ga_2O_3 power diodes.

TOC GRAPHIC



Keywords: β-Ga_2O_3; capacitance transient spectroscopy; surface states

Beta gallium oxide (β-Ga_2O_3) has attracted extensive efforts in developing high-performance power devices [1]. Dry etching is a crucial fabrication process to define device patterns or remove surface contaminants [2], but in turn inevitably induces surface damages and deteriorates device performance [3]. To overcome this barrier, various surface treatments have been reported, which had substantial impacts on the electrical properties of β-Ga_2O_3 power diodes [2-7]. Notably, the majority traps (E_C−0.75 eV, named as E2*) was attributed to an intrinsic defect that has been reported to be related to gallium vacancies (V_{Ga}) [8-9] or di-vacancy complexes (V_{Ga}-V_O) [9-10] in β-Ga_2O_3. Recently, the E2* trap was also reported as a dominant contributor to limit the Schottky diode performance, and as the primary source of the subthreshold instability of β-Ga_2O_3 MESFETs [11-13]. So far, the underlying trap evolution and the associated correlation of carrier transport and surface electronic structures still lacks of exploration.

In this letter, we evaluated the direct impact of various surface treatments on the evolution of surface states induced by the dry etching of β-Ga_2O_3. Deep level transient spectroscopy (DLTS) as well as isothermal capacitance transient spectroscopy (ICTS) identify that the dry-etching generated traps (E_C−0.75 eV), that is reported to be related to di-vacancies (V_{Ga}-V_O), are effectively suppressed by the combined oxygen annealing and Piranha treatment. The trap suppression is evidenced by the reduced donor-acceptor pair (DAP) recombination emissions, the negligible hysteresis current-voltage (*I-V*) characteristics, and the reduced upward bending potential at the β-Ga_2O_3 surface.

The 5×5 mm^2 β-Ga_2O_3 epi-wafer used in this work was diced from the commercial 2-inch β-Ga_2O_3 epi-wafer purchased from Tamura Corporation, Japan. It consists of a Sn heavily doped β-Ga_2O_3 (001) substrate and a 10-μm-thick unintentionally doped (UID) β-Ga_2O_3 epilayer grown by halide vapor phase epitaxy (HVPE). The virgin β-Ga_2O_3 wafer is denoted as sample S0. Sample S1 was produced

by the inductively coupled plasma (ICP) etching for 20 min with a power of 40 W and a BCl_3 flow rate of 10 sccm, as schematically shown in Figure. 1 (a). The etched wafer was soaked in Piranha solution (H_2SO_4:H_2O_2=3:1, 90℃) for 3 min (marked as S2), or separately annealed in oxygen ambient at 900℃ for 2 hours (marked as S3). Sample S4 was obtained by the oxygen annealing and the consequent Piranha treatment under the same conditions as samples S2 and S3, respectively. Afterward, all samples were used to fabricate vertical Schottky barrier diodes (SBDs) with the formation of Ti/Au (20/80 nm) back Ohmic contact and 1×1 mm^2 squared Ni/Au (100/100 nm) Schottky electrodes by electron beam evaporation.

Figure. 1 (b) shows the DLTS spectra of samples S0 and S1 at V_R=-6 V and -2 V, respectively, while fixing the pulse voltage (V_P) of 0.5 V, the pulse width (t_p) of 0.02 ms, and a lock-in frequency (f) of 1 Hz. Note that t_p=0.02 ms is sufficient to complete the dynamic capture and emission of electrons by traps, since the curves recorded at t_p=0.02 ms and t_p=1 ms coincide exactly, as shown in Figure.S1. Two electron trap signatures were distinct at 310 and 350 K. The V_R reduction from -6 to -2 V shrinks the depletion width from 529 to 333 nm, allowing the detection of near-surface traps. One additional weak peak at 410 K is also observed for the virgin sample S0 but absent for S1-S4, as evidenced by the absence of peak at 410 K in the DLTS spectra of samples S1-S4 recorded at V_R=-2 V (see Figure. S2). Figure. 1 (c) shows the summarized Arrhenius space of the majority carrier traps in this work and Ref [8, 14]. The DLTS peaks at 310, 350, and 410 K have been assigned to the E2* traps related to intrinsic defects (V_{Ga} or V_{Ga}-V_O), the unintentional doped impurity E2 traps related to Fe substituting for Ga (Fe_{Ga}), and E3 traps in the HVPE-grown β-Ga_2O_3, respectively [8-10, 15-17]. Table 1 summarizes the detailed trap parameters. The E3 trap has been reported to be related to surface contaminants (e.g. Ti[16],

Fe[18], Co[18]) with an energy level of E_C−1.09 eV and capture cross-section of σ_{E3}=4.30×10^{-14} cm^2, which are completely removed by the dry etching, together with the reduced E2 trap (E_C−0.83 eV, σ_{E2}=2.56×10^{-15} cm^2) in concentration (N_{TE2}). However, the N_{TE2*} of E2* (E_C−0.75 eV, σ_{E2*}=1.12×10^{-14} cm^2) was enhanced by the dry etching. Thus, the surface treatment was reported to suppress these traps for improving the device of β-Ga_2O_3 SBDs [2].

Figure. 2 (a) show the semi-logarithmic *J-V* of diodes S1-S4. All diodes exhibit high rectification ratios >10^9 at ±2 V. Notably, the oxygen-annealed sample S3 exhibits the lowest reverse leakage current due to the charge compensation effect in a formed ultra-thin semi-insulating (SI) surface layer [6]. All forward *J-V* features obey strictly the thermionic emission (TE) model, as given by [3]

$$J_{TE} = J_0\left(\frac{q(V - JR_s)}{\eta kT} - 1\right), J_0 = A^* T^2 \exp\left(-\frac{\phi_{B,JV}}{\eta kT}\right) \quad (1)$$

where J_0=(1.50~2.43)×10^{-11} A/cm^2 is the saturation current density obtained by fitting, A^*=33.65 A/(cm^2 K^2) is the Richardson constant of β-Ga_2O_3 [19], R_s is the series resistance. The obtained Schottky barrier heights (SBHs) of $\phi_{B,JV}$=1.02~1.06 V, and the extracted ideality factors (η) of diodes S1-S4 were 1.04, 1.03, 1.02, and 1.00, respectively. The feature of nearly ideal unity indicates the etching-induced damage are effectively repaired by surface treatments [3-5, 20]. Furthermore, the dynamic carrier trapping by the Ni/β-Ga_2O_3 interfacial defects has been investigated by the hysteresis *J-V* characterization [20]. In Figure. 2 (a), traps are filled by electrons during the forward sweep, while saturated under a high initial current during the backward sweep. The voltage hysteresis intervals (ΔV) are 0.10, 0.04, 0.02, and 0.01 V for diodes S1-S4 at J=12.5 A/cm^2, respectively. Such negligible ΔV for sample S4 reflects the remarkable reduction of surface traps after the combined oxygen annealing and Piranha treatment.

Figure.2 (b) show the *C-V* and $1/C^2$-*V* characteristics measured at 100 kHz. The built-in potentials (V_{bi}) exhibit negligible variation in the range of 1.00~1.04 V, Thus, the uniform $\phi_{B,CV}$=1.13~1.18 V were determined from $\phi_{B,CV}=V_{bi}+(kT/q)\ln[N_C/(N_D-N_A)]$, $N_C=3.71\times10^{18}$ cm^{-3} is the effective state density of the conduction band for β-Ga_2O_3 calculated by $N_C=2[2\pi m_n^* kT/(h^2)]^{3/2}$, *h* is Plank's constant and $m_n^*=0.28\ m_0$ is the electron effective mass of β-Ga_2O_3 [19]. The derived $\phi_{B,CV}$ is slightly larger than $\phi_{B,JV}$, which is possibly due to the barrier inhomogeneity across the large contact area ($1\times1\ mm^2$) [19, 21]. The net donor concentration (N_D-N_A) in the β-Ga_2O_3 epilayer is extracted from the slope of $1/C^2$-*V* plot, see Table 1. The $1/C^2$ slope difference results from the charge density variation of surface states in the UID β-Ga_2O_3 epilayer [6]. In particular, sample S3 exhibits the lowest capacitance corresponding to its minimum leakage current [2], as the SI interfacial layer contributes an additional capacitance (C_I) in series with the capacitance (C_L) of depletion region the β-Ga_2O_3 epilayer. In terms of $1/C=1/C_I+1/C_L$, the SI thickness (*d*) is estimated to be 13 nm, which exactly equals to the difference of the depletion widths for samples S3 and S4.

The trap evolution has been quantified by DLTS and ICTS spectra shown in Figure. 3 (a) and (b). Both N_{TE2} and N_{TE2*} decrease sequentially after various surface treatments, which directly corresponds to the improved electrical properties of the diodes. As summarized in Table 1, N_{TE2*} decreases drastically from 3.37×10^{14} to 0.90×10^{14} cm^{-3} after oxygen annealing followed by Piranha treatment, while N_{TE2} is one order lower than N_{TE2*} and drops slightly from 3.29×10^{13} to 2.22×10^{13} cm^{-3}. Thus, the damage repair is mainly reflected by the suppression of etching-induced E2* traps. It is also supported by the evolution of DAP recombination emissions investigated by photoluminescence (PL) characterization. In Figure. 4 (a), all PL spectra are well deconvoluted into the ultraviolet (UV) and

blue (BL) defective emissions, which were reported to be associated with the DAP transitions between donors (Si_{Ga} or V_O) and acceptors (V_{Ga} or V_{Ga}-V_O divacancy complexes) [22], among them, V_{Ga} or V_{Ga}-V_O divacancy complexes are consistent with the origin of E2* traps. Both UV and BL emissions are weakened with the N_{TE2*} reduction, further suggesting the partial elimination of E2* traps by the combined surface treatments.

To identify the damage origin, the surface chemical states were characterized by the X-ray photoemission spectroscopy (XPS). In Figure. 4 (b), all O 1s core level XPS spectra are composed of a primary peak at 530.5 eV (labelled as L_O) related to lattice oxygen bonded in stoichiometric Ga_2O_3 and a shoulder peak at 532.0 eV contributed by the presence of V_O [23-24]. The V_O/L_O area ratio increases from 0.25 for the virgin sample S0 to 0.43 for the dry-etched sample S1, suggesting the increasing V_O induced by the plasma bombardment effect during the dry etching [25]. With the surface treatment, the V_O/L_O area ratios decrease from 0.43 to 0.19 [24, 26]. Note that, the variation of V_O/L_O area ratios exactly follows the changes of N_{TE2*}. It further strengthens the correlation between E2* traps and V_O-related complexes.

Besides tailoring the surface chemical states, dry etching and the following surface treatments also modify the surface electronic structures. The valence band (VB) XPS spectra in Figure. 4 (c) shows that the VB structures are dominated by the O 2*p* orbitals with three distinct coordination sites (O_I, O_{II}, O_{III}) [27]. A linear fit of the low binding energy (BE) edge to background yields the energy difference (ζ) between the VB maximum and the Fermi level (E_F). Thus, the surface bending energies (V_{bb}) are determined to be 0.91, 1.23, 1.15, 1.78, 1.11 eV, for samples S0-S4, respectively, in terms of $V_{bb}=E_g-\xi-\zeta$. Here, E_g is the experimental band gap (4.85 eV) of β-Ga_2O_3 [27], ξ=0.13 eV is E_C-E_F in the flat-band

bulk region calculated by $\xi=(kT/q)\ln[N_C/(N_D-N_A)]$ [27-28].

Notably, the initial increase of V_{bb} from 0.91 for S0 to 1.23 for S1 indicates the enhanced upward band bending after dry etching. It is resulted from the ionization of V_O^{2+} in the near-surface space-charge region, and the negatively charged states, such as V_{Ga}^{3-}, are predictably accumulated at surface to ensure the charge neutrality [29-32], as schematically illustrated in Figure.5 (a). Afterward, the ultra-thin surface damaged layer was removed by the Piranha treatment, resulting in the reductions of both V_O^{2+}, V_{Ga}^{3-} and even (V_{Ga}-V_O) di-vacancies, as evidenced by the reduction of E2* traps in samples S2 and S4 that having lower V_{bb} values of 1.15 and 1.11 eV, respectively. One exception is for sample S3 with only oxygen annealing. With further reduced E2* traps, the V_{bb} abnormally rises to 1.78 eV and the O 2*p* states in the coordination sites O_{III} are profoundly enhanced. It can be understood that, the oxygen annealing is expected to not only annihilate V_O distributed in the near surface region but also modify the surface stoichiometry by introducing oxygen interstitials that having a lower formation energy in an oxygen-rich environment [31]. Furthermore, the band tail states at the low-energy edge of the VB XPS spectrum for the sample S3 indicate the presence of additional sub-gap states induced by oxygen interstitials at the near surface region [33]. As shown in Figure. 5 (b), the charge transition takes place from donors in the surface depletion region to these newly induced oxygen interstitials. Thus, an interfacial dipole layer is formed between the negatively charged states (O_i^{2-}) and the ionized donors, leading to the additional barrier and making surface semi-insulating [34], which is consistent with the widened depletion region and the lowest N_D-N_A for sample S3 [6].

In summary, the majority surface states induced by the dry etching has been identified to be E2* traps (E_C−0.75 eV) related to di-vacancies (V_{Ga}-V_O) in β-Ga_2O_3, which are subsequently suppressed

via the optimized surface treatments. With the combined oxygen annealing and Piranha treatment, the resultant SBDs exhibit the negligible hysteresis current-voltage characteristics and unity ideality factor. In particular, besides the V_O elimination, the oxygen annealing modifies the surface electronic structure with an interfacial dipole layer. These findings deepen understanding on the trap evolution through surface treatments, which is crucial to improve surface quality towards high performance power diodes.

EXPERIMENTAL METHODS

Transient capacitance measurements: Deep level transient spectroscopy (DLTS) and isothermal capacitance transient spectroscopy (ICTS) were conducted to investigate the majority carrier traps (electrons) in *n*-type β-Ga_2O_3 epilayer by utilizing a lock-in amplifier-based Deep Level Spectrometer (Model: Semilab, DLS83D). The diode is mounted in a hermetically sealed cryostat with a pressure on the order of 10^{-3} mbar, and liquid nitrogen is employed to cool the diode to the target temperature. In the DLTS measurements, the experimental temperature interval is 240-450 K and the heating rate is maintained at 100 mK/s. Repeated temperature-scans with varying lock-in frequency (*f*) can obtain a series of trap signatures ($\tau_{e,max}$, T_{max}) for Arrhenius fitting, τ_e is the emission time constant of electron traps. While in the ICTS measurements, the experimental temperature is constant and the lock-in frequency sweep range is 1 to 2500 Hz, repeated *f*-scans with varying temperature can also obtain a series of trap signatures for Arrhenius fitting. Therefore, the trap energy level below conduction band (E_T) and electron capture cross section (σ_n) can be determined by the well-known Arrhenius equation of $\ln\left[1/\left(\tau_e T^2\right)\right] = -\left[1/\left(kT\right)\right]E_T + \ln\left(\gamma\sigma_n\right)$[35], where *k* is the Boltzmann constant, γ is a constant related to electron velocity (v_{th}) and effective state density of the conduction band (N_C). Figure. S3 and S4

show the *f*-dependent DLTS spectra and temperature-dependent ICTS spectra for all diodes, respectively. Furthermore, carrier freezing effects and quality factor (Q) are also evaluated. At reverse bias (V_R) of -6 V, all samples exhibit negligible carrier freezing and high quality factors (Q≥49) in the experimental temperature range of 240~450 K [36], as shown in Figure. S5 (a) and (b), validating the accuracy of detecting traps using transient spectroscopies.

Other measurements: The current density-voltage (*J-V*) and capacitance-voltage (*C-V*) characteristics were measured at room temperature (RT) by using a Keithley 2634B current source meter and a Keysight E4980A LCR meter, respectively. The photoluminescence (PL) measurement was performed at RT using Horiba monochromator (iHR550) with a commercial Si-based photomultiplier tube detector and a 261 nm laser for excitation, scanning from 270 to 650 nm with steps of 0.5 nm. The X-ray photoemission spectroscopy (XPS) was performed using an Al α (hν=1486.6 eV) as the X-ray radiation source with resolution of 0.5 eV and calibrated by the C 1s peak at 284.6 eV.

ASSOCIATED CONTENT

Supporting Information

- The t_p-dependent DLTS spectra for diode S2 (Figure. S1)
- The DLTS spectra for diodes S1-S4 recorded under V_R=-2 V, V_P=0.5 V, t_p=0.02 ms, and *f*=1Hz (Figure. S2)
- The *f*-dependent DLTS spectra for all diodes recorded under condition of V_R=-6V, V_P=0.5V, and t_p=0.02ms (Figure. S3)

- The temperature-dependent DLTS spectra for all diodes recorded under condition of V_R=-6V, V_P=0.5V, and t_p=0.02ms (Figure. S4)
- (a) The capacitance-temperature and conductance-temperature spectra for all samples. (b) The Q-T spectra for all samples (Figure. S5)

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Notes

The authors declare no competing financial interest.

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Figures

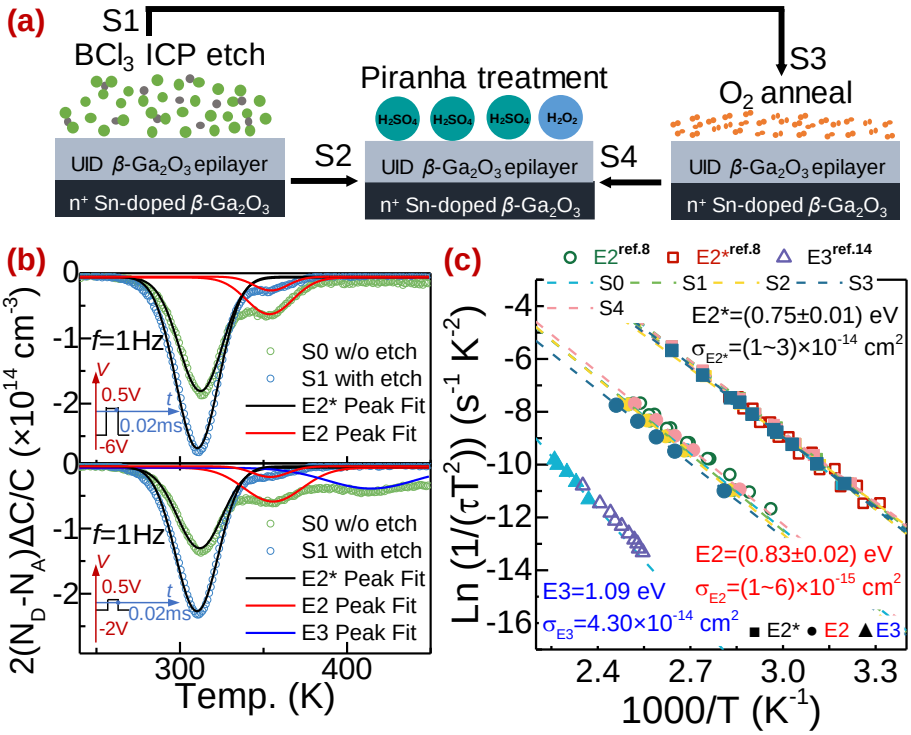

Figure.1 (a) Schematic of process sequence for samples S1-S4. (b) DLTS spectra of samples S0 and S1 recorded at V_R=-6 V and V_R=-2 V, respectively. (c) the summarized Arrhenius space of traps in this work and from Ingebrigtsen et al [8] (E2 and E2* trap) as well as Polyakov et al [14] (E3 trap).

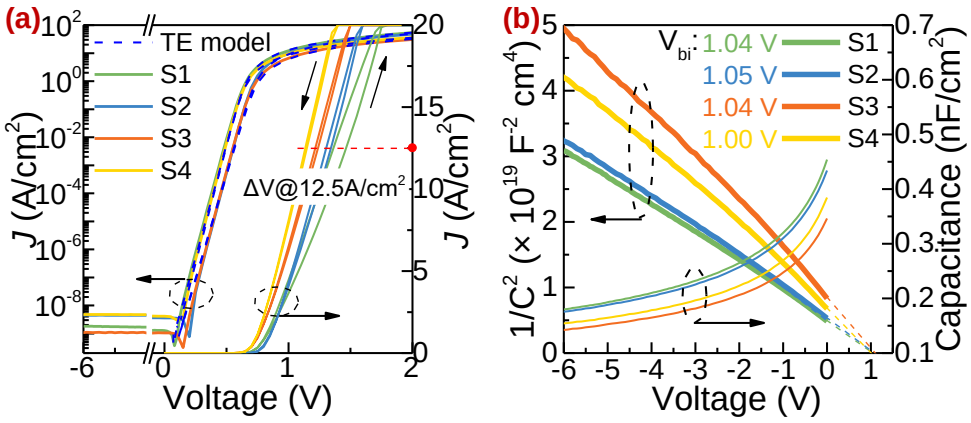

Figure. 2 (a) Semi-logarithmic *J*-*V* and linear-scaled hysteresis characteristics for samples S1-S4 that were measured from 0 to 2 V and then back toward with a limiting maximum current of 0.2 A. (b) *C*-*V* and $1/C^2$-*V* characteristics.

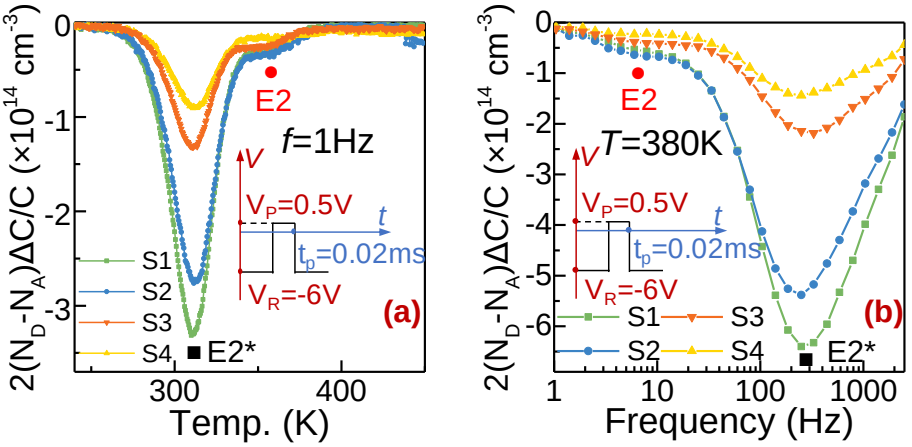

Figure. 3 (a) DLTS spectra of diodes S1-S4 recorded under condition of V_R=-6 V, V_P=0.5 V, t_p=0.02 ms, and f=1 Hz. (b) ICTS spectra recorded under condition of V_R=-6 V, V_P=0.5 V, t_p=0.02 ms, T=380 K, and f=1~2500 Hz.

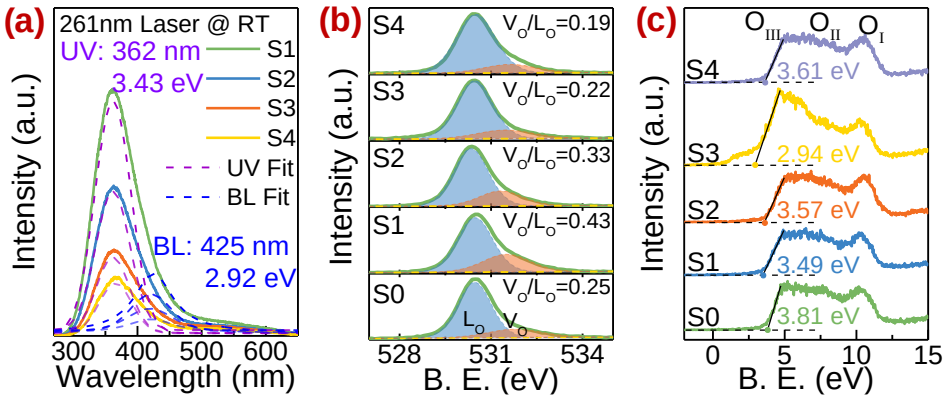

Figure. 4 (a) RT-PL spectra. (b) The O 1s core level and (c) VB XPS spectra.

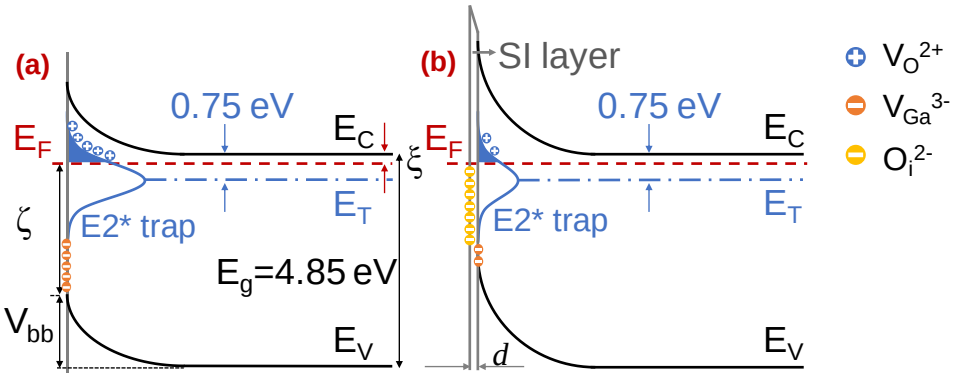

Figure. 5 Energy band diagrams of sample (a) without and (b) with SI layer.

Tables

Table 1. Summary of trap parameters detected in diodes S1-S4

Diode	N_D-N_A ($\times 10^{16}$ cm^{-3})	E_C-E_T (eV)		σ (cm^2)		N_T (cm^{-3})	
		E2*	E2	σ_{E2*} ($\times 10^{-14}$)	σ_{E2} ($\times 10^{-15}$)	N_{TE2*} ($\times 10^{14}$)	N_{TE2} ($\times 10^{13}$)
S1	2.70	0.76	0.82	1.12	2.56	3.37	3.29
S2	2.93	0.75	0.85	1.01	6.05	2.72	3.44
S3	2.07	0.76	0.84	1.18	6.04	1.31	2.60
S4	2.22	0.75	0.81	1.04	1.45	0.90	2.22